HITACHI
55HK6T64U
55293DLB
MB100
SERVICE MANUAL

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1. INTRODUCTION

17MB100 main board is driven by MStar SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU. This IC also supports 4K2K (UHD).

Key features includes,

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The MACEpro video processor
- Home theatre sound processor
- Internet and Variety of Connectivity Support
- Dual-stream decoder for 3D contents
- Mılti-purpose CPU for OS and multimedia
- Peripheral and power management

Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Side AV (CVBS, R/L_Audio)
- 1 Side SCART socket(Common)
- 1 YPbPr (Common)
- 1 Side S-Video(Common)
- 1 PC input(Common)
- 4 HDMI input(Common)
- 1 Common interface(Common)
- 1 Optic S/PDIF output(Common)
- 1 Stereo audio input for PC(Common)
- 1 Subwoofer output(Common)
- 1 Headphone(Common)
- 2x USB3.0 and 1xUSB2.0(Common)
- 1 Ethernet-RJ45 (Common)
- 1 External Touchpad(Common)
- Internal Wi-Fi and BT

2. TUNER

A. SI2157 TERRESTRIAL AND CABLE TV TUNER

Description

The Si2157 is Silicon Labs' fifth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wirewound inductors or LNAs, the Si2157 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2157 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners and discrete MOPLL-based tuners. The Si2157 also incorporates a harmonic-rejection mixer to deliver excellent Wi-Fi and LTE immunity. For the best performance with next-generation digital TV standards such as DVB-T2/C2, the Si2157 delivers industry-leading phase noise performance.

Features

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVBT2/T/C2/C, ISDB-T/C, DTMB
  - 42-1002 MHz frequency range
- Industry-leading margin to A/74,
- NorDig, DTG, ARIB, EN55020,
- OpenCable™
- Lowest BOM for a hybrid TV tuner
  - No balun at RF input
  - Integrated tracking filters requiring no external inductors or SAW filters
  - Increased ESD protection on 6 pins
- Best-in-class real-world reception
  - Exceeds MOPLL-based tuners
  - Lowest phase noise
  - High Wi-Fi and LTE immunity
- Low power consumption
  - 3.3 V and 1.8 V power supplies
  - 3.3 V single-supply option
- Integrated power-on reset circuit
- Single or separate output pins for ALIF/DLIF connection to SoC
- Standard CMOS process
- 4 x 4 mm, 28-pin QFN package
- RoHS compliant

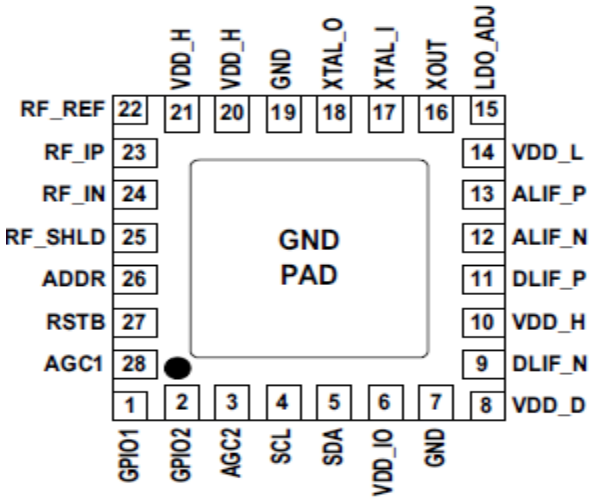


Figure: Si2157 Pin description

Pin Number(s)	Name	I/O	Description
1*	GPIO1	I/O	General purpose input/output #1
2*	GPIO2	I/O	General purpose input/output #2
3*	AGC2	I	ALIF/DLIF output amplitude control input #2 (optional)
4	SCL	I	I^2C clock input
5	SDA	I/O	I^2C data input/output
6	VDD_IO	S	I/O supply voltage, 3.3 V
7	GND	S	Ground. Connect GND pins to GND_PAD.
8	VDD_D	S	Digital supply voltage, 1.8 V
9*	DLIF_N	O	DLIF differential output to DTV demodulator (negative)
10	VDD_H	S	Analog high supply voltage, 3.3 V
11*	DLIF_P	O	DLIF differential output to DTV demodulator (positive)
12*	ALIF_N	O	ALIF differential output to SoC or ATV demodulator (negative)
13*	ALIF_P	O	ALIF differential output to SoC or ATV demodulator (positive)
14	VDD_L	S	Analog low supply voltage, 1.8 V
15*	LDO_ADJ	O	Control output for external PNP transistor used for single-supply operation
16*	XOUT	O	Output reference clock to secondary tuner or receiver
17	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
18*	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
19	GND	S	Ground. Connect GND pins to GND_PAD.
20	VDD_H	S	Analog high supply voltage, 3.3 V
21	VDD_H	S	Analog high supply voltage, 3.3 V
22	RF_REF	O	RF reference voltage output
23	RF_IP	I	RF input (positive)
24	RF_IN	I	RF input (negative)
25	RF_SHLD	S	RF input shield
26	ADDR	I	I^2C address select
27*	RSTB	I	Hardware reset (active low)
28*	AGC1	I	ALIF/DLIF output amplitude control input #1 (optional)
*Note: Pin should be left floating if unused.			

Table: Pin Functions

B. M88TS2022 SATELLITE TUNER

Features

- Single-chip tuner
- Compliant with DVB-S2 and ABS-S standards
- Support QPSK, 8PSK and 16APSK
- Direct-conversion from L-band to baseband
- Symbol rate: 1 to 45 Msymbol/s
- Integrated VCOs and PLL, with on-chip inductors, varactors and loop filter
- Integrated baseband filters: 4 MHz to 40 MHz bandwidth
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation (patent-pending) removes external loop filters
- Excellent immunity to strong adjacent undesired channels
- Integrated clock driver provides auxiliary divided clock output for other devices
- Selectable RF bypass
- Support sleep mode
- 2-wire serial bus with 3.3 V compatible logic levels
- Power supply: +3.3 V
- 28-pin QFN (Quad Flat No-lead) package
- RoHS compliant

Applications

- Digital satellite receiver front-end for DVB-S2 and ABS-S applications

General Description

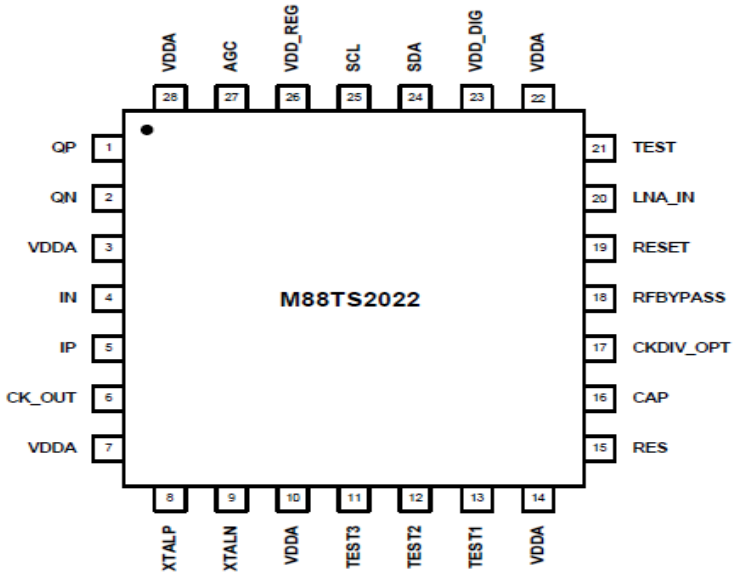
The M88TS2022 is a single-chip, direct-conversion tuner for digital satellite receiver applications. It offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end designs. The device also provides an RF bypass output for driving a second tuner module.

This device incorporates the following functional blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with an integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS2022 has the least number of pins compared with other conventional solutions, and requires the least external components. In typical applications, the M88TS2022 requires only one crystal, one bypass capacitor, one matching network, and a few external resistors. The device also has the industry's smallest latency, as it uses a fast locking PLL and a fast settling DC offset cancellation architecture.

The M88TS2022 can be configured via a 2-wire serial bus. The chip is available in a 28-pin QFN package.

Pin Assigment



Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Notes
VDDA	Analog power supply	-0.6	5	V	
VDD_DIG	Digital power supply	-0.6	5	V	
$V_{2\text{-wire}}$	Voltage on 2-wire bus pins	-0.6	5	V	
V_{IN}	Voltage on other input pins	-0.6	2.5	V	
V_{OUT}	Output voltage	-0.6	VDDA + 0.5	V	
T_{STG}	Storage temperature	-55	150	°C	
T_{OP}	Operating ambient temperature	0	70	°C	
Note: Stresses above the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended period may affect device reliability.					

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VDDA, VDD_DIG	Analog power supply	3.0	3.3	3.6	V	With respect to VSS
T_{OP}	Operating ambient temperature	0		70	°C	
Note: Device functionality is not guaranteed at any conditions beyond the recommended operating conditions.						

3. AUDIO AMPLIFIER STAGES

A. MAIN AMPLIFIER (TAS5719)

General Description

The TAS5717/TAS5719 is a 10-W/15-W, efficient,digital audio-power amplifier for driving stereo bridge-tied speakers. One serial data input allows processing of up to two discrete audio channels and seamless integration to most digital audio processors and MPEG decoders. The device accepts a wide of input data and data rates. A fully programmable data path routes these channels to the internal speaker drivers.

The TAS5717/9 is a slave-only device receiving all clocks from external sources. The TAS5717/TAS5719 operates with a PWM carrier between a 384-kHz switching rate and a 352-KHz switching rate, depending on the input sample rate. Oversampling combined with a fourth-order noise shaper provides a flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

Features

- Audio Input/Output
  - TAS5717 Supports 2×10 W and TAS5719 Supports 2×15 W Output
  - Wide PVDD Range, From 4.5 V to 26 V
  - Efficient Class-D Operation Eliminates Need for Heatsinks
  - Requires Only 3.3 V and PVDD
  - One Serial Audio Input (Two Audio Channels)
  - I2C Address Selection via PIN (Chip Select)
  - Supports 8-kHz to 48-kHz Sample Rate (LJ/RJ/I2S)
  - External Headphone-Amplifier Shutdown Signal
  - Integrated CAP-Free Headphone Amplifier
  - Stereo Headphone (Stereo 2-V RMS Line Driver) Outputs
- Audio/PWM Processing
  - Independent Channel Volume Controls With 24-dB to Mute
  - Programmable Two-Band Dynamic Range Control
  - 14 Programmable Biquads for Speaker EQ
  - Programmable Coefficients for DRC Filters
  - DC Blocking Filters
  - 0.125-dB Fine Volume Support
- General Features
  - Serial Control Interface Operational Without MCLK
  - Factory-Trimmed Internal Oscillator for Automatic Rate Detection
  - Surface Mount, 48-Pin, 7-mm × 7-mm HTQFP Package
  - AD, BD, and Ternary PWM-Mode Support
  - Thermal and Short-Circuit Protection
- Benefits
  - EQ: Speaker Equalization Improves Audio Performance
  - DRC: Dynamic Range Compression. Can Be Used As Power Limiter. Enables Speaker Protection, Easy Listening, Night-Mode Listening
  - DirectPath Technology: Eliminates Bulky DC Blocking Capacitors
  - Stereo Headphone/Stereo Line Drivers: Adjust Gain via External Resistors, Dedicated Active Headpone Mute Pin, High Signal-to-Noise Ratio
  - Two-Band DRC: Set Two Different Thresholds for Low- and High-Frequency Content

Pin descriptions and functions:

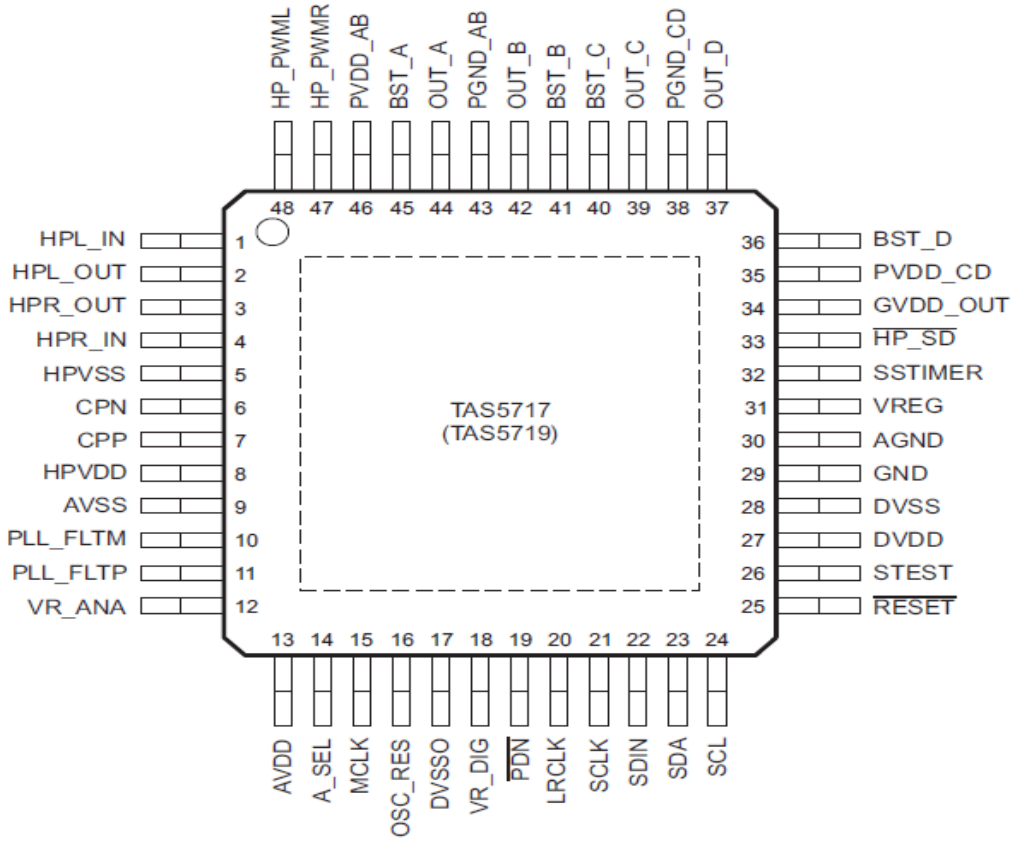


Figure: TAS5719 Pin descriptions

PIN		TYPE(1)	5-V TOLERANT	TERMINATION(2)	DESCRIPTION
NAME	NO.				
AGND	30	P			Analog ground for power stage
A_SEL	14	DIO			This pin is monitored on the rising edge of RESET. A value of 0 makes the I^2C dev address 0x54, and a value of 1 makes it 0x56.
AVDD	13	P			3.3-V analog power supply
AVSS	9	P			Analog 3.3-V supply ground
BST_A	45	P			High-side bootstrap supply for half-bridge A
BST_B	41	P			High-side bootstrap supply for half-bridge B
BST_C	40	P			High-side bootstrap supply for half-bridge C
BST_D	36	P			High-side bootstrap supply for half-bridge D
CPN	6	IO			Charge-pump flying-capacitor negative connection
CPP	7	IO			Charge-pump flying-capacitor positive connection
DVDD	27	P			3.3-V digital power supply
DVSS	28	P			Digital ground
DVSSO	17	P			Oscillator ground
GND	29	P			Analog ground for power stage

PIN		TYPE[1]	5-V TOLERANT	TERMINATION[2]	DESCRIPTION
NAME	NO.				
GVDD_OUT	34	P			Gate drive internal regulator output
HPL_IN	1	AI			Headphone left IN (single-ended, analog IN)
HPL_OUT	2	AO			Headphone left OUT (single-ended, analog OUT)
HP_PWML	48	DO			PWM left-channel headphone out
HP_PWMR	47	DO			PWM right-channel headphone out
HPR_IN	4	AI			Headphone right IN (single-ended, analog IN)
HPR_OUT	3	AO			Headphone right OUT (single-ended, analog OUT)
$\overline{\text{HP\_SD}}$	33	AI			Headphone shutdown (active-low)
HPVDD	8	P			Headphone supply
HPVSS	5	P			Headphone ground
LRCLK	20	DI	5-V	Pulldown	Input serial audio data left/right clock (sample rate clock)
MCLK	15	DI	5-V	Pulldown	Master clock input
OSC_RES	16	AO			Oscillator trim resistor. Connect an 18-kΩ 1% resistor to DVSSO.
OUT_A	44	O			Output, half-bridge A
OUT_B	42	O			Output, half-bridge B
OUT_C	39	O			Output, half-bridge C
OUT_D	37	O			Output, half-bridge D
$\overline{\text{PDN}}$	19	DI	5-V	Pullup	Power down, active-low. $\overline{\text{PDN}}$ prepares the device for loss of power supplies by shutting down the noise shaper and initiating the PWM stop sequence.
PGND_AB	43	P			Power ground for half-bridges A and B
PGND_CD	38	P			Power ground for half-bridges C and D
PLL_FLTM	10	AO			PLL negative loop-filter terminal
PLL_FLTP	11	AO			PLL positive loop-filter terminal
PVDD_AB	46	P			Power-supply input for half-bridge output A
PVDD_CD	35	P			Power-supply input for half-bridge output C
$\overline{\text{RESET}}$	25	DI	5-V	Pullup	Reset, active-low. A system reset is generated by applying a logic low to this pin. $\overline{\text{RESET}}$ is an asynchronous control signal that restores the DAP to its default conditions, and places the PWM in the hard-mute (high-impedance) state.
SCL	24	DI	5-V		I^2C serial control clock input
SCLK	21	DI	5-V	Pulldown	Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.
SDA	23	DIO	5-V		I^2C serial control data interface input/output
SDIN	22	DI	5-V	Pulldown	Serial audio data input. SDIN supports three discrete (stereo) data formats.
SSTIMER	32	AI			Controls ramp time of OUT_X to minimize pop. Leave this pin floating for BD mode. Requires capacitor of 2.2 nF to GND in AD mode. The capacitor determines the ramp time.
STEST	26	DI			Factory test pin. Connect directly to DVSS.
VR_ANA	12	P			Internally regulated 1.8-V analog supply voltage. This pin must not be used to power external devices.
VR_DIG	18	P			Internally regulated 1.8-V digital supply voltage. This pin must not be used to power external devices.
VREG	31	P			Digital regulator output. Not to be used for powering external circuitry.

Table: TAS5719 Pin Functions

			MIN	NOM	MAX	UNIT
	Digital/analog supply voltage	DVDD, AVDD	3	3.3	3.6	V
	Half-bridge supply voltage	PVDD_X	4.5			V
V_{IH}	High-level input voltage	5-V tolerant	2			V
V_{IL}	Low-level input voltage	5-V tolerant			0.8	V
T_A	Operating ambient temperature range		0		85	°C
T_J (1)	Operating junction temperature range		0		125	°C
R_L (BTL)	Load impedance	Output filter: L = 15 µH, C = 680 nF	4	8		Ω
L_O (BTL)	Output-filter inductance	Minimum output inductance under short-circuit condition	4.7			µH

(1) Continuous operation above the recommended junction temperature may result in reduced reliability and/or lifetime of the device.

Table: Recommended Operating Conditions

B. HEAD-PHONE AMPLIFIER STAGE

Head-phone is a SoC (single on chip) configuration in mainboard, Design scheme is shown in figure 3.

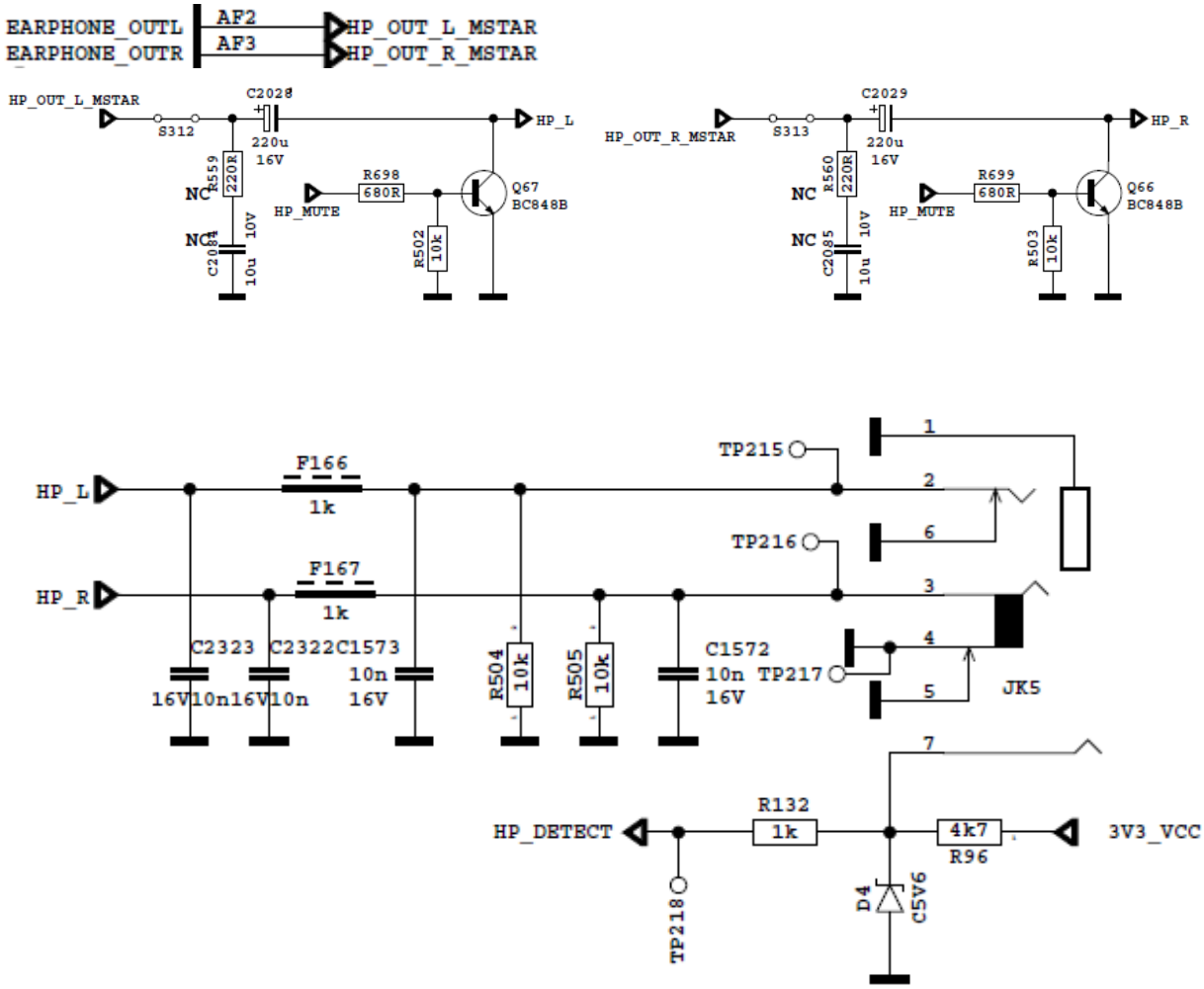


Figure: Head-phone

C. SUBWOOFER AMPLIFIER STAGE

PREAMPLIFIER (DRV632)

Description

The DRV632 is a 2-VRMS pop-free stereo line driver designed to allow the removal of the output dc-blocking capacitors for reduced component count and cost. The device is ideal for single-supply electronics where size and cost are critical design parameters.

Designed using TI's patented DirectPath™ technology, The DRV632 is capable of driving 2 VRMS into a 10-kΩ load with 3.3-V supply voltage. The device has differential inputs and uses external gain-setting resistors to support a gain range of ±1 V/V to ±10 V/V, and gain can be configured individually for each channel. Line outputs have ±8-kV IEC ESD protection, requiring just a simple resistor-capacitor ESD protection circuit. The DRV632 has built-in active-mute control for pop-free audio on/off control. The DRV632 has an external undervoltage detector that mutes the output when the power supply is removed, ensuring a pop-free shutdown.

Using the DRV632 in audio products can reduce component count considerably compared to traditional methods of generating a 2-VRMS output. The DRV632 does not require a power supply greater than 3.3 V to generate its 5.6-Vpp output, nor does it require a split-rail power supply. The DRV632 integrates its own charge pump to generate a negative supply rail that provides a clean, pop-free ground-biased 2-VRMS output.

The DRV632 is available in a 14-pin TSSOP.

Features

- Stereo DirectPath™ Audio Line Driver
  - 2 Vrms Into 10 kΩ With 3.3-V Supply
- Low THD+N < 0.01% at 2 Vrms Into 10 kΩ
- High SNR, >90 dB
- 600-Ω Output Load Compliant
- Differential Input and Single-Ended Output
- Adjustable Gain by External Gain-Setting Resistors
- Low DC Offset, <1 mV
- Ground-Referenced Outputs Eliminate DC-Blocking Capacitors
  - Reduce Board Area
  - Reduce Component Cost
  - Improve THD+N Performance
  - No Degradation of Low-Frequency Response Due to Output Capacitors
- Short-Circuit Protection
- Click- and Pop-Reduction Circuitry
- External Undervoltage Mute
- Active Mute Control for Pop-Free Audio On/Off Control
- Space-Saving TSSOP Package

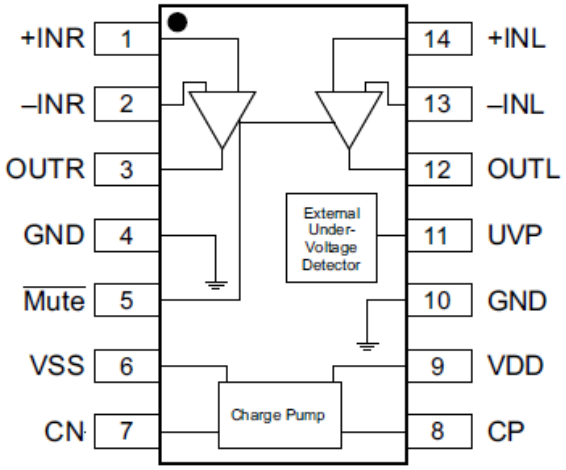


Figure: PW package

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
CN	7	I/O	Charge-pump flying capacitor negative connection
CP	8	I/O	Charge-pump flying capacitor positive connection
GND	4, 10	P	Ground
–INL	13	I	Left-channel OPAMP negative input
+INL	14	I	Left-channel OPAMP positive input
–INR	2	I	Right-channel OPAMP negative input
+INR	1	I	Right-channel OPAMP positive input
$\overline{\text{Mute}}$	5	I	Mute, active-low
OUTL	12	O	Left-channel OPAMP output
OUTR	3	O	Right-channel OPAMP output
UVP	11	I	Undervoltage protection; connect to PVDD with a 10-kΩ resistor if function is unused.
VDD	9	P	Positive supply
VSS	6	P	Supply voltage

(1) I = input, O = output, P = power

Table: Pin functions

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	DC supply voltage	3	3.3	3.6	V
R_L	Load impedance		0.6	10		kΩ
V_{IL}	Low-level input voltage	$\overline{\text{Mute}}$		40		% of VDD
V_{IH}	High-level input voltage	$\overline{\text{Mute}}$		60		% of VDD
T_A	Operating free-air temperature		–40	25	85	°C

Table: Recommended operating conditions

SUB WOOFER MAIN AMPLIFIER (TAS5727)

Description

The TAS5727 is a 25-W, efficient, digital-audio power amplifier for driving stereo bridge-tied speakers.One serial data input allows processing of up to two discrete audio processors and MPEG decoders. The device accepts a wide range of input data and data rates. A fully programmable data path routes these channels to the internal speaker drivers.

The TAS5727 is a slave-only device receiving all clocks from external sources. The TAS5727 operates with a PWM carrier between a 384-kHz switching rate amd a 288-kHz switching rate, depending on the input sample rate. Oversampling combined with a fourth-order noise shaper provides a flat noise flor and excellent dynamic range from 20 Hz to 20 Khz.

Features

- Audio Input/Output
  - 25 W Into an 8-Ω Load From a 20-V Supply
  - Wide PVDD Range, From 8V to 26V
  - Supports BTL Configuration with 4- Ω Load
  - Efficient Class-D Operation Elminates Need for Heatsinks
  - One serial Audio Input (Two Audio Channels)
  - I^2C Address Selection Pin (Chip Select)
  - Single Output Filter PBTL Support
  - Supports 441-kHz to 48-kHz Sample Rate (LJ/RJ/I^2S)
- Audio/PWM Processing
  - Indepent Channel Volume Control With Gain of 24 dB to Mute With 0.125-dB Resolution Steps
  - Programmable Two-Band Dynamic-Range Control
  - 18 Programmable Biquads for Speaker EQ and Other Audio-Processing Features
  - Programmable Coefficients for DRC Filters
  - DC Blocking Filters
- General Features
  - I^2C Serial Control Interface Operational Without MCLK
  - Requires Only 3.3 V and PVDD
  - No External Oscillator: Internal Oscillator for Automatic Rate Detection
  - Surface-Mount, 48-Pin HTQFP Package
  - Thermal and Short-Circuit Protection
  - 106-dB SNR, A-Weighted
  - AD,BD, and Ternary Modulation
  - Up to 90% Efficient
  - PWM Level Meter to Measure the Digital Power Profile
- Benefits
  - EQ: Speaker Equalization Improves Audio Performance
  - Two-Band DRC: Dynamic Range Compression. Can Be Used As Power Limiter. Enables Speaker Protection, Easy Listening, Night-Mode Listening
  - Autodetect: Automatically Detects Sample-Rate Changes. No need for External Microprocessor Intervention
- Applications:
  - LCD TV, LED TV, Soundbar

T_A = 25°, PVCC_x = 18 V, DVDD = AVDD = 3.3 V, R_L = 8 Ω, BTL AD mode, f_S = 48 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	A_SEL_$\overline{FAULT}$ and SDA	I_{OH} = –4 mA DVDD = 3 V	2.4			V
V_{OL}	Low-level output voltage	A_SEL_$\overline{FAULT}$ and SDA	I_{OL} = 4 mA DVDD = 3 V			0.5	V
I_{IL}	Low-level input current		$V_I < V_{IL}$; DVDD = AVDD = 3.6V			75	µA
I_{IH}	High-level input current		$V_I > V_{IH}$; DVDD = AVDD = 3.6V			75(1)	µA
I_{DD}	3.3 V supply current	3.3 V supply voltage (DVDD, AVDD)	Normal mode		49	68	mA
			Reset ($\overline{RESET}$ = low, $\overline{PDN}$ = high)		23	38	
I_{PVDD}	Supply current	No load (PVDD_x)	Normal mode		32	50	mA
			Reset ($\overline{RESET}$ = low, $\overline{PDN}$ = high)		3	8	
$r_{DS(on)}$ (2)	Drain-to-source resistance, LS	T_J = 25°C, includes metallization resistance			75		mΩ
	Drain-to-source resistance, HS	T_J = 25°C, includes metallization resistance			75		
I/O Protection							
V_{uvp}	Undervoltage protection limit	PVDD falling			7.2		V
$V_{uvp,hyst}$	Undervoltage protection limit	PVDD rising			7.6		V
OTE (3)	Overtemperature error				150		°C
OTE_{HYST} (3)	Extra temperature drop required to recover from error				30		°C
I_{OC}	Overcurrent limit protection				4.5		A
I_{OCT}	Overcurrent response time				150		ns
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when drivers are in the high-impedance state to provide bootstrap capacitor charge.			3		kΩ

(1) I_{IH} for the PBTL pin has a maximum limit of 200 µA due to an internal pulldown on the pin.
(2) This does not include bond-wire or pin resistance.
(3) Specified by design

Table: Electrical Characteristics

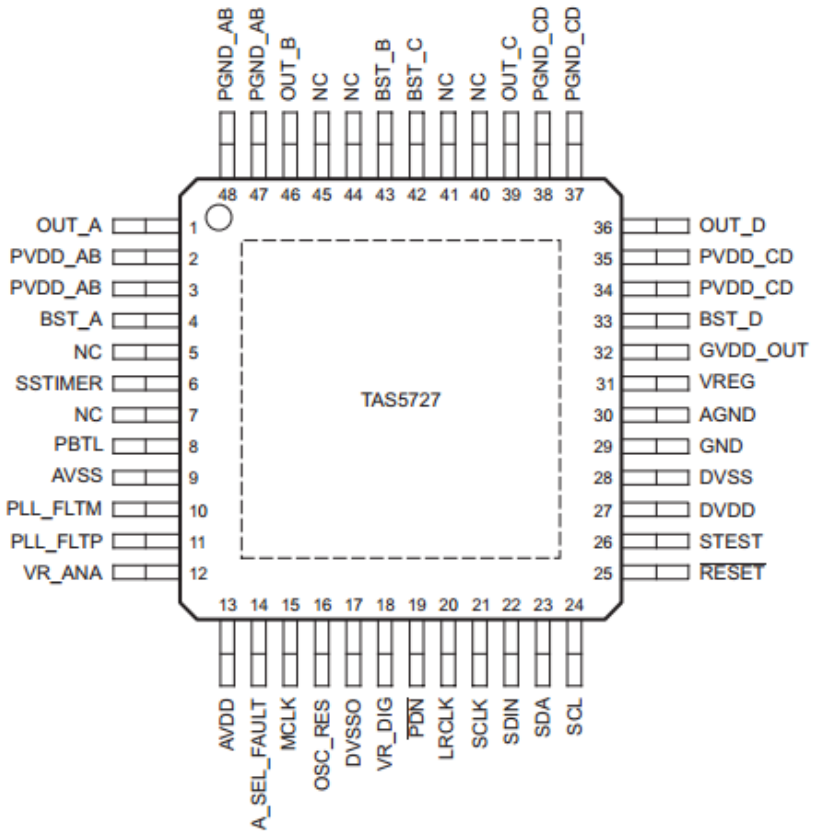


Figure: PHP Package (Top View)

PIN		TYPE[1]	5-V TOLERANT	TERMINATION[2]	DESCRIPTION
NAME	NO.				
AGND	30	P			Local analog ground for power stage
A_SEL_$\overline{\text{FAULT}}$	14	DIO			This pin is monitored on the rising edge of $\overline{\text{RESET}}$. A value of 0 (15-kΩ pulldown) sets the I^2C device address to 0x54 and a value of 1 (15-kΩ pullup) sets it to 0x56. this dual-function pin can be programmed to output internal power-stage errors.
AVDD	13	P			3.3-V analog power supply
AVSS	9	P			Analog 3.3-V supply ground
BST_A	4	P			High-side bootstrap supply for half-bridge A
BST_B	43	P			High-side bootstrap supply for half-bridge B
BST_C	42	P			High-side bootstrap supply for half-bridge C
BST_D	33	P			High-side bootstrap supply for half-bridge D
DVDD	27	P			3.3-V digital power supply
DVSS	28	P			Digital ground
DVSSO	17	P			Oscillator ground
GND	29	P			Analog ground for power stage
GVDD_OUT	32	P			Gate drive internal regulator output
LRCLK	20	DI	5-V	Pulldown	Input serial audio data left/right clock (sample-rate clock)
MCLK	15	DI	5-V	Pulldown	Master clock input
NC	5, 7, 40, 41, 44, 45	–			No connect
OSC_RES	16	AO			Oscillator trim resistor. Connect an 18.2-kΩ, 1% resistor to DVSSO.
OUT_A	1	O			Output, half-bridge A
OUT_B	46	O			Output, half-bridge B
OUT_C	39	O			Output, half-bridge C
OUT_D	36	O			Output, half-bridge D
PBTL	8	DI			Low means BTL mode; high means PBTL mode. Information goes directly to power stage.
$\overline{\text{PDN}}$	19	DI	5-V	Pullup	Power down, active-low. $\overline{\text{PDN}}$ prepares the device for loss of power supplies by shutting down the noise shaper and initiating the PWM stop sequence.
PGND_AB	47, 48	P			Power ground for half-bridges A and B
PGND_CD	37, 38	P			Power ground for half-bridges C and D
PLL_FLTM	10	AO			PLL negative loop-filter terminal
PLL_FLTP	11	AO			PLL positive loop-filter terminal
PVDD_AB	2, 3	P			Power-supply input for half-bridge output A
PVDD_CD	34, 35	P			Power-supply input for half-bridge output D
$\overline{\text{RESET}}$	25	DI	5-V	Pullup	Reset, active-low. A system reset is generated by applying a logic low to this pin. $\overline{\text{RESET}}$ is an asynchronous control signal that restores the DAP to its default conditions and places the PWM in the hard-mute (high-impedance) state.
SCL	24	DI	5-V		I^2C serial control clock input
SCLK	21	DI	5-V	Pulldown	Serial audio-data clock (shift clock). SCLK is the serial-audio-port input-data bit clock.
SDA	23	DIO	5-V		I^2C serial control data interface input/output
SDIN	22	DI	5-V	Pulldown	Serial audio data input. SDIN supports three discrete (stereo) data formats.
SSTIMER	6	AI			Controls ramp time of OUT_x to minimize pop. Leave this pin floating for BD mode. Requires capacitor of 2.2 nF to GND in AD mode. The capacitor determines the ramp time.
STEST	26	DI			Factory test pin. Connect directly to DVSS.
VR_ANA	12	P			Internally regulated 1.8-V analog supply voltage. This pin must not be used to power external devices.
VR_DIG	18	P			Internally regulated 1.8-V digital supply voltage. This pin must not be used to power external devices.
VREG	31	P			Digital regulator output. Not to be used for powering external circuitry.

Table: Pin Functions

4. POWER STAGE

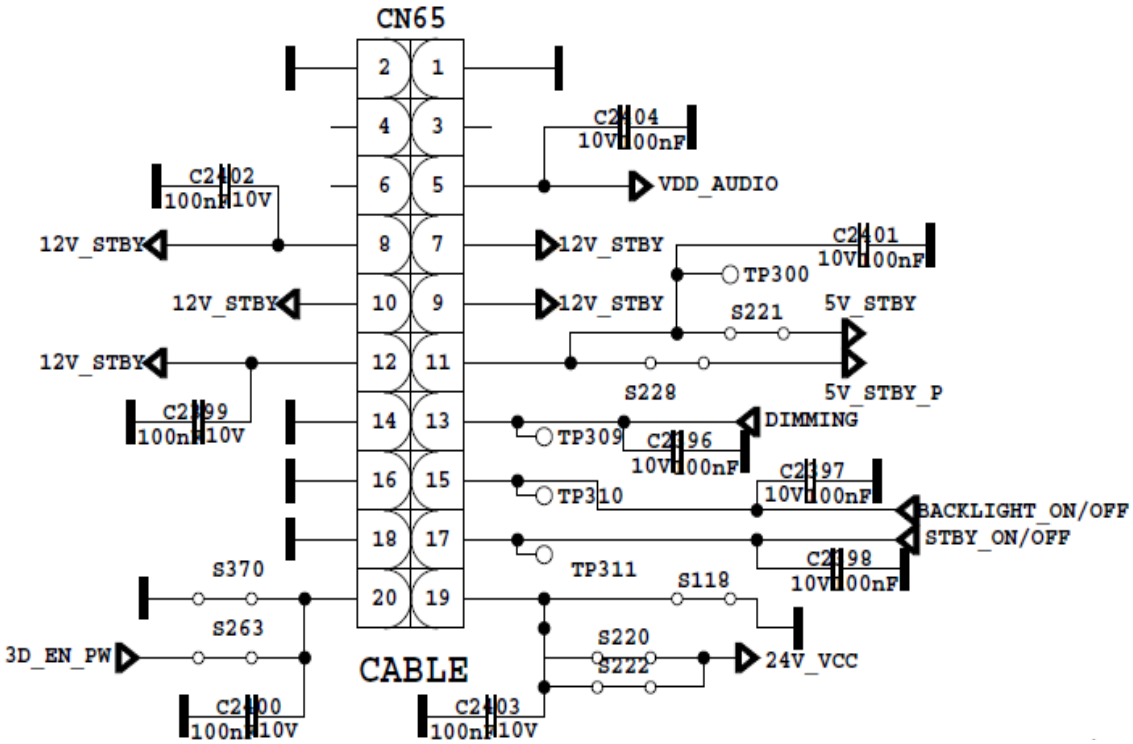


Figure: Power socket and options

Power socket is used for taking voltages which are 12V, 5V and 24V(VDD_Audio). These voltages are produced in power board. Also socket is used for giving dimming, backlight and standby signals with power board. It is shown in figure 7.

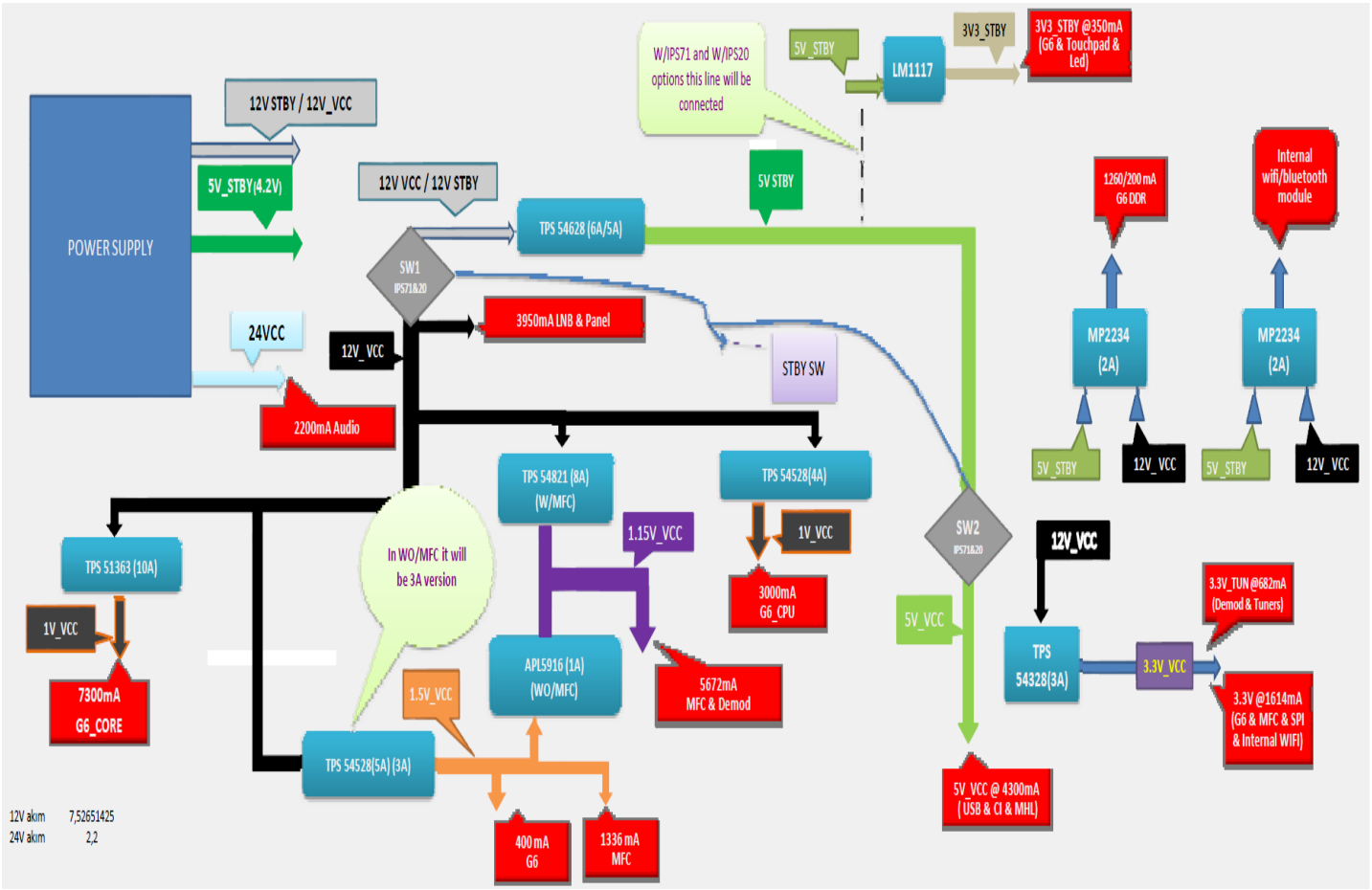


Figure: General illustration of voltage stages on main board

24V(VDD_Audio) goes directly to the audio side, through power socket other incoming voltages from power card are converted several voltages, shown in figure 8.

List of the components are:

- TPS54528
- TPS54328
- TPS54821
- TPS51363
- APL5910
- LM1117

TPS54528

General Description

The TPS54528 is an adaptive on-time D-CAP2 mode synchronous buck converter.The TPS54528 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54528 uses the D-CAP2 mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode operation at light loads. Eco-mode allows the TSP54528 to maintain high efficiency during lighter load conditions. The TPS54528 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR)output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 6 V. The device also features an adjustable soft start time. The TPS54528 is available in the 8-pin DDA package, and designed to operate from -40 C to 85 C.

Features

- D-CAP2 Mode Enables Fast Transient Response
- Low Output ripple and Allows Ceramic Output Capacitor
- Wide V_{IN} Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 6 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications- 65 mOhm (High Side) and 36 mOhm (Low Side)
- High Efficiency, less than 10 mikroAmper at shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 650-kHz Switching Frequency (f_{SW})
- Cycle By Cycle Over Current Limit
- Auto-Skip Eco-mode for High Efficiency at Light Load

Applications

- Wide Range of Applications for Low Voltage System
- Digital TV Power Supply
- High Definition Blu-ray Disc Players

- Networking Home Terminal
- Digital Set Top Box(STB)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		18	V
T_J	Junction temperature	–40		125	°C

Table: Recommended operating conditions

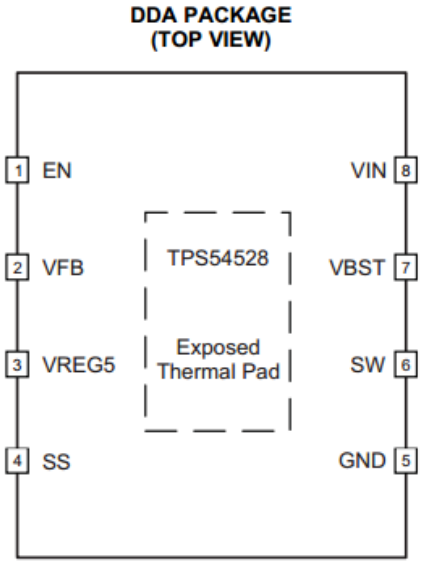


Figure: Pin Description

PIN		DESCRIPTION
NAME	NO.	
EN	1	Enable input control. EN is active high and must be pulled up to enable the device.
VFB	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	5.5 V power supply output. A capacitor (typical 1 µF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	Soft-start control. An external capacitor should be connected to GND.
GND	5	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	Switch node connection between high-side NFET and low-side NFET.
VBST	7	Supply input for the high-side FET gate drive circuit. Connect 0.1µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	Input voltage supply pin.
Exposed Thermal Pad	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

Table: Pin functions

TPS54328

General Description

The TPS54328 is an adaptive on-time D-CAP2 mode synchronous buck converter.The TPS54328 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54328 uses the D-CAP2 mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode operation at light loads. Eco-mode allows the TSP54328 to maintain high efficiency during lighter load conditions. The TPS54328 also has a proprietary circuit that enables the device to adopt to both low equivalent

series resistance (ESR)output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 7 V. The device also features an adjustable soft start time. The TPS54328 is available in the 8-pin DDA and 10-pin DRC packages, and is designed to operate over the ambient temperature range of -40C to 85C.

Features

- D-CAP2 Mode Enables Fast Transient Response
- Low Output ripple and Allows Ceramic Output Capacitor
- Wide V_{IN} Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 7 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications- 100 mOhm (High Side) and 70 mOhm (Low Side)
- High Efficiency, less than 10 mikroAmper at shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 700-kHz Switching Frequency (f_{SW})
- Cycle By Cycle Over Current Limit
- Auto-Skip Eco-mode for High Efficiency at Light Load

Applications

- Wide Range of Applications for Low Voltage System
- Digital TV Power Supply
- High Definition Blu-ray Disc Players
- Networking Home Terminal
- Digital Set Top Box(STB)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		18	V
T_J	Junction temperature	–40		125	°C

Table: Recommended operating conditions

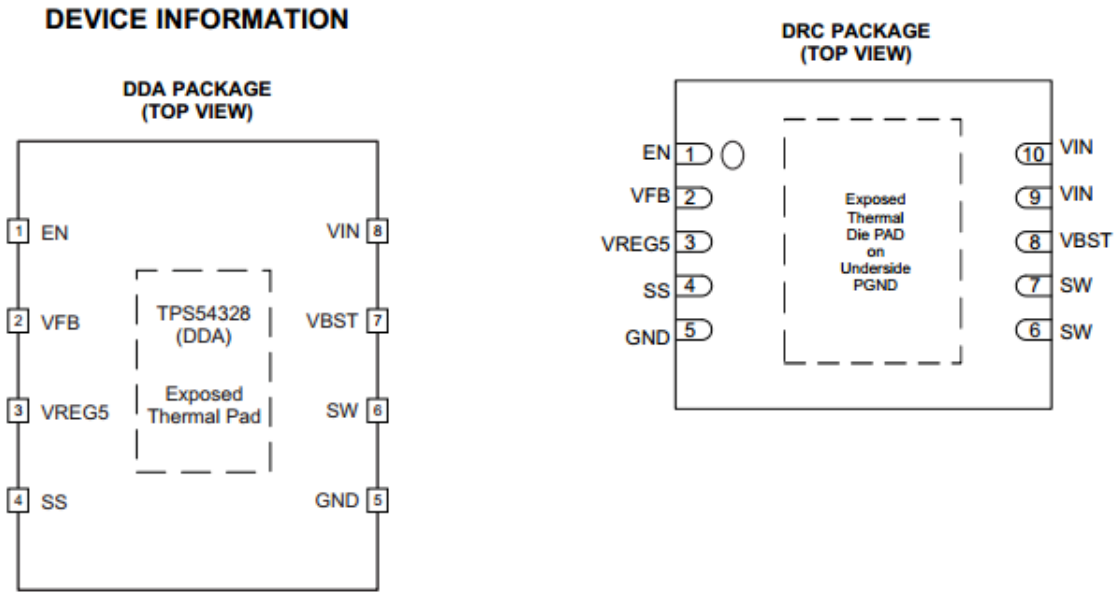


Figure: Pin Description

Pin #	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01µF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 18V power source. See *Input Capacitor*.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground (Connect the exposed pad to Pin 4).
5	FB	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage. The feedback threshold is 0.925V. See *Setting the Output Voltage*.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required. See *Compensation Components*.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. Attach to IN with a 100kΩ pull up resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1µF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.

Table: Pin functions

PIN			DESCRIPTION
NAME	DDA	DRC	
EN	1	1	Enable input control. Active high.
VFB	2	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	3	5.5 V power supply output. A capacitor (typical 1 µF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	4	Soft-start control. An external capacitor should be connected to GND.
GND	5		Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
GND		5	Ground pin. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	6, 7	Switch node connection between high-side NFET and low-side NFET.
VBST	7	8	Supply input for the high-side FET gate drive circuit. Connect 0.1µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	9, 10	Input voltage supply pin.
Exposed Thermal Pad	Back side		Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.
Exposed Thermal Pad		Back side	Thermal pad of the package. PGND power ground return of internal low-side FET. Must be soldered to achieve appropriate dissipation.

Table: Pin description

TPS51363

General Description

The TPS51363 is a high-voltage input, synchronous converter with integrated FET, based on D-CAP2™ control topology, which enables fast transient response and supports both POSCAP and all MLCC output capacitors. TI proprietary FET technology combined with TI leading-edge package technology provides the highest density solution for single-output power rail such as VCCIO and VDDQ for DDR notebook memory, or any point-of-load (POL) in wide application. The feature set includes switching frequency of 400 kHz and 800 kHz. Programmable soft-start time with an external capacitor. auto skip, pre-bias startup, integrated bootstrap switch, power good, enable and a full suite of fault protection schemes, including OCL, UVP, OVP, 5-V UVLO and thermal shutdown. It is packaged in 3.5 mm × 4.5 mm, 0.4-mm pitch, 28-pin QFN (RVE), and specified from -10°C to 85°C.

Features

- Input Voltage Range: 3 V to 22 V
- Output Voltage Range: 0.6 V to 2 V
- 8-A or 10-A Integrated FET Converter
- Fewest External Components
- Soft-Start Time Programmable by External Capacitor
- Switching Frequency: 400 kHz and 800 kHz
- D-CAP2™ Architecture to Enable POSCAP and All MLCC Output Capacitor Usage
- Integrated and Temperature Compensated Low-Side On-Resistance Sensing for Accurate OCL Protection
- Powergood Output OCL, OVP, UVP and UVLO Protections
- Thermal Shutdown (non-latch)
- Output Discharge Function Table 1. Current Ratings
- Integrated Boost MOSFET Switch
- 28-Pin, 3.5-mm × 4.5-mm, RVE, QFN Package with 0.4-mm Pitch and 1-mm Height

Applications

- Notebook Computers (VCCIO)
- Memory Rails (DDR VDDQ)

		MIN	MAX	UNIT
Supply voltage range	VIN	3	22	V
	V5	4.6	5.5	
Input voltage range	BST	–0.1	33.5	
	SW	–3	27	
	EN, TRIP, NU, MODE	–0.1	5.5	
	SLEW, VSNS, REFIN, REFIN2	–0.1	3.5	
	GSNS	–0.1	0.3	
	PGND	–0.1	0.1	
Output voltage range	PGOOD	–0.1	5.5	
	VREF, SLEW	–0.1	3.5	
Operating free-air temperature, T_A		–10	85	°C

Table: Recommended operating conditions

RVE PACKAGE
28 PINS
(TOP VIEW)

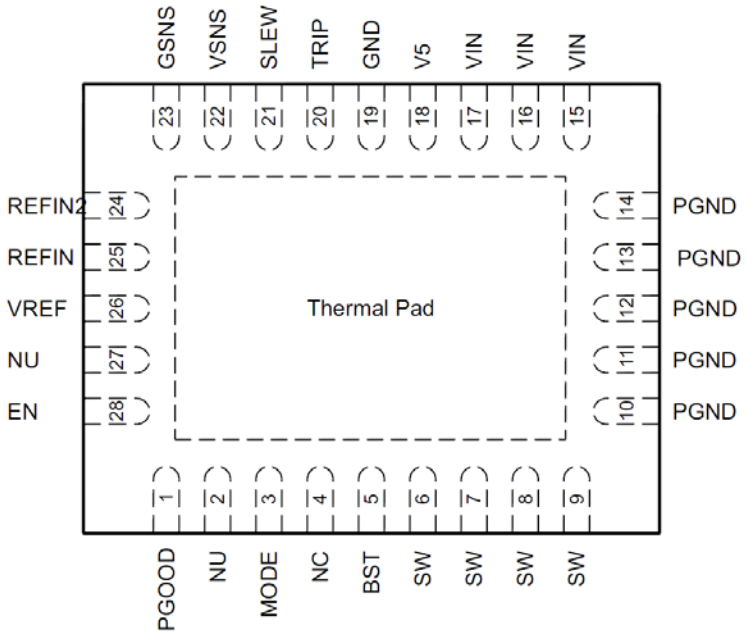


Figure: Pin Description

NAME	NO.	I/O/P	DESCRIPTION
BST	5	I	Power supply for internal high side MOSFET. Connect a 0.1-µF bootstrap capacitor between this pin and SW pin.
EN	28	I	Enable signal, 1.05-V logic compatible.
GND	19	—	General device ground.
GSNS	23	O	GND sense input. Connect GSNS to general/system ground or GND sensing point at the output return.
MODE	3	I	Frequency (400 kHz or 800 kHz) programmable input.
NC	4	—	Not connected.
NU	2, 27	—	Not used for external applications.
PGND	10	—	Power ground. Connect to the system ground.
	11		
	12		
	13		
	14		
PGOOD	1	O	PGOOD output. Connect a pull-up resistor with a value of 100 kΩ to this pin.
Power PAD	29	—	Connect to system ground by multiple vias.
REFIN	25	I	Target output voltage input pin. 0.6 V to 2 V, 1.05 V/1.2 V built-in (GND and Open).
REFIN2	24	I	Tie to GND or float. This input is used to determine the fixed voltage setpoint.
SLEW	21	O	Connect a capacitor between this pin and GND for soft start and integrator functions.
SW	6	O	Switching node output. Connect external inductor.
	7		
	8		
	9		
TRIP	20	I	OCL programmable input.
V5	18	I	5-V power supply for analog circuits and gate driver.
VIN	15	I	Power supply input pin. Apply 3-V to 22-V of supply voltage.
	16	I	
	17	I	
VREF	26	O	2-V reference output. Connect A 0.22-µF ceramic capacitor between this pin and the GNDS pin.
VSNS	22	I	Output voltage sense input.

Table: Pin functions

TPS54821

General Description

The TPS54821 in thermally enhanced 3.5 mm x 3.5 mm QFN package is a full featured 17 V, 8 A synchronous step down converter which is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are achieved through current mode control, which reduces component count, and by selecting a high switching frequency, reducing the inductor's footprint. The output voltage startup ramp is controlled by the SS/TR pin which allows operation as either a stand alone power supply or in tracking situations. Power sequencing is also possible by correctly configuring the enable and the open drain power good pins. Cycle by cycle current limiting on the high-side FET protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-side MOSFET to prevent excessive reverse current. Hiccup protection will be triggered if the overcurrent condition has persisted for longer than the preset time. Thermal hiccup protection disables the device when the die temperature exceeds the thermal shutdown temperature and enables the part again after the built-in thermal shutdown hiccup time.

Features

- Integrated 26 mΩ / 19 mΩ MOSFETs
- Split Power Rail: 1.6 V to 17 V on PVIN
- 200 kHz to 1.6 MHz Switching Frequency
- Synchronizes to External Clock
- 0.6V ±1% Voltage Reference Over Temperature
- Low 2 μA Shutdown Quiescent Current
- Monotonic Start-Up into Pre-biased Outputs
- –40°C to 125°C Operating Junction Temperature Range
- Adjustable Input Undervoltage Lockout
- Adjustable Slow Start/Power Sequencing
- Power Good Output Monitor for Undervoltage and Overvoltage
- Adjustable Input Undervoltage Lockout

Applications

- Digital TV Power Supplies
- Set Top Boxes
- Blu-ray DVDs
- Home Terminals

		VALUE		UNIT
		MIN	MAX	
Input Voltage	VIN	–0.3	20	V
	PVIN	–0.3	20	
	EN	–0.3	6	
	BOOT	–0.3	27	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	6	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	6	
Output Voltage	BOOT-PH	0	7.5	V
	PH	–1	20	
	PH 10ns Transient	–3	20	
Vdiff (GND to exposed thermal pad)		–0.2	0.2	V
Source Current	RT/CLK		±100	µA
	PH		Current Limit	A
Sink Current	PH		Current Limit	A
	PVIN		Current Limit	
	COMP		±200	µA
	PWRGD	–0.1	5	mA
Electrostatic Discharge (HBM) QSS 009-105 (JESD22-A114A)			2	kV
Electrostatic Discharge (CDM) QSS 009-147 (JESD22-C101B.01)			500	V
Operating Junction Temperature		–40	125	°C
Storage Temperature		–65	150	

Table: Recommended operating conditions

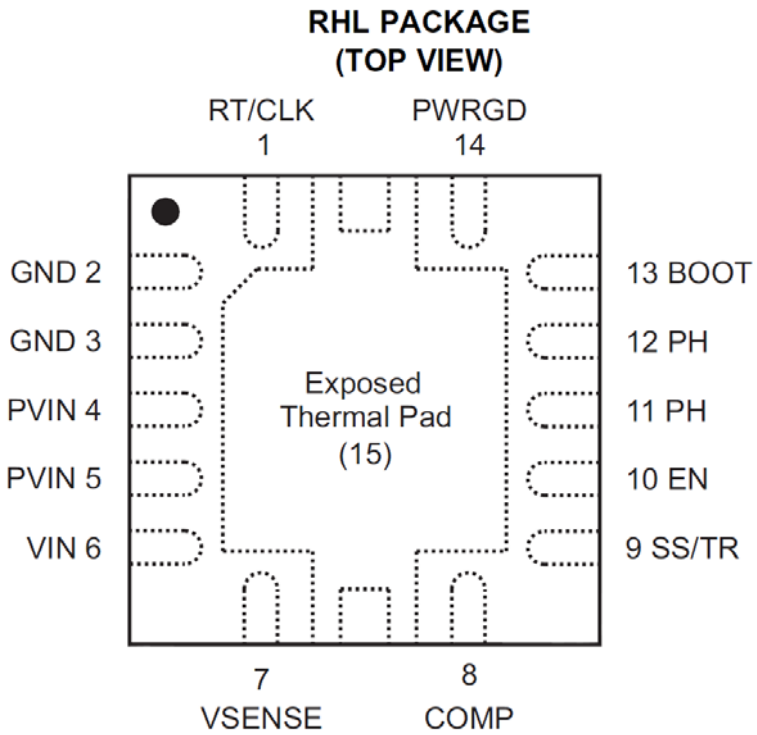


Figure: Pin Description

PIN		DESCRIPTION
NAME	NO.	
RT/CLK	1	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device; In CLK mode, the device synchronizes to an external clock.
GND	2, 3	Return for control circuitry and low-side power MOSFET.
PVIN	4, 5	Power input. Supplies the power switches of the power converter.
VIN	6	Supplies the control circuitry of the power converter.
VSENSE	7	Inverting input of the gm error amplifier.
COMP	8	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
SS/TR	9	Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing.
EN	10	Enable pin. Float to enable. Adjust the input undervoltage lockout with two resistors.
PH	11, 12	The switch node.
BOOT	13	A bootstrap cap is required between BOOT and PH. The voltage on this cap carries the gate drive voltage for the high-side MOSFET.
PWRGD	14	Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, over-voltage, EN shutdown or during slow start.
Exposed Thermal PAD	15	Thermal pad of the package and signal ground and it must be soldered down for proper operation.

Table: Pin functions

MP2234

General Description

The MP2234 is a high frequency synchronous rectified step-down switch mode converter with built in internal power MOSFETs. It offers a very compact solution to achieve 3A continuous output current over a wide input supply range with excellent load and line regulation. The MP2234 has synchronous mode operation for higher efficiency over output current load range. Current mode operation provides fast transient response and eases loop stabilization. Full protection features include OCP and thermal shut down. The MP2234 requires a minimum number of readily available standard external components and is available in a space saving 8-pin TSOT23 package.

Features

- Wide 4.5V to 16V Operating Input Range
- 2A Load Current
- 100mΩ/40mΩ Low Rds(on) Internal Power MOSFETs
- High Efficiency Synchronous Mode Operation
- Fixed 800kHz Switching Frequency
- Frequency Sync from 300kHz to 2MHz External Clock
- Power Save Mode at Light Load
- External Soft Start
- OCP Protection and Hiccup

- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an 8-pin TSOT-23 package

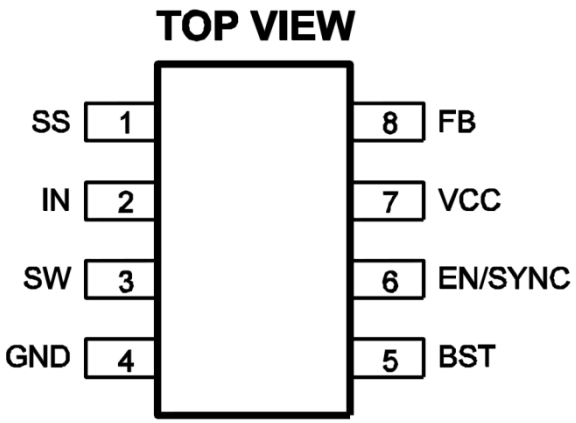


Figure: Pin description

Package Pin #	Name	Description
1	SS	Soft-Start. Connect an external capacitor to program the soft start time for the switch mode regulator.
2	IN	Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The MP2234 operates from a +4.5V to +16V input rail. Requires a low-ESR, and low-inductance capacitor (C1) to decouple the input rail. Place the input capacitor very close to this pin and connect it with wide PCB traces and multiple vias.
3	SW	Switch Output. Connect to the inductor and bootstrap capacitor. This pin is driven up to V_{IN} by the high-side switch during the PWM duty cycle ON time. The inductor current drives the SW pin negative during the OFF time. The ON resistance of the low-side switch and the internal body diode fixes the negative voltage. Connect using wide PCB traces and multiple vias.
4	GND	System Ground. Reference ground of the regulated output voltage. PCB layout Requires extra care. For best results, connect to GND with copper and vias.
5	BST	Bootstrap. Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver.
6	EN/SYNC	Enable. EN=high to enable the MP2234. Apply an external clock change the switching frequency. For automatic start-up, connect EN pin to V_{IN} with a 100kΩ resistor.
7	VCC	Internal 5V LDO output. Powers the driver and control circuits. Decouple with 0.1μF-to-0.22μF capacitor. Do not use a capacitor ≥0.22μF.
8	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 400mV to prevent current limit runaway during a short circuit fault. Place the resistor divider as close to the FB pin as possible. Avoid placing vias on the FB traces.

Table: Pin functions

APL5910

General Description

The APL5910 is a 1A ultra low dropout linear regulator. The IC needs two supply voltages, one is a control voltage (VCNTL) for the control circuitry, the other is a main supply voltage (VIN) for power conversion, to reduce power dissipation and provide extremely low dropout voltage. The APL5910 integrates many functions. A Power-On- Reset (POR) circuit monitors both supply voltages on VCNTL and VIN pins to prevent erroneous operations. The functions of thermal shutdown and current-limit protect the device against thermal and current over-loads. A POK indicates that the output voltage status with a delay time set internally. It can control other converter for power sequence. The APL5910 can be enabled by other power systems. Pulling and holding the EN voltage below 0.4V shuts off the output.

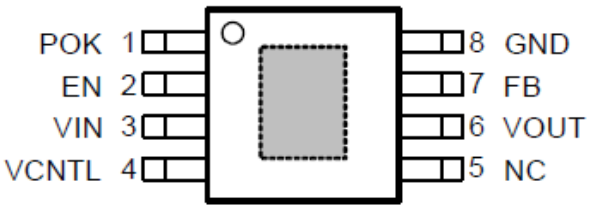
The APL5910 is available in a SOP-8P package which features small size as SOP-8 and an Exposed Pad to reduce the junction-to-case resistance to extend power range of applications.

Features

- Ultra Low Dropout
  - 0.12V (Typical) at 1AOutput Current
- 0.8V Reference Voltage
- High Output Accuracy
  - ±1.5%over Line, Load, and Temperature Range
- Fast Transient Response
- Adjustable Output Voltage
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Current-Limit and ShortCurrent-Limit Protections
- Thermal Shutdown with Hysteresis
- Open-Drain VOUT Voltage Indicator (POK)
- Low Shutdown Quiescent Current (< 30mA)
- Shutdown/Enable Control Function
- Simple SOP-8P Package with Exposed Pad
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Motherboards, VGA Cards
- Notebook PCs
- Add-in Cards
-



SOP-8P (Top View)

Figure: Pin configuration

Symbol	Parameter		Range	Unit
V_{CNTL}	VCNTL Supply Voltage		3.0 ~ 5.5	V
V_{IN}	VIN Supply Voltage		1.0 ~ 5.5	V
V_{OUT}	VOUT Output Voltage (when V_{CNTL}-V_{OUT}>1.4V)		0.8 ~ V_{IN} - V_{DROP}	V
I_{OUT}	VOUT Output Current		0 ~ 1	A
R2	FB to GND		1k ~ 24k	Ω
C_{OUT}	VOUT Output Capacitance	I_{OUT}=1A at 25% nominal V_{OUT}	8 ~ 600	μF
		I_{OUT}=0.5A at 25% nominal V_{OUT}	8 ~ 900	
		I_{OUT}=0.25A at 25% nominal V_{OUT}	8 ~ 1100	
ESR_{COUT}	ESR of VOUT Output Capacitor		0 ~ 200	mΩ
T_A	Ambient Temperature		-40 ~ 85	°C
T_J	Junction Temperature		-40 ~ 125	°C

Table: Recommended operating conditions

PIN		FUNCTION
NO.	NAME	
1	POK	Power-OK signal output pin. This pin is an open-drain output used to indicate the status of output voltage by sensing FB voltage. This pin is pulled low when output voltage is not within the Power-OK voltage window.
2	EN	Active-high enable control pin. Applying and holding the voltage on this pin below the enable voltage threshold shuts down the output. When re-enabled, the IC undergoes a new soft-start process. When left this pin open, an internal pull-up current (5μA typical) pulls the EN voltage and enables the regulator.
3	VIN	Main supply input pin for voltage conversions. A decoupling capacitor (≥10μF recommended) is usually connected near this pin to filter the voltage noise and improve transient response. The voltage on this pin is monitored for Power-On-Reset purpose
4	VCNTL	Bias voltage input pin for internal control circuitry. Connect this pin to a voltage source (+5V recommended). A decoupling capacitor (1μF typical) is usually connected near this pin to filter the voltage noise. The voltage at this pin is monitored for Power-On-Reset purpose.
5	NC	No Connection.
6	VOUT	Output pin of the regulator. Connecting this pin to load and output capacitors (10μF at least) is required for stability and improving transient response. The output voltage is programmed by the resistor-divider connected to FB pin. The VOUT can provide 1A (max.) load current to loads. During shutdown, the output voltage is quickly discharged by an internal pull-low MOSFET.
7	FB	Voltage Feedback Pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.

Table: Pin description

LM1117

General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V.

The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

The LM1117 series is available in LLP, TO-263, SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10μF tantalum capacitor is required at the output to improve the transient response and stability.

Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 and LLP Packages

- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range:
  - LM1117 0˚C to 125˚C
  - LM1117I −40˚C to 125˚C

Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators
- Battery Charger
- Battery Powered Instrumentation

5. MICROCONTROLLER (MSTAR MSD95C0H)

General Description

The MSD95C0H is MStar's most up-to-date system-on-chip solution for flat panel integrated digital television products. Building on the success of MStar's advanced technologies, the MSD95C0H hosts the most advanced picture processing engine, MStarACE-PRO3^{UC}, for all the *Experts* in various of TV video quality tuning fields to develop the state-of-the-art DTV system. The powerful CPUs and GPUs deliver high performance for modern Linux and Android TVs. The popular ARM and Mali architecture ensures the best software compatibility. Applications with HTML5, Java, Flash, etc., can be realized on MSD95C0H with minimized developer efforts.

MACE-PRO3^{UC}, the Professional UC Edition of MStar video processor, includes all MStar's successful color-tuning tools and a newly added multi-dimensional color/sharpening/NR formula that can quickly reflect subtle or sudden changes in even darker, brighter, or mixture scenes. With this ultimate color processor, a specially designed color remapping system for modern wide gamut displays, and an easy-to-use color-tool UI, developers can quickly and easily identify PQ characteristic from the most high-end panel models to the most conventional panel models. MStar's innovated UltraClear DTV video processor adopts multi-frame video recovery technology to perfectly restore the contents/details, and eliminate the noise/artifacts from broadcasting or Internet videos.

MSD95C0H also integrates all-purpose AV decoders for DTV/multi-media applications, ATSC/QAM, DVB-T, DVB-C, ISDB-T, DTMB Demadulators and Sound/Video processors into a single device. This allows the overall BOM to be reduced significantly and making the MSD95C0H a very cost effective multi-standard DTV solution.

MSD95C0H enables feature rich products that bring differentiation to the iDTV market. By the use of powerful CPU/GPU and AV decoders capable of decoding a plethora of high definition content from Ethernet, USB 3.0 connectivity and MHL. MSD95C0H based systems can provide a high quality media-center experience.

MSD95C0H provides legacy multi-standard analog TV support with adaptive 3D video decoding and VBI data extraction. Similarly the audio decoder is capable of decoding FM, AM, NICAM, A2, BTSC and sound standards.

The MSD95C0H supplies all the necessary A/V inputs and outputs to complete a receiver design including a multi-port HDMI receiver and component video ADC. All input selections multiplexed for video and audio are integrated, including full SCART supported with CVBS output.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, MSD95C0H has an ultra low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

Features

MSD95C0H is a highly integrated smart TV solution which supports dual channel 8/10bit LVDS output, DTV channel decoding, MPEG decoding, VP decoding, 3D formatter, and security OS. MSD95C0H serves full functions of multi-media centers with a high performance CPU, GPU, and AV CODEC/security engines.
Key features includes:

1. *ATSC/DVB-C/DVB-T/DTMB/ISDB-T Front-End Demodulator*
2. *Advanced ARM CPU and 3D GPU*
3. *3D Formatter Engine*
4. *Multi-Standard A/V Format Decoder*
5. *The MACE-PRO3^{UC} Video Processor*
6. *Home Theater Sound Processor*
7. *Internet and Variety of Connectivity Support*
8. *Peripheral and Power Management*
9. *Robust and Efficient Security Engine*
10. *Full Multi-Media Decoders Including HEVC Decoder Supporting up to UHD/60fps Resolution*

- High Performance Micro-processor
  - ARM Cortex Advanced CPU
  - 32KB/32KB I/D cache
  - 512KB L2 cache
  - Supports Neon instruction sets
- 3D Graphic GPU
  - ARM MaliT760 GPU
  - Supports OpenGL ES 1.1/2.0/3.1
  - Supports OpenGL VG 1.1
  - Support DirectX 11.1
  - Supports rendering size up to UHD
- Transport Stream De-multiplexer
  - Supports five parallel TS interfaces, with or without sync signal
  - Supports two programmable TS input/output for external CI module
  - Supports external demodulators
  - TS data rate is 120Mbit/s for serial and 24MByte/s for parallel
  - 144 general purpose PID filters and 128 section filters for all transport stream de-multiplexer
  - Supports additional audio/video/PCR filters
  - Supports TS DMA channel for time-shift
  - Supports 3DES/DES and AES encryption/decryption
- MPEG-2 Video Decoder
  - ISO/IEC 11172-2 MPEG-1 video format decoding
  - ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
  - Supports resolution up to HDTV (1080p, 1080i, 720p) and SDTV
  - Supports dual stream decoding for 3D content
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
  - Supports resolutions up to HDTV (1080p@30fps)
  - Supports DivX[1] Home Theater & HD profiles^{Optional}
  - Supports FLV version1 video format decoding
  - Supports dual stream decoding for 3D content

- H.264 Decoder
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 5.0) video decoding
  - Supports SVAF 2ES (for Dual Decode)
  - Profile Level 5 with bitrate up to 135Mbps, the upper limit of level 5
  - Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
  - Supports resolution up to 4096x2160@30fps
  - Supports CABAC and CAVLC stream types
  - Processing of ES and PES streams, extraction and provision of time stamps
- H.264 MVC Decoder
  - ITU-T H.264, ISO/IEC 14496-10 video decoding (Main and high profile up to level 4.2)
  - Supports resolution up to 1080p@60fps
- VP Decoder Optional
  - Supports VP8 decoder
  - Supports resolution up to 1920x1080@30p
  - Supports maximum bitrate upto 50Mbps
- Google VP9:
  - Support profile 0 -4:2:0 subsampling, 8-bit color depth
  - HW decoder supports resolution and frame rate upto 4k@30fps
  - Supports bitrate upto 100Mbps
- AVS+ Decoder Optional
  - Supports Broadcasting profile, level 6.0.1.08.60
  - Supports Jizhun profile, level 6.0
  - Supports bitrate up to 50Mbps
  - Supports resolution up to 1920x1080 @60fps
  - Supports dual stream decoding
- RealMedia Decoder Optional
  - Supports maximum resolution up to 1080p@30fps
  - Supports RV8, RV9, RV10 decoders
  - Supports file formats with RM and RMVB
  - Supports Picture Re-sampling
  - Supports in-loop de-block for B-frame
  - Supports dual stream decoding
- HEVC (H.265) Decoder
  - Supports Main/Main-10 profile, level 5.1, high tier
  - Supports resolution up to 4096x2160@60fps
  - Supports bitrate upto 110Mbps, the upper limit of level 5 and high-tier.
- H.264 Encoder
  - Supports H.264 baseline encoding, main profile encoding, level 4.0
  - Supports MVs: 16x16, 16x8, 8x16, 8x4, 4x8, 4x4
  - Supports up to quarter-pel
  - Maximum output resolution: 1920x1080@30fps
- Hardware PNG / GIF Decoder
  - Supports up to 8192 x 8192 (per channel 8 bits), or 4096 x 8192(per channel 16 bits) pixel image
  - PNG format 1bpp/2bpp/4bpp/8bpp index(palette) mode support
  - PNG transparency mode support
  - Interlaced / non-interlaced GIF support
  - ARGB8888, RGB565, YUV422(YUYV),YUV422(YVYU),gray, gray with alpha output format support
- Hardware JPEG Decoder
  - Supports sequential mode, single scan
  - Supports both color and grayscale pictures
  - Following the file header scan the hardware decoder fully handles the decode process
  - Supports programmable Region of Interest (ROI)
  - Supports formats: 422/411/420/444/422T
  - Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
  - Supports 1280x720@30p

- VC-1 Video Decoder[Optional]
  - Supports SMPTE-421 (WMV video) decoding up to MH@HL
  - Supports SMPTE-421 (VC1 video) decoding up to AP@L3
  - Supports dual stream decoding for 3D content
- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
  - Automatic standard detection
  - Motion adaptive 3D comb filter
  - Three configurable CVBS & Y/C S-video inputs
  - Supports Teletext, Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE
- Multi-Standard TV Sound Processor
  - Supports BTSC/A2 demodulation
  - Supports NICAM/FM/AM demodulation
  - Supports MTS Mode Mono/Stereo/SAP in BTSC mode
  - Supports Mono/Stereo/Dual in A2/NICAM mode
  - Built-in audio sampling rate conversion (SRC)
  - Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
  - Advanced sound processing options available, for example: Dolby[2], DTS[3]
  - Supports digital audio format decoding:
    - MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3)[Optional], AAC-LC, HE-AAC, WMA, and WMA9 Pro
    - Supports[3Optional] Dolby Digital Plus, Dolby Pulse, and MS10/MS11 multistream decoder, including Dolby Digital Encoder for trans-coding streams to Dolby Digital 5.1(DDCO)
  - Supports Audio Description
  - Supports MPEG audio encoding
  - Supports time-shifting PVR
  - Supports programmable delay for audio/video synchronization
- Audio Interface
  - Four L/R audio line-inputs
  - Two L/R outputs for main speaker and one additional line-output
  - Supports stereo headphone driver
  - I2S digital audio output and input
  - S/PDIF digital audio output and input
  - Supports HDMI receiver ARC function
- Analog RGB Compliant Input Ports
  - Three analog ports support up to 1080P
  - Supports PC RGB input up to SXGA@75Hz
  - Supports HDTV RGB/YPbPr/YCbCr
  - Supports Composite Sync and SOG Sync-on-Green
  - Automatic color calibration
- Analogue RGB Auto-Configuration & Detection
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset and gain configuration
  - Sync Detection for H/V Sync
- DVI/HDCP/HDMI/MHL Compliant Input Ports
  - Four HDMI/DVI Input ports
  - HDMI 2.0 Compliant
  - MStar iSwitch for fast HDMI switching
  - HDCP 1.4/2.2 Compliant
  - Up to 600MHz @ 4K2K 60Hz 444 8-bit mode or 422 12-bit mode
  - Supports HDMI CEC
  - Supports HDMI 3D formats
  - Supports HDMI ARC
  - Single link DVI 1.0 compliant
  - Robust receiver with excellent long-cable support
- MHL Input Ports
  - One MHL Input port (combo with HDMI/DVI)
  - MHL 2.1 compliant
  - Supports up to 150MHz @ 1080p 24/30/60Hz MHL input signal

- MStar Advanced Color Engine - Professional UC Edition (MACE-PRO3^{UC})
  - 10/12-bit internal Data Processing
  - Dual-Engine Architecture supporting PIP/PBP
  - MACE-PRO3^{UC} Advanced Scaling Engine:
    - Multi-directional Scaling Technology
    - High-Tap Filters with Programmable Parameter
    - De-jagging Support
    - Video Feather Artifact Detection and Removal
    - Nonlinear Video Scaling
    - Dynamic Scaling for RM, VC-1^{Optional}
  - MACE-PRO3^{UC} DTV Video Processing Technology:
    - UltraClear-PRO3 Video Deinterlacing with Motion Object Stabilizer
    - Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
    - Automatic 3:2/2:2/M:N Pull-Down Detection and Recovery
    - UltraClear-PRO3 Noise Reduction
    - Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming
    - MACE^{LIVE}-PRO Color Engine with Accurate Color Tuning Support
    - Cross-Color Suppression Support
    - Supports Hanging Dot Search & Removal
    - UltraClear-Based De-Flickering
    - MPEG Artifact Removal Including Blocking and Mosquito Noise Cancellation
    - Arbitrary Frame Rate Conversion
  - MACE-PRO3^{UC} Picture Enhancement:
    - Enhancements in All Features of MACE-3/4 Engine
    - Super Resolution for Detail Enhancement & Recovery
    - Scene Detection
    - 3D Adaptive Color Control
    - 3D Adaptive Sharpness Control
    - sRGB and xvYCC Color Processing Engine
    - Supports HDMI 1.4 Deep Color Format
    - Supports HDMI 1.4 sYCC601 / AdobeRGB / AdobeYCC601 Color Formats
    - Supports BT.2020 Color Space
    - Supports Enhanced and Seamless Color Mapping for Wide Gamut Panels
  - Programmable 12-bit RGB gamma CLUT
  - Top/Bottom, Left-Right and ChessBoard 3D Format Auto-Detection
  - Supports 2D to 3D conversion
- Output Interface
  - Single/Dual link 8/10-bit LVDS output/Mini-LVDS output
  - 8 lane 8/10-bit Vby1 output (configurable width: 2/4/8 lane)
  - Supports programmable timing controller
  - Supports panel resolution up to Full HD 1920x1080@ 60Hz (LVDS 2ch)
  - Supports panel resolution up to Ultra HD 4k2k@ 60Hz (Vby1 8 lane)
  - Supports dithering options
  - Spread spectrum output frequency for EMI suppression
  - Supports direct and edge types local dimming
  - Supports 60Hz 3D polarizd panel (line interleave)
  - Supports Cinema output mode
- CVBS Video Encoder
  - Supports all NTSC/PAL TV Standard
  - Stand-alone scaling engine (no vertical scaling up)
  - Programmable Hue, Contract, Brightness
  - Supports TTX/CC/WSS output
- CVBS Video Output
  - Allows CVBS output of digital content to SCART
  - Supports on-line CVBS bypass output

- 2D Graphics Engine
  - Hardware Graphics Engine for responsive interactive applications
  - Supports point draw, line draw, rectangle draw/fill and text draw
  - Supports BitBlt, stretch BitBlt, italic Bitblt, Mirror BitBlt and rotate BitBlt
  - Supports alpha-blending operation
  - Supports source/destination color key and alpha key
  - Supports dither
  - Supports color format conversion and format transformation
  - Raster Operation (ROP)
  - Support DFB and Porter-Duff operation
- VIF Demodulator
  - Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
  - Supports IF/low IF architecture, IF includes single SAW and SAWless tuner
  - Audio/Video internal dual-path processor
- ATSC/QAM Demodulator
  - ATSC A/53 compliant 8VSB
  - ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - Integrated deinterleaver RAM for Level 1 J =1 and Level 2 J= 1,2,3.4
  - Supports IF/low IF interfaces
  - I2C repeater for tuner control from backend host controller
  - 2010 - A74 compliant
- DVB-C Demodulator
  - ITU J.83 Annex A/C DVB-C (EN 300 429) compliant
  - Supports 1-7.2 M Baud symbol rate
  - Automatic blind channel scan (constellation and symbol rate)
  - Supports IF/low IF interfaces
- DVB-T Demodulator
  - Compliant with DVB-T (ETSI EN 300 744)
  - Accept IF/low IF inputs in 6, 7, 8MHz channel bandwidths
  - Supports all guard intervals (1/32 to 1/4)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM
  - Ultra fast automatic blind UHF/VHF channel scan
  - Nordig 2.2.2, D-book 7.0
  - Optimized for SFN channels with pre/post-cursive echoes inside/outside the guard
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
- DTMB Demondulator
  - Compliant with DTMB GB 20600-2006
  - Support all valid combinations of FH mode, modulation, code rate and interleaving mode
  - Support LIF/IF interfaces
  - Automatic co-channel and adjacent channel interference suppression
  - CCI and ACI rejection capability
  - Impulse-noise suppression
- ISDB-T Demodulator
  - Compliant with ISDB-T ARIB STD-B31
  - Compliant with ISDB-Tsb ARIB STD-B29
  - Supports all modes defined in ISDB-T spec
  - Supports all guard ratios: 1/4, 1/8, 1/16, 1/32
  - 42ms/channel, excluding AGC time and PLL sync
  - Support IF/low IF interfaces
  - Impulse-noise suppression

- Connectivity
  - Three USB 2.0 host ports
  - Two USB 3.0 host ports
  - USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
  - USB port supports efficient battery charger
  - Embedded 10/100 PHY
  - Support Ethernet Wake-On-Lan

- Miscellaneous
  - DRAM interface three channel, 32bitx3 DRAM bus up to six 16-bit DDR3 or three 32-bit DDR3 @ 1.833GHz
  - Supports PVR
  - Supports Common Interface for conditional access support
  - Bootable SPI interface with serial flash support
  - Parallel interface for external parallel eMMC flash (optional) and NAND flash support
  - Power control module with ultra low power MCU available in standby mode
  - TBD-ball BGA package
  - Operating Voltages: 1.5V (DDR3), and 3.3V (I/O and analog)

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	3.14		3.46	V
1.5V Supply Voltages	V_{VDD_15}	1.43		1.57	V
Core Supply Voltages	V_{VDD_core}	0.97	1.00 (VID Case1)	1.05	V
		0.97	1.00 (VID Case0)	1.05	
CPU Core Power Voltages	V_{VDD_cpu}	0.97	1.00 (VID Case1)	1.05	V
		0.97	1.00 (VID Case0)	1.05	
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Table: Recommended operating conditions

6. VIDEO BACK-END PROCESSOR (MSTAR)

MST7410DY

General Description

The MST7410DY is a highly integrated ASIC for doubling the frame rate of the video input to provide a conversion from 50Hz to 100Hz or 60Hz to 120Hz. The MST7410DY comprises LVDS/V-By-One receiver, film source detection and inversion, motion frame rate conversion, color space conversion and management.

With HS-LVDS technology, the MST7410DY can support up to 2-channel input video source which can support up to QFHD 30Hz. With 12-lane V-By-One technology, the MST7410DY can support up to 8-lane input video source which can support up to QFHD 60Hz. It can also support up to 4-lane V-By-One input OSD source which can support up to QFHD 30Hz. With HDMI 1.4a technology, the MST7410DY can support up to QFHD 30Hz video source. With HDMI 2.0 technology, the MST7410DY can support up to QFHD (YCbCr 4:4:4 Format) 60Hz video source. With HDMI dual link technology, the MST7410DY can support up to QFHD 60 Hz video source.

MACE-PRO3^{UC}, the Professional UC Edition of MStar video processor, includes all MStar's successful color-tuning tools and a newly added multi-dimensional color/sharpening/NR formula that can quickly reflect subtle or sudden changes in even darker, brighter, or mixture scenes. With this ultimate color processor, a specially designed color remapping system for modern wide gamut displays, and an easy-to-use color-tool UI, developers can quickly and easily identify PQ characteristic from the most high-end panel models to the most conventional panel models. MStar's innovated UltraClear video processor adopts multi-frame video recovery technology to perfectly restore the contents/details, and eliminate the noise/artifacts.

By utilizing MStar 9th generation MFC technology, the MST7410DY realizes an optimum frame rate conversion to meet the output display frame rate, a wide horizontal and vertical search range for QFHD input source, and detects any cadences for best motion compensation. Moreover, the MST7410DY provides a clearer and halo-free moving picture quality without motion blur or judder. With 9th generation MFC, the MST7410DY provides a Logo and Small object detection and protection technology.

Armed with MStar Genuine3D^{PRO} 2D/3D Conversion Engine, the MST7410DY provides an idealized 3D Video quality output. Moreover, the MST7410DY provides an adjustable gain and depth tuning methodology for customerized 3D effect.

For green power saving, the MST7410DY provides a local dimming control circuit. The dimming control range maximum region is 96. The output interface could be SPI interface or direct PWM output pin.

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	3.14		3.46	V
1.5V Supply Voltages	V_{VDD_15}	1.43		1.57	V
1.15V Supply Voltages[Note]	V_{VDD_115}	1.12		1.18	V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Note: 1.15V (RMS value), Supplying voltages ripple within 150mV (+/-75mV)

Table: Recommended operating conditions

Features

- High Speed Input Interface
  - Input interface selectable as:
    - 2 HS-LVDS Links up to 150MHz for 4K2K[1] @ 60Hz
    - 12 lane V-By-One up to 3.75Gbps, 8-lane for 4K2K @ 60Hz, 4-lane for 4k2k @ 30Hz
- High Speed Output Interface
  - 16 lane V-By-One up to 3.75Gbps for 4K2K @ 120Hz QFHD panel
  - Supports HDMI1.4a Tx bypass output from HDMI 1.4a RX
- HDCP/HDMI[2] Compliant Input Ports
  - 3 HDMI input ports and 0 HDMI output ports (bypass)
  - HDMI 1.4b compliant
  - HDCP 1.4 compliant
  - Supports HDMI CEC
  - Supports HDMI 1.4a 3D formats
  - Supports HDMI 1.4 UHD 30Hz input
  - Supports HDMI 1.4 dual ports for UHD 60Hz input
  - Supports HDMI 2.0 YCbCr 4:2:0 UHD 60Hz input
  - Supports HDMI 2.0 YCbCr 4:4:4 UHD 60HZ input
- Memory Interface
  - 2 memory interfaces supporting up to 64-bit DDRIII @ 1.866GHz
- 9th Generation MFC Engine (FRC9)
  - Advanced Halo Reduction plus
  - Motion Compensated Frame Rate Conversion
  - Motion Blur Elimination to improve MPRT
  - Automatic Film-Mode Detection
  - Film Judder Cancellation
  - MStar Genuine3D^{PRO} 2D/3D Conversion Engine
  - 3D Depth Control for native 3D / Converted 3D Inputs
  - Major frame rate conversion:
    - 24Hz → 120Hz
    - 25Hz → 100/120Hz
    - 30Hz → 120Hz
    - 50Hz → 100/120Hz
    - 60Hz → 120Hz
  - Multi-Cadence Conversion
  - Artifical Object Detection
  - Search range: Big H and V search range to handle fast H/W motion
  - Supports logo detection and protection
  - Supports small object detection and protection
  - Advanced handling for small object, logo rim detection, fade in/out, flash, periodical etc.
- Uniformity Correction Engine
  - Block Size: 8 pixel x 8 line
  - Layer Number: 6 layers
  - Data Length: 10-bit
- 3D Formatter
  - Supports mandatory HDMI1.4a 3D video timing
  - Supports 1080p and 720p frame pack mode handling
  - Supports Checker Board and Pixel Alternative 3D mode
  - Supports 3D format translator
  - 3D Output Support: SG/PR
  - Supports 3D Frame ID Output
- MStar Advanced Color Engine – Professional UC Edition (MACE-PRO3^{UC})
  - 10/12-bit internal Data Processing
  - MACE-PRO3^{UC} Advanced Scaling Engine:
    - Multi-directional Scaling Technology
    - High-Tap Filters with Programmable Parameter
    - De-jagging support
    - Video Feather Artifact Detection and Removal
  - MACE-PRO3^{UC} Picture Enhancement:
    - Enhancements in all features of MACE-3/4 Engine
    - Super Resolution for Detail Enhancement & Recovery
    - Scene Detection

[1] 4k2k resolution is 4096 x 2160.

  - 3D Adaptive Color Control
  - 3D Adaptive Sharpness Control
  - sRGB and xvYCC Color Processing Engine
  - Supports HDMI 1.4 Deep Color Format
  - Supports HDMI 1.4 sYCC601 / AdobeRGB / AdobeYCC601 Color Formats
  - Supports Enhanced and Seamless Color Mapping for Wide Gamut Panels
- Programmable 12-bit RGB gamma CLUT

■ Local Dimming Support
- Supports Direct/Edge Type Local Dimming
- Max Block number: 96
- Programmable Light Spread Profile

■ Miscellaneous
- Dual Core RISC CPU
- Dual Full Duplex UART Interface
- Two Channel SPI Interface / One I2C-M for Dimming Control
- Supports memory minor mode
- Supports 3D_SYNC output pin
- Shutter glasses control signals:
  - L/R sync signal phase, polarity, duration programmable
  - IR Sync programmable
- Supports PWM output for scan backlight control
- One I2C Master Channel and one I2C Slave Channel
- Supports built-in spread spectrum clock for reducing EMI issue
- 27x27 BGA Package
- Operating Voltages: 1.15V, 1.5V and 3.3V

■ Separate OSD Data Path Support
- Max resolution support: 4K2K @ 30Hz
- Supports OSD scaling up
- Supports OSD sharpness adjustment
- OSD support format:
  - Supports ARGB 1555
  - Supports ARGB 4444
  - Supports ARGB 8888
  - Supports Color Key with one programmable key value

Block Diagram

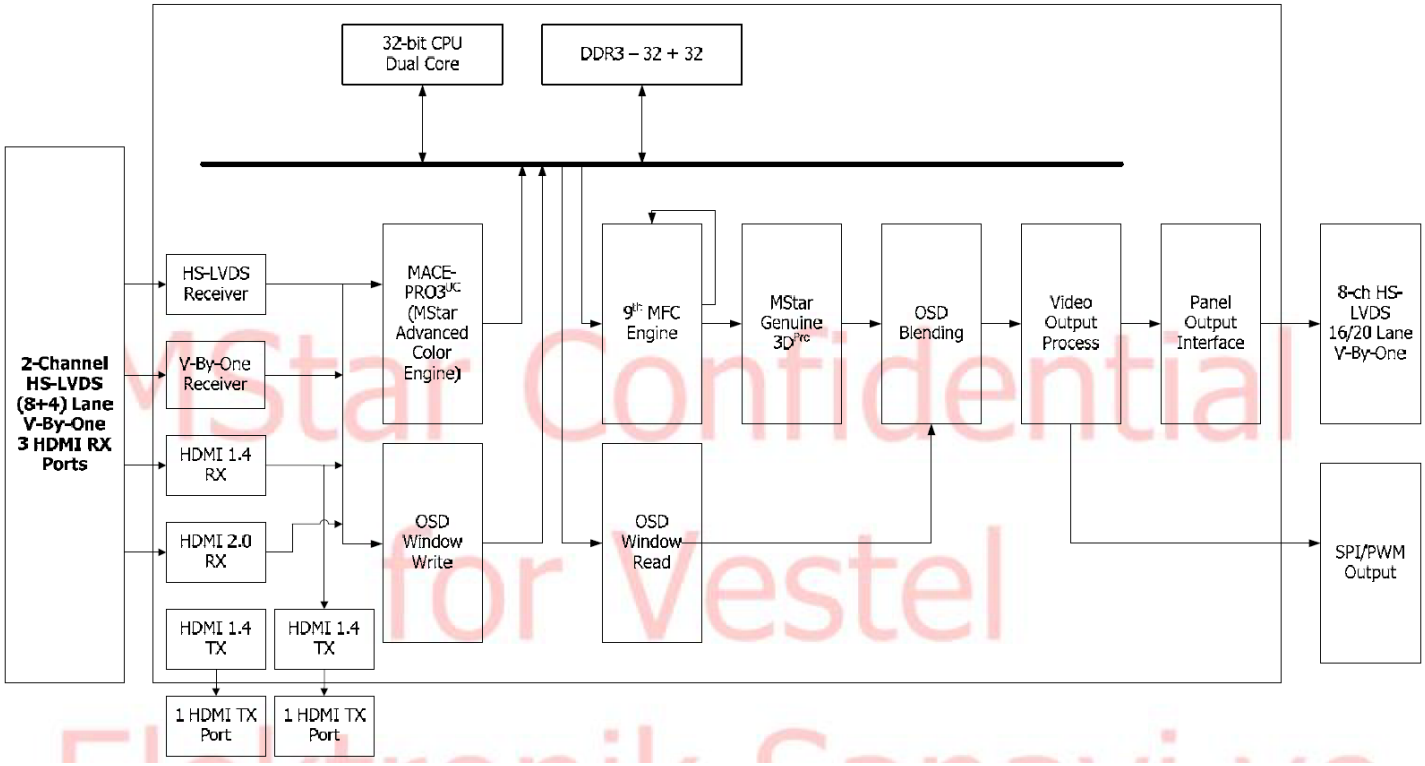


Figure: Block diagram

7. 1GB DDR3 SDRAM

HYNIX H5TQ1G63DFR

Description

The H5TQ1G63DFR-xxx series are a 1,073,741,824-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. Hynix 1Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Features

- DQ Power & Power supply : VDD & VDDQ = 1.5V +/- 0.075V
- DQ Ground supply : VSSQ = Ground
- Fully differential clock inputs (CK, CK) operation
- Differential Data Strobe (DQS, DQS)
- On chip DLL align DQ, DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 6, 7, 8, 9, 10, 11, 12, 13 and 14 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8, 9, 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- Programmable PASR(Partial Array Self-Refresh) for Digital consumer Applications.
- Programmable BL=4 supported (tCCD=2CLK) for Digi-tal consumer Applications.
- Programmable ZQ calibration supported
- BL switch on the fly
- 8banks
- 8K refresh cycles/64ms
- JEDEC standard 96ball FBGA(x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- Auto Self Refresh supported
- Write Levelization supported
- On Die Thermal Sensor supported
- 8 bit pre-fetch

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Table: Recommended operating conditions

8. 2GB DDR3 SDRAM

HYNİX H5TQ2G63DFR

Description

The H5TQ2G63DFR is a 2,147,483,648-bit CMOS Double Data Rate III (DDR3) Synchronos DRAM, ideally suited fort he main memory applications which requires large memory density and high bandwidth. SK Hynix 2Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control input are latched on the rising edges of the CK (falling edges of the CK), Data, Data stobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Features

- VDD & VDDQ = 1.5V +/- 0.075V
- Fully differential clock inputs (CK, CK) operation
- Differential Data Strobe (DQS, DQS)
- On chip DLL align DQ, DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5,6, 7, 8, 9, 10, 11, 12, 13 and 14 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle (Tcase 0C – 95C)
  - 7.8 uS at 0C - 85C
  - 3.9 uS at 85C – 95C

  Commercial Temperature(0C – 85C)
  Industrial Temperature(-40C- 95C)
- Auto Self Refresh supported
- JEDEC standard 78ball FBGA(x8), 96ball FBGA(x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported

- TDQS (Terminal Data Stobe) supported (x8 only)
- Write Levelization supported
- 8 bit pre-fetch

Symbol	Parameter	Rating	Units	NOTE
V_{DD}	Voltage on V_{DD} pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Table: Absolute Maximum DC Ratings

Symbol	Parameter	Rating			Units	NOTE
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1,2

NOTE :
1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.

Table: Recommended operating conditions

9. 32GBİT (4G X 8 BİT) NAND FLASH MEMORY

HYNIX H26M31001HPR

Key Features

- **eMMC4.5 compatible**
  (Backward compatible to eMMC4.41)
- **Bus mode**
  - Data bus width : 1 bit(default), 4 bits, 8 bits
  - Data transfer rate: up to 200MB/s (HS200)
  - MMC I/F Clock frequency : 0~200MHz
  - MMC I/F Boot frequency : 0~52MHz
- **Operating voltage range**
  - Vcc (NAND) : 2.7 - 3.6V
  - Vccq (Controller) : 1.7 - 1.95V / 2.7 - 3.6V
- **Temperature**
  - Operation (-25°C ~ +85°C)
  - Storage without operation (-40°C ~ +85°C)
- **Others**
  - This product is compliance with the RoHS directive
- **Supported features**
  - HS200
  - HPI, BKOPS
  - Packed CMD, Cache, Data tag, Context ID
  - Partitioning, RPMB
  - Discard, Trim, Erase, Sanitize, Secure TRIM,
  - Write protect, Lock / Unlock
  - PON, Sleep / Awake
  - Reliable write
  - Boot feature, Boot partition
  - HW / SW Reset

- Health(Smart) report

Description

SK hynix e-NAND consists of NAND flash and MMC controller.e-NAND has the built-in intelligent controller which manages interface protocols, wear leveling, bad block management, garbage collection, and ECC. e-NAND protects the data contents from the host sudden power off failure.e-NAND is compatible with JEDEC standard eMMC4.5 specification.

3.1 Performance

Density	Sequential read (MB/s)	Sequential write (MB/s)	Test condition
4GB	130	10	• Option: Cache / Packed CMD / HS200 • Test tool: uBOOT (Without O/S) • Chunk size : 1MB, Test area : 1GB

3.2 Power

3.2.1 Active power consumption during operation

Density		Icc	Iccq
4GB(SDP)	Average	40mA	100mA
	Peak	80mA	200mA

- Room temperature : 25℃
- Average current consumption is over a period of 100ms
- Peak current consumption is over a period of 20us
- V_{cc} : 3.3V & V_{ccq} : 1.8V
- HS200 enabled

3.2.2 Low power mode (Standby)

Density	Icc	Iccq
4GB(SDP)	100uA	30uA

- In Standby Power mode, CTRL V_{ccq} & NAND V_{cc} power supply is switched on
- No data transaction period before entering sleep status
- Room temperature : 25℃

3.2.3 Low power mode (Sleep)

Density	Icc	Iccq
4GB(SDP)	0	30uA

- In sleep state, triggered by CMD5, NAND V_{cc} power supply is switched off (CTRL V_{ccq} on)
- Room temperature : 25℃

3.3 Endurance

This section provides "TBW(Total Bytes Written)" information that indicates how much data can be written on an e-NAND before the device reaches its end of life.
The data is based on the SK hynix's data pattern which is designed to be a good indication of endurance for mainstream application users.

Density	TBW
4GB	2.4TB

[Table 2]Write endurance

10. 16M-BIT [16M X 1] CMOS SERIAL FLASH EEPROM

MX25L1602 MSTAR SPI FLASH

Key Features

■ HIGH DENSITY NAND FLASH MEMORIES

General

- 16,777,216 x 1 bit structure
- 256 Equal Sectors with 8K-byte each
  - Any sector can be erased
- 4096 Equal Segments with 512-byte each
  - Provides sequential output within any segment
- Single Power Supply Operation
  - 3.0 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is equal to or less than 2.5V

Performance

- High Performance
  - Fast access time: 20MHz serial clock (50pF + 1TTL Load)
  - Fast program time: 5ms/page (typical, 128-byte per page)
  - Fast erase time: 300ms/sector (typical, 8K-byte per sector)
- Low Power Consumption
  - Low active read current: 10mA (typical) at 17MHz
  - Low active programming current: 10mA (typical)
  - Low active erase current: 10mA (typical)
  - Low standby current: 30uA (typical, CMOS)
- Minimum 100,000 erase/program cycle

Software Features

- Input Data Format
  - 1-byte Command code, 3-byte address, 1-byte byte address
- 512-byte Sequential Read Operation
- Built in 9-bit (A0 to A8) pre-settable address counter to support the 512-byte sequential read operation
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algroithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
  - Provides detection of program and erase operation completion.
  - Provides auto erase/ program error report

Hardware Features

- SCLK Input
  - Serial clock input

- SI Input
  - Serial Data Input
- SO Output
  - Serial Data Output
- PACKAGE
  - 28-pin SOP (330mil)

General Description

The MX25L1602 is a CMOS 16,777,216 bit serial Flash EEPROM, which is configured as 2,097,152 x 8 internally. The MX25L1602 features a serial peripheral interface and software protocol allowing operation on a simple 3- wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS input.

The MX25L1602 provide sequential read operation on whole chip. The sequential read operation is executed on a segment (512 byte) basis. User may start to read from any byte of the segment. While the end of the segment is reached, the device will wrap around to the beginning of the segment and continuously outputs data until CS goes high.

After program/erase command is issued, auto program/ erase algorithms which program/erase and verify the specified page locations will be executed. Program command is executed on a page (128 bytes) basis, and erase command is executed on both chip and sector (8K bytes) basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion and error flag status of a program or erase operation.

When the device is not in operation and CS is high, it is put in standby mode and draws less than 30uA DC current.

The MX25L1602 utilizes MXIC's proprietary memory cell which reliably stores memory contents even after 100,000 program and erase cycles.

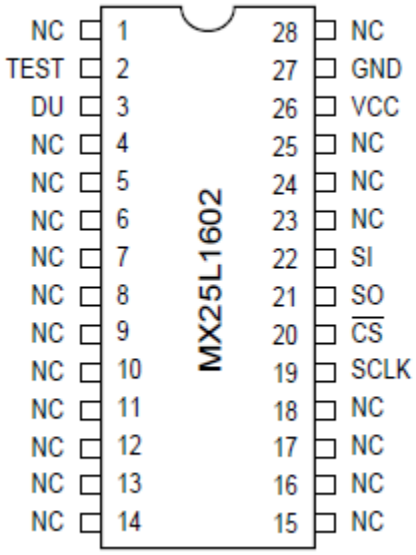


Figure: Pin configuration

PIN DESCRIPTION

SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select
TEST(1)	Test Mode Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
VCC	+ 3.3V Power Supply
GND	Ground
DU(2)	Do Not Use(for Test Mode only)
NC	No Internal Connection

Note:

1. TEST input is used for in-house testing and must be tied to ground during normal user operation.

2. DU pin is used for in-house testing and can be tied to VCC, GND or open for normal operation.

Table: Pin description

M25Q32FV SPI FLASH

Key Features

- **New Family of SpiFlash Memories**
  - W25Q32FV: 32M-bit/ 4M-byte
  - Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI:CLK, /CS, IO_0, IO_1, /WP, /Hold
  - Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - QPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
  - Software & Hardware Reset
- **Highest Performance Serial Flash**
  - 104MHz Single, Dual/Quad SPI clocks
  - 208/416Mhz equivalent Dual/Quad SPI
  - 50 MB/S continuous data transfer rate
  - More than 100,000 erase/program cycles
  - More than 20-year retention
- **Efficient "Continuous Read" and QPI Mode**
  - Continuous Read with 8/16/32/64-Byte Wrap
  - As few as 8 clocks to address memory
  - Quad Peripheral Interface (QPI) reduces instruction overhead
  - Allows true XIP (execute in place) operation
  - Outperforms X16 Parallel Flash
- **Low Power, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 4mA active current, <1uA Power-down(typ.)
  - -40C to +85C operating range
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector/Block Erase (4K/32K/64K-Byte)
  - Program 1 to 256 byte per programmable page

- Erase/Program Suspend&Resume
- **Advanced Security Features**
  - Software and Hardware Write-Protect
  - Power Supply Lock-Down and OTP protection
  - Top/Bottom, Complement array protection
  - Individual Block/Sector array protection
  - 64-Bit Unique ID for each device
  - Discoverable Parameters (SFDP) Register
  - 3x256-Bytes Security Registers with OTP locks
  - Volatile & Non-volatile Status Register Bits
- **Space Efficient Packaging**
  - 8-pin SOIC 208-mil / VSOP 208-mil
  - 8-pad WSON 6x5-mm / 8x6-mm
  - 16-pin SOIC 300-mil (additional / RESET pin)
  - 8-pin PDIP 300-mil
  - 24-ball TFBGA 8x6-mm (6x4/5x5 ball array)
  - Contact Winbond for KGB and other options

General Description

This W25Q32FV (32M-bit) Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The device operates on a single 2.7V to 3.6V power supply with current consumption as low as 4mA active and 1uA for power-down. All devices are offered in space-saving packages.

The W25Q32FV array is organized into 16,384 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time.Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The W25Q32FV has 1,024 erasable sectors and 64 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

The W25Q32FV support the standart Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripharel Interface (QPI): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (D0), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz (104MHz x 2) for Duad I/O and 416Mhz (104MHz x 4) for Quad I/O when using the Fast Read Dual/Quad I/O and QPI instructions. These transfer rates can outperform standart Asynchronous 8 an 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory Access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP(execute in place) operation.

A Hold pin, Write Protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standart manufacturer and device ID and SFDP Register, a 64-bit Unique Serial Number and three 256-bytes Security Registers.

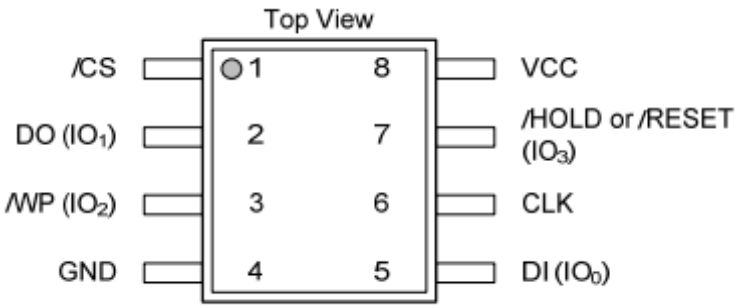


Figure: Pin configuration

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO (IO1)	I/O	Data Output (Data Input Output 1)[1]
3	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)[2]
4	GND		Ground
5	DI (IO0)	I/O	Data Input (Data Input Output 0)[1]
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	Hold or Reset Input (Data Input Output 3)[2]
8	VCC		Power Supply

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions
2. IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.

Table: Pin description

11. DEMODULATOR STAGE

MSB1240 DVB-T2

Key Features

- DVB-T2
  - Compliant with ETSI EN 302 755 v 1.3.1
  - Supports T2-base and T2-Lite profile
  - Supports 1.7, 5, 6, 7, 8MHz bandwidth
  - Supports all guard intervals (1/128 to 1/4)
  - Supports all FFT modes from 1K to 32K
  - Supports all long and short block code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6 and 1/3, 2/5 specific to T2-Lite)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM, 256-QAM)
  - Supports transmit diversity (MISO)
  - Supports all scattered pilot patterns (PP1 to PP8)
  - Supports rotated and non-rotated constellations
  - Supports single and multiple PLPs
  - Compliant with Nordig 2.2.2, D-Book 7.0 and Ghana test suite v1.1
  - Automatic co-channel and adjacent channel interference suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Impulse-Noise suppression
  - Advanced performance for SFN networks
- DVB-T
  - Compliant with ETSI EN 300 744
  - Supports all guard intervals (1/32 to 1/4)
  - Supports 2K and 8K FFT modes
  - Supports all code rates (1/2, 2/3, 3/4, 5/6, 7/8)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM)
  - Automatic co-channel and adjacent channel interference suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Impulse-Noise suppression
  - Advanced performance for SFN networks
- DVB-C
  - Compliant with ETSI EN 300 429
  - Supports symbol rate from 1 to 7.2 MHz
  - Automatic symbol rate detection and QAM-mode detection
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset

- DVB-S2/S
  - Compliant with DVB-S2 (ETSI EN 302 307)
  - Compliant with DVB-S (ETSI EN 300 421)
  - DVB-S2:
    - Data Rate: 1-45 Msps
    - Constellations: QPSK and 8PSK
    - Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9 and 9/10
    - Roll-off factors for pulse shaping: 0.2, 0.25, and 0.35
  - DVB-S:
    - Data Rate: 1-45 Msps
    - Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
  - Directly interfaces with tuner for easy implementation
  - Integrated dual A/D converters
  - Carrier frequency acquisition range: ±5MHz
  - Fast automatic blind scan of symbol rates and carrier freuqencies
  - Equalizer compensates for channel impairment
  - DiSEqC™ 2.0 compatible with LNB controller
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Novel carrier recovery algorithms for tracking and compensating large phase noises
  - Integrated FEC decoders for near Shannon limit performances
- Miscellaneous
  - For DVB-T2/T/C, accepts IF, low IF inputs
  - For DVB-S2/S, accepts ZIF inputs
  - Integrated signal quality and BER monitors
  - Configurable parallel/serial MPEG-2 transport stream interface
  - Fast channel acquisition and auto-scan time
  - Clock generation from a single crystal
  - On chip MCU to reduce host control overhead
  - Supports I2C interface with bypass mode
  - 48-pin LQFP package

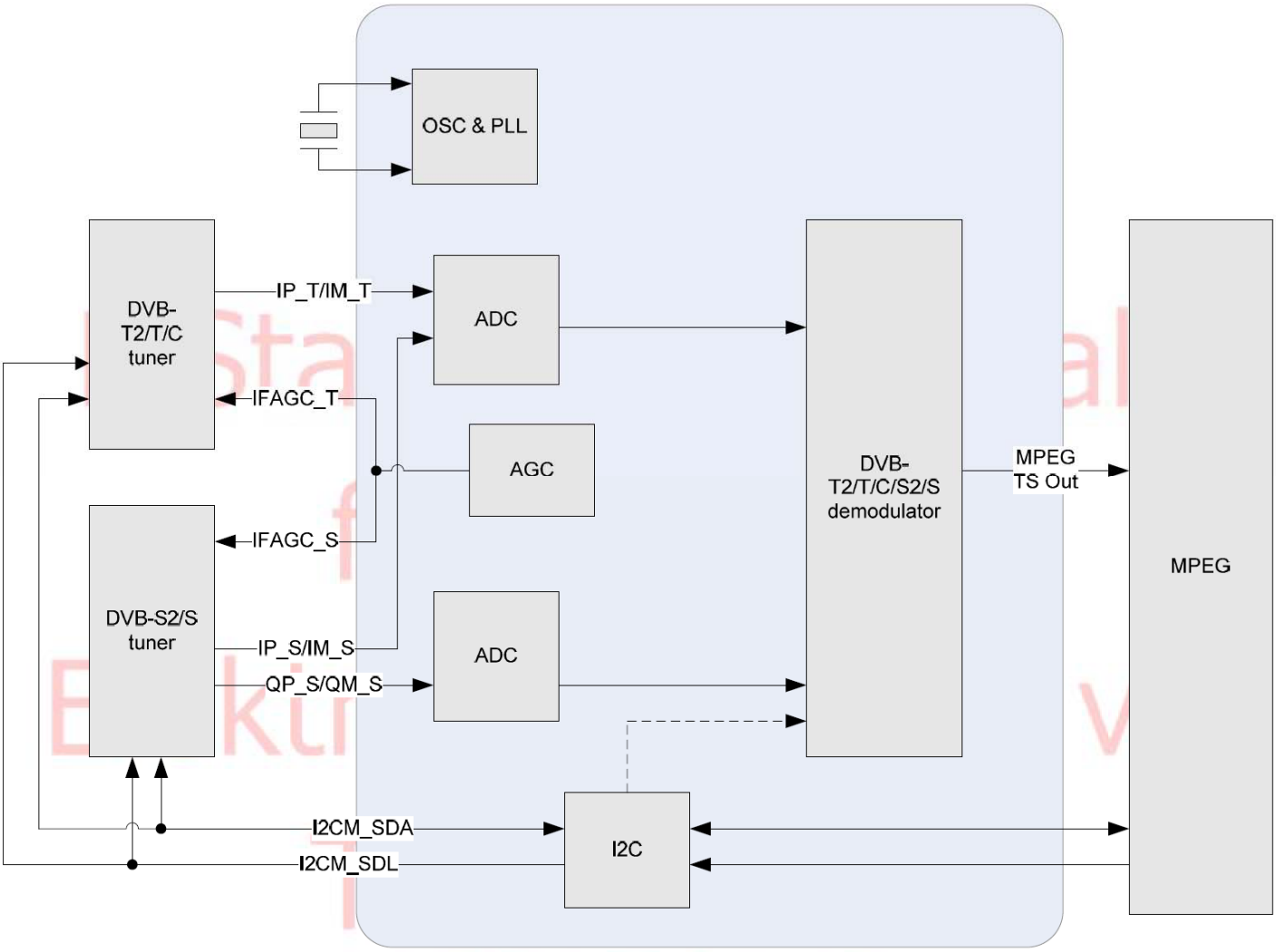
General Description

The MSB1240 is a single chip demodulator supporting DVB-T2, DVB-T, DVB-C, DVB-S2 and DVB-S standards. The device integrates a house keeping microcontroller that takes care of all real time and algorithmic tasks simplifying the host control interface.

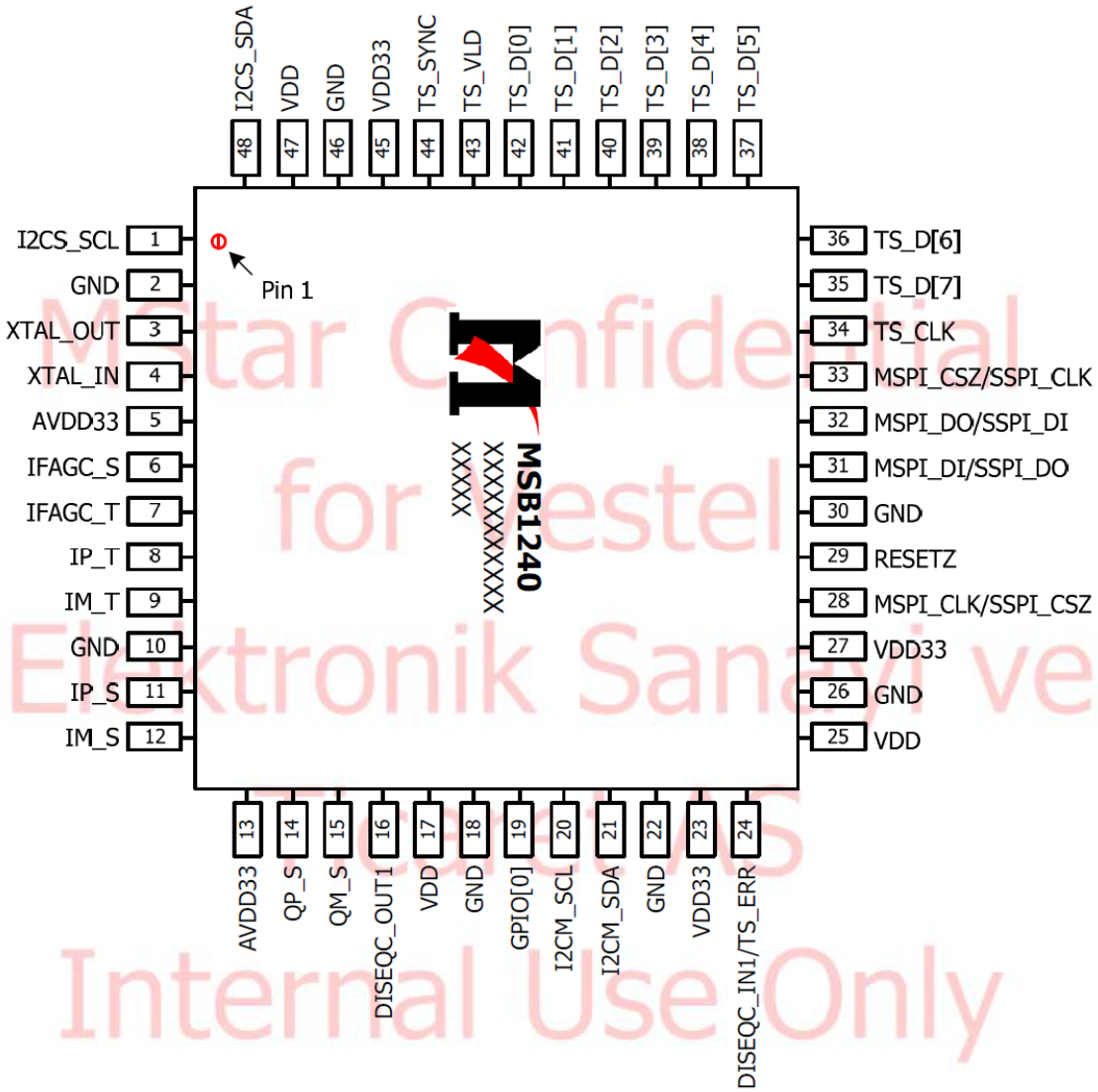
For DVB-T2/T/C, the MSB1240 front end can accept tuners that provide IF or low IF output. For DVB-S2/S, the MSB1240 front end can accept tuners that provide zero-IF output. A high rejection channel filter has been included easing the channel filtering requirement of the tuner whilst still meeting the stringent requirements for adjacent channel interference. The MSB1240 may be clocked directly using a crystal, typically 24MHz.

The MSB1240 is capable of blind acquisition of DVB-T/T2, DVB-C and DVB-S2/S signals. All parameters may be detected in this mode enabling fast and accurate auto scanning. Its frequency recovery circuit is able to compensate for all typical tuner and broadcast frequency errors.

Block Diagram



Pinning



Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
3.3V Supply Voltages	V_{VDD_33}		3.6	V
1.15V Supply Voltages	V_{VDD_115}		1.26	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Storage Temperature	T_{STG}	-40	150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	3.14	3.3	3.46	V
1.15V Supply Voltages	$V_{VDD\ 115}$	1.09	1.15	1.21	V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

12. LNB SUPPLY AND CONTROL IC

LNBH29

General Description

LNBH29 IC is intended for analog and digital Satellite receivers/Sat-TV, Sat-PC cards, the LNBH29 series is a monolithic voltage regulator and interface IC, assembled in QFN3x3-16L and QFN4x4-16L, specifically designed to provide the 13/18V power supply and the 22KHz tone signaling to the LNB down-converter in the antenna dish or to the multi-switch box. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with simple design and I2C standard interfacing.

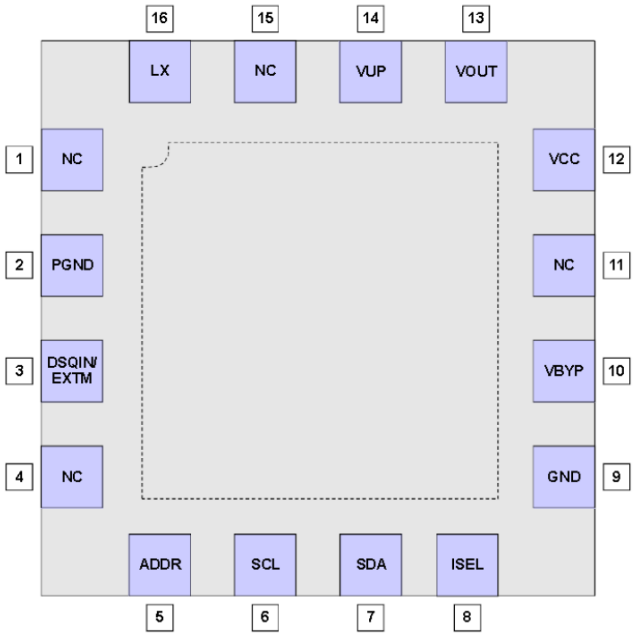
Key Features

- COMPLETE INTERFACE BETWEEN LNB AND I2C BUS
- BUILT-IN DC/DC CONVERTER FOR SINGLE 12V SUPPLY OPERATION AND HIGH
- EFFICIENCY (TYP. 93% @ 0.5A)
- SELECTABLE OUTPUT CURRENT LIMIT BY EXTERNAL RESISTOR
- COMPLIANT WITH MAIN SATELLITE RECEIVERS OUTPUT VOLTAGE
- SPECIFICATION
- ACCURATE BUILT-IN 22 kHz TONE GENERATOR SUITS WIDELY ACCEPTED
- STANDARDS
- 22 KHz TONE WAVEFORM INTEGRITY GUARANTED ALSO AT NO LOAD
- CONDITION
- LOW-DROP POST REGULATOR AND HIGH EFFICIENCY STEP-UP PWM WITH
- INTEGRATED POWER N-MOS ALLOW LOW POWER LOSSES.
- OVERLOAD AND OVER-TEMPERATURE INTERNAL PROTECTIONS WITH I2C
- DIAGNOSTIC BITS
- LNB SHORT CIRCUIT DYNAMIC PROTECTION
- +/- 4KV E.S.D. TOLERANT ON OUTPUT POWER PINS

Applications

- LNB Power Supply and Control for Satellite Set Top Boxes

a) Package Reference



QFN 3X3 16L (TOP VIEW)

Same pin configutation for QFN 4x4-16L package

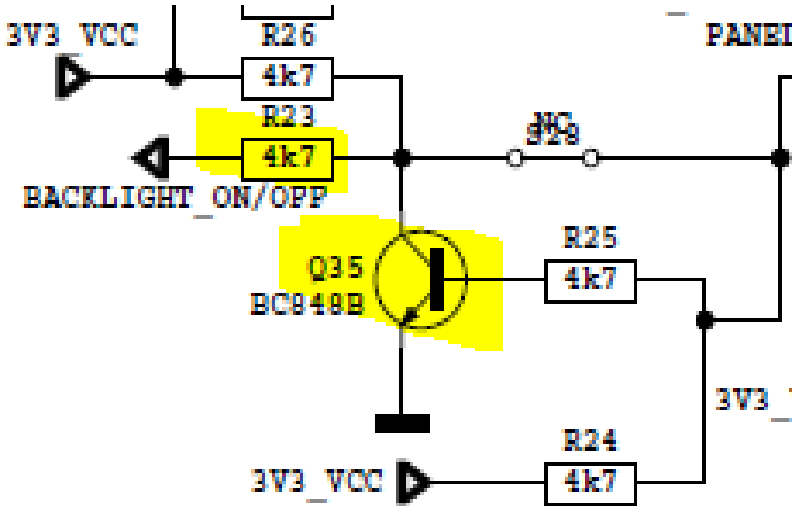
13. TROUBLESHOOTING

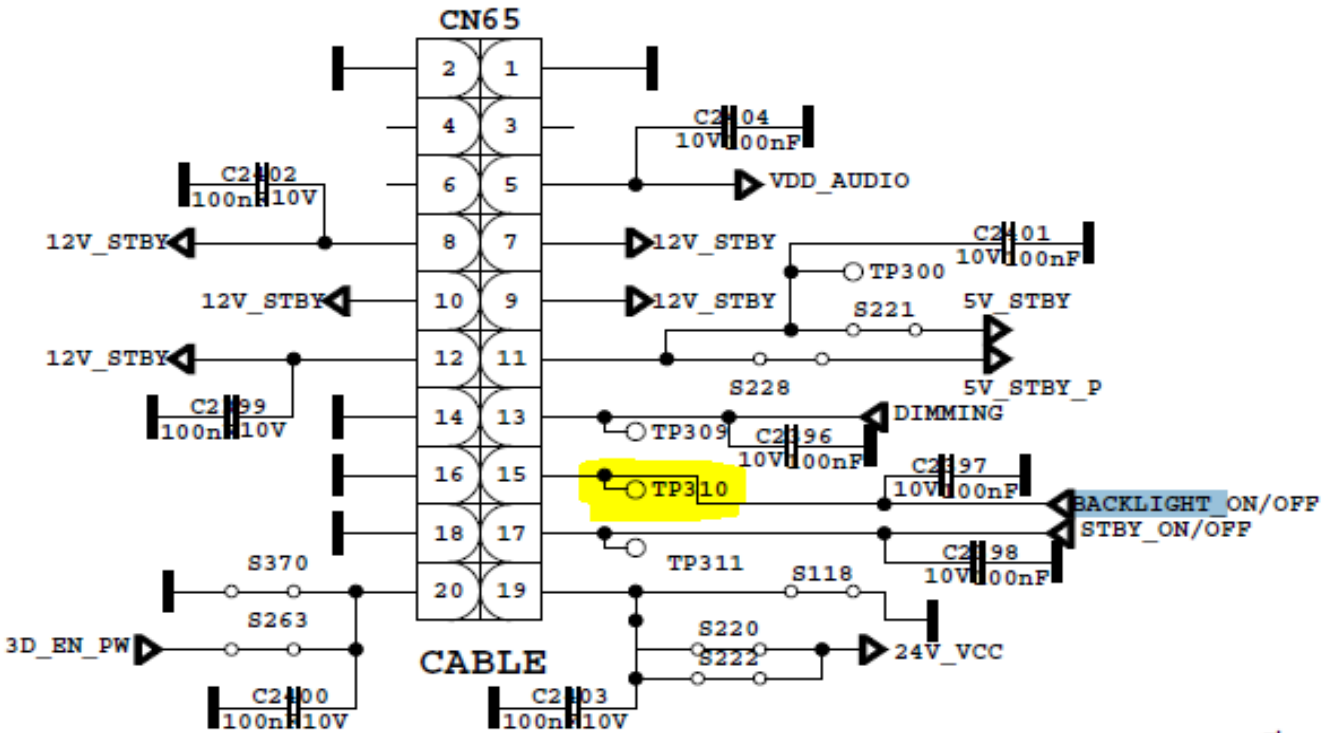
A. NO BACKLIGHT PROBLEM

Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

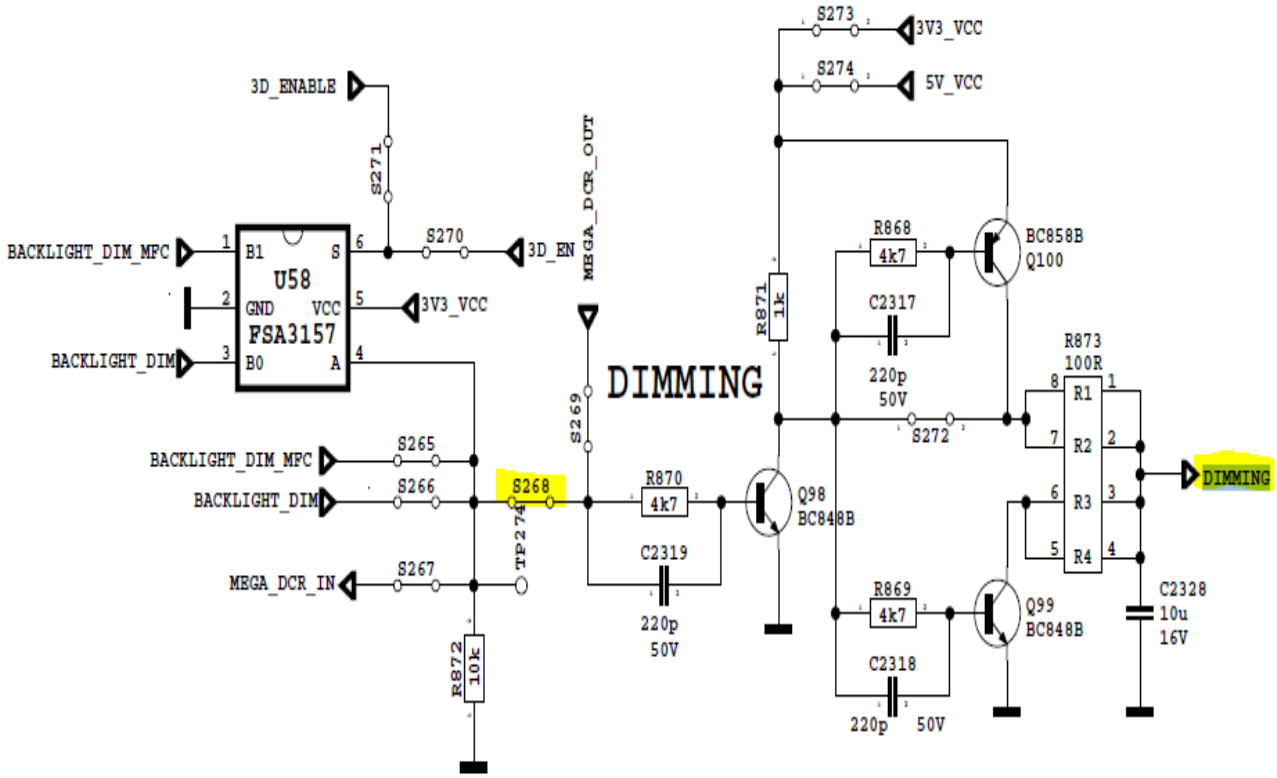
Possible couses: Backlight pin, dimming pin, backlight supply, stby on/off pin

BACKLIGHT_ON/OFF pin should be high when the backlight is ON. R23 must be low when the backlight is OFF. If it is a problem, please check Q35 and the panel cables. Also it can be tested in TP310 in main board.

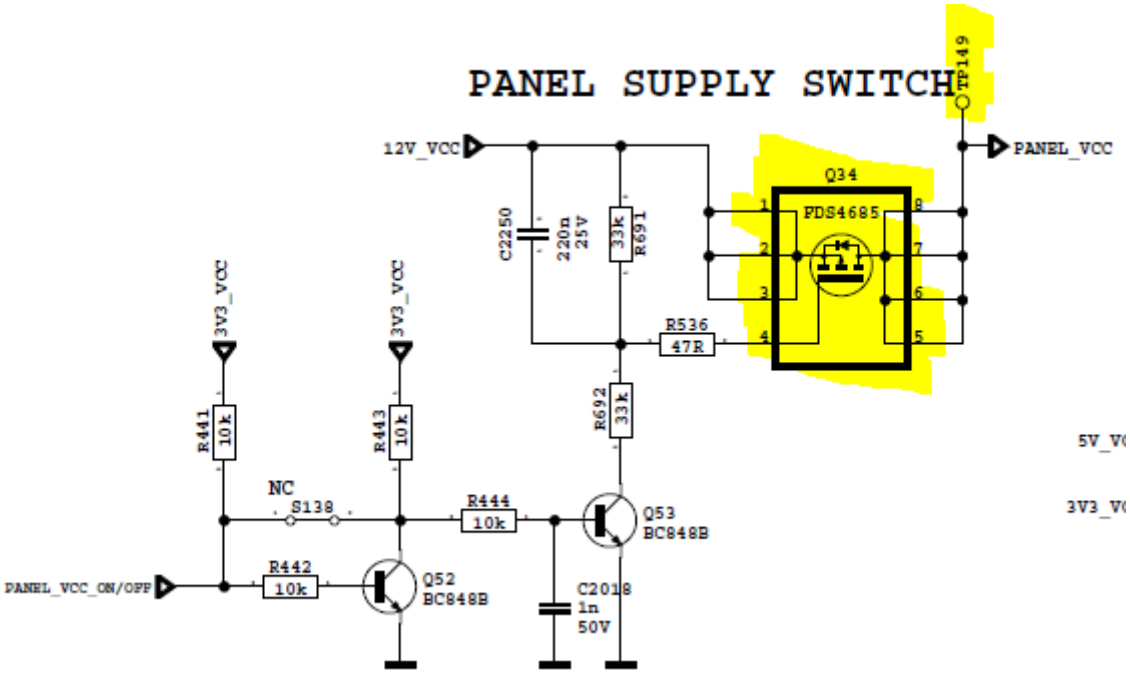




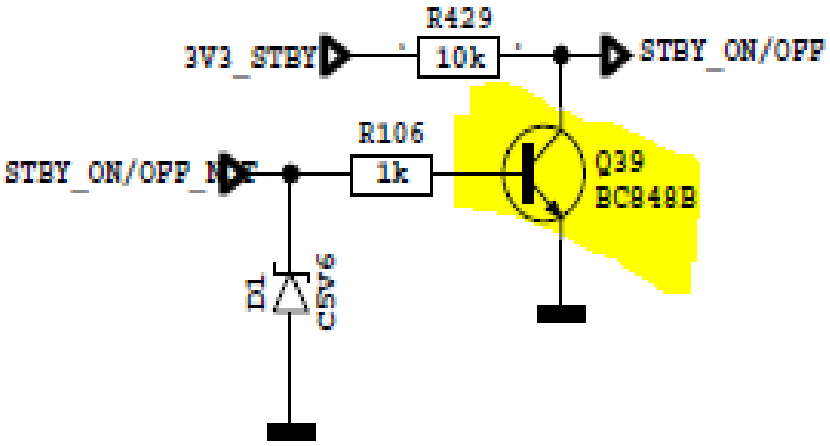
Dimming pin should be high or square wave in open position. If it is low, please check S268 for Mstar side and panel or power cables, connectors.



Backlight power supply should be in panel specs. Please check Q34, shown below; also it can be checked TP149.



STBY_ON/OFF_NOT should be low for tv on condition, please check Q39's collector.

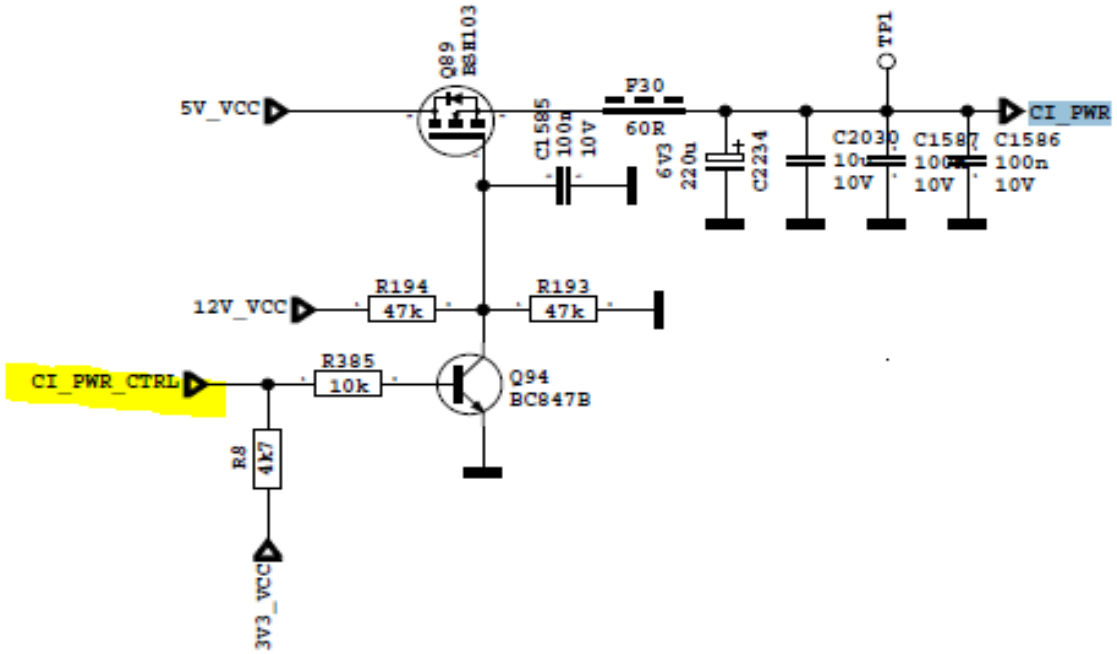


D. CI MODULE PROBLEM

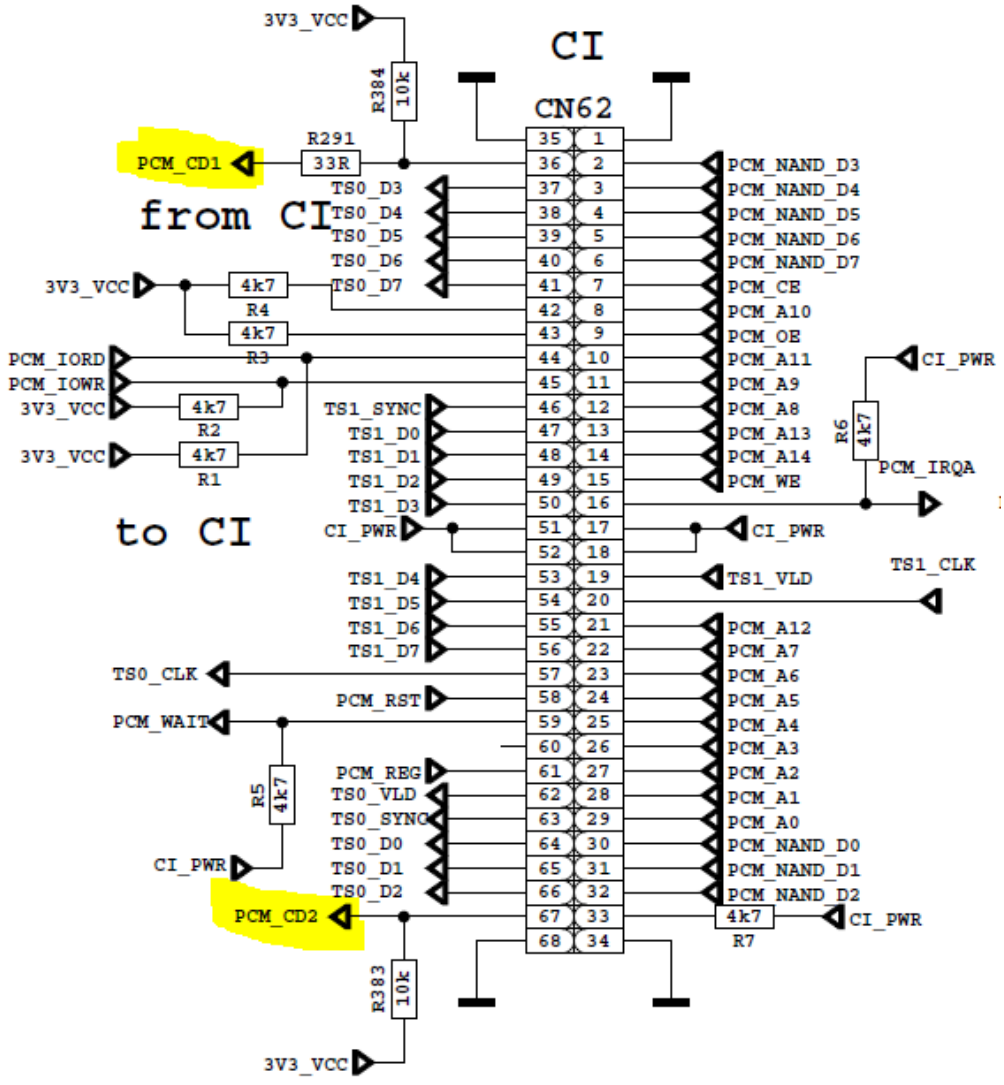
Problem: CI is not working when CI module inserted.

Possible couses: Supply, suply control pin, detect pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTRL, this pin should be low.



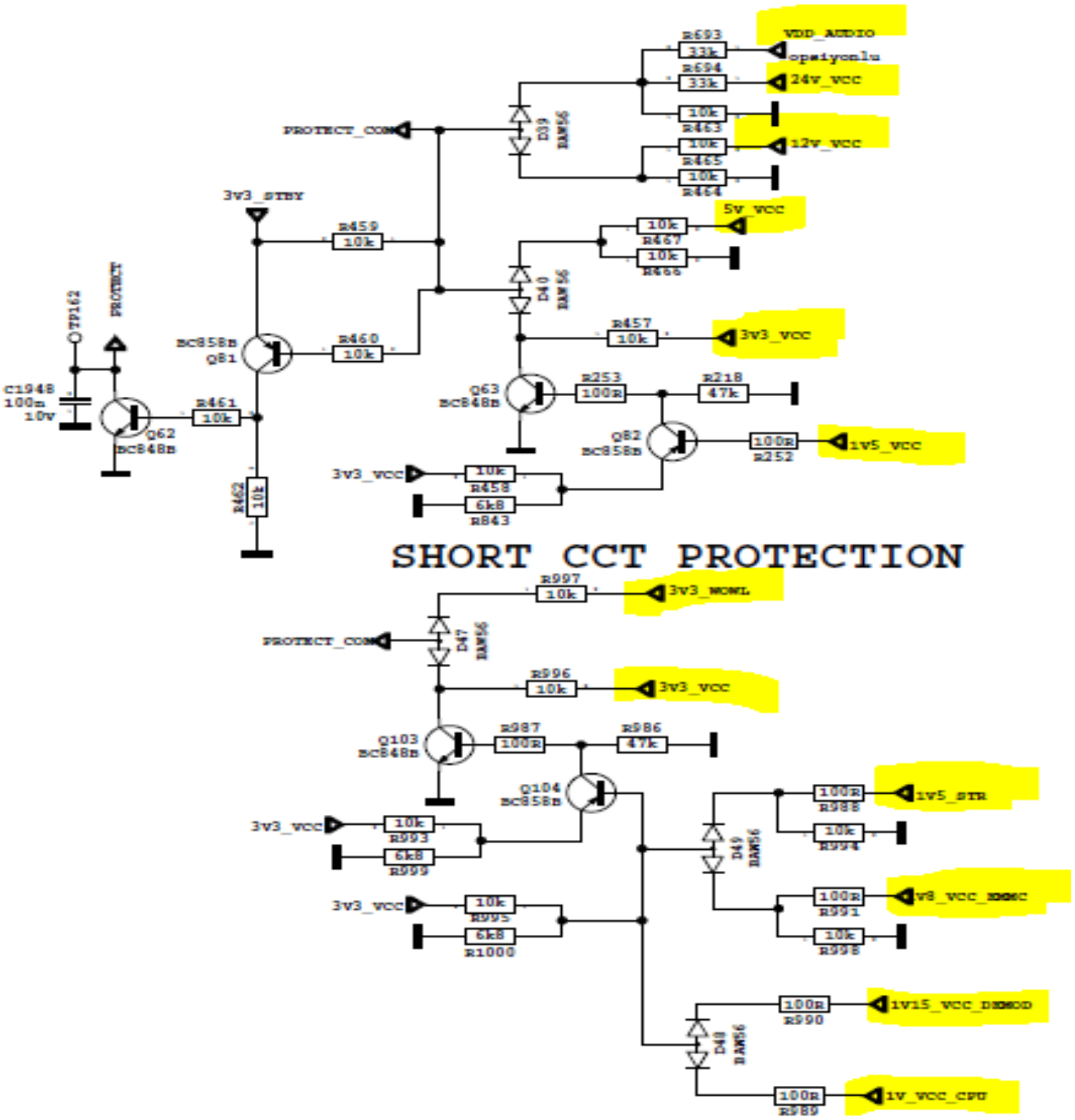
- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.



E. STAYING IN STAND-BY MODE

Problem: Staying in stand-by mode, no other operation

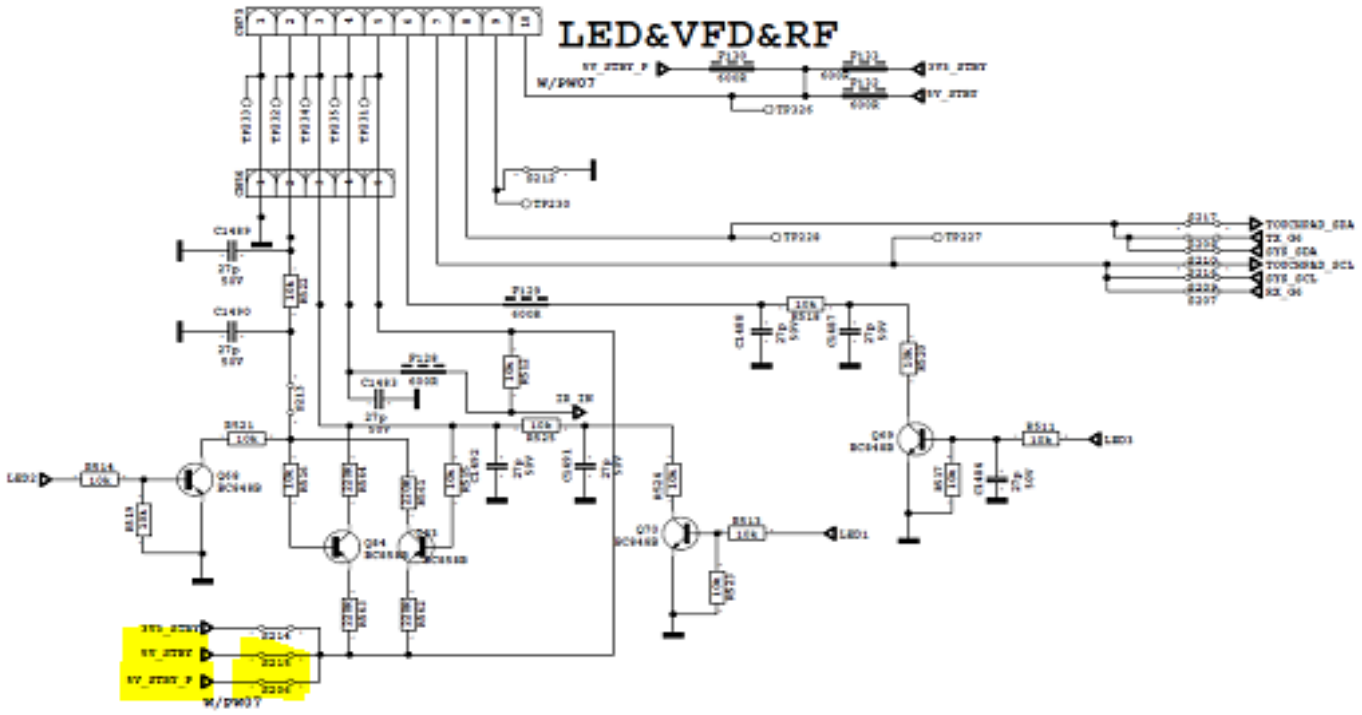
This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a multimeter to find the shorted voltage to ground.



F. IR PROBLEM

Problem: LED or IR not working

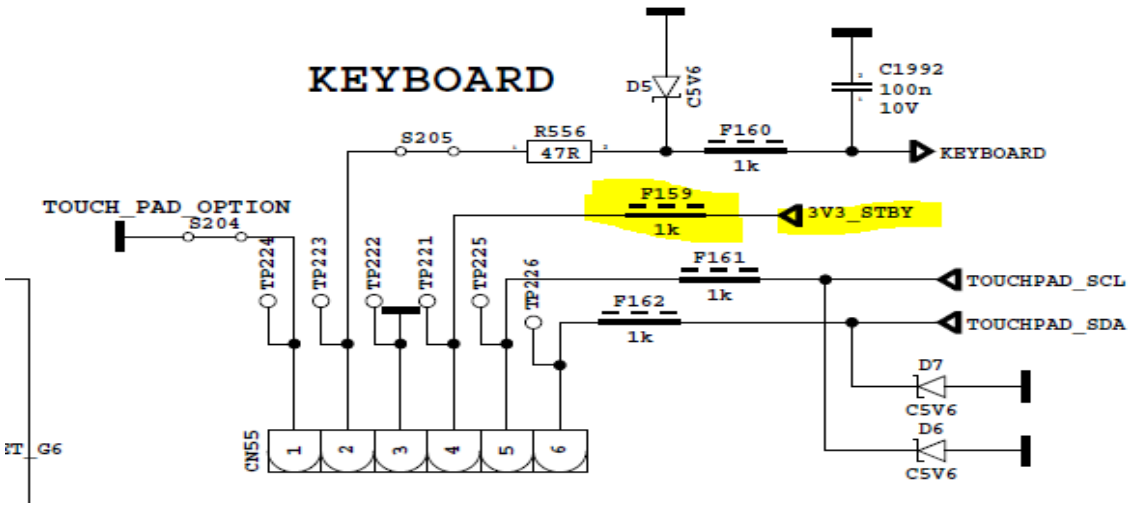
Check LED card supply on MB100 chasis.



G. KEYPAD TOUCHPAD PROBLEMS

Problem: Keypad or Touchpad is not working

Check keypad supply on MB100.

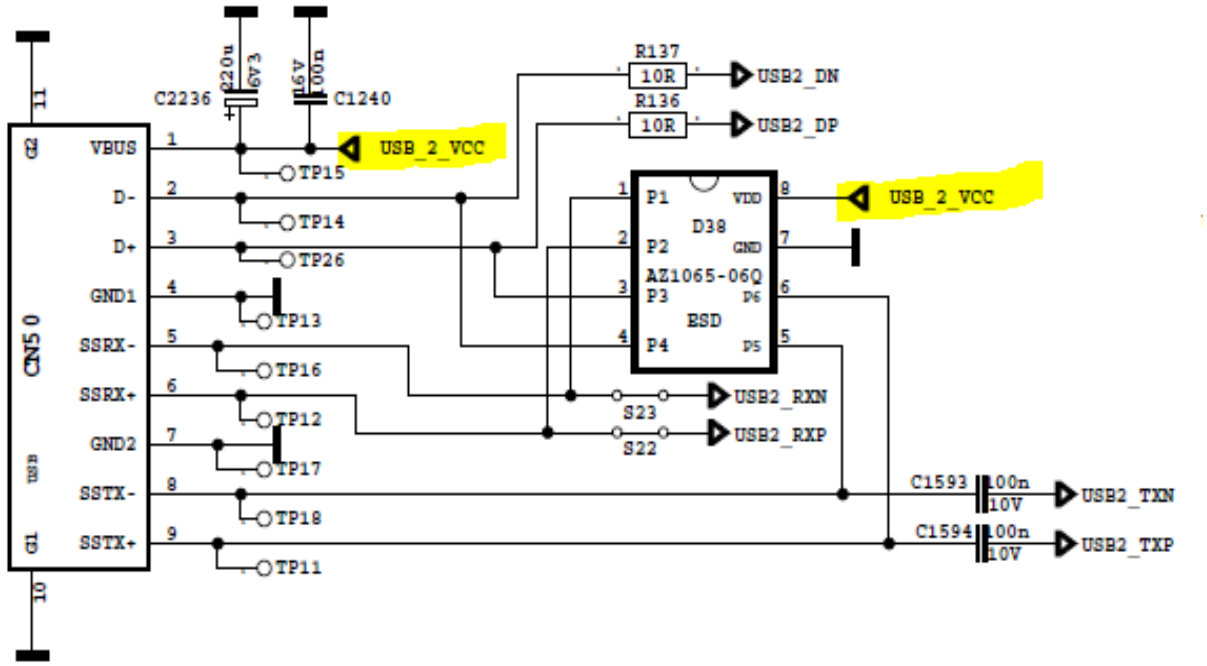


H. USB PROBLEMS

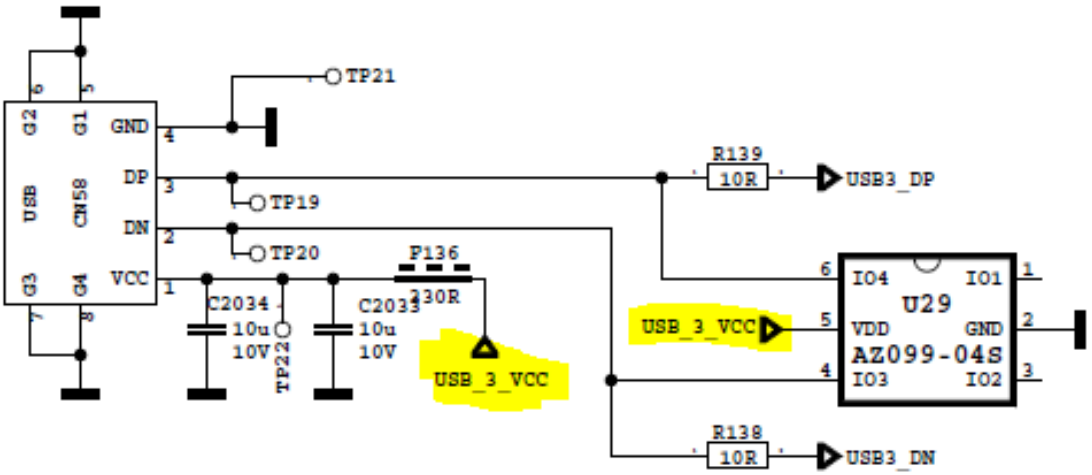
Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

For USB 3.0 ports:



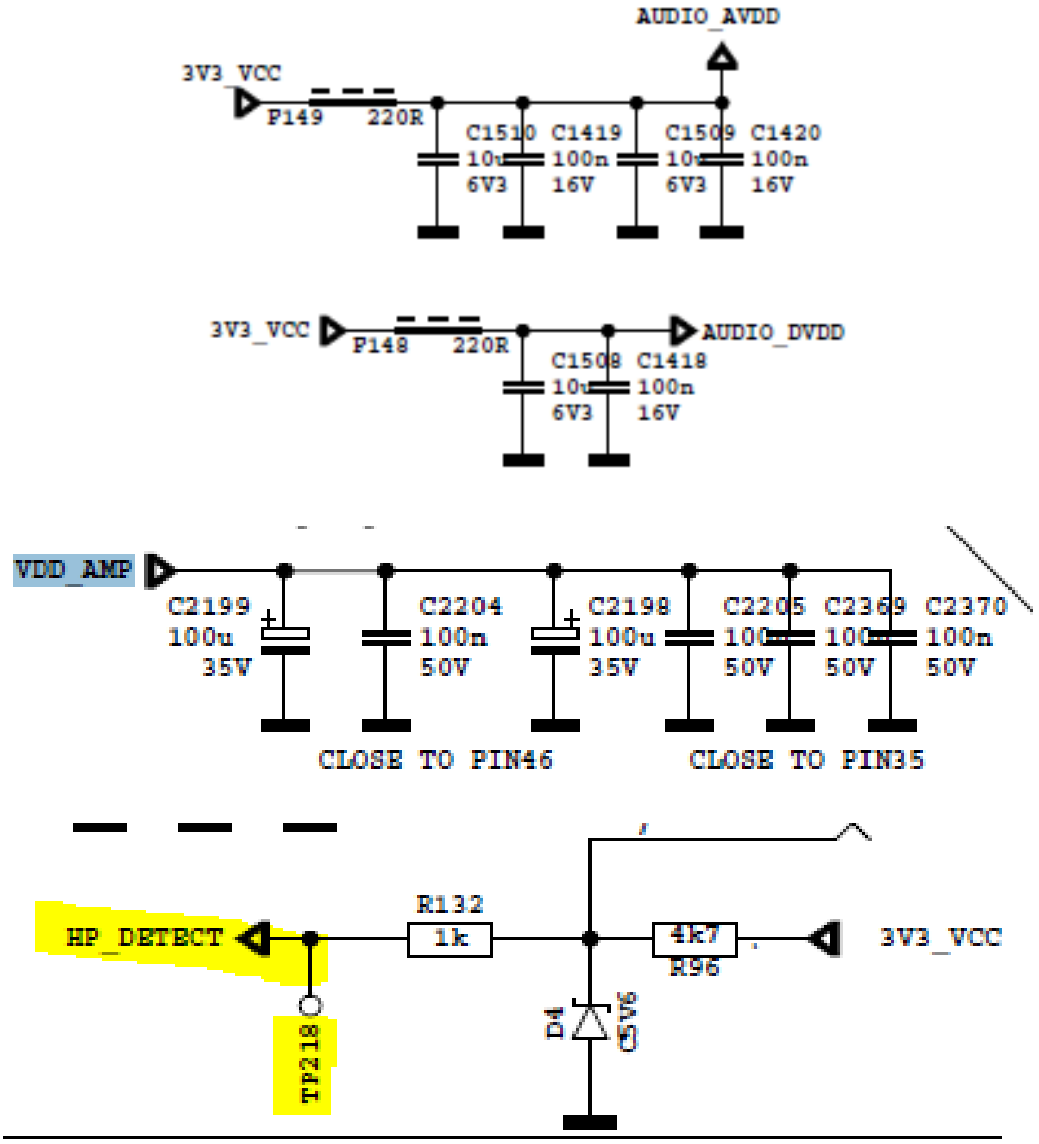
For USB 2.0 port:



İ. ***NO SOUND PROBLEM***

Problem: No audio at main TV speaker outputs.

Check supply voltages of 24V VDD_AUDIO, 3.3V AUDIO_AVDD and AUDIO_DVDD with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.



J. *STANDBY ON/OFF PROBLEM*

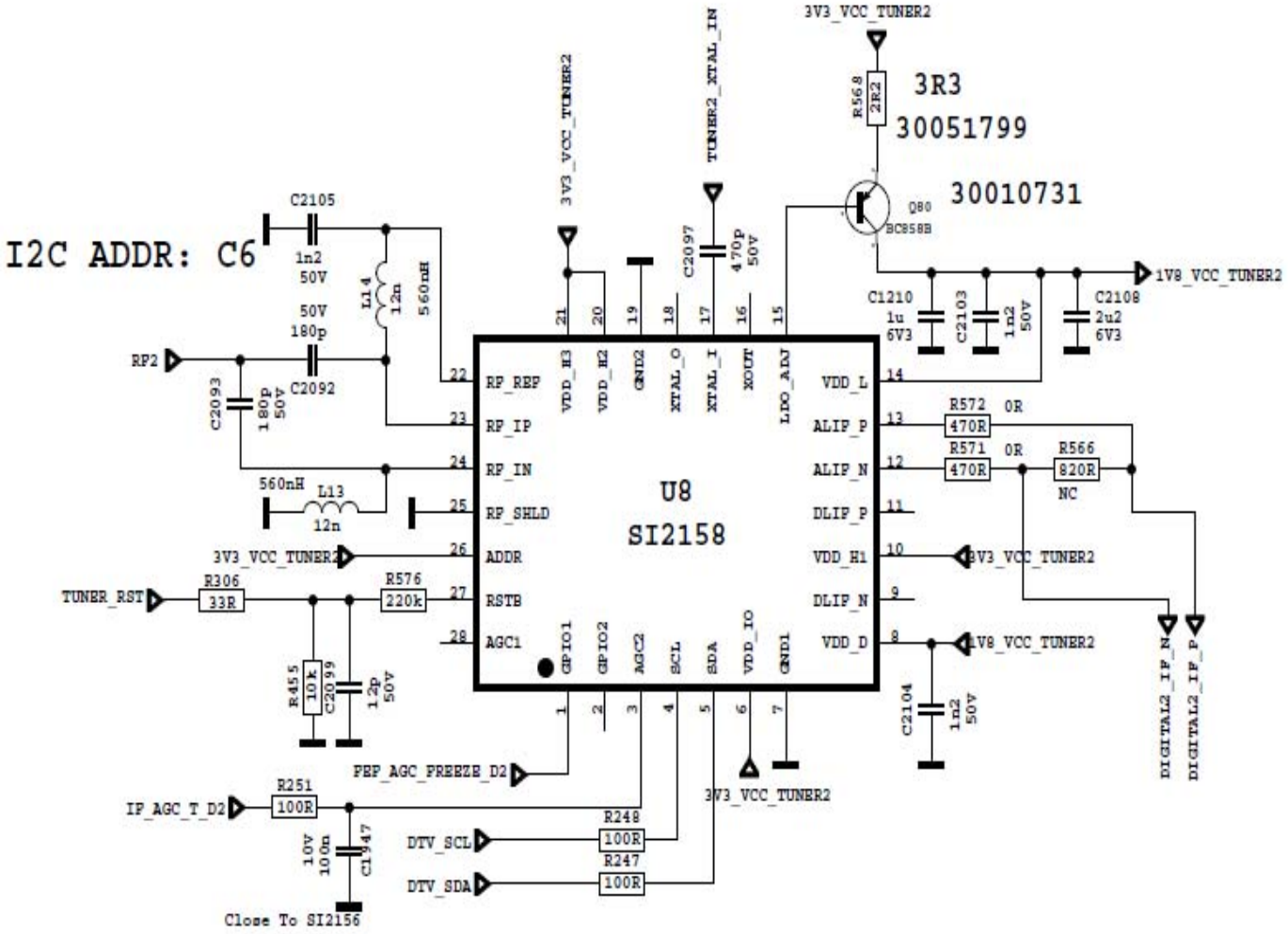
Problem: Device can not boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm. These printouts may give a clue about the problem. You can use mini scart for terraterm connection.

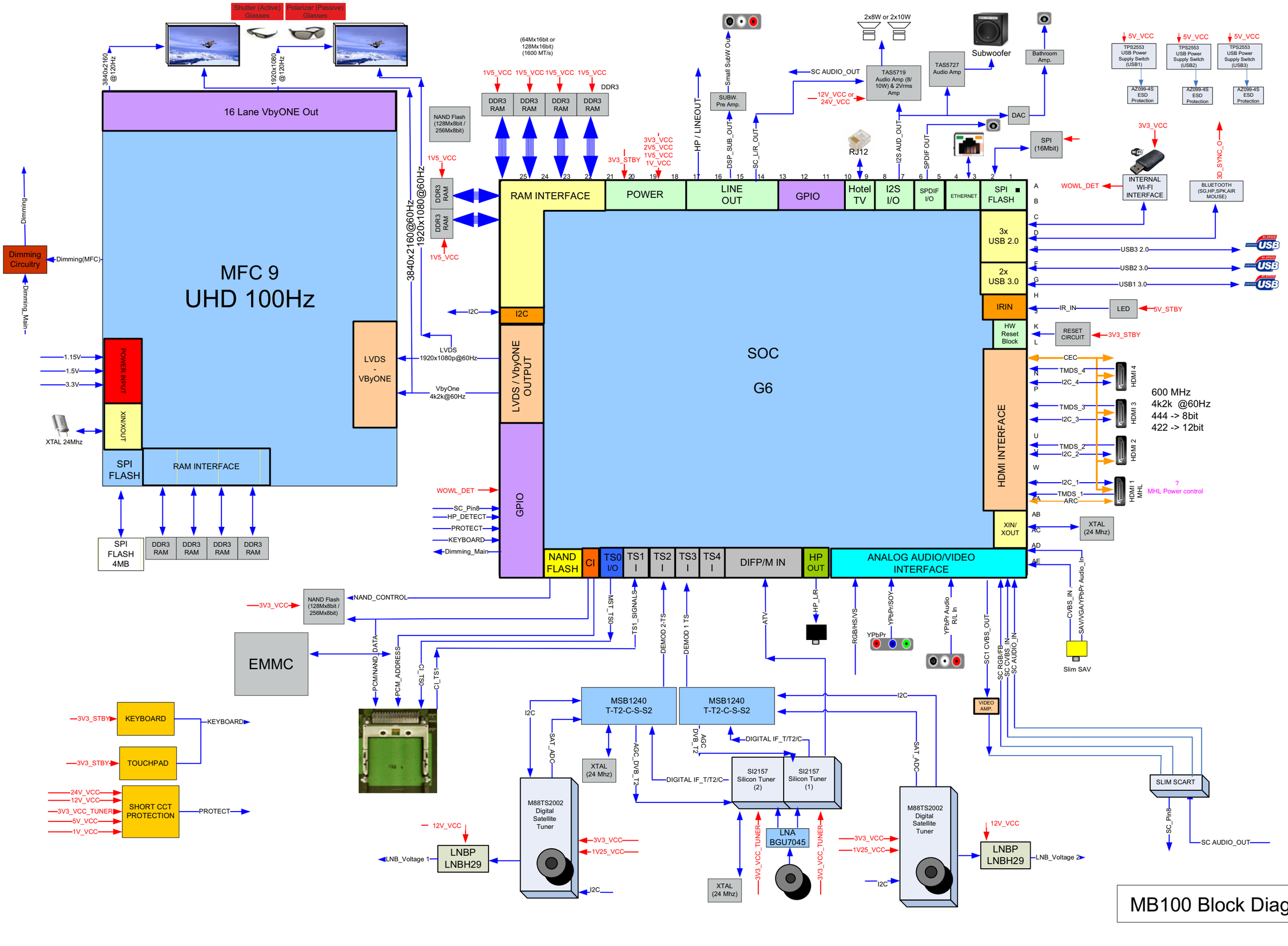
K. *NO SIGNAL PROBLEM*

Problem: No signal in TV mode.

Check tuner supply voltage; 5V_VCC, 3V3_TUNER and 1V8_TUNER. Check tuner options are correctly set in Service menu. Check AGC voltage at IF_AGC pin of tuner.

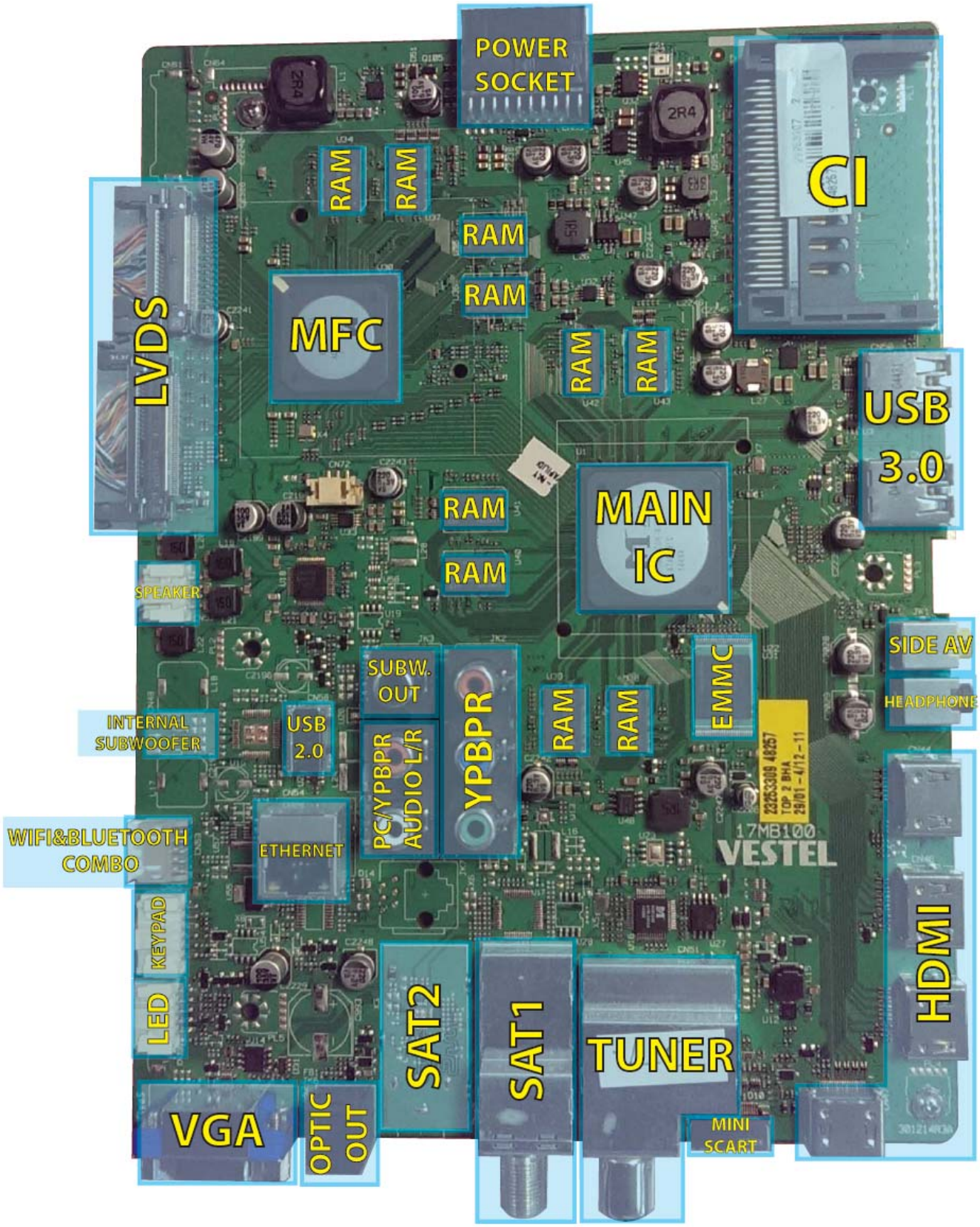

I2C ADDR: C6
U8
SI2158
3V3_VCC_TUNER2
TUNER2_XTAL_IN
1V8_VCC_TUNER2
3R3
30051799
30010731
Q80
BC858B
C2105
1n2
50V
L14
12n
560nH
50V
180p
C2092
C2093
180p
50V
RP2
560nH
L13
12n
R306
33R
TUNER_RST
R576
220k
R455
10k
C2099
12p
50V
Close To SI2156
R251
100R
IF_AGC_T_D2
10V
100n
C1947
PEP_AGC_FREEZE_D2
DTV_SCL
DTV_SDA
R248
100R
R247
100R
C2097
470p
50V
C1210
1u
6V3
C2103
1n2
50V
C2108
2u2
6V3
R572
0R
470R
R571
0R
470R
R566
820R
NC
C2104
1n2
50V
DIGITAL2_IF_N
DIGITAL2_IF_P
RF_REP
RF_IP
RF_IN
RF_SHLD
ADDR
RSTB
AGC1
VDD_H3
VDD_H2
GND2
XTAL_O
XTAL_I
XOUT
LDO_ADJ
VDD_L
ALIF_P
ALIF_N
DLIF_P
VDD_H1
DLIF_N
VDD_D
GPIO1
GPIO2
AGC2
SCL
SDA
VDD_IO
GND1

14. GENERAL BLOCK DIAGRAM



MB100 Block Diagram

15. PLACEMENT OF BLOCKS



CN65
CABLE
C2404 100nH10V
C2402 100nH10V
C2401 10V100nF
C2399 100nH10V
C2396 10V100nF
C2397 10V100nF
C2398 10V100nF
C2400 100nH10V
C2403 100nH10V
VDD_AUDIO
12V_STBY
TP300
5V_STBY
S221
S228
5V_STBY_P
DIMMING
TP309
TP310
BACKLIGHT_ON/OFF
STBY_ON/OFF
TP311
S118
24V_VCC
S370
S263
3D_EN_PW
S220
S222

S223
S226
S225
S224
TP308
FS1
7A/32VDC
TP145
FS2
12V_VCC
Q32
FDS4685
C2249 220n 25V
R682 33k
R535 47R
R681 33k
Q40 BC848B
R435 10k
STBY_ON/OFF_NOT

12V_VCC_SWITCH

5V_VCC_SWITCH
TP143
5V_VCC
C2054 10u 10V
Q95 NTGS3446
R679 33k
R534 47R
100n C1266 16V
R104 1k
STBY_ON/OFF
R105 1k
Q38 BC848B

1V5
TPS54528
F65 0R 60R
C2256 22u 16V
C2257 22u 16V
C1272 100n 16V
C1434 22p 50V
R791 47k
R785 51k
R789 100k
R427 10k
U47
EN VIN VFB VBST VREG5 SSW VSS GND
C1271 100n 16V
L26 1u5
C2213 22u 6V3
C2214 22u 6V3
F64 60R
F63 60R
C2157 1u 16V
C2281 8n2 50V
C2215 22u 6V3

1V15 W/MFC
L1 2u4
C472 22u 6V3
C473 22u 6V3
C2216 22u 6V3
C2217 22u 6V3
C1273 100n 16V
C2277 22n 6V3
U44
TPS54821
PROTECT
S125
PWRGD
RT/CLK
BOOT PH_1 PH_0 EN SS/TR
GND_0 GND_1 PVIN_0 PVIN_1 VIN
COMP
VSENSE
V_SNS
C2286 39p 50V
R50 4k7
C2011 4n7 50V
R733 100R
R837 2k
C2169 560p 50V
R838 2k2
R740 100k
C2278 4u7 16V
R680 33k
R591 8k2
C2283 10u 16V
C2284 10u 16V
C2285 10u 16V
EN_1V15

1V_CORE
***** feedback resistors
1V_VCC_CORE
6V3 2u2
C2107 10n 16V
5V_VCC
C2269 100n 16V
C2268 22u 16V
F67 60R
12V_VCC
VREFIN
S120
R786 56k
VREF_2V
R787 6k8
R788 56k
C2274 100n 16V
R428 10k
R52 4k7
C2297 10n 25V
U49
TPS51363
REFIN2 REFIN VREF NU_2 EN
GSNS VSNS SLEW TRIP GND V5 VIN_2 VIN_1 VIN_0
PGND_4 PGND_3 PGND_2 PGND_1 PGND_0
PGOOD NU_1 MOD NC BST SW_0 SW_1 SW_2 SW_3
NC NC
R992 22R
PROTECT
C1275 100n 16V
30047395 270uF 2V Opt.
C2237 220u 6V3
C2260 22u 16V
C2261 22u 16V
L27 1u5 1uH
1V_VCC_CORE
TP306

549k
S123
R433 200k
560k
R432 1M
R907 549k
Q75 2N7002
Q74 2N7002
R109 1k
VID_0_CORE
VREFIN
R110 1k
VID_1_CORE
***** feedback dirençlari ayarlanacak

3V3_STBY
R429 10k
STBY_ON/OFF
STBY_ON/OFF_NOT
R106 1k
Q39 BC848B
D1 C5V6

5V
TPS54528 / TPS54628
F58 0R 60R
F59 0R 60R
12V_STBY
C2252 22u 16V
C2253 22u 16V
C1268 100n 16V
C1432 22p 50V
VFB_5V_VCC
R835 120k
R796 4k7
R588 22k
R436 10k
U45
EN VIN VFB VBST VREG5 SSW VSS GND
C1267 100n 16V
L2 2u4
F55 60R
F58 60R
F57 60R
F56 60R
5V_VCC
5V_STBY
TP299
C2155 1u 16V
C2279 8n2 50V
C2207 22u 6V3
C2208 22u 6V3
C2209 22u 6V3

1V_CPU
TPS54528
F62 0R 60R
12V_VCC
R867 4k7
C2325 10n 25V
22u 16V
C2254
C2410 10u 16V
C2409 10u 16V
C1433 22p 50V
VFB_1V_CPU
R836 39k
S314
R834 100k
R908 68k
R426 10k
U46
EN VIN VFB VBST VREG5 SSW VSS GND
C1269 100n 16V
L25 1u5
S374
S375
TP305
1V_VCC_CPU
VFB_1V_CPU
C2210 22u 6V3
C2211 22u 6V3
C2212 22u 6V3
C2156 1u 16V
C2280 8n2 50V

1V15 WO/MFC
5V_VCC
R51 4k7
U23
APL5910
POK GND EN FB VIN VOUT VCNTL NC
C1784 100nF 10V
R732 470R
R2
R729 10k
R798 4k7
R1
1V15_VCC_DEMOD
TP144
1V5_VCC
60R
F66
C2056 10uF 10V
S119
C2055 10uF 10V
C1198 22uF 6V3

1V5_STR
12V_VCC
S380
D43
1N5819
5V_STBY
D44
1N5819
C2313 10n 16V
U56
MP1498
SS FB IN VCC SW EN/SYNC GND BST
C2300 10u 16V
C2299 10u 16V
MP2234 kullanilacak
R862 22k
C2304 100n 16V
R856 10k
STR_EN
22R
R852
100n C2303 16V
N.C.
C2315 15p 50V
R864 47k
47k
R859
R904 6k8
L28 10u
2U2 olacak
TP303
1V5_STR
C2309 10u
100n
6V3
10u
C2310
C2308

3V3_STBY
R847 4k7
S260
STR_EN
Q96 BC848B
R848 4k7
STR_ENABLE

5V_STBY
R906 680k
R430 56k
VFB_1V_CPU
R905 470k
R431 1M
***** feedback dirençlari a
Q72 2N7002
Q73 2N7002
R107 1k
VID_0
R108 1k
VID_1

3V3_VCC
12V_VCC
F69 0R 60R
C2374 22u 16V
C2375 22u 16V
C1277 100n 16V
C1435 22p 50V
VFB_3V3_VCC
R784 33k
R697 680R
R730 10k
R437 10k
U48
TPS54528
EN VIN VFB VBST VREG5 SSW VSS GND
C1278 100n 16V
L3 3u3
F70 60R
TP301
3V3_VCC
C2220 22u 6V3
C2219 22u 6V3
C2158 1u 16V
C2282 8n2 50V

3V3_WOWL
12V_VCC
S381
D41
1N5819
5V_STBY
D42
1N5819
C2314 10n 16V
U57
MP1498
SS FB IN VCC SW EN/SYNC GND BST
C2302 10u 16V
C2301 10u 16V
MP2234 kullanilacak
R863 22k
C2306 100n 16V
R857 10k
WOWL_EN
22R
R853
100n C2305 16V
N.C.
C2316 15p 50V
R865 47k
R860 15k
S259
L29 3u3
TP302
3V3_WOWL
C2307
6V3
10u
C2311
100n
6V3
10u
C2312

3V3_STBY
R849 4k7
S261
WOWL_EN
Q97 BC848B
R850 4k7
WOWL_ENABLE

3V3_STBY LDO
UA: 30069495 AP2111
U55
LM1117
IN OUT ADJ VOUT
5V_STBY
10V
10uF
C2059
TP304
3V3_STBY
C2218 22u 6V3
R756 1k
R735 680R
1k
R734

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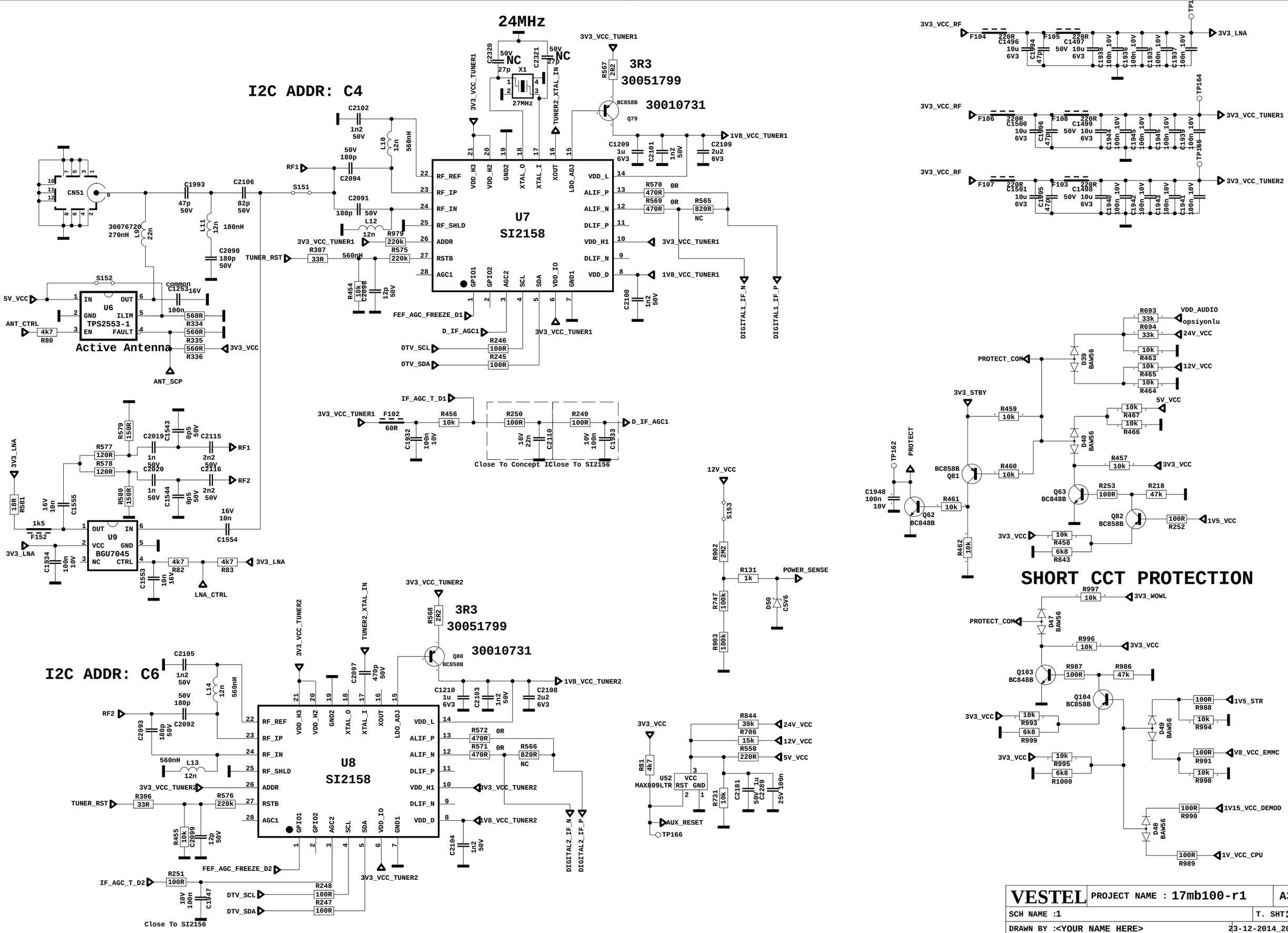
24MHz
I2C ADDR: C4
U7
SI2158
RF_REF
RF_IP
RF_IN
RF_SHLD
ADDR
RSTB
AGC1
VDD_H3
VDD_H2
GND2
XTAL_O
XTAL_I
XOUT
LDO_ADJ
VDD_L
ALIF_P
ALIF_N
DLIF_P
VDD_H1
DLIF_N
VDD_D
GPIO1
GPIO2
AGC2
SCL
SDA
VDD_IO
GND1
3V3_VCC_TUNER1
1V8_VCC_TUNER1
TUNER2_XTAL_IN
3R3
30051799
30010731
BC858B
Q79
27MHz
X1
NC
TUNER_RST
FEF_AGC_FREEZE_D1
D_IF_AGC1
DTV_SCL
DTV_SDA
DIGITAL1_IF_N
DIGITAL1_IF_P
Active Antenna
U6
TPS2553-1
ANT_CTRL
ANT_SCP
5V_VCC
3V3_VCC
CN51
S151
S152
common
RF1
RF2
3V3_LNA
LNA_CTRL
U9
BGU7045
F152
Close To Concept IClose To SI2156
I2C ADDR: C6
U8
SI2158
3V3_VCC_TUNER2
1V8_VCC_TUNER2
TUNER_RST
FEF_AGC_FREEZE_D2
IF_AGC_T_D2
DTV_SCL
DTV_SDA
DIGITAL2_IF_N
DIGITAL2_IF_P
Close To SI2156
12V_VCC
POWER_SENSE
AUX_RESET
TP166
3V3_STBY
PROTECT_COM
PROTECT
SHORT CCT PROTECTION
3V3_WOWL
3V3_LNA
3V3_VCC_RF
3V3_VCC_TUNER1
3V3_VCC_TUNER2
VDD_AUDIO
opsiyonlu
24V_VCC
12V_VCC
5V_VCC
1V5_STR
1V8_VCC_EMMC
1V15_VCC_DEMOD
1V_VCC_CPU
1V5_VCC
TP162
TP163
TP164
TP165
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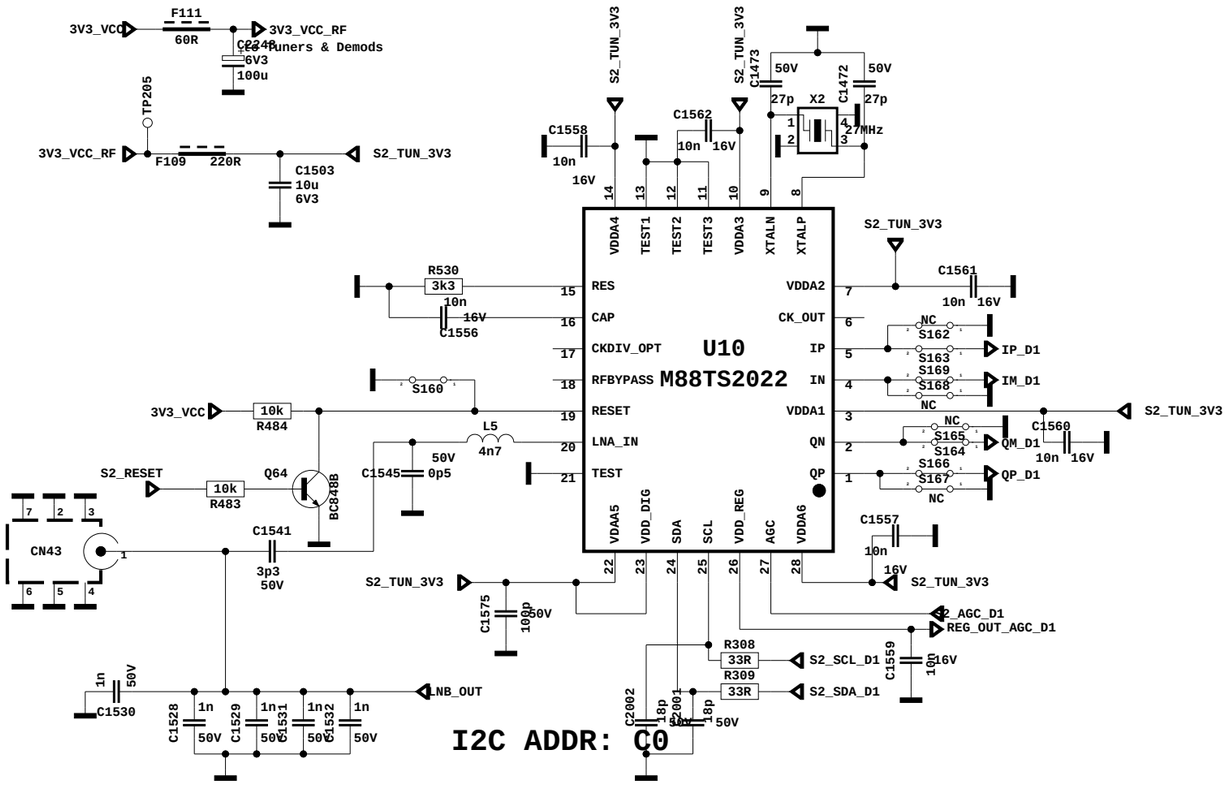

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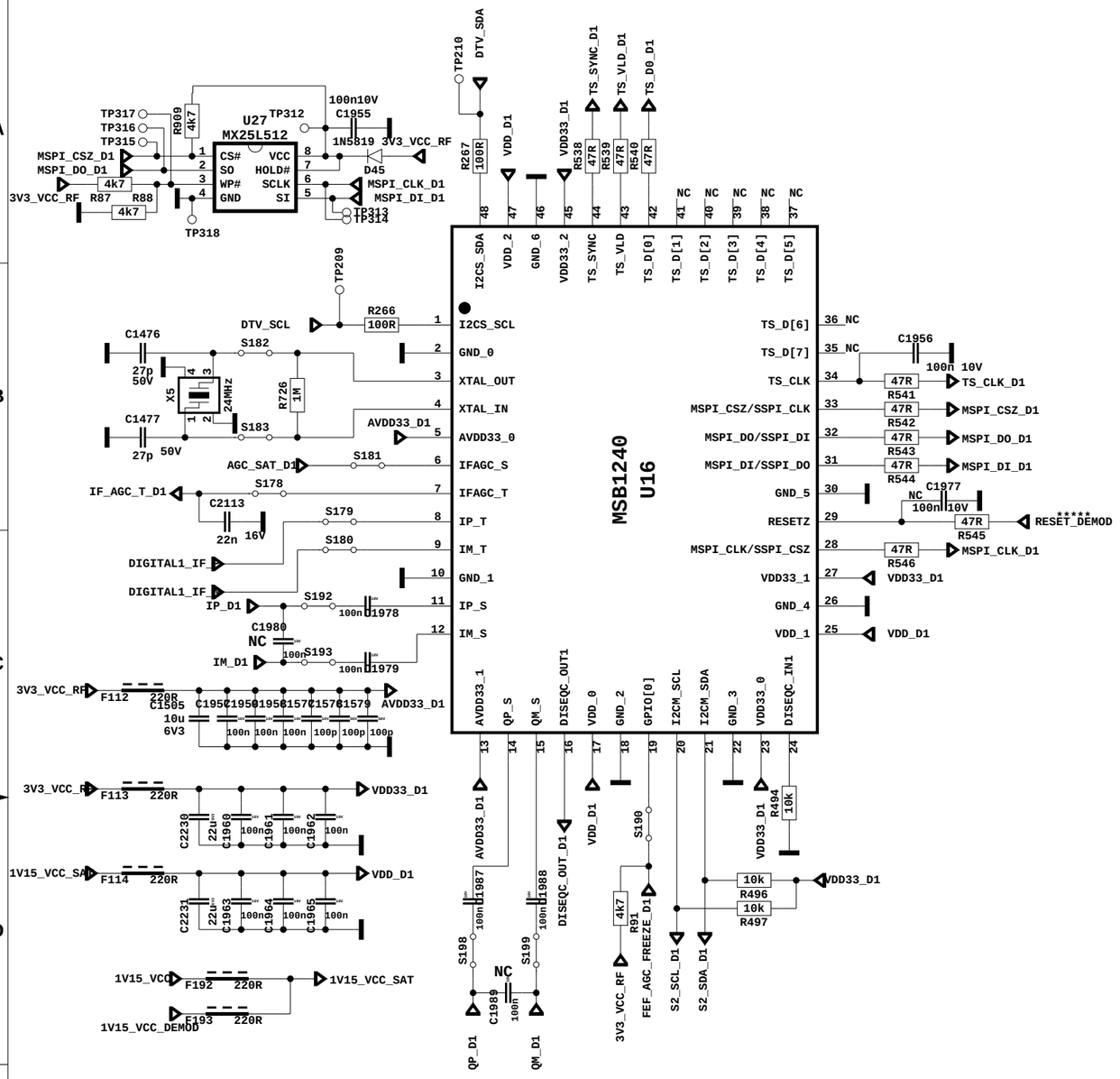

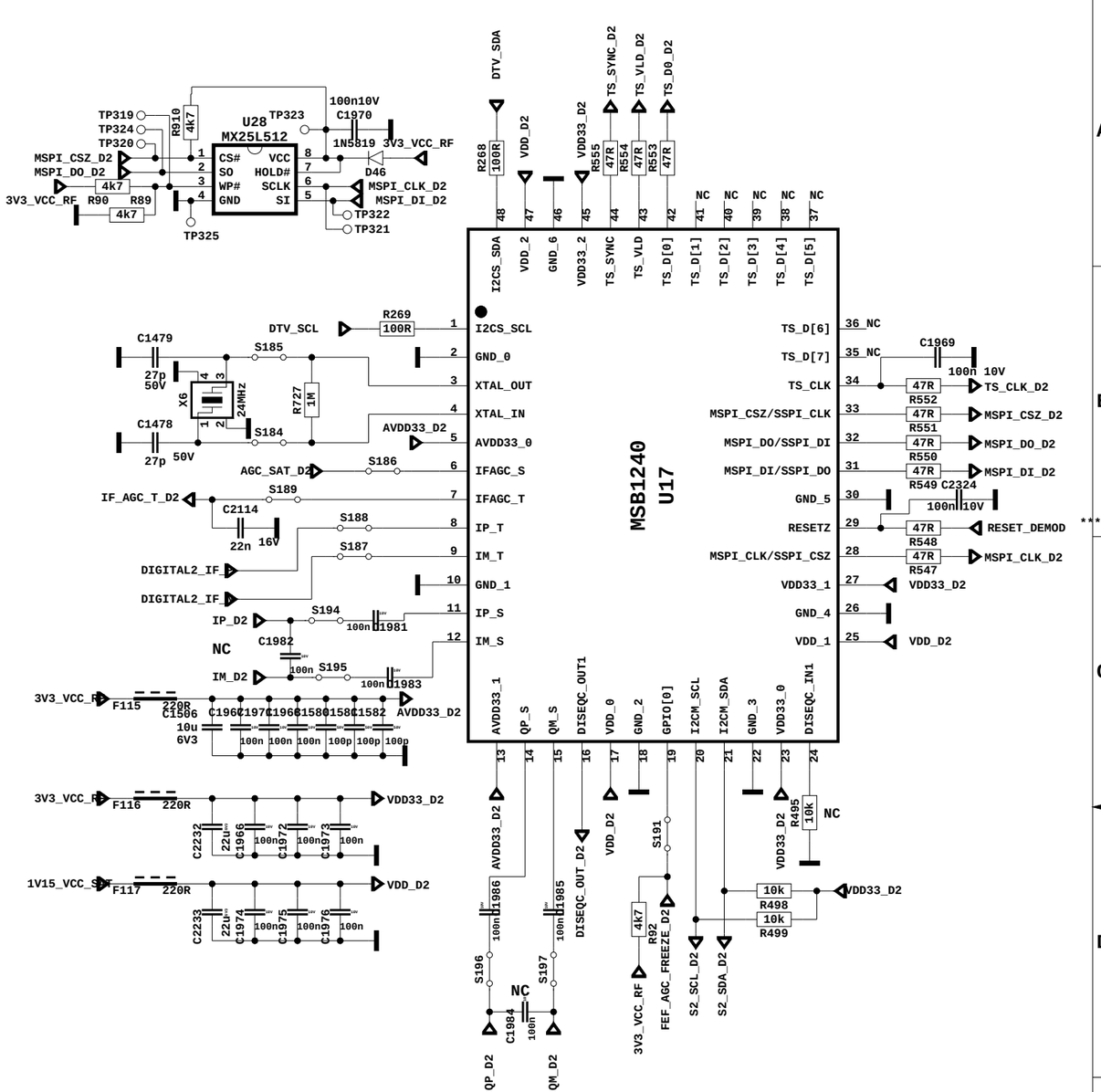

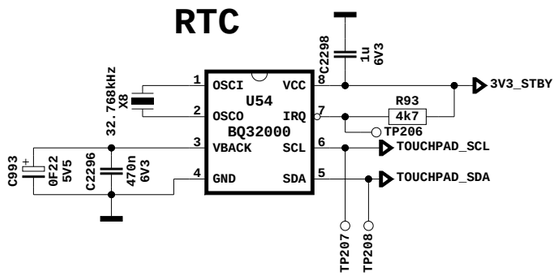

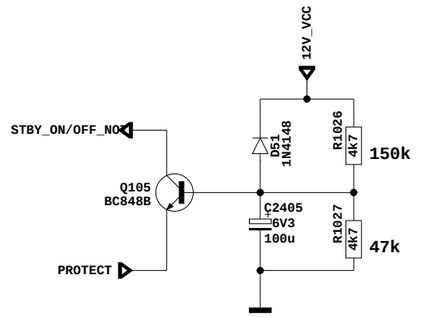

PROTECTION CIRCUIT

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SCART 1

SC1

TP176 TP175 TP174 TP173 TP168 TP167 TP169 TP170 TP171 TP177 TP179 TP178 TP180 TP186

D11 CDA4C16GTH D10 CDA4C16GTH

R372 75R

C2006 33p 50V

SC_CVBS_IN

C2010 33p 50V

SC_CVBS_OUT

R371 75R

C2007 33p 50V

R537 47R

SC_FB

C2008 33p 50V

SC_R

R370 75R

UART-TX-SC

R369 75R

C2009 33p 50V

D15 C15V

SC_G

R366 75R

UART-RX-SC

R367 75R

R557 22k

SC_PIN8

SC_B

R84 4k7

C1949 100n 10V

C2005 33p 50V

C1448 330p 50V

SCART_AUD_L_IN

C1449 330p 50V

SCART_AUD_R_IN

F118 600R

R254 100R

SC_AUD_L_OUT

C2012 50V 4n7

F119 600R

R255 100R

SC_AUD_R_OUT

C2013 4n7 50V

SCART AUDIO FILTERS

SCART_AUD_L_IN R476 10k SC_AUD_L_IN

SCART_AUD_R_IN R475 10k SC_AUD_R_IN

C1454 330p 50V C1455 330p 50V R606 12k R607 12k C2172 560p 50V C2173 560p 50V

SAV_AUD_L_IN R482 10k SAV_L_IN

SAV_AUD_R_IN R481 10k SAV_R_IN

C1456 330p 50V C1457 330p 50V R609 12k R608 12k C2175 560p 50V C2174 560p 50V

SLIM SIDE AV

TP181 TP182 D3 C5V6 C1463 220p 50V R373 75R

F120 600R SAV_CVBS C1450

TP183 F122 600R 330p 50V SAV_AUD_L_IN

JK1 F123 600R C1451 330p 50V

F121 600R SAV_AUD_R_IN

TP184

YPBPR INPUT or SOUNDBAR & SUBWOOFER

TP185 S231 S230 SUBW_OUT_P F124 600R PR_IN

JK2 RED S232 S233 SUBW_OUT_N

S234 S237 SOUNDB_R_P F125 600R PB_IN

BLU TP187 S236 SOUNDB_R_N

GRN S235

TP186 S238 SOUNDB_L_P

F126 600R 220n L4 50V 4p7 C1493 C1440 50V 22p Y_IN

S154 50V 22p TP188 1441

C1468 27p 50V C1466 27p 50V C1467 27p 50V R376 75R R374 75R R375 75R

S239 S240 SOUNDB_L_N

YPBPR AUDIO & SUB WOOFER

S241 TP192 WHT RED JK3 BLK

C1453 330p 50V R603 12k C2170 560p 50V R604 12k

TP191 R469 10k YPBPR_L

TP190 R468 10k YPBPR_R

C1452 330p 50V R602 12k R605 12k

TP189 F127 600R C2171 560p 50V R256 100R SUBW_OUT

R597 75k C2021 1n 50V

SUB WOOFER AMP

TAS5727 U15

VDD_SUBW CLOSE TO PIN34 & 35 CLOSE TO PIN2 & 3

C2196 100u 35V C2201 100n 50V C2202 100n 50V C2198 100u 35V C2203 100n 50V C2200 100n 50V

3V3_VCC F147 330R SUBW_AVDD

C1502 10u 6V3 C1412 100n 16V

C2014 4n7 50V C1212 47n 16V R573 470R

C2015 4n7 50V C1213 47n 16V R574 470R

3V3_VCC R480 10k C2117 2n2 50V C2134 33n 50V VDD_SUBW

24V_VCC S245 S244 VDD_SUBW

VDD_AUDIO S378 S379

SUBW_AVDD 4k7 3V3_VCC ADRES SECIMI R85 4k7 S156 R86 10k nc R479

10V 4u7 R652 18k2 C2176 C1411 100n 16V I2S_OUT_MCK

PDN

I2S_OUT_WS S159 I2S_OUT_BCK S158 I2S_OUT_SD S157

SYS_SDA 100R R259 SYS_SCL 100R R258

AVDD A_SEL_FAULT MCLK OSC_RES DVSSO VR_DIG PDNN LRCLK SCLK SDIN SDA SCL

VR_ANA PLL_FLTP PLL_FLTM AVSS PBTL NC_2 SSTIMER NC_1 BST_A PVDD_AB_2 PVDD_AB_1 OUT_A

RESETN STEST DVDD DVSS GND AGND VREG GVDD_OUT BST_D PVDD_CD_1 PVDD_CD_2 OUT_D

PGND_AB_2 PGND_AB_1 OUT_B NC_6 NC_5 BST_B BST_C NC_4 NC_3 OUT_C PGND_CD_2 PGND_CD_1

L17 4u7 SUBW_OUT_N

50V 33n C2132 10R R582 C2122 680p 50V C2121 680p 50V C2149 220n 50V C2150 220n 50V

50V 33n C2133

L18 4u7 SUBW_OUT_P

R583 10R C2120 680p 50V C2119 680p 50V C2152 220n 50V C2151 220n 50V

EXT_RESET 100R R257 C1527 1n 50V C1409 100n 16V C2159 16V C1410 100n 16V C2131 33n 50V VDD_SUBW

AMP_EN R477 10k SUBWOOFER_EN R478 10k PDN

3V3_VCC F146 330R

CN48 SUBW_OUT_P TP204 SUBW_OUT_N TP203

VGA INPUT

VGA CONNECTOR

VGA CN52 SHIELD1 GND1 SCL VSYNC HSYNC SDA ID0 SGND KEY BGND GGND RGND GND RESERVED BLUE GREEN RED SHIELD2 GND2

D13 CDA4C16GTH

R470 10k R472 10k R473 10k C1950 100n 10V

5V_VCC D30 BAV70 VGA_DDC_5V

24C02 option R471 10k R650 100R

U14 ST24LC216 VCC A0 WP A1 SCL A2 SDA GND

TP195 TP194 TP193 TP196

S155 F153 1k VGA_DDC_5V TP201

R474 10k R612 510R VGA_VSNC R613 510R VGA_HSNC R651 2k4

TP200

C1470 27p 50V C1471 27p 50V C1469 27p 50V

F154 1k F155 1k F156 1k

VGA_B VGA_G VGA_R

D31 NUP4604M5

TP199 TP198 TP202

R379 75R R377 75R R378 75R

VESTEL	PROJECT NAME : 17mb100-r1		A3
SCH NAME :5		T. SHT	5
DRAWN BY :<YOUR NAME HERE>		24-12-2014_08:52	

hotel tv locatel

OPTIONAL RESISTORS
75R R382
75R R381
75R R380

VGA_R
VGA_G
VGA_B
VGA_G
VGA_HSNC
VGA_VSNC
SC_R
SC_G
SC_B
PR_IN
Y_IN
PB_IN
Y_IN
SC_FB
SC_CVBS_IN
SAV_CVBS
SC_CVBS_OUT
75R R861
to avoid EMI close to NC
C2087 120p 50V
R790 75R

U1 MSD95C0H

RIN0M RIN0P GIN0M GIN0P BIN0M BIN0P SOGIN0 HSYNC0 VSYNC0
RIN1M RIN1P GIN1M GIN1P BIN1M BIN1P SOGIN1 HSYNC1 VSYNC1
RIN2M RIN2P GIN2M GIN2P BIN2M BIN2P SOGIN2 HSYNC2
VCOM
CVBS0 CVBS1 CVBS2
CVBSOUT1

TN TP RN RP
GPIO80 GPIO79
HWRESET
XIN XOUT
IRIN
DM_P0 DP_P0 DM_P1 DP_P1 DM_P2 DP_P2
SSUSB_TXP1 SSUSB_TXN1 DM_PSS1 DP_PSS1 SSUSB_RXP1 SSUSB_RXN1 SSUSB_TXP0 SSUSB_TXN0 DM_PSS DP_PSS SSUSB_RXP0 SSUSB_RXN0

ETH_TXN ETH_TXP ETH_RXN ETH_RXP
3V3_VCC
R723 5k1 R724 5k1
NC
ETH_YEL ETH_GRN
5k1 R721 5k1 R722
TP219R275 100R RESET_G6
XIN_G6 XOUT_G6
R276 100R IR_IN
USB3_DN USB3_DP USB_WIFI_DN USB_WIFI_DP USB_BT_DN USB_BT_DP USB1_TXP USB1_TXN USB1_DN USB1_DP USB1_RXP USB1_RXN USB2_TXP USB2_TXN USB2_DN USB2_DP USB2_RXP USB2_RXN

JK7
TV_CLOCK DCM_DATA VCC TV_DATA GND TR_DATA
D14 CDA4C16GTH
TP236 TP237 TP238 TP239 TP240
C2089 10u 10V
3V3_STBY
R101 4k7
Q71 8C848B
IR_IN
R277 100R
F151 330R
100R R284
100R R285
R99 4k7 nc
4k7 R100
3V3_STBY
RS232_TX RS232_RX
5V_STBY

U53 ST3222
EN SHDN C1+ VCC V+ GND C1- T1OUT C2+ R1IN C2- R1OUT V- NC2 T2OUT T1IN R2IN T2IN R2OUT NC1
C1423 100n 16V
C1424 100n 16V
C1425 100n 16V
C1426 100n 16V
C1427 100n 16V
3V3_STBY
RS232_TX
RS232_RX
100R R280 RX_HOTEL
100R R281 TX_HOTEL
100R R283 RX_G6
4k7 R97 3V3_STBY
100R R282 TX_G6
4k7 R98 3V3_STBY
R278 100R 3V3_STBY
R279 100R 5V_STBY
TX_HOTEL S219 RS232_TX
RX_HOTEL S218 RS232_RX

ETHERNET

CN54
ETH_TXP ETH_TXN ETH_RXP ETH_RXN
TD+ TD- TCT RD+ RD- RCT NC1 NC2 GR+ GR- YL+ YL- SHLD1 SHLD2
ETH_GRN 510R R615
ETH_YEL 510R R614
TP220
1uC2167 16V
C2241 100n 16V
1uC2168 16V
C1255 100n 16V
Place these capacitors close to transformer
speed nets, except for the chassis ground.
Also keep traces short and route as matched length differential pairs. Do not place any parts or traces under the transformer.
Ethernet lines must be 100ohm differential pairs

LED&VFD&RF

CN73 1 2 3 4 5 6 7 8 9 10
TP233 TP232 TP234 TP235 TP231
CN56 1 2 3 4 5
5V_STBY_P F130 600R F133 600R 3V3_STBY
W/PW07
F132 600R 5V_STBY
TP326
S212
TP230
TP228 TP227
S217 TOUCHPAD_SDA
S208 TX_G6
S210 SYS_SDA
S216 TOUCHPAD_SCL
S209 SYS_SCL
S207 RX_G6
C1489 27p 50V
C1490 27p 50V
S213
F129 600R
F128 600R
C1483 27p 50V
10k R522
10k R512
10k R518
10k R520
C1488 27p 50V
C1487 27p 50V
IR_IN
10k R525
R521 10k
LED2
R514 10k
Q68 BC848B
R519 10k
Q84 BC858B
Q83 BC858B
220R R564
220R R561
220R R563
220R R562
10k R516
10k R515
C1492 27p 50V
C1491 27p 50V
R524 10k
Q70 BC848B
R513 10k LED1
10k R523
Q69 BC848B
R517 10k
C1484 27p 50V
R511 10k LED3
3V3_STBY S214
5V_STBY S215
5V_STBY_P S206
W/PW07

XIN_G6 XOUT_G6
S203 S202
24MHz
X7
27p C1480
C1482 27p
XTAL

3V3_STBY
R133 1k
C1990 100n 10V
C1206 22u 16V
RESET
RESET_G6
D36 1N4148
R510 10k
C1991 100n 10V

KEYBOARD

D5 C5V6
C1992 100n 10V
S205 R556 47R F160 1k KEYBOARD
TOUCH_PAD_OPTION
S204
F159 1k 3V3_STBY
F161 1k TOUCHPAD_SCL
F162 1k TOUCHPAD_SDA
TP224 TP223 TP222 TP221 TP225 TP226
D7 C5V6
D6 C5V6
CN55 1 2 3 4 5 6

VESTEL	PROJECT NAME : 17mb100-r1	A3
SCH NAME :9		T. SHT 9
DRAWN BY :<YOUR NAME HERE>		28-10-2014_10:16

AUDIO

TAS5719
U18

CN53
R_AUDIO_P TP212
R_AUDIO_N TP213
L_AUDIO_P TP211
L_AUDIO_N TP214

VDD_AUDIO
24V_VCC
S243 S251 S250 S249 S248 S242
S360 S361 S362
VDD_AMP
12V_VCC

VDD_AMP
C2199 100u 35V
C2204 100n 50V
C2198 100u 35V
C2205 100n 50V
C2369 100n 50V
C2370 100n 50V
CLOSE TO PIN46
CLOSE TO PIN35

AUDIO_AVDD
3V3_VCC
ADRES SECIMI
I2S_OUT_MCK
I2S_OUT_WS
I2S_OUT_BCK
I2S_OUT_SD
SYS_SDA
SYS_SCL
AMP_EN
EXT_RESET

AVDD
A_SEL
MCLK
OSC_RES
DVSSO
VR_DIG
PDN
LRCLK
SCLK
SDIN
SDA
SCL
VR_ANA
PLL_FLTP
PLL_FLTM
AVSS
HPVDD
CPP
CPN
HPVSS
HPR_IN
HPR_OUT
HPL_OUT
HPL_IN
RESETN
STEST
DVDD
DVSS
GND
AGND
VREG
SSTIMER
HP_SD
GVDD_OUT
PVDD_CD
BST_D
HP_PWML
HP_PWMR
PVDD_AB
BST_A
OUT_A
PGND_AB
OUT_B
BST_B
OUT_C
PGND_CD
OUT_D

L22 15u
L21 15u
L19 15u
L20 15u
CLOSE TO TAS5719
SOUNDB_L_P
SOUNDB_L_N
SOUNDB_R_P
SOUNDB_R_N
L_AUDIO_P
L_AUDIO_N
R_AUDIO_P
R_AUDIO_N
S252 S253 S254 S255

HEADPHONE OUTPUT

HP_OUT_L_MSTAR
HP_OUT_R_MSTAR
HP_MUTE
HP_L
HP_R
Q67 BC848B
Q66 BC848B

DAC
for bathroom speaker

U19
CS4334
SDATA AOUTL
SCLK VA
LRCK AGND
MCLK AOUTR
I2S_OUT_SD
I2S_OUT_BCK
I2S_OUT_WS
I2S_OUT_MCK
Bathroom_L
Bathroom_R

Bathroom Speaker Amplifier

GND(pins 1- 2) ortaklanmali.

U20
LM4675SD
IN+ VO2
IN- PVDD
VDD GND
SHDN VO1
Bathroom_IN
AMP_EN
Bathroom_Out1
Bathroom_Out2
VDD_Bath

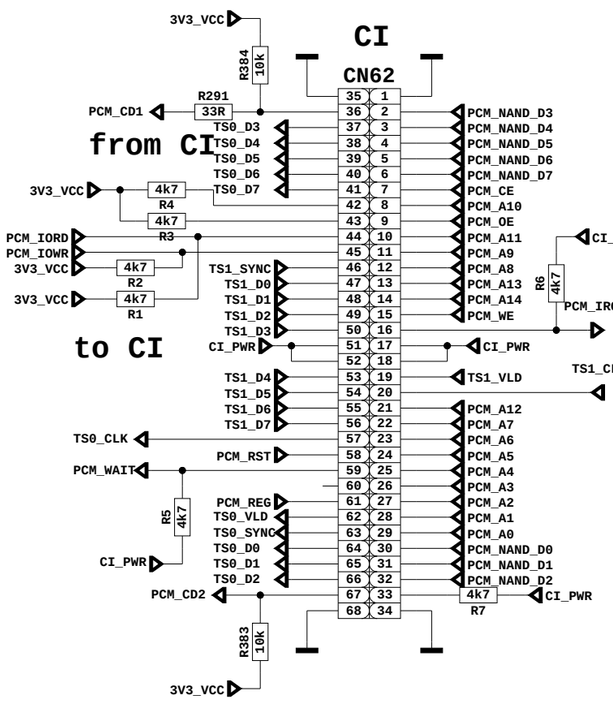
BATHROOM SPK.

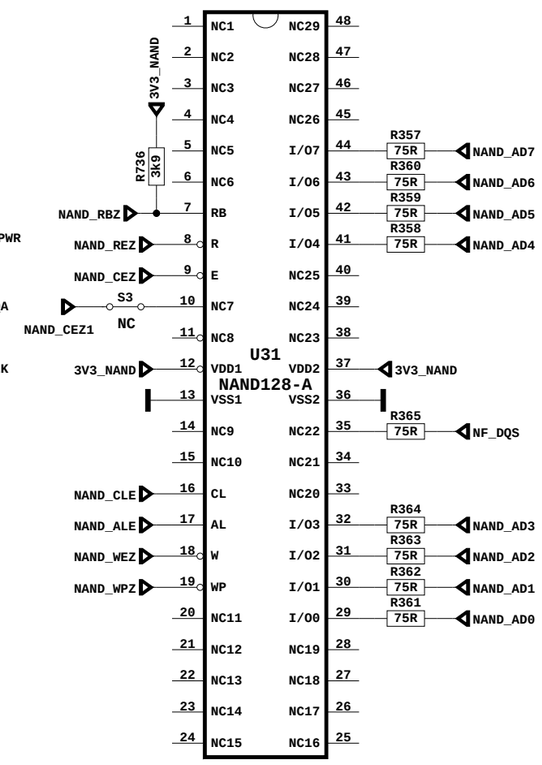
JK4
Bathroom_Out1_1
Bathroom_Out2_2

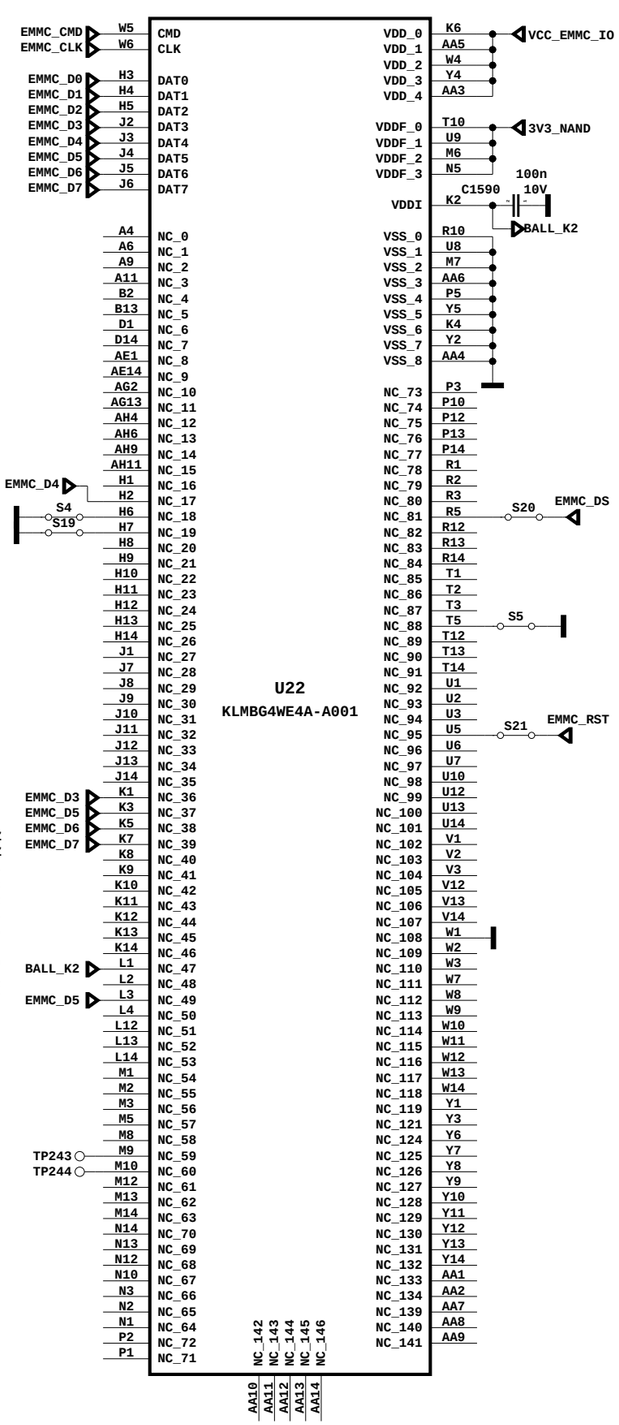
SUB WOOFER PREAMP

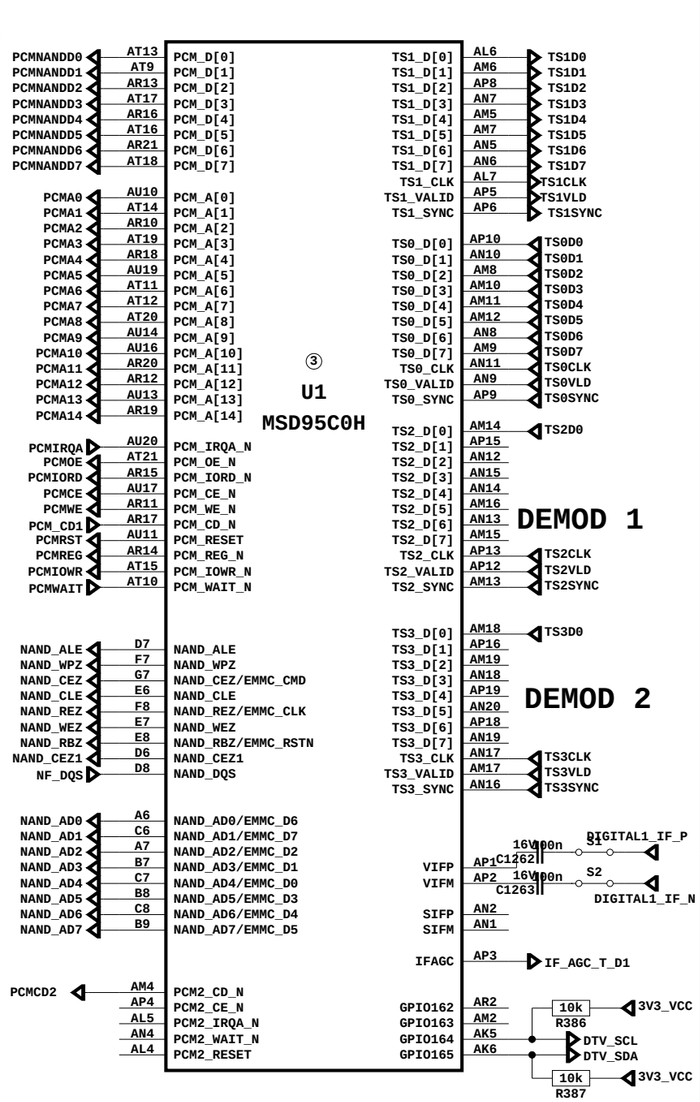
U21
DRV632
INR_P INL_P
INR_N INL_N
OUTR OUTL
GND UVP
MUTE GND1
VSS VDD
CN CP
SUB_R_OUT
SUB_L_OUT
SUBW_OUT
SUBWOOFER_EN
AMP_EN

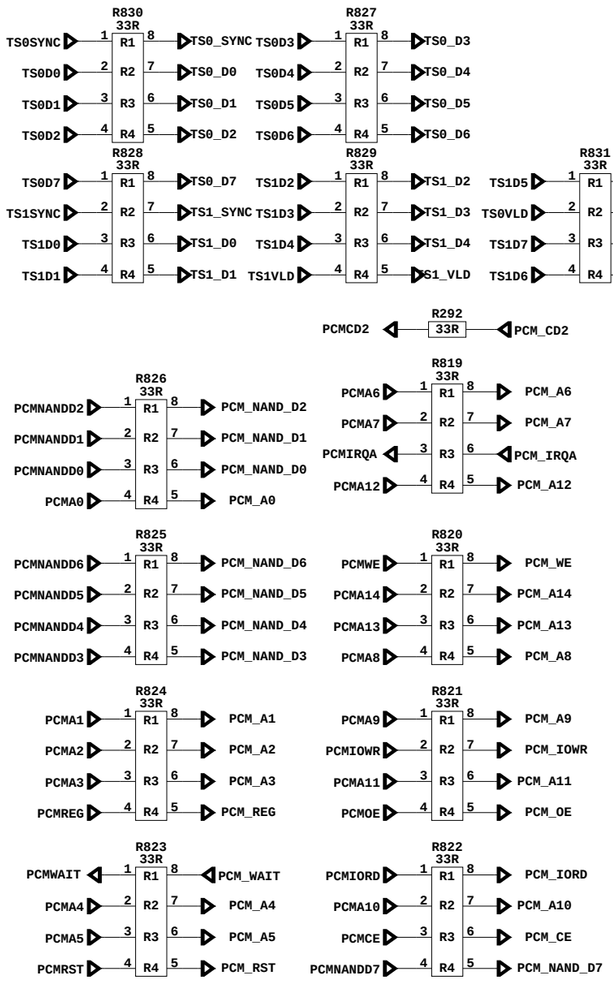
DSP_SUB_L_OUT
DSP_SUB_R_OUT
DSP_SC_L_OUT
DSP_SC_R_OUT
SUB_L
SUB_R
SC_L_OUT
SC_R_OUT
SC_AUD_L_OUT
SC_AUD_R_OUT
LINE_L_IN
LINE_R_IN

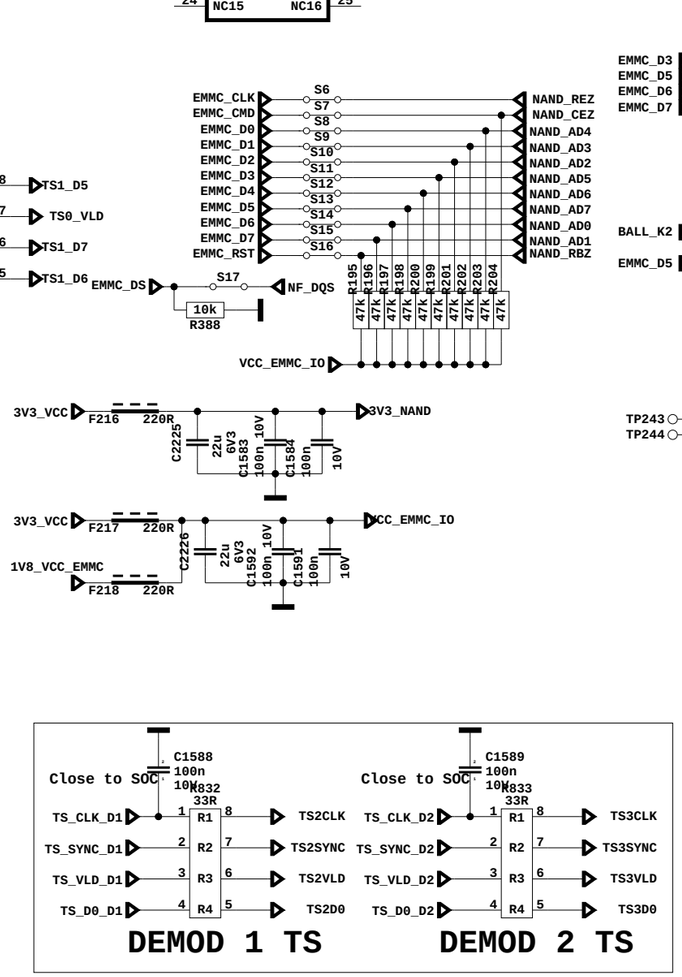


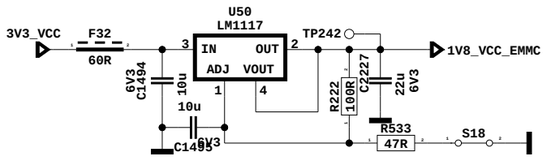


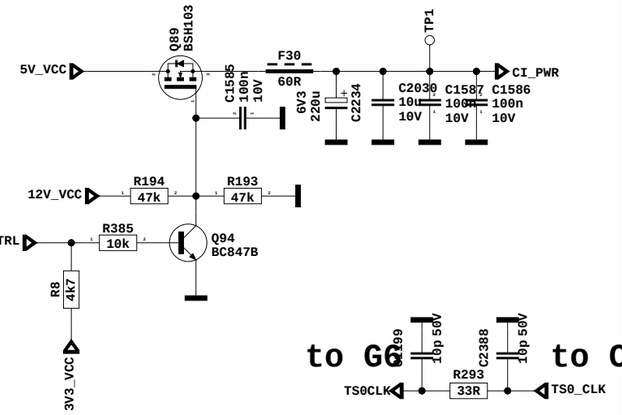




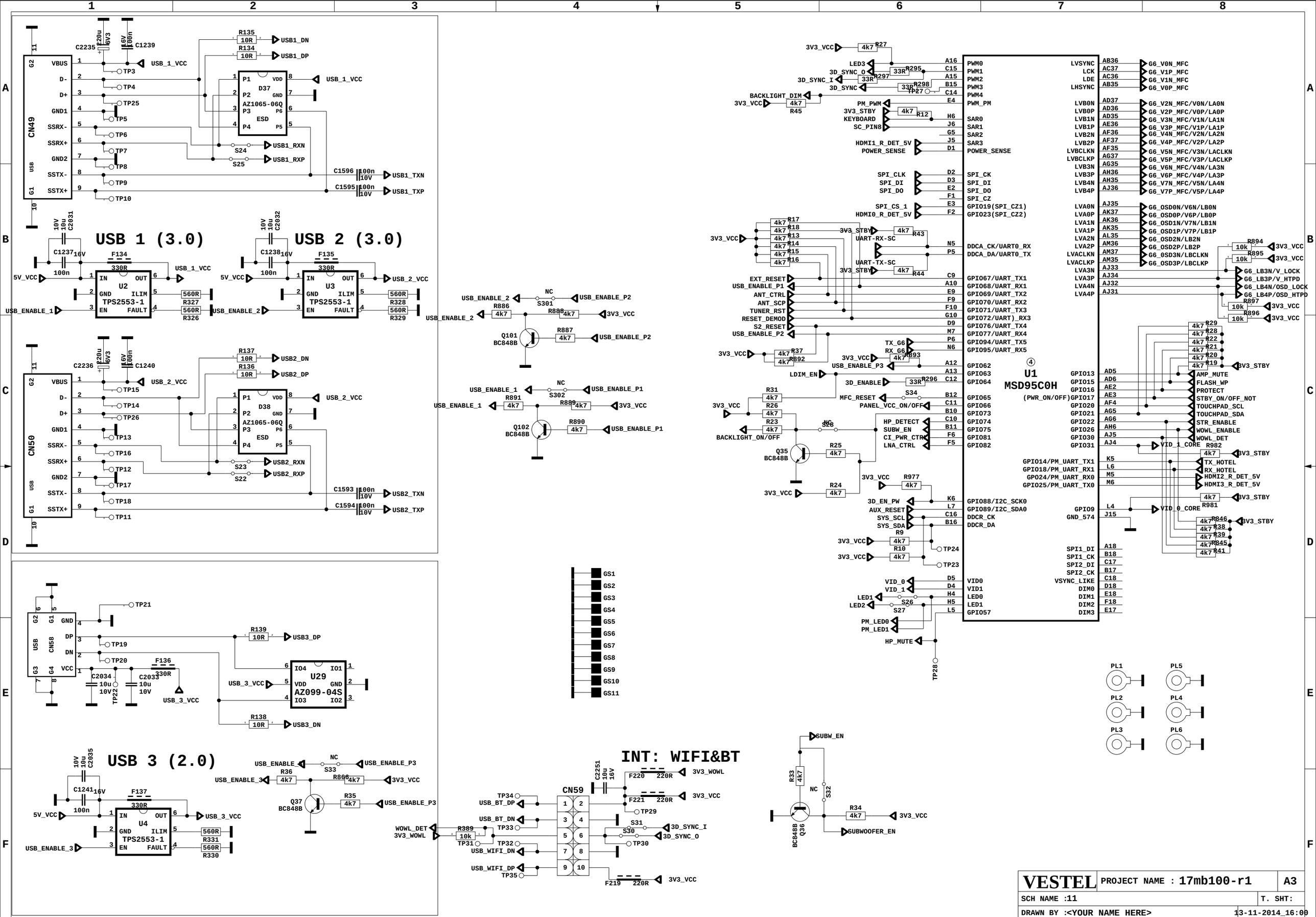






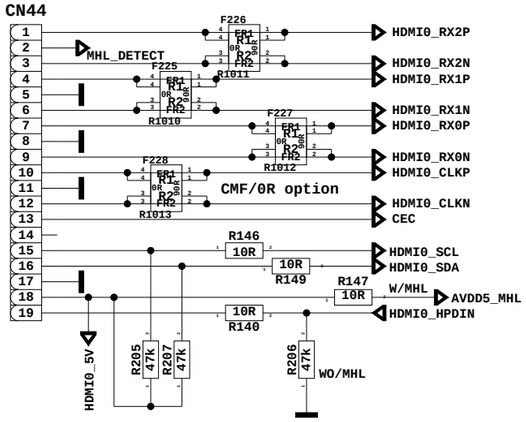


VESTEL	PROJECT NAME : 17mb100-r1	A3
	SCH NAME :1	T. SHT 1
	DRAWN BY :<YOUR NAME HERE>	13-11-2014_09:49


CN49
USB 1 (3.0)
U2
TPS2553-1
U3
TPS2553-1
D37
AZ1065-06Q
ESD
CN50
USB 2 (3.0)
U4
TPS2553-1
D38
AZ1065-06Q
ESD
CN58
USB 3 (2.0)
U29
AZ099-04S
Q101
BC848B
Q102
BC848B
Q35
BC848B
Q37
BC848B
Q36
BC848B
CN59
INT: WIFI&BT
U1
MSD95C0H
(PWR_ON/OFF)
PL1
PL2
PL3
PL4
PL5
PL6
VESTEL
PROJECT NAME : 17mb100-r1
A3
SCH NAME :11
T. SHT:
DRAWN BY :<YOUR NAME HERE>
13-11-2014_16:00

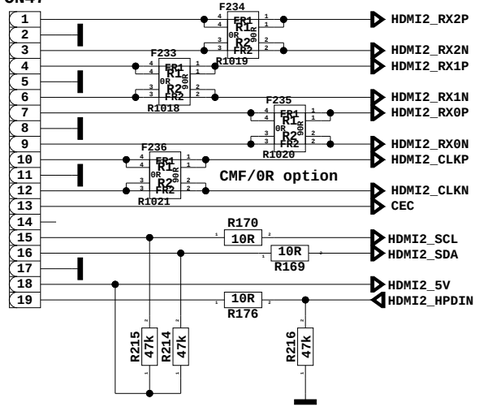
HDMI 4 (MHL)

CN44



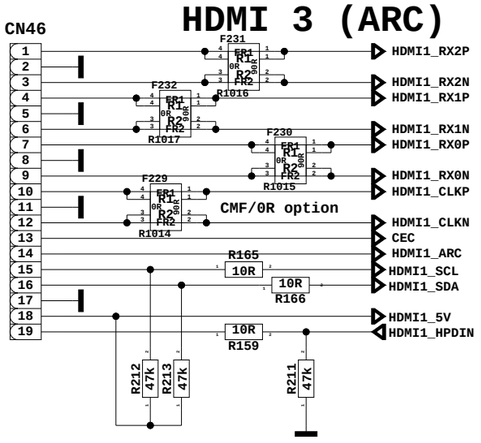
HDMI 1

CN47



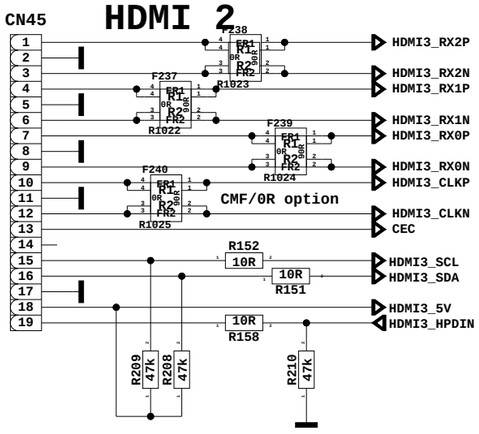
HDMI 3 (ARC)

CN46

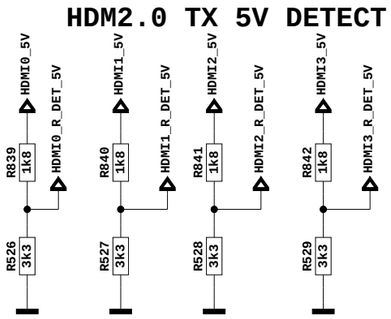


HDMI 2

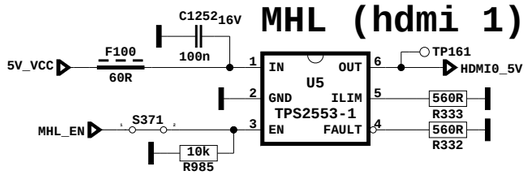
CN45



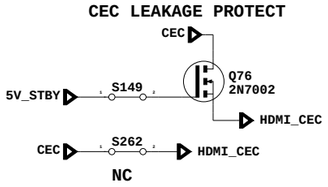
HDM2.0 TX 5V DETECT



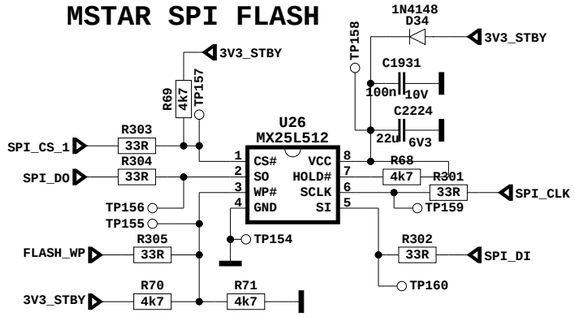
MHL (hdmi 1)



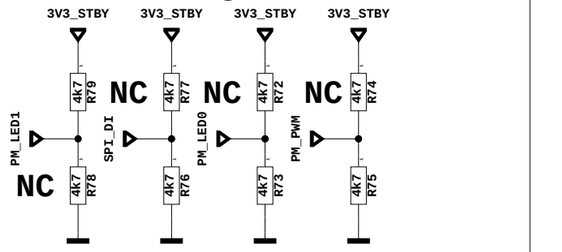
CEC LEAKAGE PROTECT



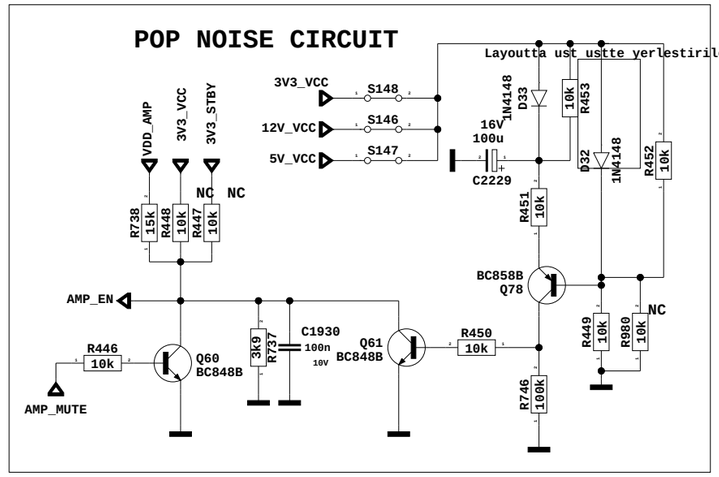
MSTAR SPI FLASH



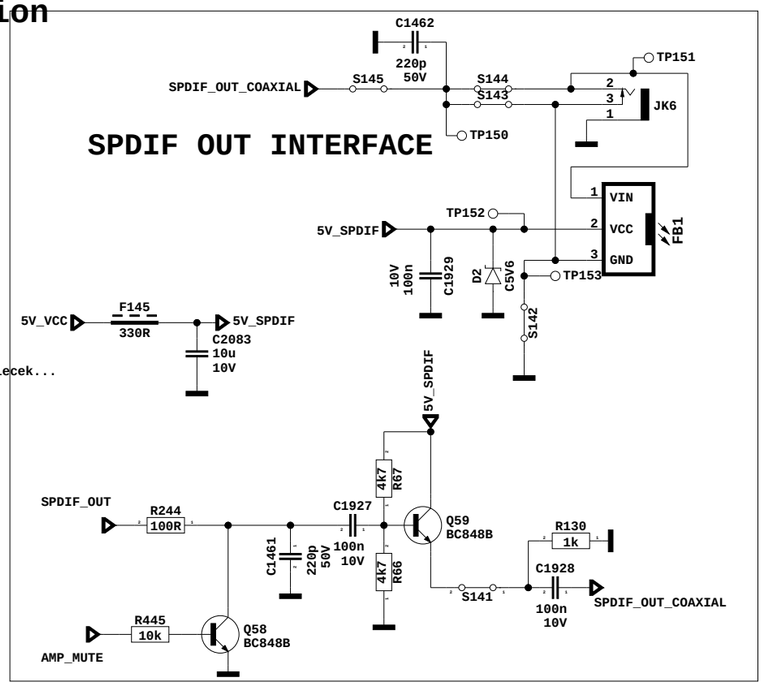
IC Configuration Selection



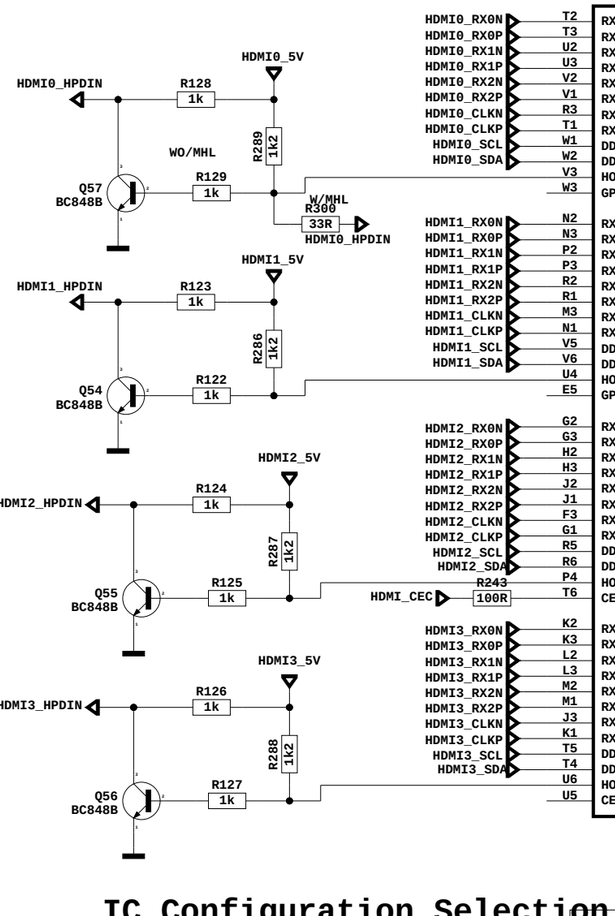
POP NOISE CIRCUIT



SPDIF OUT INTERFACE



IC Configuration Selection



VESTEL	PROJECT NAME : 17mb100-r1	A3
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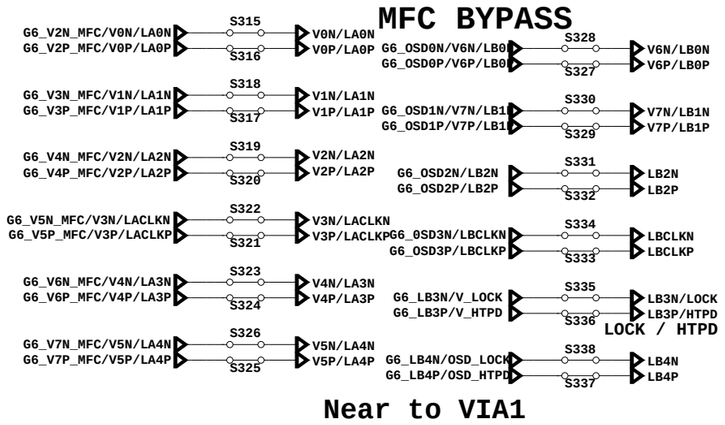

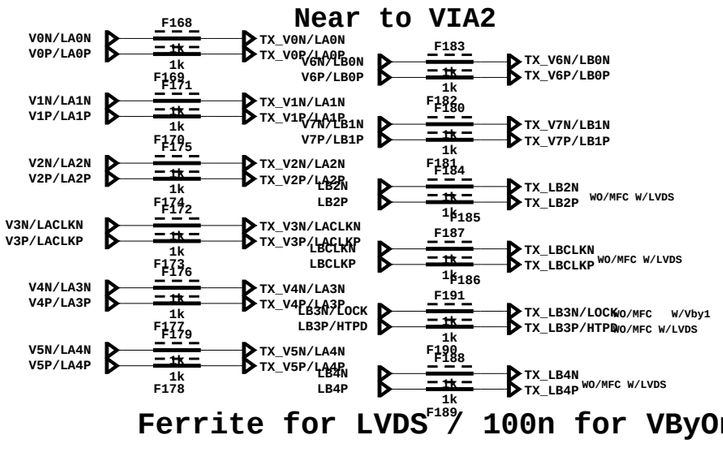

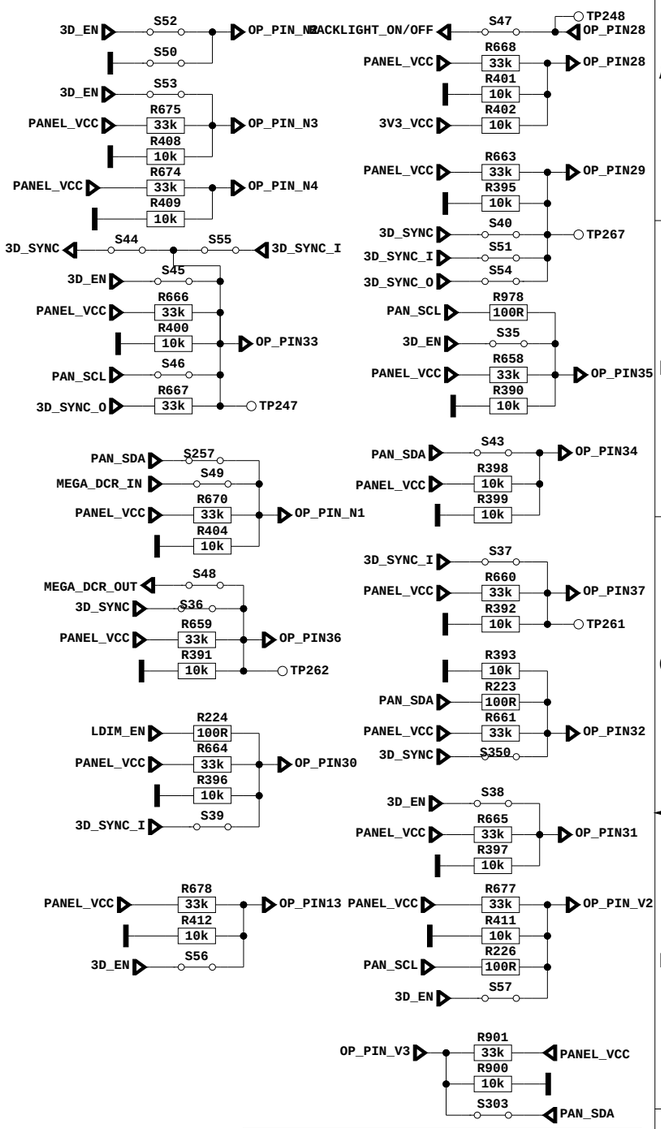

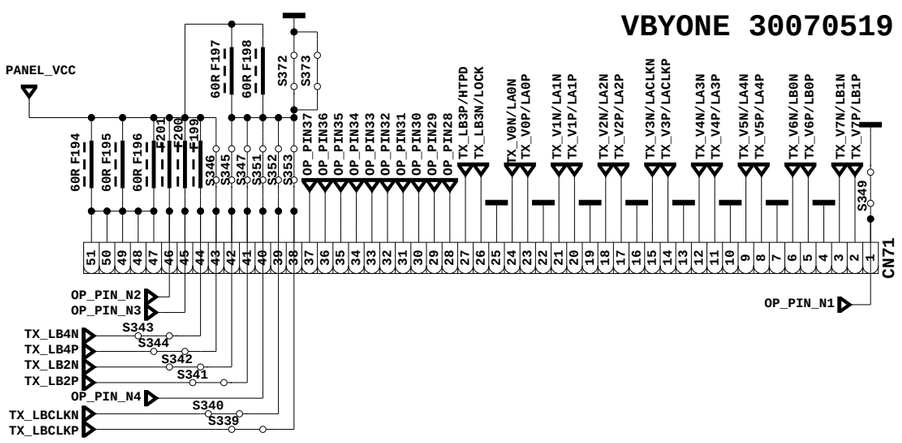

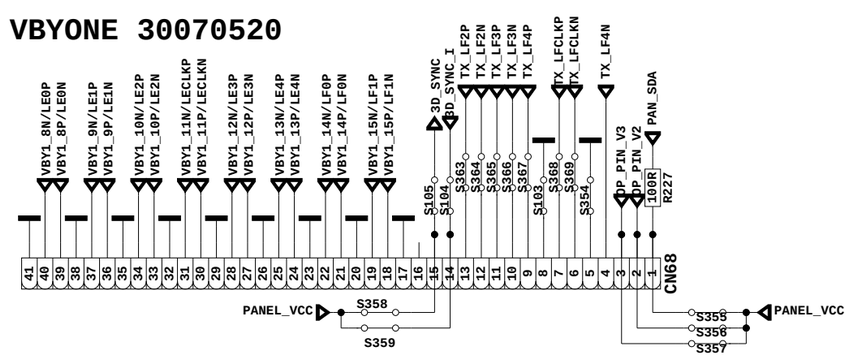

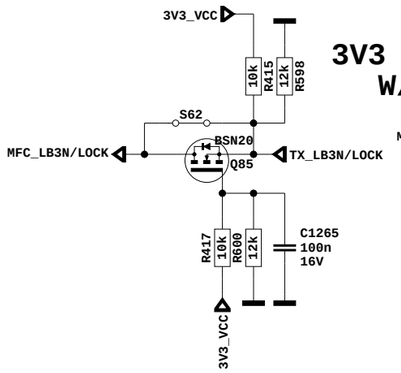

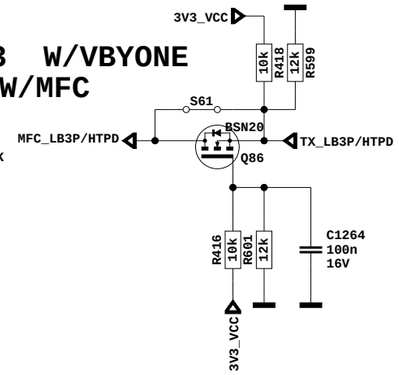

3V3 W/VBYONE W/MFC

OLD OPTIONS / NEW OPTIONS

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op_pin9 = op_pin36
op_pin10 = op_pin30
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op_pin27 = op_pin_29
op_pin42 = op_pin_n3
op_pin43 = op_pin_n4

op_pin46 = op_pin_35
op_pin48 = op_pin_32
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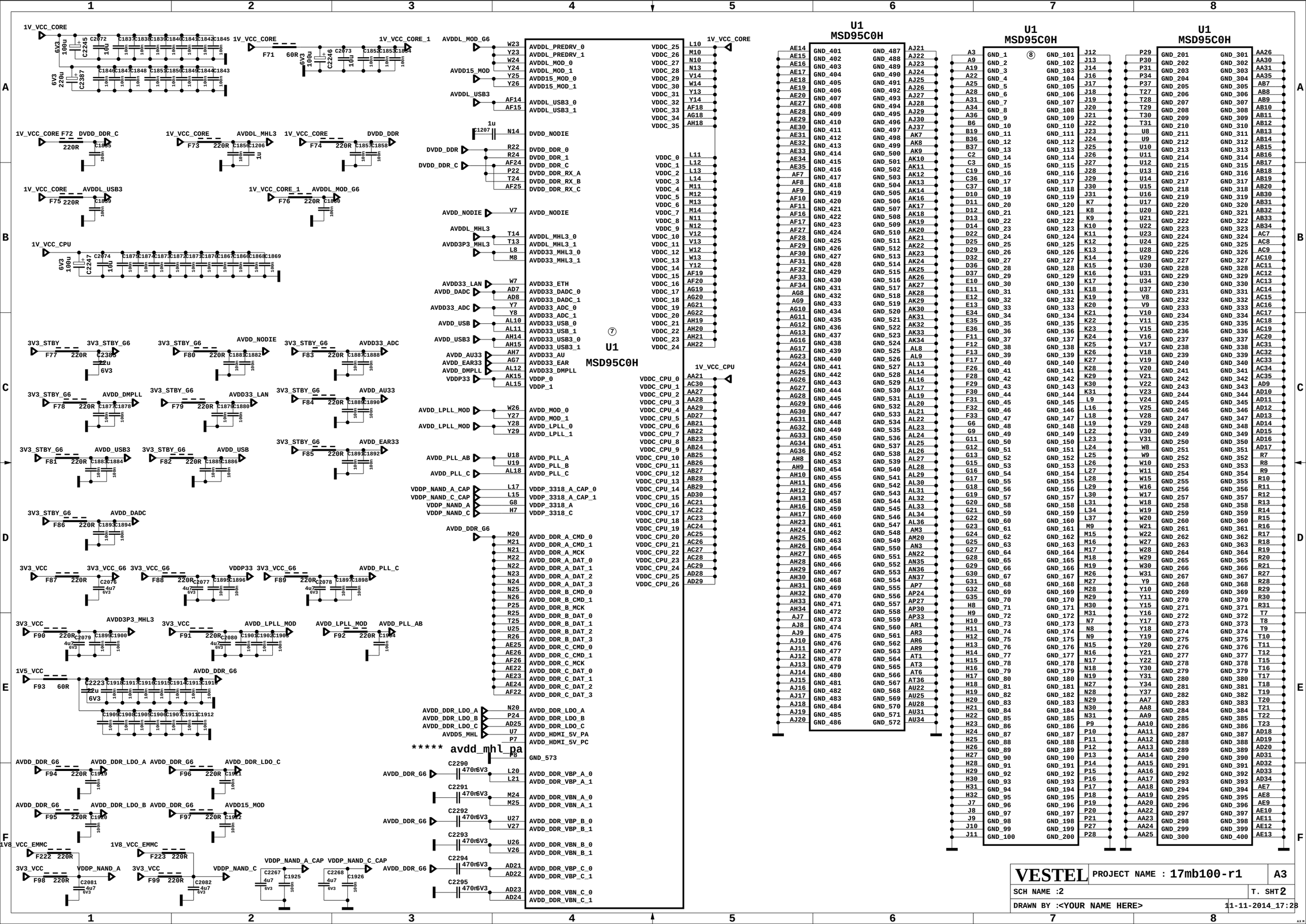
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C2072 10u
C1837 C1838 C1839 C1840 C1841 C1842 C1845 100n
6V3 220u C2387
C1846 C1847 C1848 C1851 C1850 C1849 C1844 C1843 100n
1V_VCC_CORE F71 60R 1V_VCC_CORE_1
6V3 100u C2246
C2073 10u
C1852 C1853 C1854 100n
1V_VCC_CORE F72 DVDD_DDR_C 220R C1855 100n
1V_VCC_CORE AVDDL_MHL3 F73 220R C1856 C1206 100n 1u
1V_VCC_CORE DVDD_DDR F74 220R C1857 C1858 100n
1V_VCC_CORE AVDDL_USB3 F75 220R C1859 100n
1V_VCC_CORE_1 AVDDL_MOD_G6 F76 220R C1860 100n
1V_VCC_CPU
6V3 100u C2247
C2074 10u
C1875 C1874 C1873 C1872 C1871 C1870 C1867 C1866 C1868 C1869 100n
3V3_STBY 3V3_STBY_G6 F77 220R C2305 22u 6V3
3V3_STBY_G6 AVDD_NODIE F80 220R C1881 C1882 100n
3V3_STBY_G6 AVDD33_ADC F83 220R C1887 C1888 100n
3V3_STBY_G6 AVDD_DMPLL F78 220R C1877 C1878 100n
3V3_STBY_G6 AVDD33_LAN F79 220R C1879 C1880 100n
3V3_STBY_G6 AVDD_AU33 F84 220R C1889 C1890 100n
3V3_STBY_G6 AVDD_USB3 F81 220R C1883 C1884 100n
3V3_STBY_G6 AVDD_USB F82 220R C1885 C1886 100n
3V3_STBY_G6 AVDD_EAR33 F85 220R C1891 C1892 100n
3V3_STBY_G6 AVDD_DADC F86 220R C1893 C1894 100n
3V3_VCC 3V3_VCC_G6 F87 220R C2076 4u7 6V3
3V3_VCC_G6 VDDP33 F88 220R C2077 C1895 C1896 4u7 6V3 100n
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3V3_VCC AVDD3P3_MHL3 F90 220R C2079 C1899 C1900 4u7 6V3 100n
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AVDD_LPLL_MOD AVDD_PLL_AB F92 220R C1904 100n
1V5_VCC AVDD_DDR_G6 F93 60R C2223 22u 6V3
C1918 C1917 C1916 C1915 C1914 C1913 C1910 C1909 C1908 C1905 C1906 C1907 C1911 C1912 100n
AVDD_DDR_G6 AVDD_DDR_LDO_A F94 220R C1908 100n
AVDD_DDR_G6 AVDD_DDR_LDO_C F96 220R C1911 100n
AVDD_DDR_G6 AVDD_DDR_LDO_B F95 220R C1909 100n
AVDD_DDR_G6 AVDD15_MOD F97 220R C1912 100n
1V8_VCC_EMMC F222 220R
1V8_VCC_EMMC F223 220R
3V3_VCC VDDP_NAND_A F98 220R C2081 4u7 6V3
3V3_VCC VDDP_NAND_C F99 220R C2082 4u7 6V3
VDDP_NAND_A_CAP C2267 4u7 6V3 C1925 100n
VDDP_NAND_C_CAP C2268 4u7 6V3 C1926 100n
AVDDL_MOD_G6 W23
AVDD15_MOD Y23
W24
Y24
Y25
Y26
AVDDL_USB3 AF14
AF15
1u C1207 N14
DVDD_DDR R22
R24
DVDD_DDR_C AF24
P22
T24
AF25
AVDD_NODIE V7
AVDDL_MHL3 T14
AVDD3P3_MHL3 T13
L8
M8
AVDD33_LAN W7
AVDD_DADC AD7
AD8
AVDD33_ADC Y7
Y8
AVDD_USB AL10
AL11
AVDD_USB3 AH14
AH15
AVDD_AU33 AH7
AVDD_EAR33 AG7
AVDD_DMPLL AL12
VDDP33 AK15
AL15
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Y27
AVDD_LPLL_MOD Y28
Y29
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AVDD_PLL_C AL18
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VDDP_NAND_C_CAP L15
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VDDP_NAND_C H7
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N21
M22
N22
N23
N24
N25
N26
P25
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R26
AE25
AE26
AF26
AE22
AE23
AE24
AF22
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AVDD_DDR_LDO_C AD25
AVDD5_MHL U7
P7
***** avdd_mhl_pa *****
P8
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L21
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M25
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V26
C2294 470r6V3 AD21
AD22
C2295 470r6V3 AD23
AD24
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V25 GND_246
V28 GND_247
V29 GND_248
V30 GND_249
V31 GND_250
W8 GND_251
W9 GND_252
W10 GND_253
W11 GND_254
W15 GND_255
W16 GND_256
W17 GND_257
W18 GND_258
W19 GND_259
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W22 GND_262
W27 GND_263
W28 GND_264
W29 GND_265
W30 GND_266
W31 GND_267
Y9 GND_268
Y10 GND_269
Y11 GND_270
Y15 GND_271
Y16 GND_272
Y17 GND_273
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Y19 GND_275
Y20 GND_276
Y21 GND_277
Y22 GND_278
Y30 GND_279
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AA11 GND_287
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GND_301 AA26
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GND_366 R21
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GND_368 R28
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GND_371 R31
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GND_376 T11
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GND_381 T18
GND_382 T19
GND_383 T20
GND_384 T21
GND_385 T22
GND_386 T23
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GND_388 AD19
GND_389 AD20
GND_390 AD31
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GND_393 AD34
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GND_395 AE8
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GND_398 AE11
GND_399 AE12
GND_400 AE13
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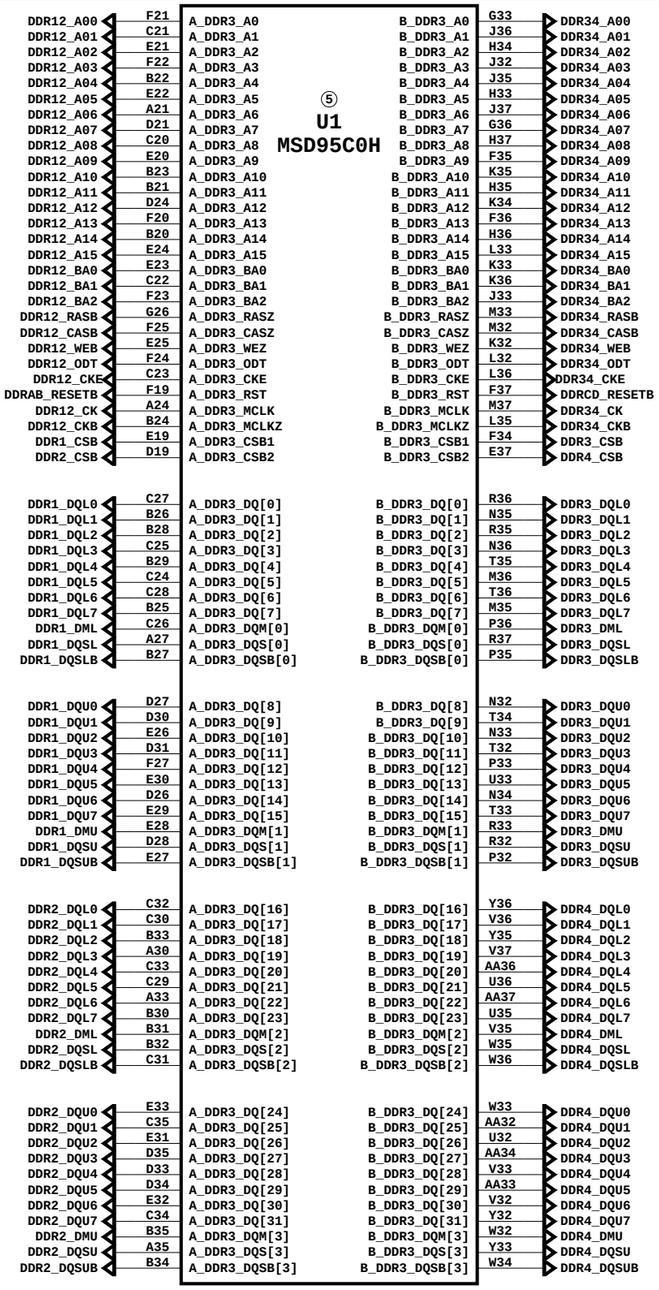
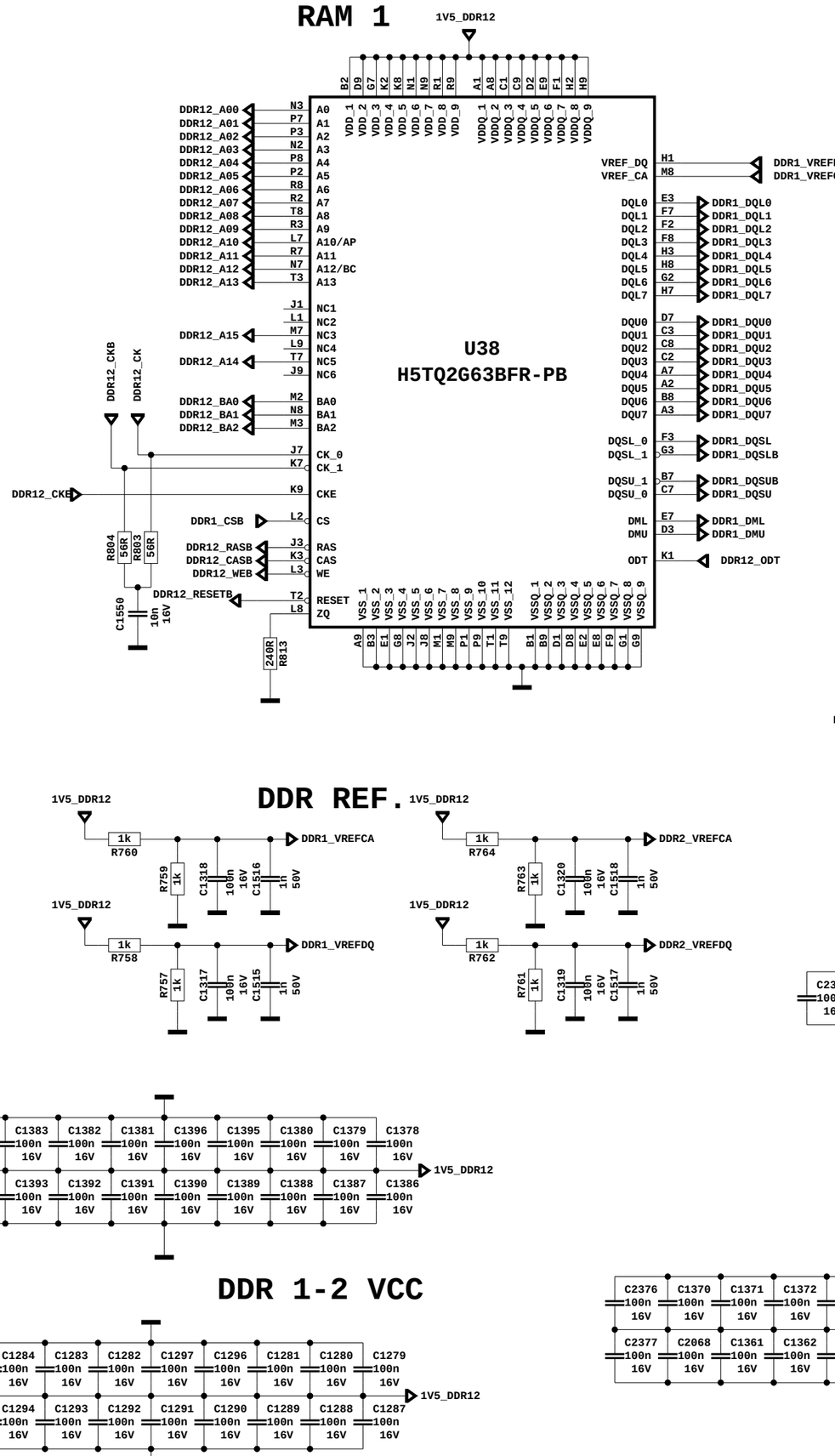
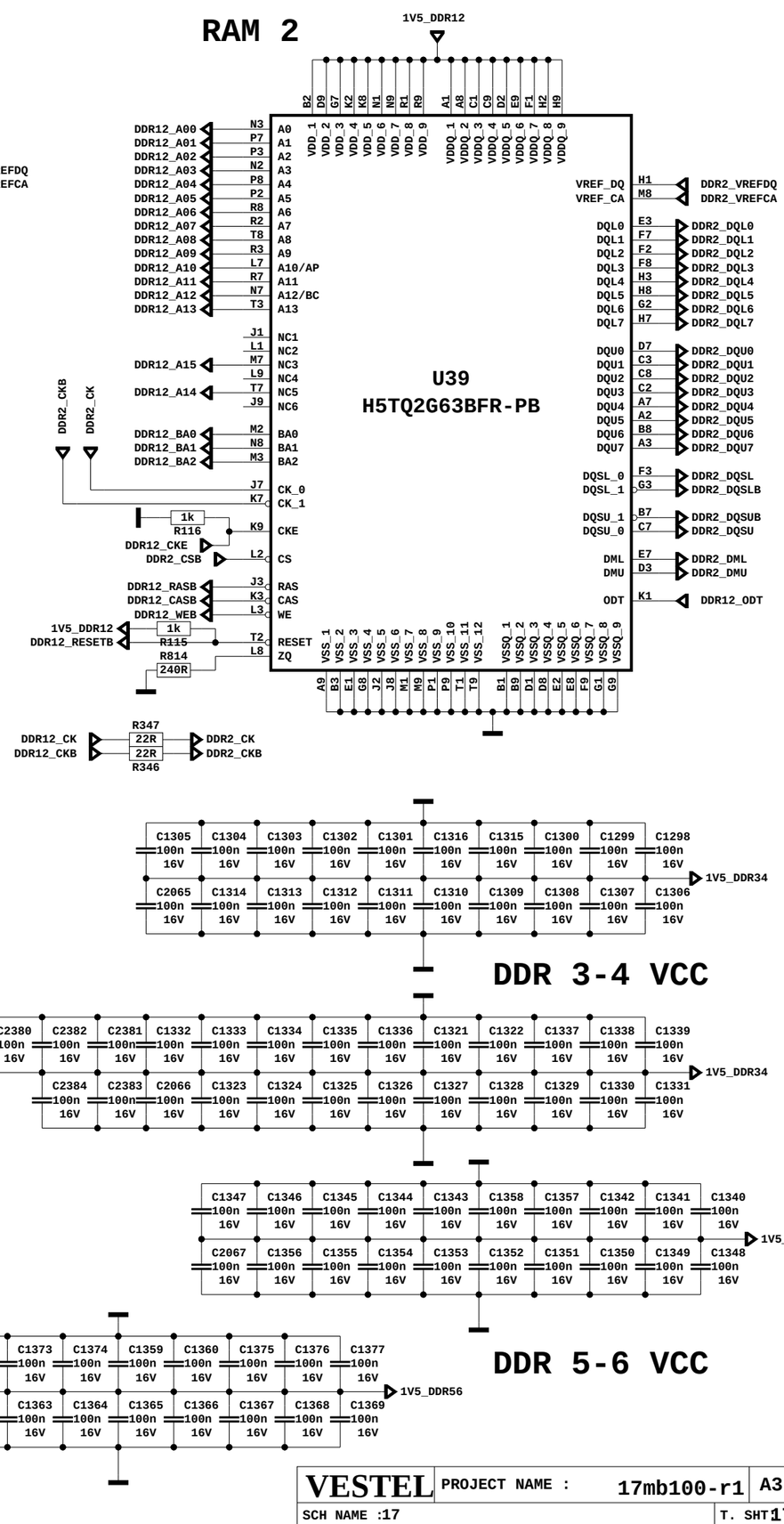
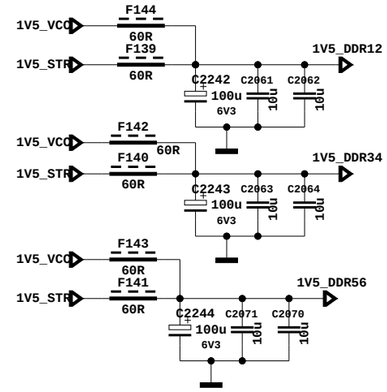
PROJECT NAME : 17mb100-r1
A3
SCH NAME :2
T. SHT 2
DRAWN BY :<YOUR NAME HERE>
11-11-2014_17:28









VESTEL	PROJECT NAME : 17mb100-r1	A3
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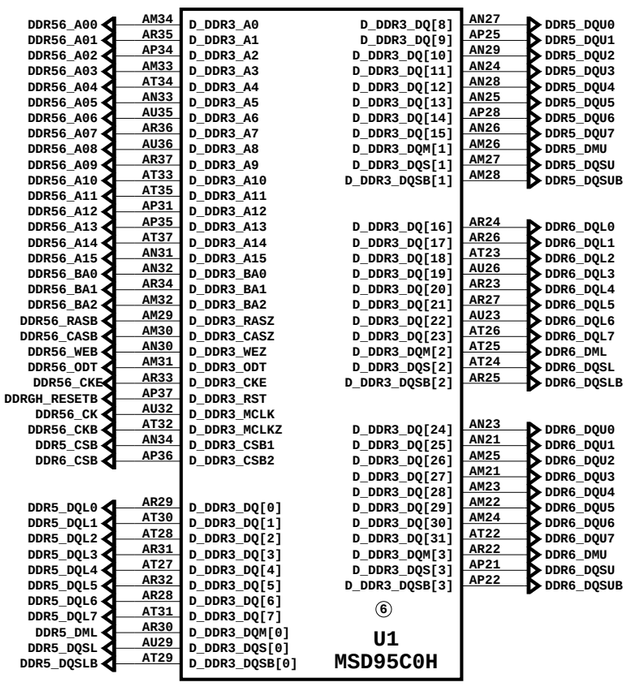

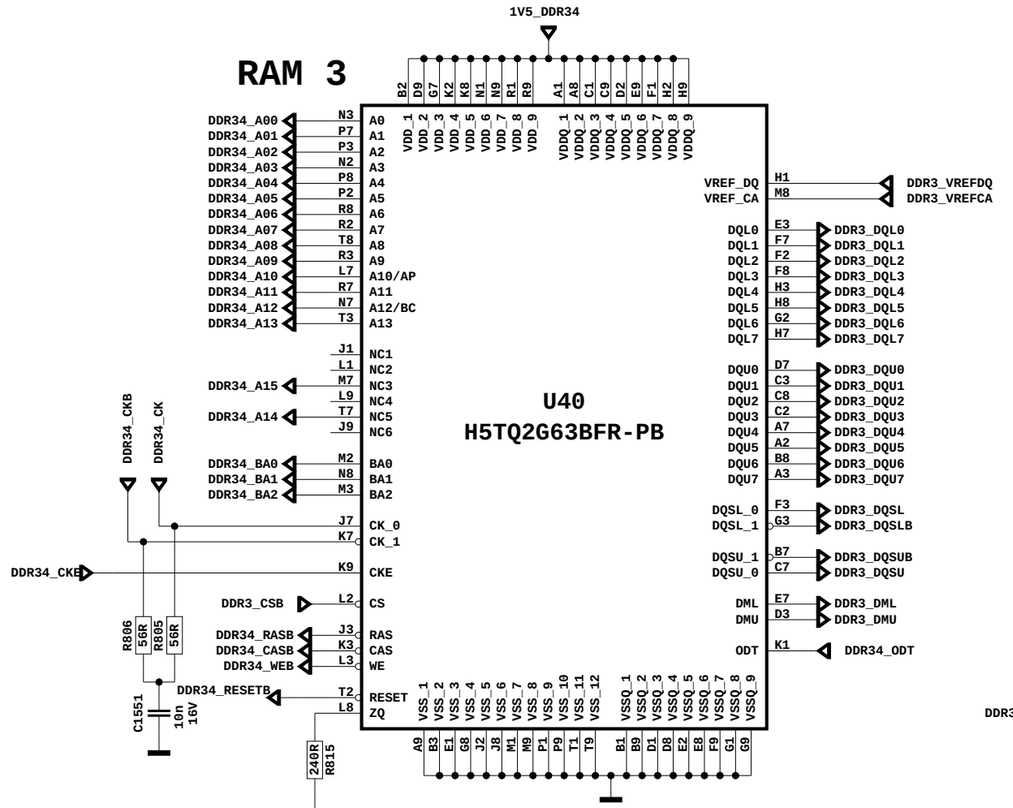

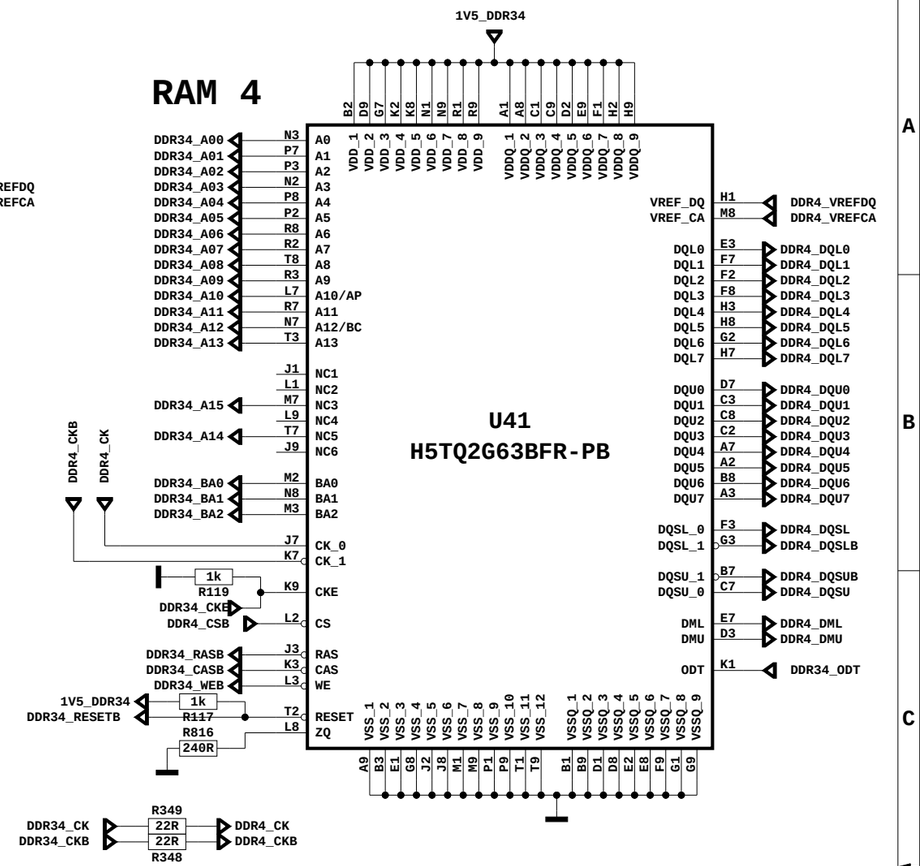

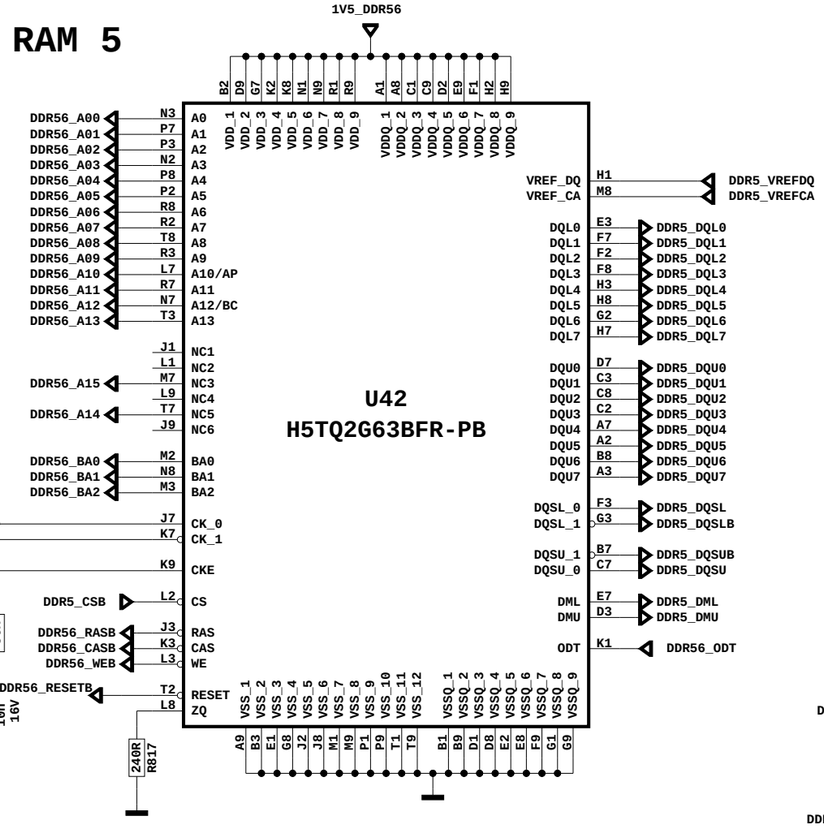

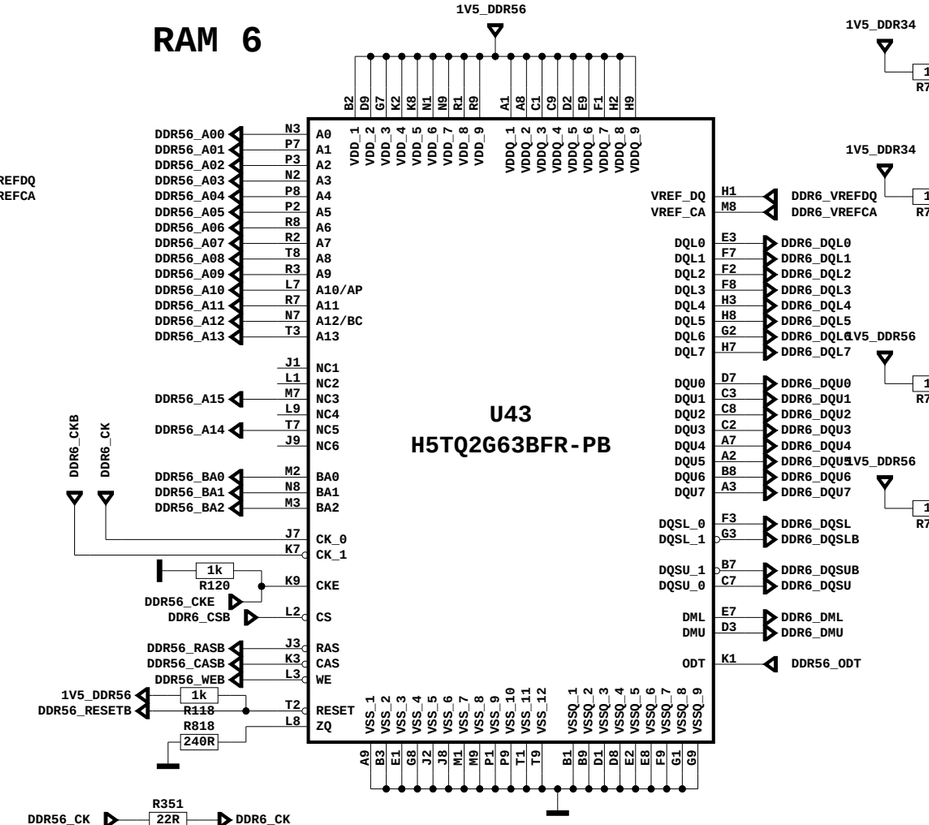

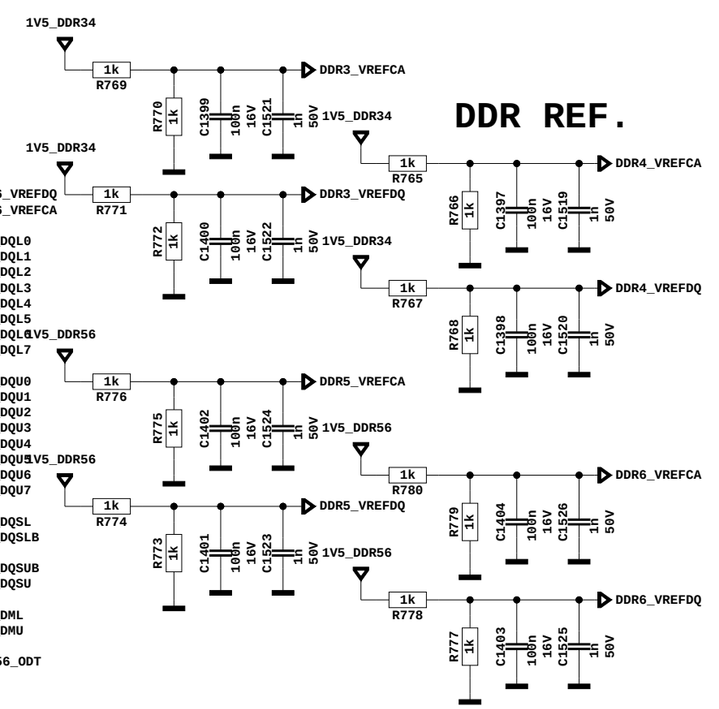

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SCH NAME :18		T. SHT 18
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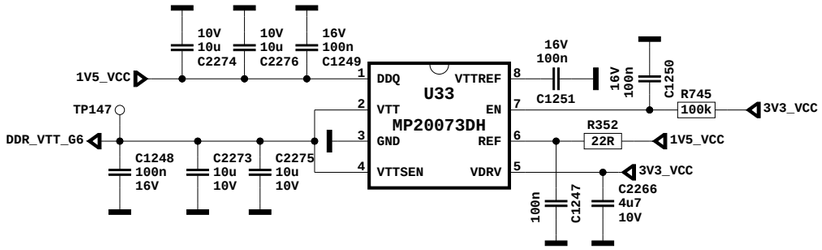
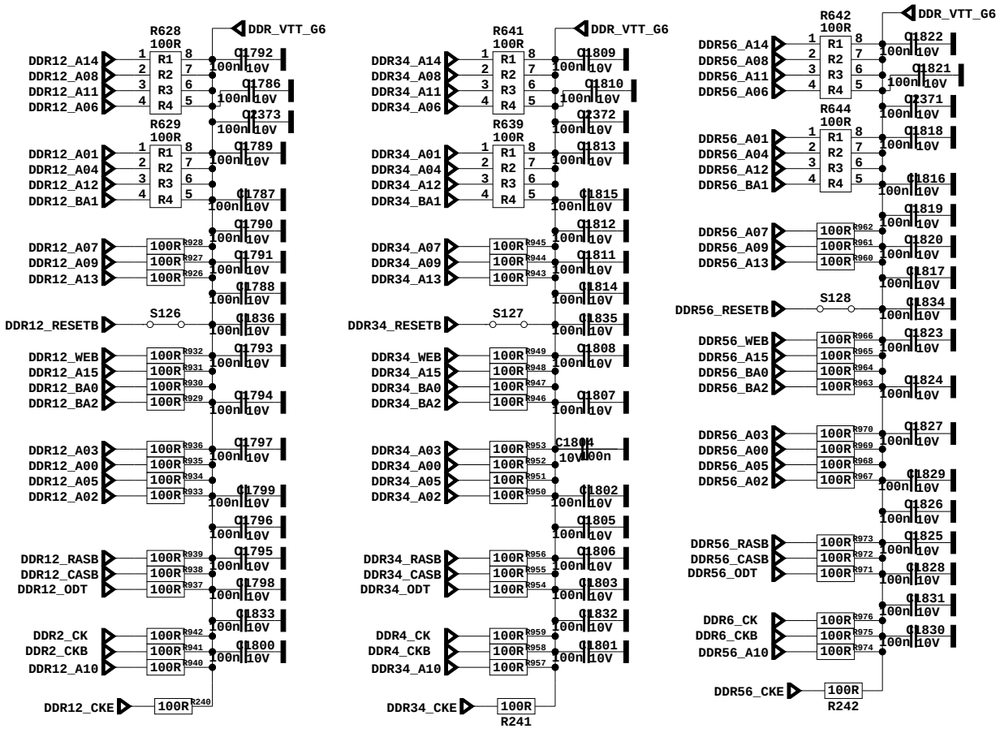
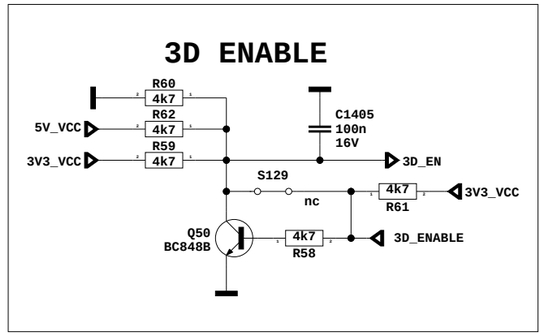
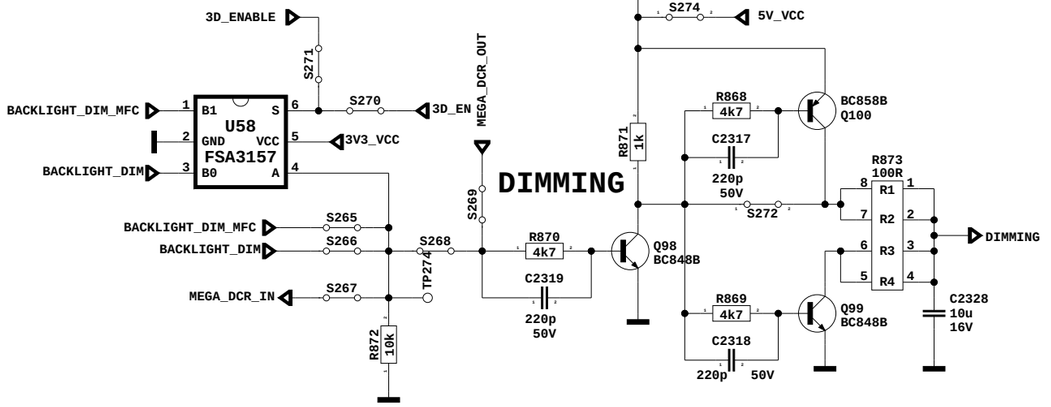
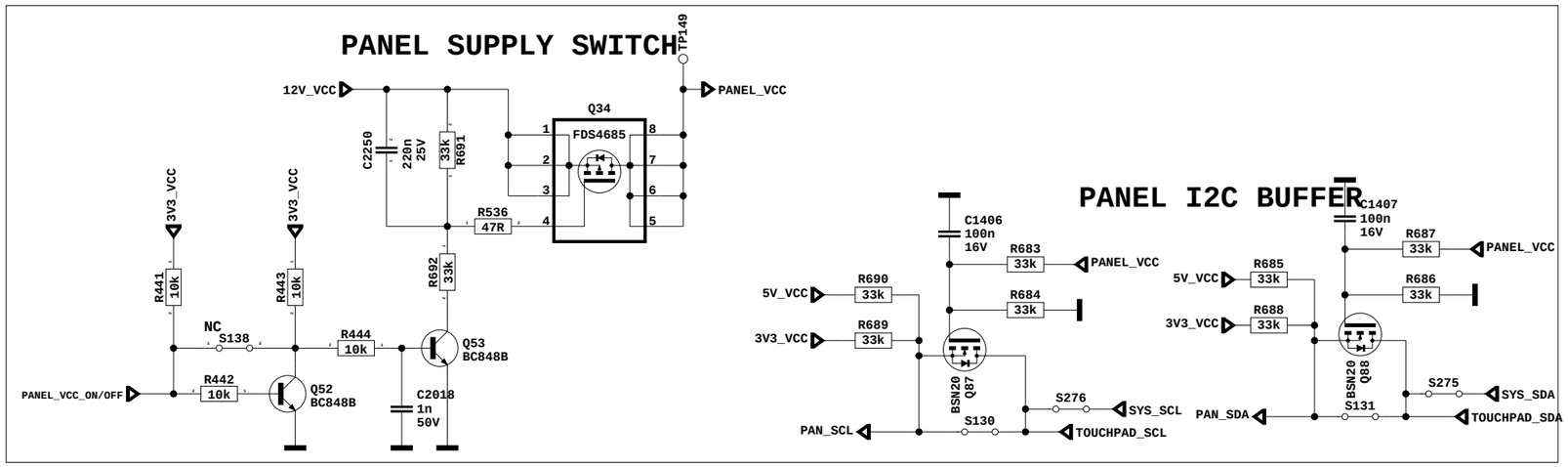


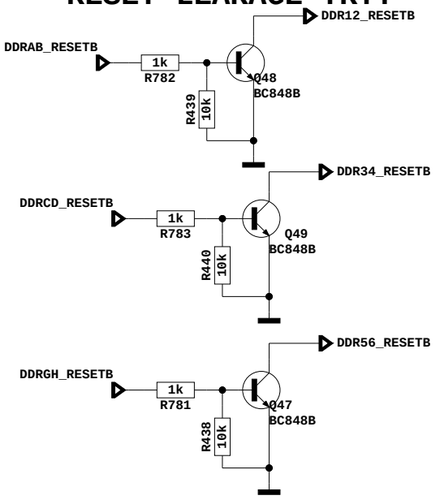
DDR TERMINATION VOLTAGE



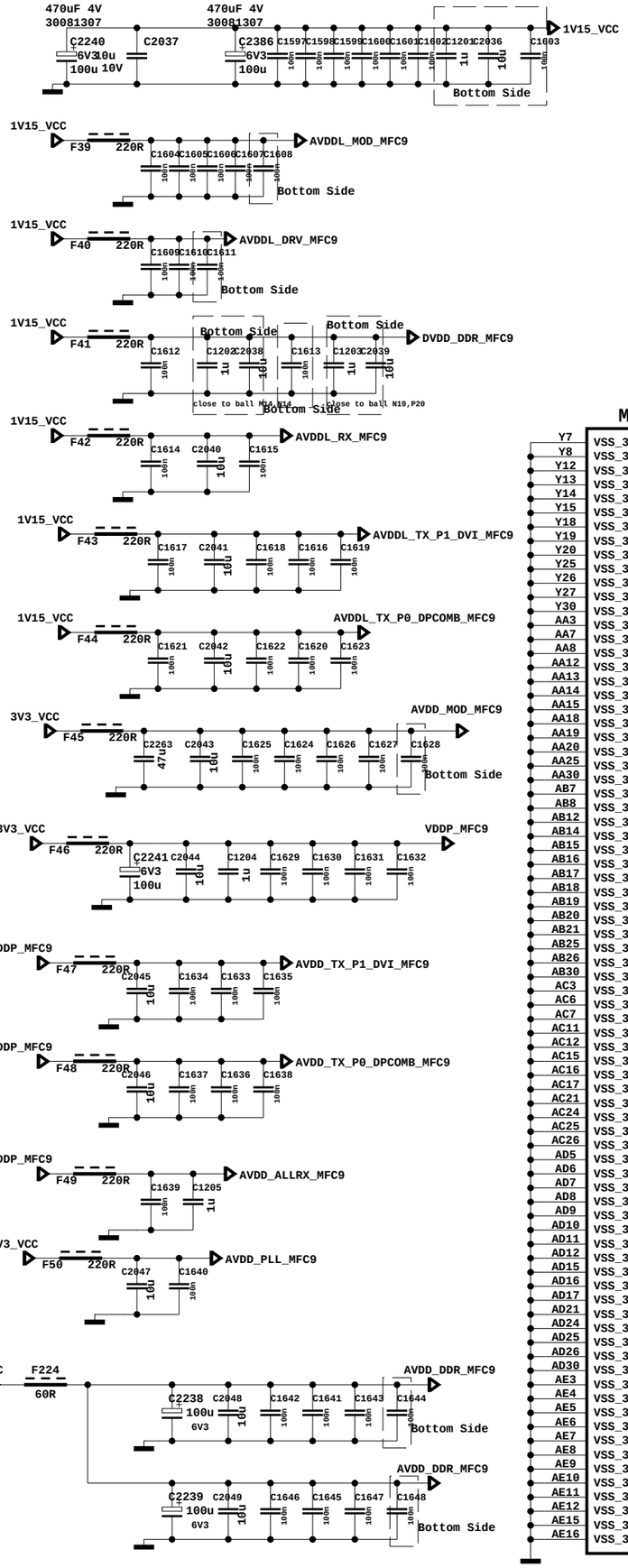


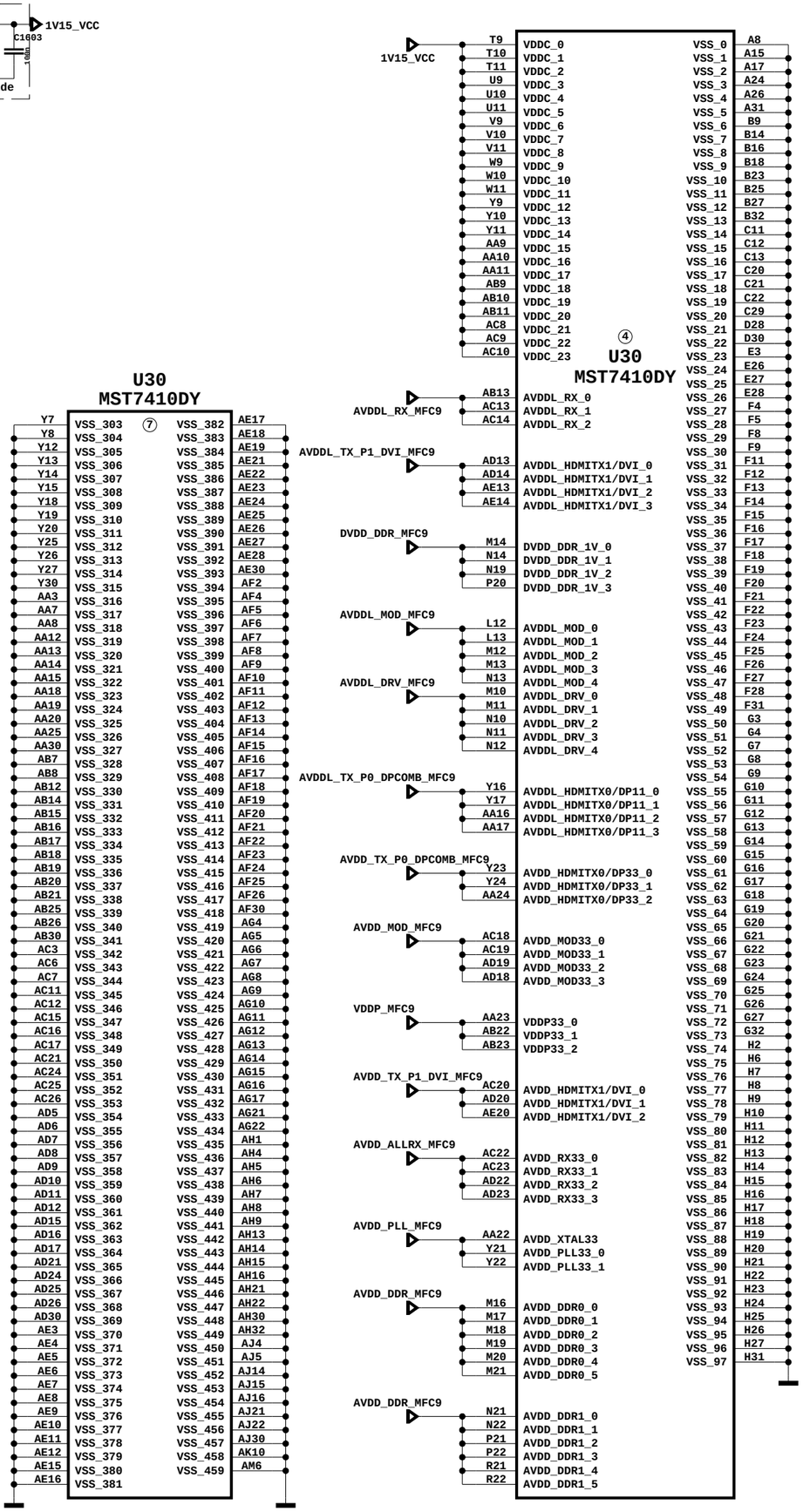






VESTEL	PROJECT NAME : 17mb100-r1	A3
SCH NAME :19		T. SHT 19
DRAWN BY :<YOUR NAME HERE>		25-10-2014_14:53





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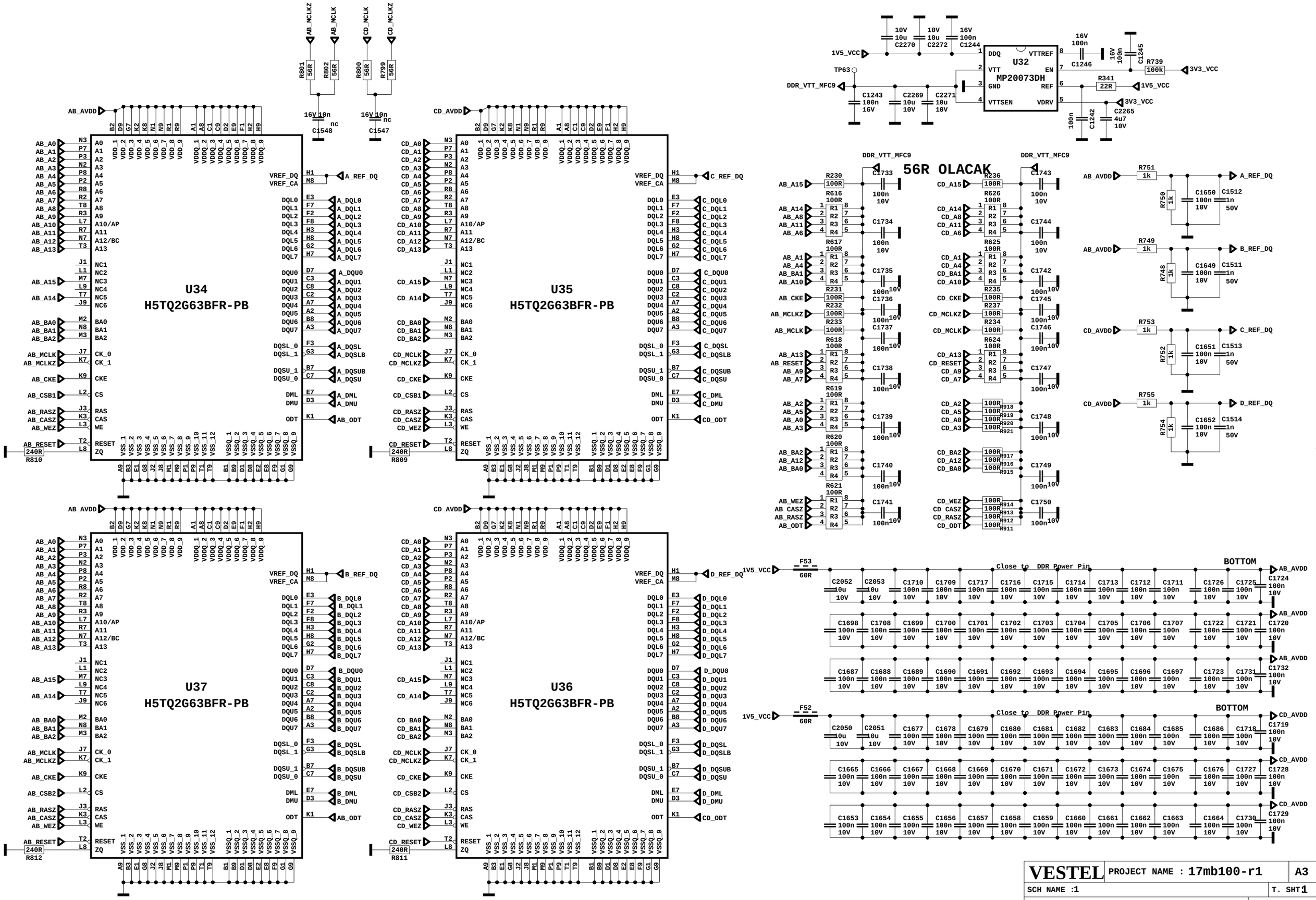
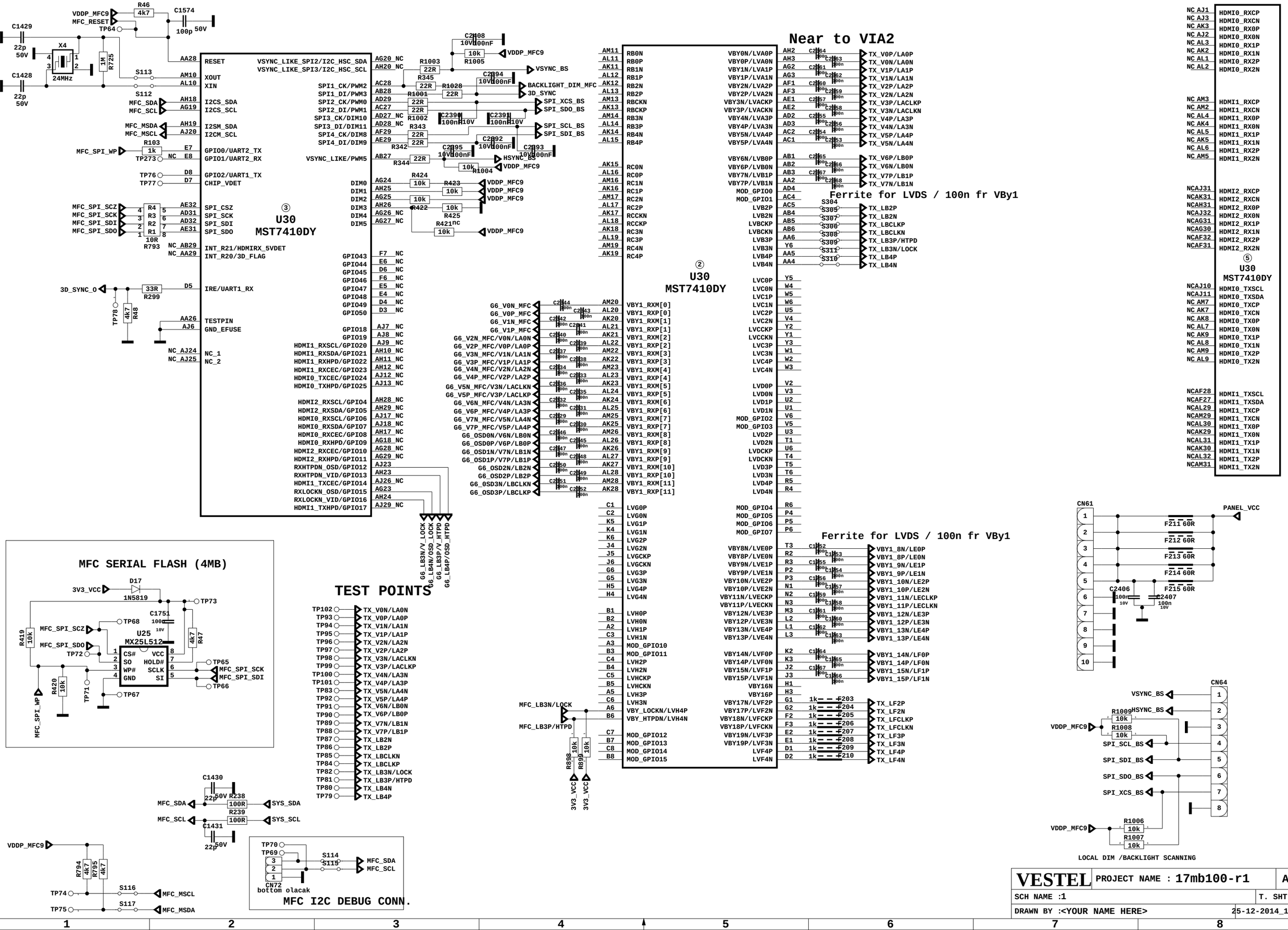
SCH NAME :	MFC_POWER_GND	T. SHT	1
DRAWN BY :	<YOUR NAME HERE>	18-12-2014_20:09	



VESTEL	PROJECT NAME : 17mb100-r1		A3
SCH NAME :1		T. SHT	1
DRAWN BY :<YOUR NAME HERE>		16-07-2014_16:14	


Near to VIA2
Ferrite for LVDS / 100n fr VBy1
Ferrite for LVDS / 100n fr VBy1
MFC SERIAL FLASH (4MB)
TEST POINTS
MFC I2C DEBUG CONN.
LOCAL DIM /BACKLIGHT SCANNING
U30
MST7410DY
U25
MX25L512
CN72
bottom olacak
CN61
CN64
PANEL_VCC
VESTEL
PROJECT NAME : 17mb100-r1
A3
SCH NAME :1
T. SHT 1
DRAWN BY :<YOUR NAME HERE>
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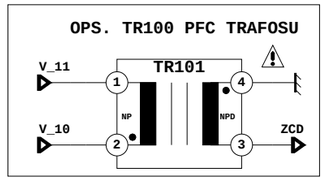
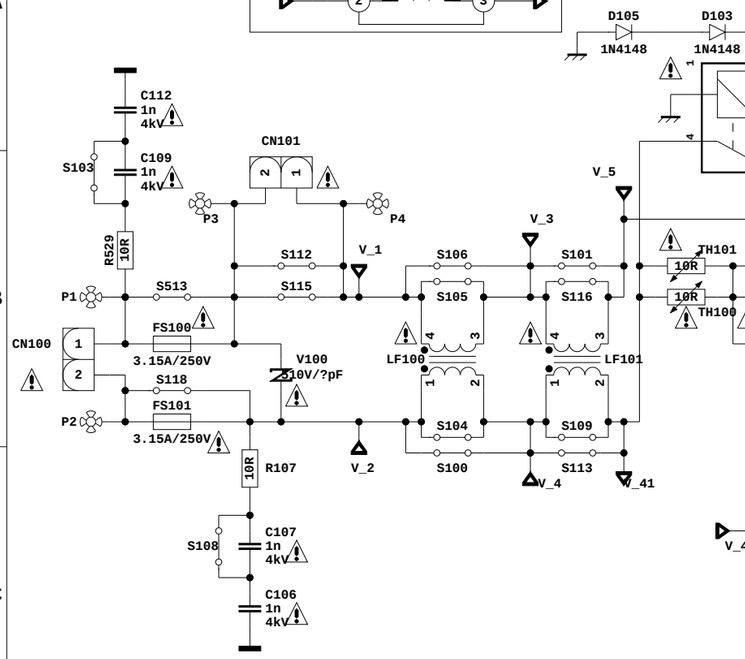
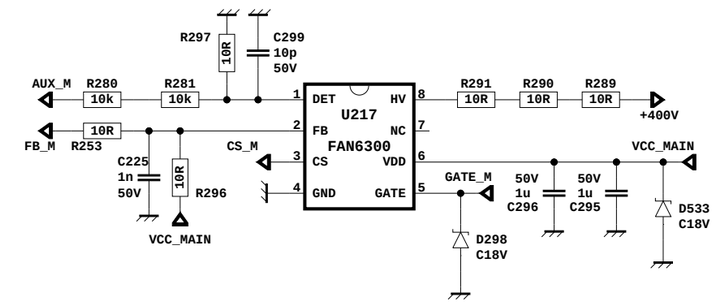
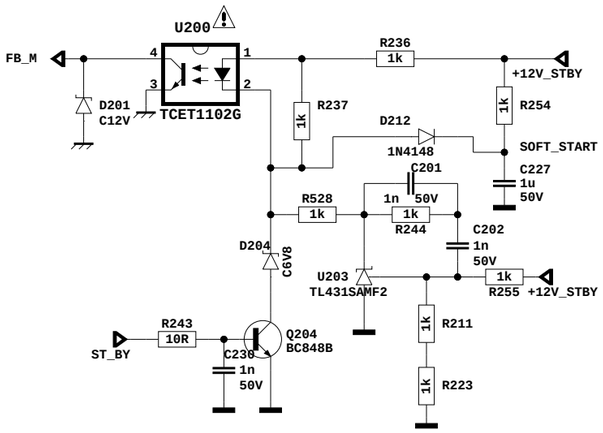
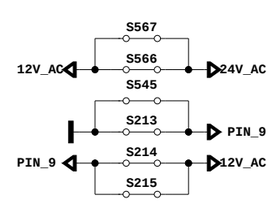
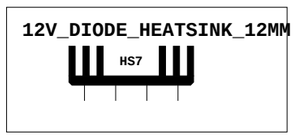


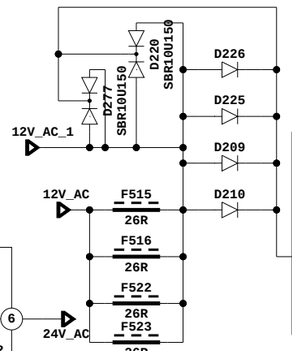


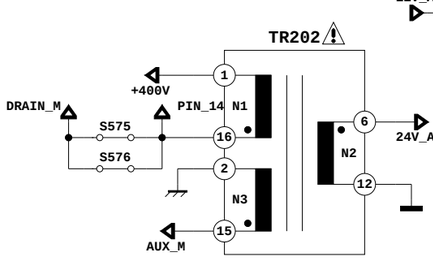


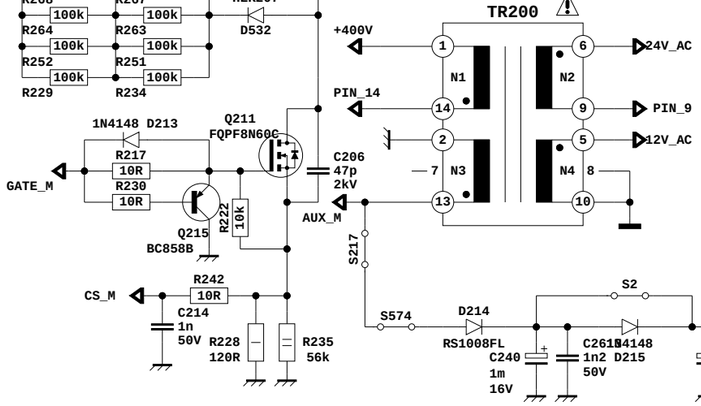


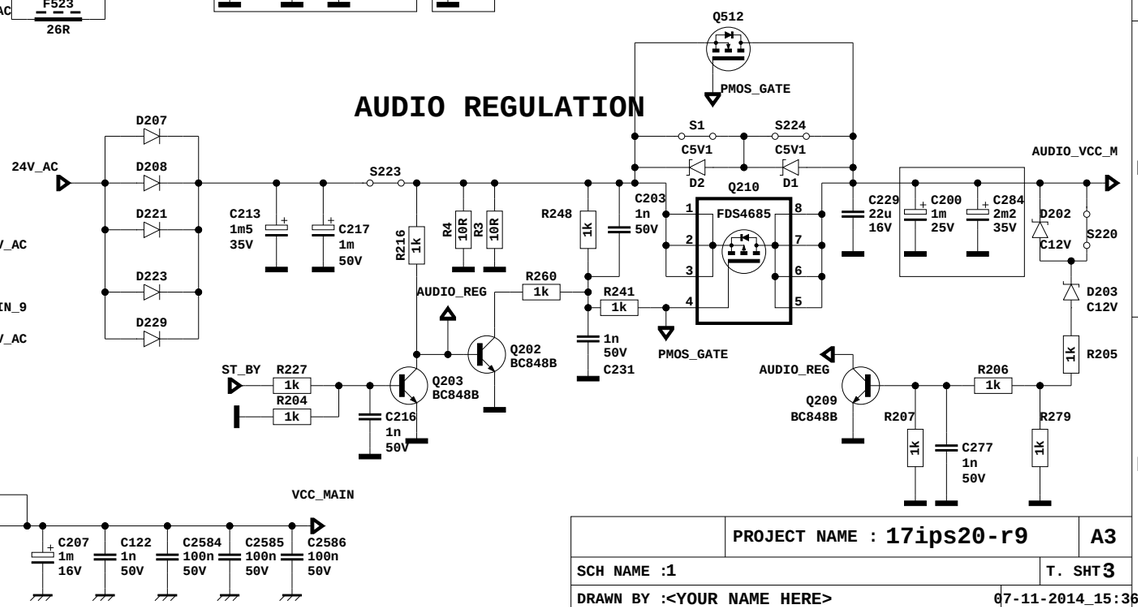




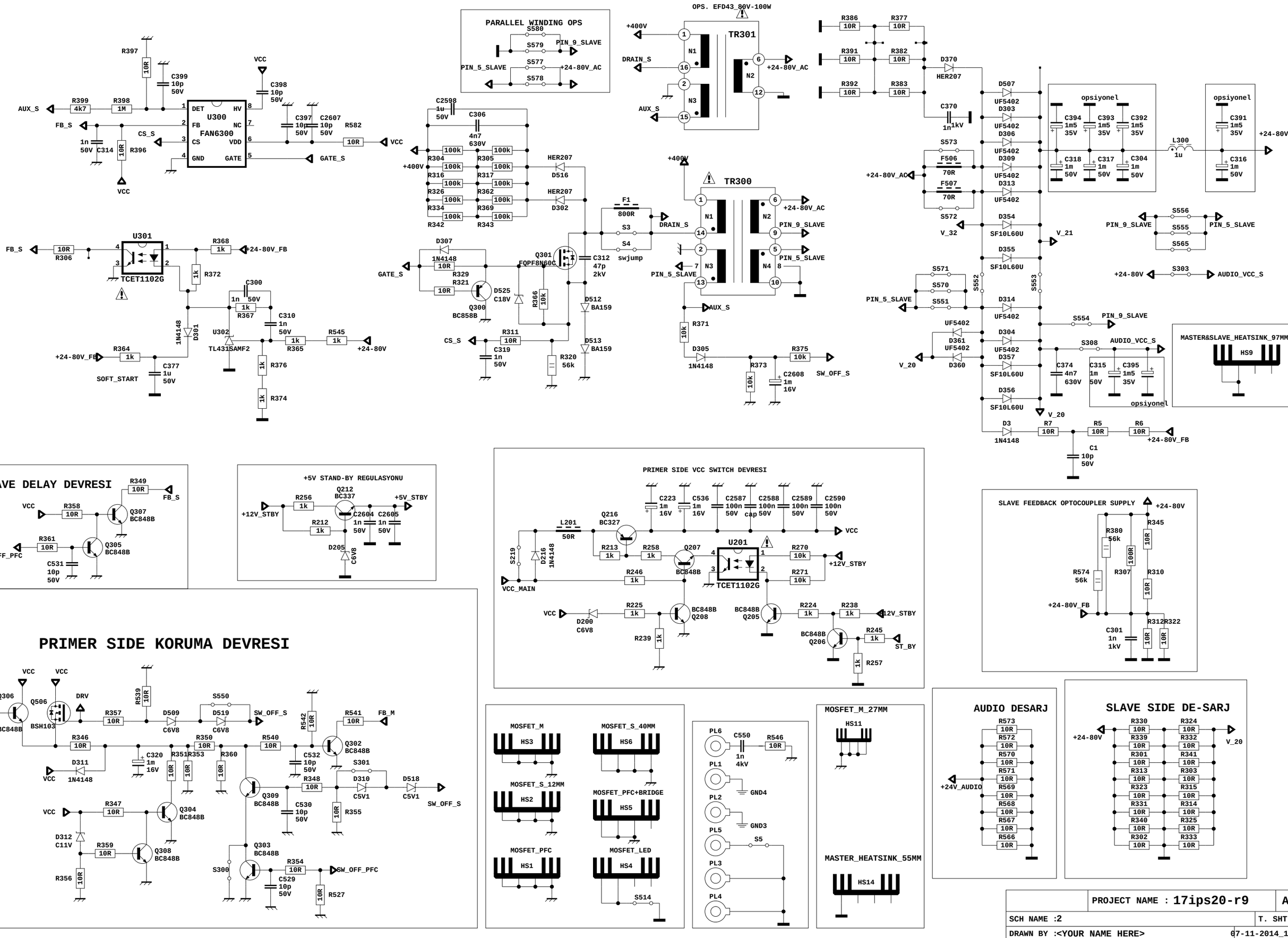






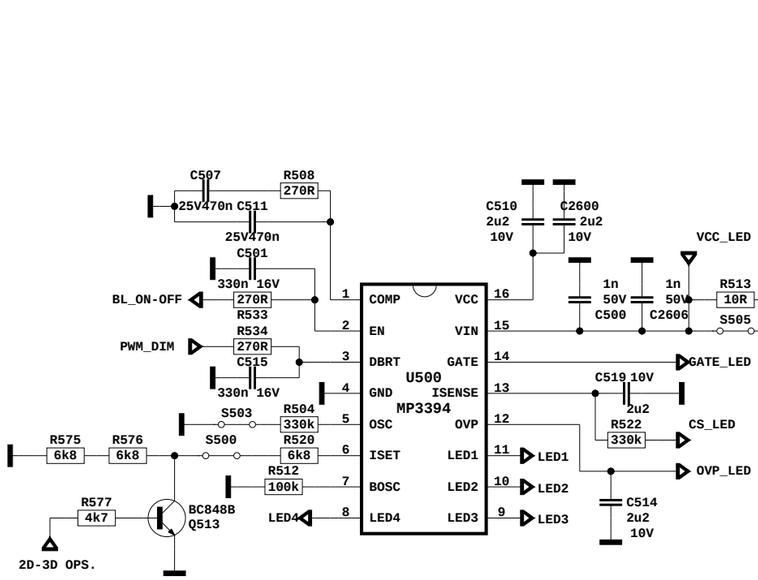


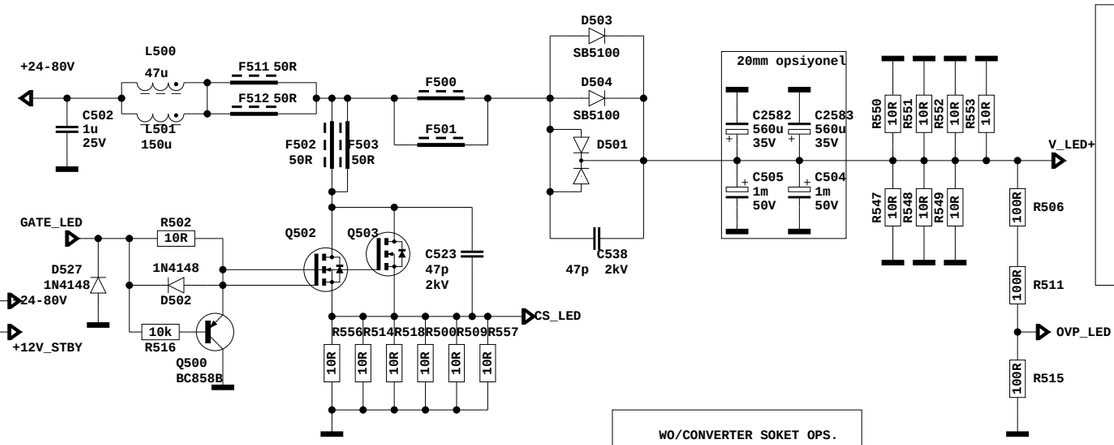
	PROJECT NAME : 17ips20-r9	A3
SCH NAME :1		T. SHT3
DRAWN BY :<YOUR NAME HERE>		07-11-2014_15:36

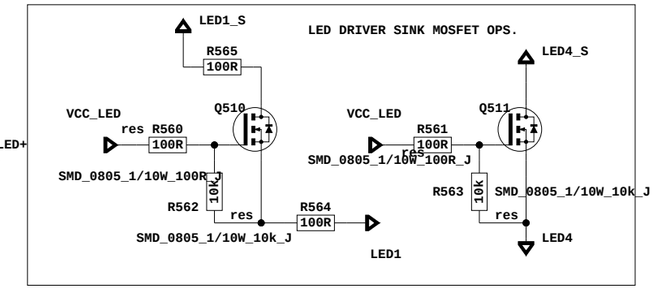


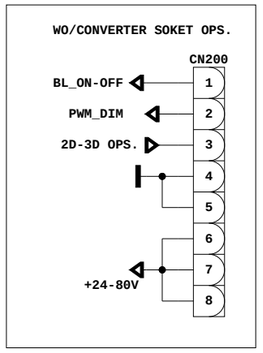
	PROJECT NAME : 17ips20-r9	A3
SCH NAME :2		T. SHT3
DRAWN BY :<YOUR NAME HERE>		07-11-2014_15:42

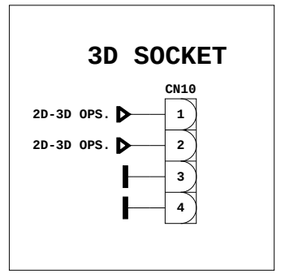
LED DRIVER CIRCUIT

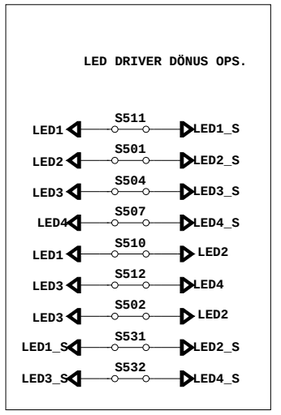


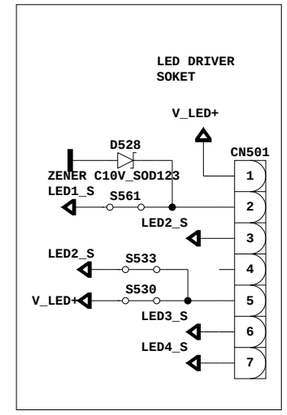


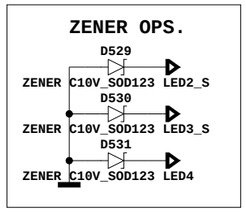




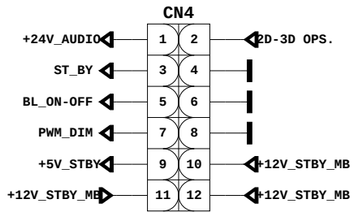


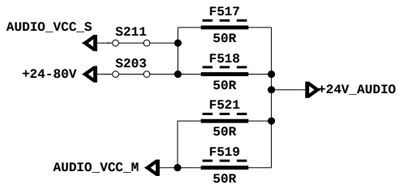


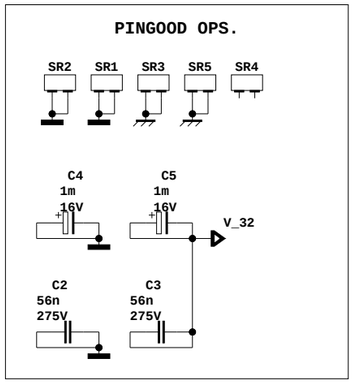


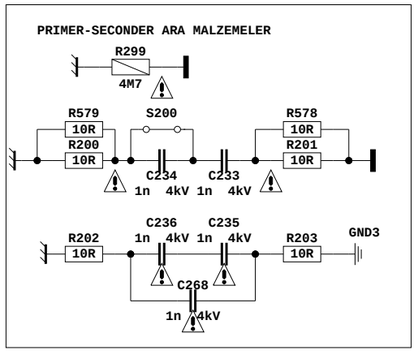


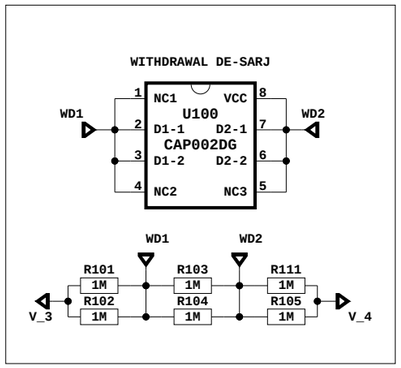
MAINBOARD SOCKET

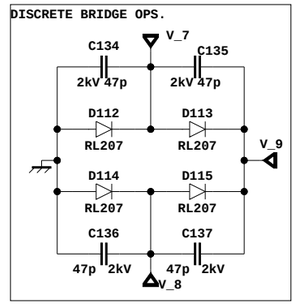


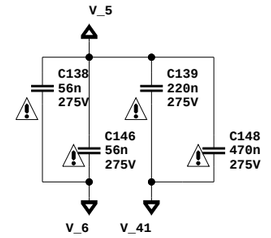


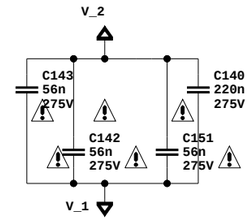


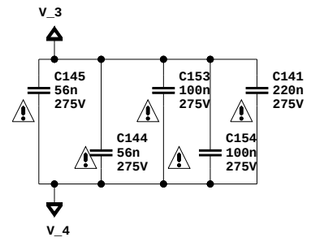












	PROJECT NAME : 17ips20-r9	A3
SCH NAME :3		T. SHT3
DRAWN BY :<YOUR NAME HERE>		07-11-2014_16:03