NVC-MDCS46 Datasheet

– Dual mode Bluetooth V5.0+ EDR Class1

Innovative Communication in Wireless World

Version – 1.4

Issue Date – Feb. 7, 2019

Description:

NVC-MDCS46 is a class 1 Bluetooth® 5.0 dual mode module. Its radio contains on board chip antenna and shielding case so as a modular approved design it can be easily integrated into customer's hardware. It has internal audio codec and amplifiers. The ACSII command interface on UART or USB interface can be used to control its Bluetooth functions on host from MCU to PC. All the Bluetooth profiles/stack run inside the module so the software on the host can be greatly simplified.

With NovaComm's iNova® Bluetooth stack firmware, designers can easily customize their applications to support different Bluetooth profiles, such as SPP, HID, HFP, A2DP and GATT based BLE profiles and etc.

Typical Bluetooth applications:

- Long distance cable replacement
- Bar code and RFID scanners, and USB HID dongle
- Long distance audio transmission
- Industrial sensors and controls
- Medical devices
- Industrial PCs and laptops

Features:

- Dual mode Bluetooth V5.0+EDR class1
- TX power +17dbm, -90dBm RX sensitivity, onboard chip antenna supports maximum 1000 meters working range
- Supports BLE master and slave
- Supports Bluetooth SPP, HID, HFP, A2DP and BLE GATT profiles.
- UART and USB control and data interfaces
- 4 digital IOs (multiplex with UART) and 1 analog IOs, 3 open-drain LED driver
- 30.78 x 14.00 x 2.20mm
- Weight :1.7g
- FCC ID: OC3BM1846
- CE NB1313
- RoHS compliant

Table 1 Ordering Information

Ordering Number	Package	Items in One Package	Comments
NVC-MDCS46	Plastic tray	60PCS	

Please also supply the customer firmware code issued by NovaComm Technologies in the order.

Release Record

Version	Release Date	Comments
0.9	May 11, 2018	Draft release for engineering samples.
1.0	July 6, 2018	Update the I2C and UART RTS and CTS information.
1.1	Sept. 18, 2018	Update the power consumption, IO characteristics. Add description of I2S interface.
1.2	Oct. 10, 2018	Update the sensitivity and work range.
1.3	Nov. 13, 2018	Add detailed electrical characteristic of RESET pin and pulse width required for reset. Also add Bluetooth QDID information
1.4	Feb. 7, 2019	Fix a typing error of FCCID.

Table of Contents

List of Tables

List of Figures

1. Pinout and Description

1.1. Pin Configuration

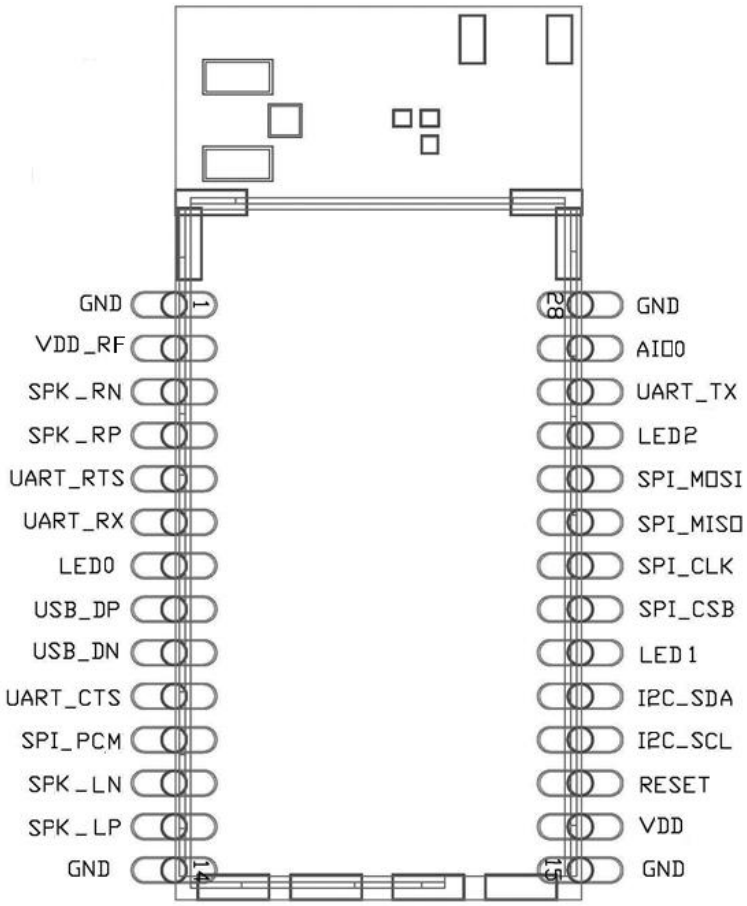

Figure 1: Pinout of NVC-MDCS46

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	VDD_RF	Power supply	3V3 power input of the RF power amplifier.
3	SPK_RN	Analog out	Speaker output negative, right
4	SPK_RP	Analog out	Speaker output positive, right
5	UART_RTS	Bidirectional	UART request to send active low
6	UART_RX	Bidirectional	UART data input
7	LED0	Open drain	LED driver
8	USB_DP	Bi-directional	USB data plus with selectable internal 1.5K pull-up resistor

9	USB_DN	Bi-directional	USB data minus
10	UART_CTS	Bidirectional	UART clear to send active low
11	SPI_PCM	Input	Set high to select SPI. When it is low the four SPI terminals acts as PCM/I2S port or general PIOs depending on firmware
12	SPK_LN	Analog out	Speaker output negative, left
13	SPK_LP	Analog out	Speaker output positive, left
14	GND	Ground	Ground
15	GND	Ground	Ground
16	VDD	Power input	3.3V power input
17	RESET	Input	Reset the device when pull high
18	I2C_SCL	Output	I2C clock
19	I2C_SDA	Bidirectional	I2C data
20	LED1	Open drain	LED driver
21	SPI_CSB	Input	SPI chip select, I2S word select or PIO4
22	SPI_CLK	Input	SPI clock, I2S serial clock or PIO5
23	SPI_MISO	Output	SPI data output, I2S data output or PIO3
24	SPI_MOSI	Input	SPI data input, I2S data input or PIO2
25	LED2	Open drain	LED driver
26	UART_TX	Bidirectional	UART data output
27	AIO0	Bidirectional	Analog programmable input line 0
28	GND	Ground	Ground

Table 2 : Pin Definition

2. Electrical Characteristic

2.1. Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+85	°C
UART_RX, UART_TX	-0.4	+3.6	V
I2C_SCL, I2C_SDA, UART_RTS, UART_CTS, RESET	-0.4	+5.5	V
Other PIOs Voltage	-0.4	+1.95	V
AIO Voltage	-0.4	+1.75	V
VDD Voltage	-0.4	+3.6	V
LED	-0.4	4.40	V

Table 3: Absolute Maximum Rating Recommended Operating Conditions

2.2. Recommend operation conditions

Operating Condition	Min	Typical	Max	Unit
Operating Temperature Range	-40	--	+85	°C
VDD Voltage	+3.3	+3.3	+3.6	V
UART_RX, UART_TX	+1.8	+3.3	+3.6	V
I2C_SCL, I2C_SDA, UART_RTS, UART_CTS, RESET	-0.4	+3.3	+5.0	V
Other PIOs Voltage	+1.7	+1.8	+1.95	V
AIO Voltage	--	--	+1.35	V
VDD Voltage	+3.1	+3.3	+3.6	V
LED	+1.1	+3.3	+4.3	V

Table 4: Recommended Operating Conditions

2.3. Power consumptions

Operating Condition	Discoverable	Connectable	Min	Typical	Max	Unit
Not connected	Yes	-	-	3.6	-	mA
Not connected	-	Yes	-	3.6	-	mA
Not connected	-	-	-	3.6	-	mA
Not connected(deep sleep on)	Yes	-	-	1.2	-	mA
Not connected(deep sleep on)	-	Yes	-	1.2	-	mA
Not connected(deep sleep on)	-	-	-	1.2	-	mA
Inquiry	-	-	-	38	-	mA
Connected (Deep sleep disable, sniff[(a)] enable)	-	-	-	3.6	-	mA
Connected (Deep sleep on, sniff[(a)] enable)	-	-	-	1.2	-	mA
Connected with data transfer (100bytes/s)	-	-	-	10	-	mA

Table 5: Power consumptions

Note:

2.4. Input/output Terminal Characteristics

2.4.1. SPI and SPI_PCM

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low	-0.4	-	+0.4	V
V_{IH} input logic level high	+1.26	-	+2.2	V
T_r/T_f	-	-	25	ns
Output Voltage Levels				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	+1.35	-	-	V
T_r/T_f	-	-	5	ns
Input and Tri-state Current				
Strong pull-up	-150	-40	-10	µA
Strong pull-down	10	40	150	µA
Weak pull-up	-5	-1.0	-0.33	µA
Weak pull-down	0.33	+1.0	5.0	µA
C_I Input Capacitance	1.0	-	5.0	pF

Table 6: Digital Terminal

2.4.2. UART_TX and UART_RX

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low	-0.4	-	+0.4	V
V_{IH} input logic level high	1.26	-	VDD+0.4	V
V_{OL} output logic level low	0.0	-	+0.1	V
V_{OH} output logic level high	VDD-0.2	-	VDD	V

Table 7: UART

Note:

The UART_TX and RX lines have internal 10k pull ups.

2.4.3. I2C_SCL, I2C_SDA

Supply Voltage Levels	Min	Typical	Max	Unit
Current when high impedance state	-	-	5	μA
Current sink state	-	-	4	mA
Voltage in sink state (4mA)	-	-	0.4	V
V_{OL} output logic level low (open drain)	-	0.0	-	V
V_{OH} output logic level high (open drain)	-	1.8	-	V
V_{IL} input logic level low	-0.4	-	+0.4	V
V_{IH} input logic level high	1.26	-	+6.5	V

Table 8: I2C

Note:

The I2C_SCL and SDA lines need external pull ups.

2.4.4. Internal CODEC - Digital to Analogue Converter

Parameter	Conditions		Min	Typ	Max	Unit
Resolution			-	-	16	Bits
Output sample rate, F_{sample}			8	-	48	kHz
Maximum ADC input signal amplitude 0dB=1600 mV_{pk-pk}			13	-	2260	mV_{pk-pk}
Signal to Noise Ratio, SNR	f_{in}=1kHz B/W=20Hz->20kHz A-Weighted THD+N<0.1% 0 dBFS input	F_{sample}/Load				
		48kHz/100 kΩ	-	96.4	-	dB
		48kHz/32 Ω	-	96.3	-	
		48kHz/16 Ω	-	96.2	-	

THD+N	f_{in}=1kHz B/W=20Hz->20kHz 0 dBFS input	F_{sample}/Load				
		8kHz/100 kΩ	-	0.0022	-	%
		8kHz/32 Ω	-	0.0022	-	%
		8kHz/16 Ω	-	0.0023	-	%
		48kHz/100 kΩ	-	0.0030	-	%
		48kHz/32 Ω	-	0.0031	-	%
		48kHz/16 Ω	-	0.0033	-	%
Digital gain	Digital Gain Resolution = 1/32 dB		-24	-	21.5	dB
Analog gain	Analog gain resolution = 3 dB		-21	-	0	dB
Output voltage	Full-scale swing (differential)		-	-	778	mV_{rms}
Stereo separation (crosstalk)			-	-90	-	dB

Table 9: Digital to Analogue Converter

2.4.5. LED Pads

USB Terminals	Min	Typical	Max	Unit
Current when high impedance state	-	-	5	μA
Current sink state	-	-	10	mA
Voltage in sink state (10mA)	-	-	0.55	V
V_{OL} output logic level low (open drain)	-	0.0	-	V
V_{OH} output logic level high (open drain)	-	0.8	-	V
V_{IL} input logic level low	-	0.0	-	V
V_{IH} input logic level high	-	0.8	-	V

Table 10: LED Terminal

2.4.6. USB

USB Terminals	Min	Typical	Max	Unit
Input Threshold				
V_{IL} input logic level low	-	-	0.99	V
V_{IH} input logic level high	2.31	-	-	V
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	3.3	V

Table 11: USB Terminal

2.4.7. AIO and Auxiliary ADC

12-bit ADC	Min	Typical	Max	Unit
Resolution	-	-	10	Bits
Input voltage range	0	-	1.35	V
Accuracy	-	-	±1.0	LSB

Input bandwidth	-	100	-	kHz
Conversion time	1.38	1.69	2.75	μS

Table 12: AIO

2.5. ESD Protection

Condition	Class	Max rating
Human Body Model Contact Discharge per ANSI/ ESDA/JEDEC JS-001	2	2 kV (all pins)
Charged Device Model Contact Discharge per JEDEC/EIA JESD22‐C101	III	500 V (all pins)

Table 13: ESD handling ratings

3. Physical Interfaces

3.1. Power Supply

NVC-MDCS46 accept 3.3V DC power input at both VDD and VDD_RF pins. The peak current at VDD is 30mA. For VDD_RF the peak when internal RF PA works at its maximum output could reach 200mA.

3.2. Reset

NVC-MDCS46 resets when the RESET pin is higher than VDD-0.5V, the pulse width shall be more than 1ms.

Pin Name / Group	Pin Status on Reset
UART_TX/RX	Strong pull up
UART_RTS/CTS/I2C_SCL/I2C_SDA	Open Drain
AIOs	Hi-Z
SPI_CSB	Weak pull down
SPI_CLK	Weak pull down
SPI_MOSI	Weak pull down
SPI_MISO	Weak pull down
SPI_PCM	Strong pull down
USB_DP/DN	Weak pull down

Table 14: Pin Status on Reset

3.3. Internal Antenna

The module integrates a chip antenna so there's no need to use antenna on customer's PCB. Simply pay attention to leave enough clearance for the antenna as shown in Figure 9.

3.4. PIO

NVC-MDCS46 has a total of 8 digital programmable I/O terminals. 4 IOs are multiplexed with UART and the other 4 are multiplexed with the debug SPI interface (the SPI is enabled when SPI_PCM is high, when it is low, the four terminals can be PCM interface or general PIO depending on firmware configuration). Inside the module all 8 IOs are powered from internal 1.8V voltage. The module has built-in level shifter for UART_TX/RX so these two pins can connect directly to 3.3V UART host interface. For other PIOs external level shifter might be needed to connect with no-1.8V interfaces. PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs.

3.5. LED Drivers

NVC-MDCS46 has 3 pulse width modulation LED driver for driving red green blue LEDS for producing a wide range of colors. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pads in series with a current-limiting resistor.

3.6. AIO

NVC-MDCS46 has an analogue I/O terminal. Its functions depend on software. Typically ADC function can be configured to make voltage measurement.

3.7. UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

The UART CTS and RTS signals can be used to implement RS232 hardware flow control where both are active low indicators.

Please note that UART_TX/RX pins have internal level shifter to connect with 3.3V host directly, while UART_RTS/CTS requires external level shifter if they are used.

If CTS and RTS are not required for hardware flow control, they are reconfigurable as PIO.

UART configuration parameters, such as baud rate and packet format, are set using firmware.

Table 15: Possible UART Settings

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

3.8. I2C

The module has an I2C mater interface. The SCL and SDA lines are multiplexed with UART_RTS and CTS, both lines needs external pull ups.

3.9. SPI interface

The synchronous serial port interface (SPI) is used for flash/debug the module only. It can not be used for any user functionality. Please always leave test points for this interface with SPI_PCM terminal on the PCB for the purpose of EMC testing/debugging.

3.10. USB

This is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller, such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v5.0+EDR or alternatively can appear as a set of endpoints appropriate to USB HID devices such as keybard.

The module has an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device.

3.11. Analog Output

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The output stage circuit is comprised a DAC with gain setting and class AB amplifier. The output is available as a differential signal between SPK_RN and SPK_RP for the

right channel, as **Figure 2** shows, and between SPK_LN and SPK_LP for the left channel.

Figure 2: Speaker output

3.12. Microphone input

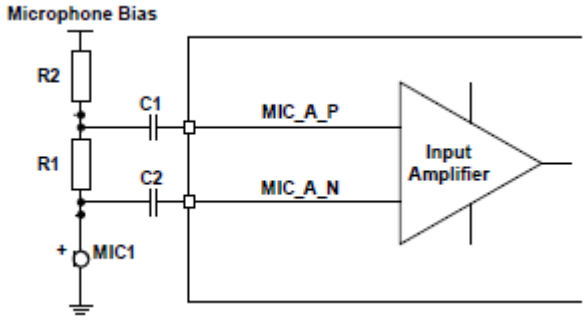

Figure 3: Microphone Biasing

NVC-MDCS46 has internal low-noise microphone bias generator. Figure 3 shows a typical biasing circuit for electret condenser microphones.

The bias resistor R1 should match the microphone load impedance, and typically is 2.2 kΩ. C1 and C2 are typically 100/150 nF to give a bass roll-off to limit wind noise on the microphone.

3.13. I2S

NVC-MDCS46 also supports I2S input and output digital audio interface, left-justified or right-justified.

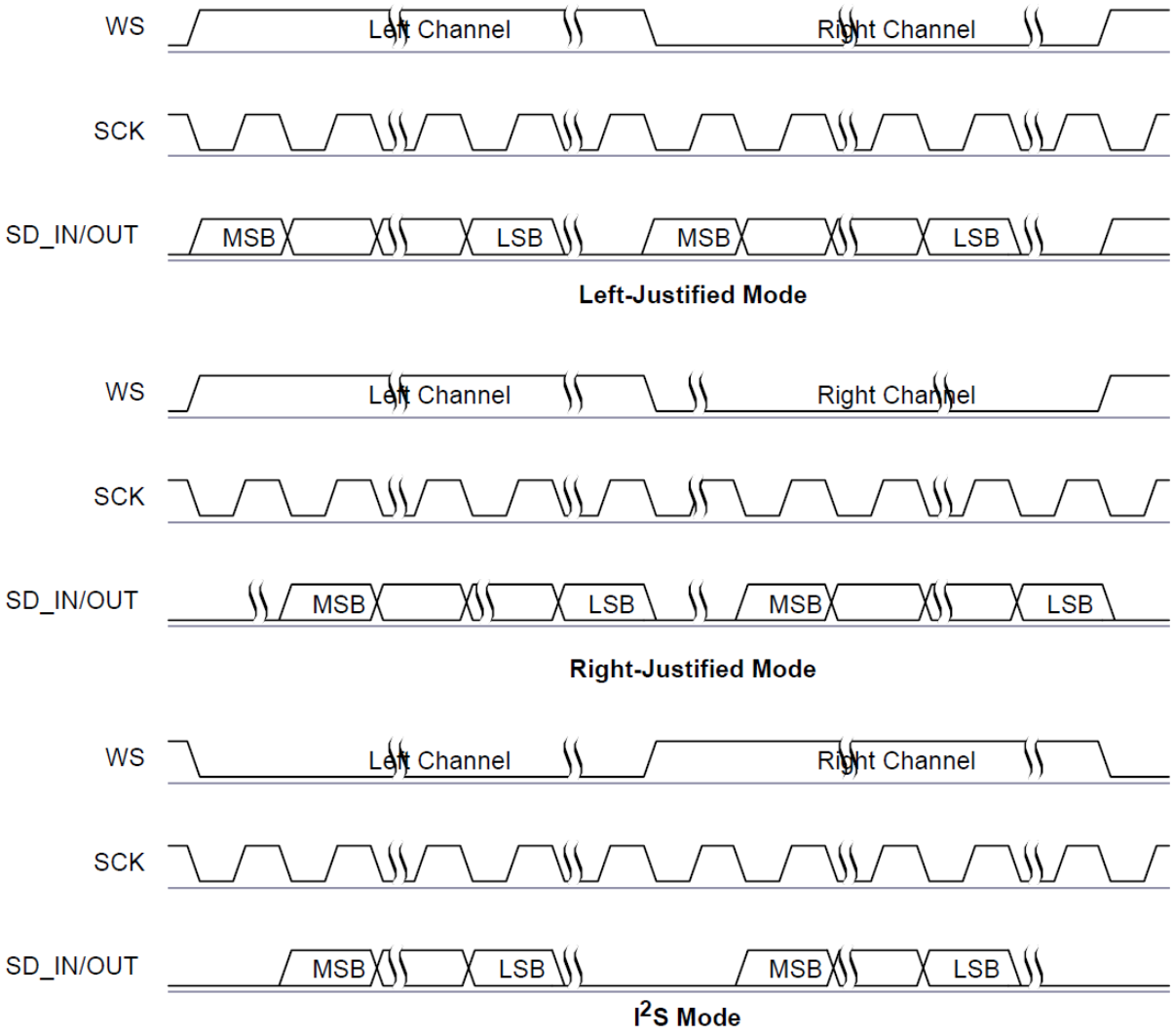

Figure 4 : Digital Audio Interface Modes

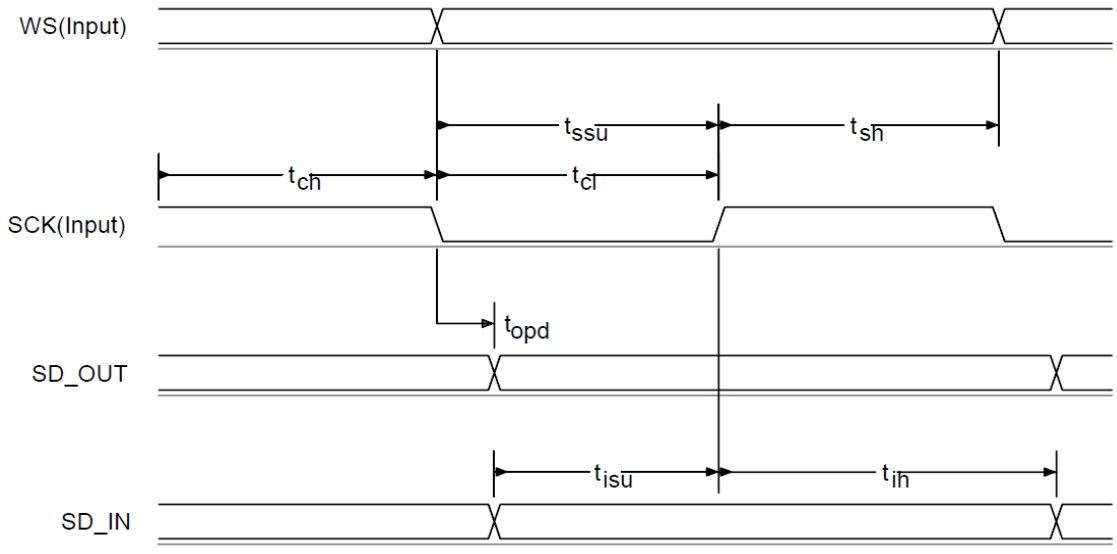

Figure 5 : Digital Audio Interface Slave Timing

Table 16 : Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typical	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{ssu}	WS to SCK set up time	20	-	-	ns
t_{sh}	WS to SCK hold time	2.5	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	2.5	-	-	ns

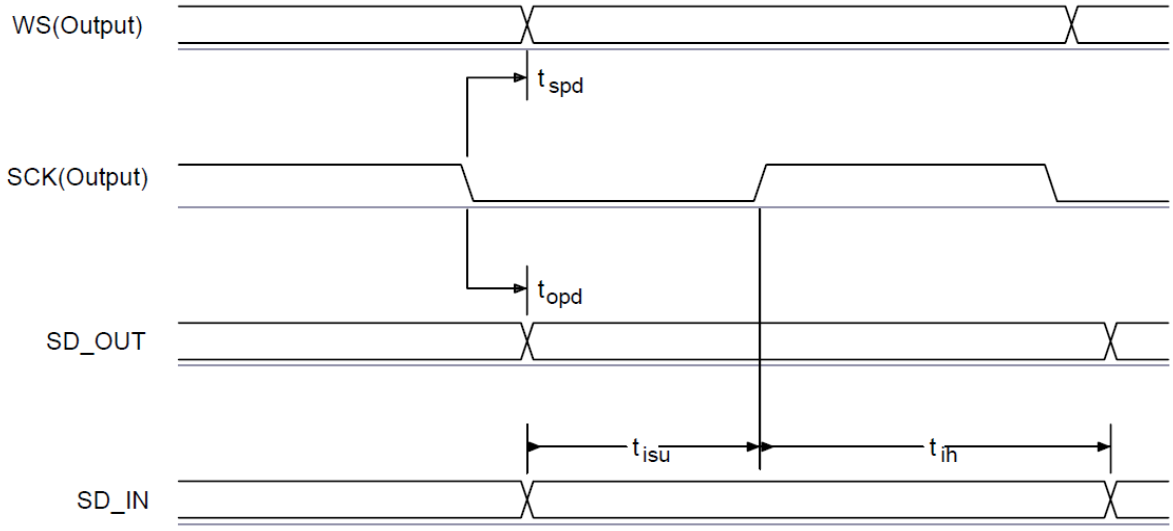

Figure 6 : Digital Audio Interface Master Timing

Table 17 : Digital Audio Interface Master Timing

Symbol	Parameter	Min	Typical	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{spd}	SCK to WS delay	-	-	20	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	10	-	-	ns

4. Software Stacks

NVC-MDCS46 is dual mode Bluetooth 5.0+EDR module, the embedded iNova Bluetooth Stack firmware supports the SPP, HID, HFP, A2DP and GATT based BLE Profiles, and supports up to seven devices simultaneously connected.

Contact with the sales agent for support for more profiles and applications with iNova Bluetooth stack firmware.

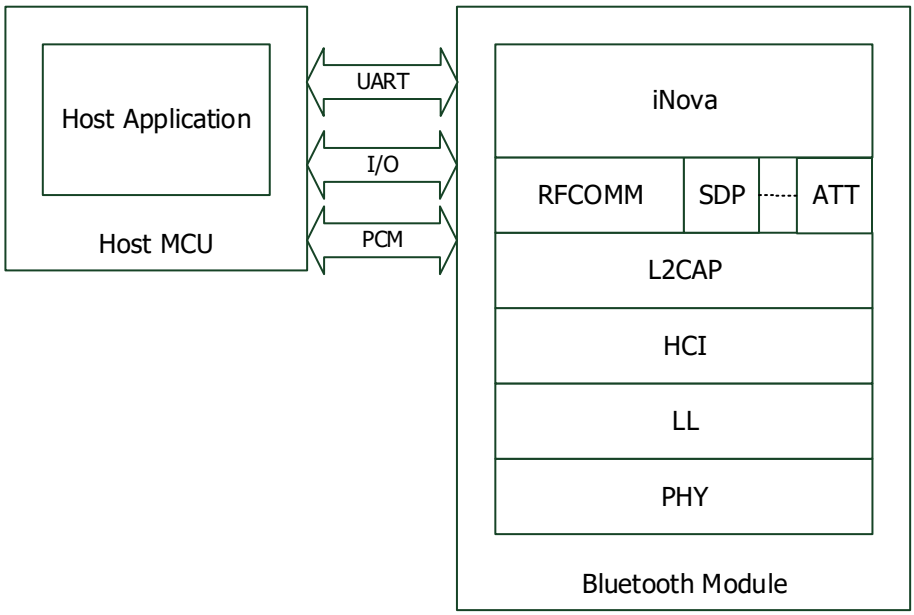

Figure 7: iNova Stack

Please refer to the Novacomm Control Interface User Guide (NCCI) for the details.

5. Reference Design

TBD

Figure 8 : Reference Design

6. RF Layout Guidelines

NVC-MDCS46 has an on-board PCB antenna. So it's very important to make a good PCB placement for the module to ensure the design a good RF performance. Please follow the recommendations shown in Figure 9.

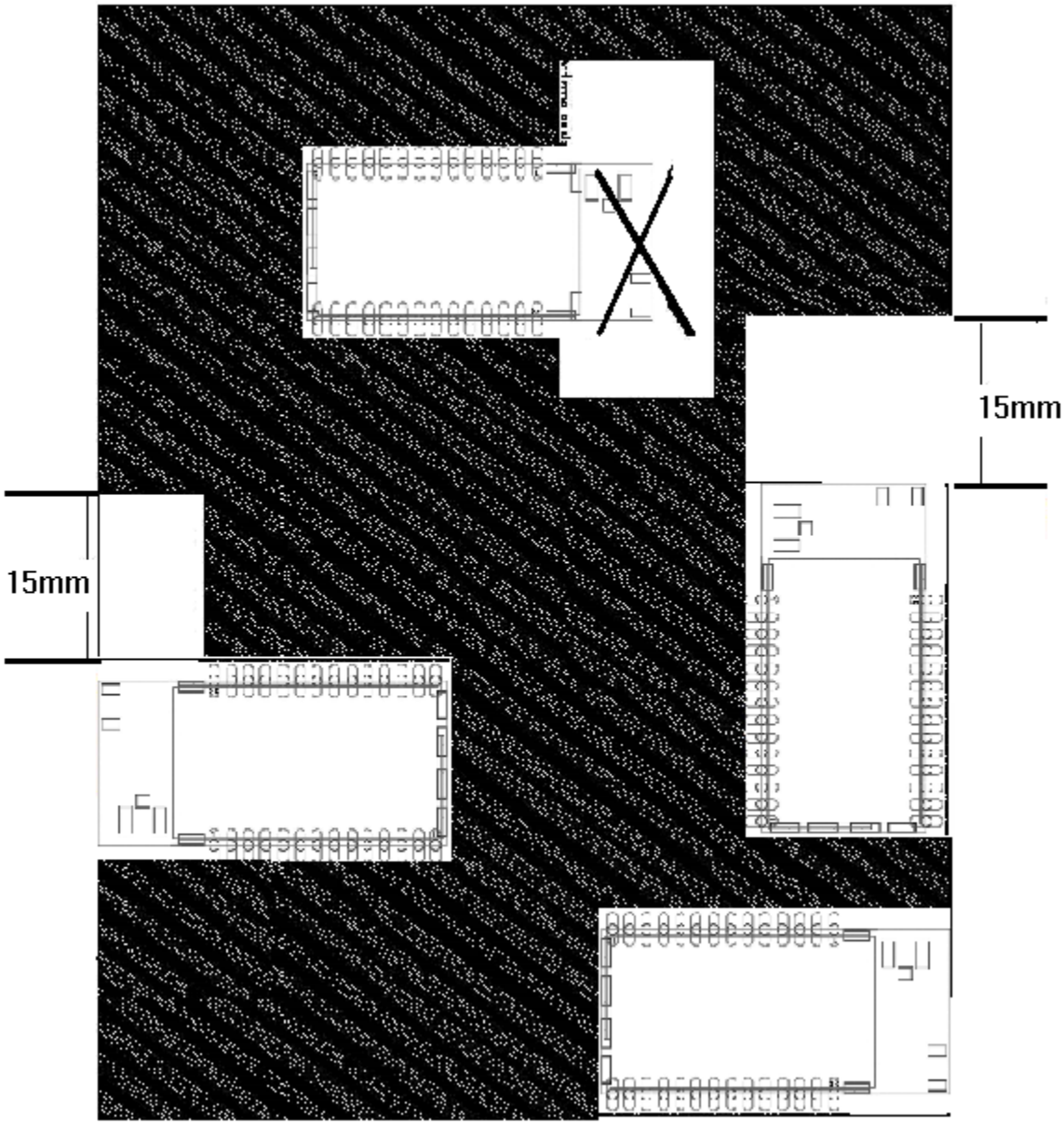

Figure 9: Placement of the Module on a Main Board

7. Reflow Profile

NVC-MDCS46 is compatible with industrial standard reflow profile for Pb-free solders. The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow.

There are four zones:

- Preheat Zone - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.

- Equilibrium Zone - This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
- Reflow Zone- The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
- Cooling Zone - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5° C/s.

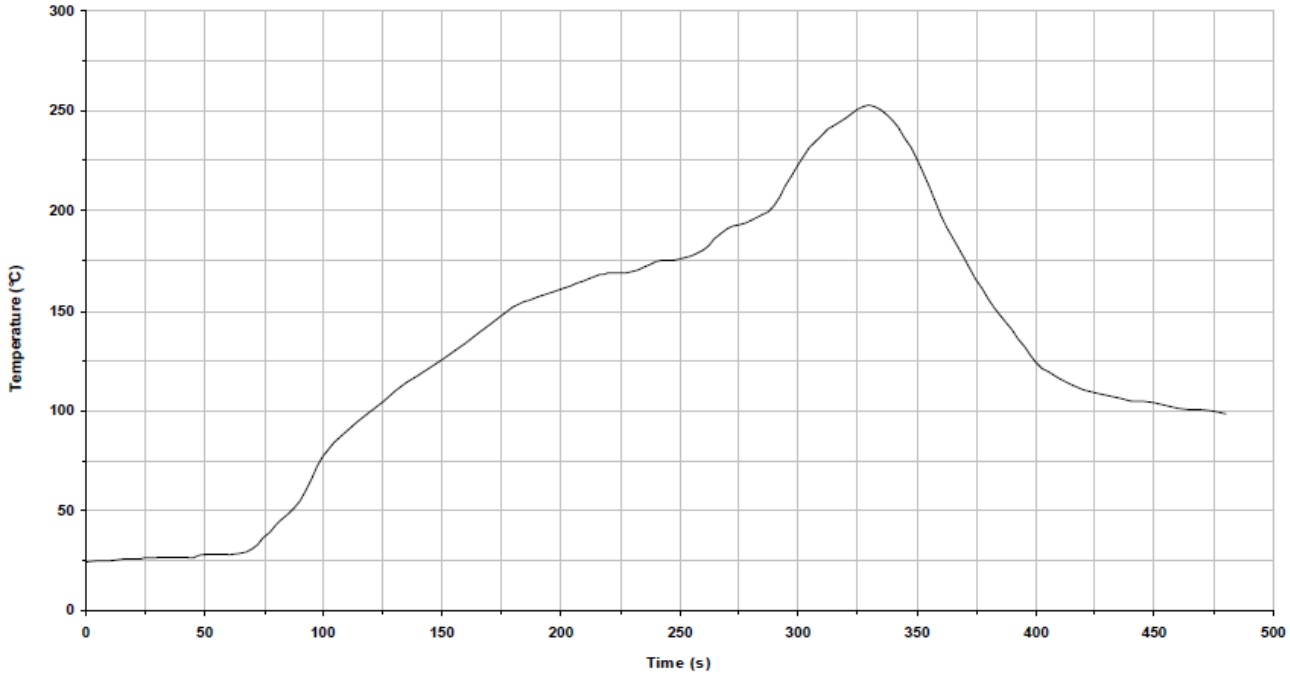

Figure 10: Typical Lead-Free Re-flow Solder Profile for NVC-MDCS46

Key features of the profile:

- Initial Ramp = 1-2.5° C/sec to 175° C ±25° C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250° C) = 3° C/sec max.
- Time above liquidus temperature (217° C): 45-90 seconds
- Device absolute maximum reflow temperature: 255° C

Note: Apply a local 0.2mm thickness solder cream for the module.

8. Physical Dimensions

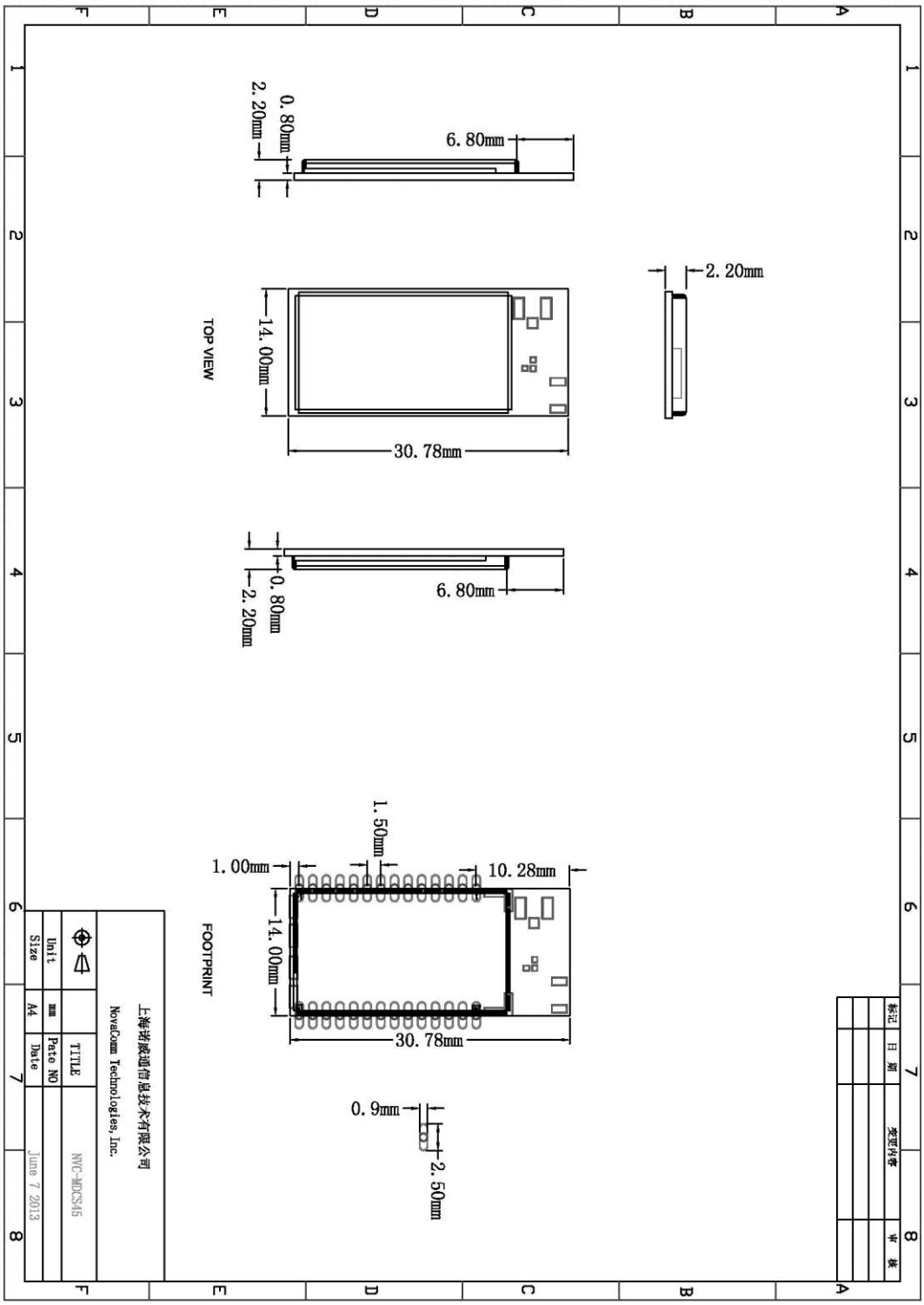

Figure 11: Physical Dimensions and Recommended Footprint (Unit: mm, Deviation:0.02mm)

9. Package

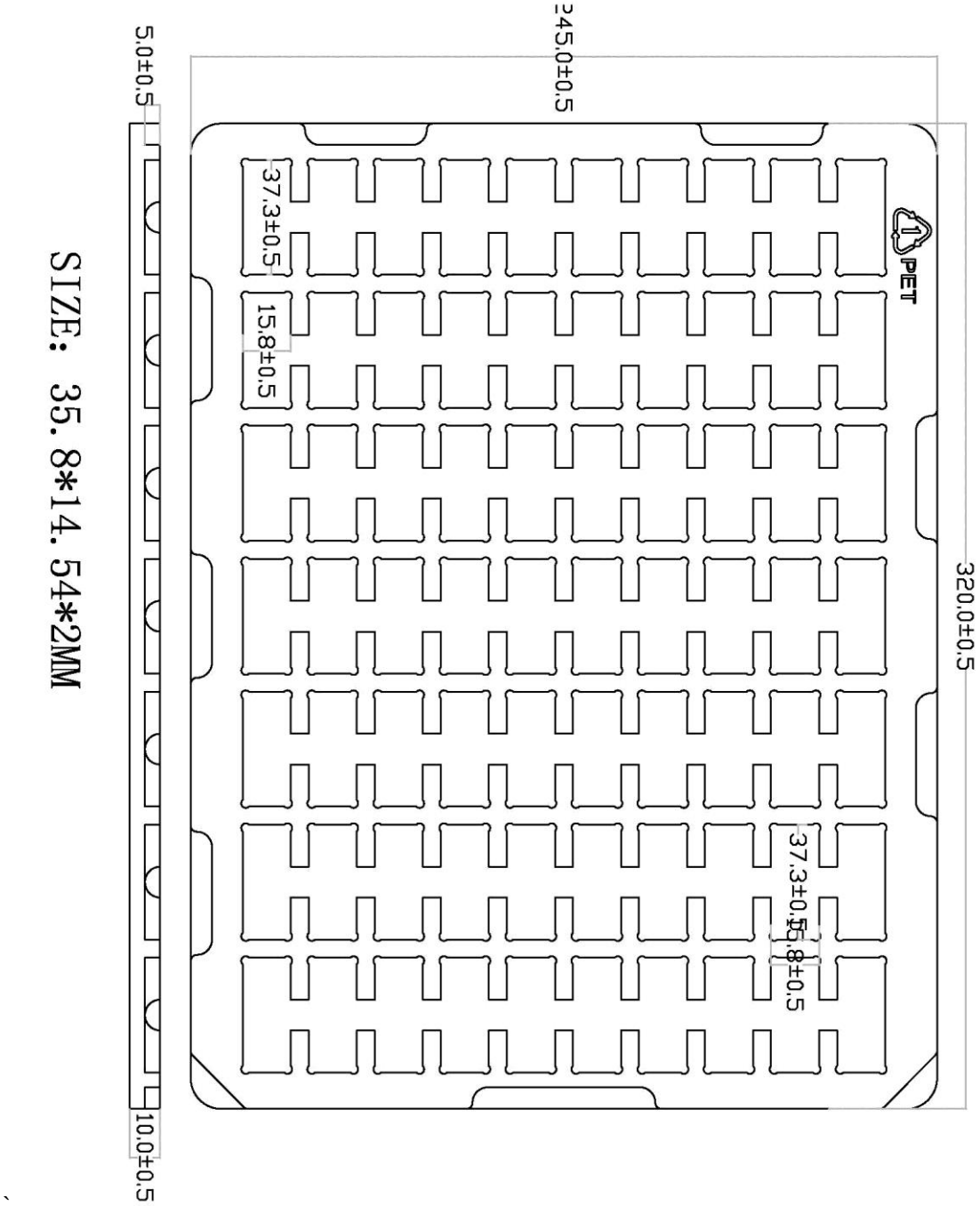

Figure 12: NVC-MDCS46 package

Plastic tray, plus aluminum bags do vacuum packing. Items in One Package number of 60PCS

10. Contact Information

Sales: sales@novacomm.cn

Technical support: support@novacomm.cn

Phone: +86 21 60453799

Fax: +86 21 60453796

Street address: 1304, No. 1077 Zu Chongzhi Rd, Zhangjiang Hi-Tech Park, Shanghai