



**SPECIFICATION
FOR
LCM Module
KD035VGRPA083**

MODULE:	KD035VGRPA083
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2017.11.16
1.1	Update LCD Optical specification	2018.03.06
1.2	Update LCD Optical specification	2018.03.29
1.3	Update DC Electrical Characteristics	2018.09.19

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

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常备库存
Stock For Sale

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range



Revision History

[illegible]

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* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.5'TFT-LCD contains 480X640 pixels, and can display up to 65K/262K colors.

* Features

-Low Input Voltage: 3.3V(TYP)

-Display Colors of TFT LCD: 65K/262K colors

Interface: 3SPI+16/18Bit RGB Interface

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	53.57(H) *71.42(V) (3.5inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K	colors	-
Number of pixels	480(RGB)*640	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.1116(H) x 0.1116 (V)	mm	-
Viewing angle	Wide angle	o'clock	-
TFT Controller IC	HX8363-A	-	-
Display mode	Transflective /Normally Black	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		64.0		mm	-
	Vertical(V)		85.0		mm	-
	Depth(D)		3.10		mm	-
Weight			34		g	-

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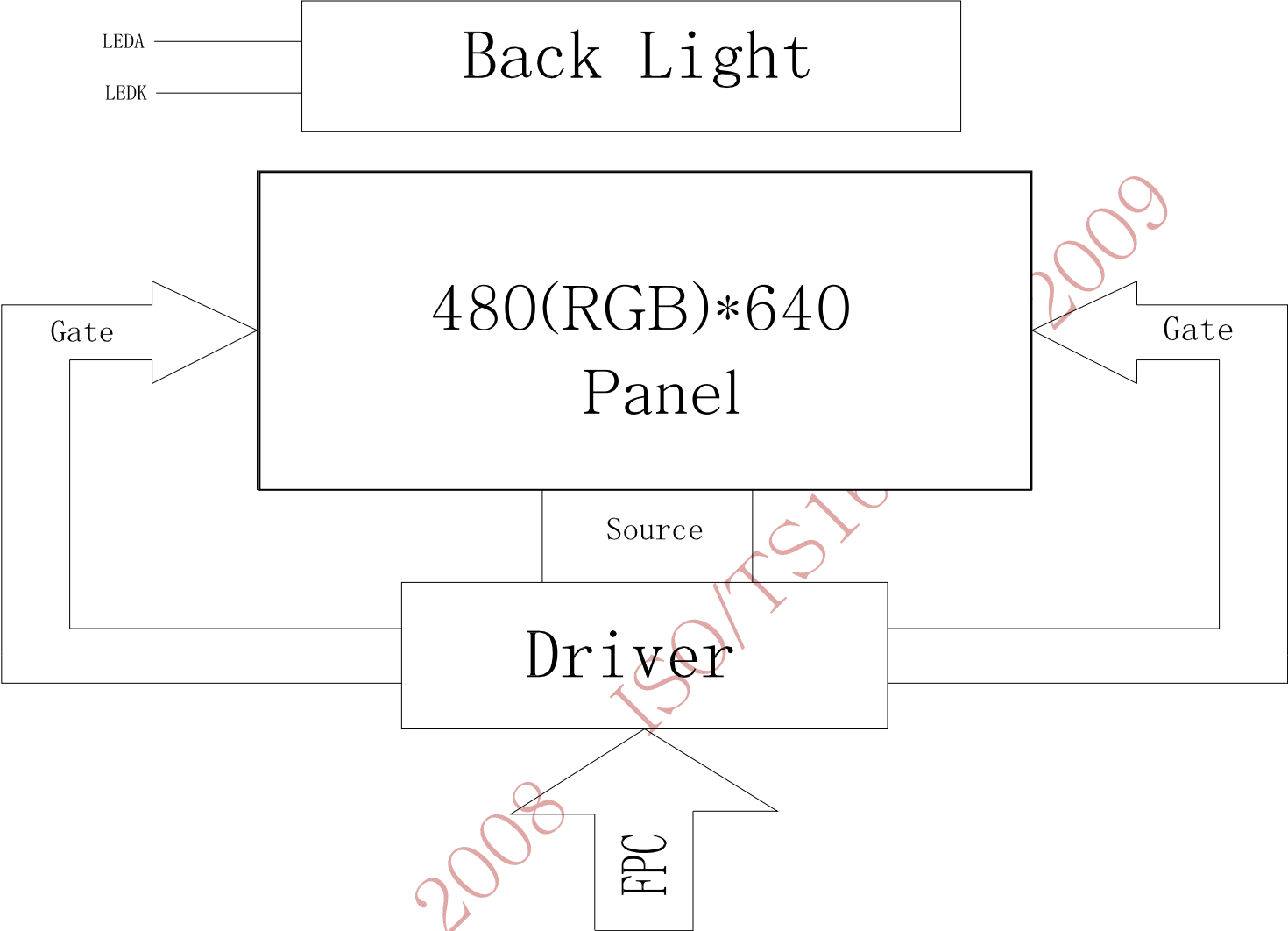
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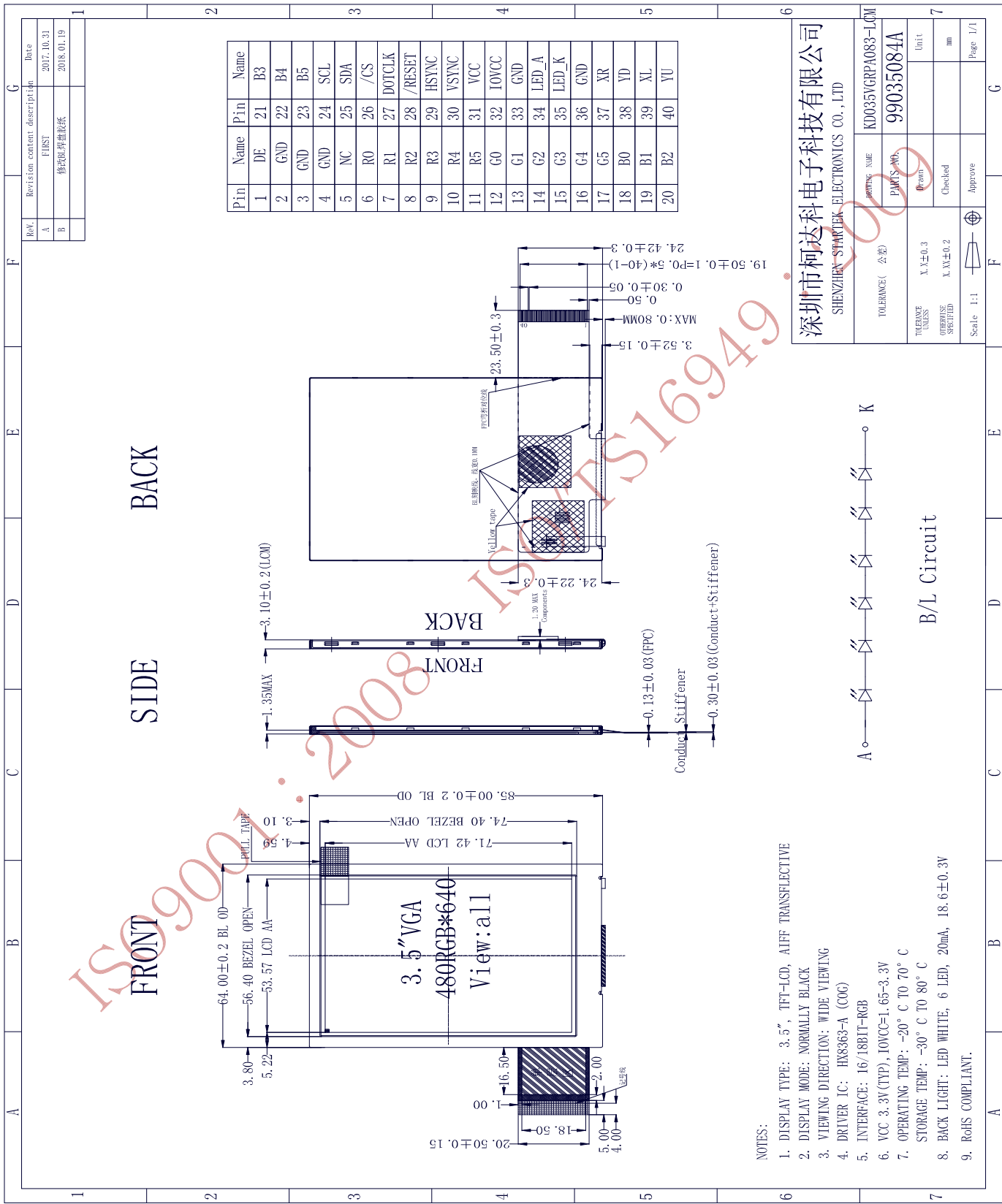
1. Block Diagram



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2. Outline dimension



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3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	DE	A data ENABLE signal in RGB I/F mode. Has to be fixed to GND level in MPU interface mode.	I
2	GND	Ground.	P
3	GND	Ground.	P
4	GND	Ground.	P
5	NC		
6-11	R0-R5	Red Data bus	I/O
12-17	G0-G5	Green Data bus	I/O
18-23	B0-B5	Blue Data bus	I/O
24	SCL	Serves as a write signal and writes data at the rising edge. When operate in serial interface, it serves as SCL (Serial Clock) If not used, let it open or connected to VCC	I
25	SDA	Serial data input pin in serial interface operation	I
26	CS	Chip select input pin ("Low" enable). fix this pin at VCI or GND when not in use.	I
27	DOTCLK	Dot clock signal. Must be connected to GND or VCC if not used.	I
28	RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to GND or VCC). (Latch type)	I
29	HSYNC	Line synchronizing signal. Must be connected to GND or VCC if not used.	I
30	VSYN	Frame synchronizing signal. Must be connected to GND or VCC if not used.	I
31	VCC	Supply voltage(3.3V).	I
32	IOVCC	A power supply for the I/O circuit. (1.65-3.3V)	I/O
33	GND	Ground.	O
34	LED_A	Anode pin of backlight	P
35	LED_K	Cathode pin OF backlight	P

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36	GND	Ground.	P
37	XR	Touch panel Right Glass Terminal	A/D
38	YD	Touch panel Bottom Film Terminal	A/D
39	XL	Touch panel Left Glass Terminal	A/D
40	YU	Touch panel Top Film Terminal	A/D

ISO9001 : 2008

ISO/TS16949 : 2009

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4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	200	300	--		
Reflection Ratio (With Polarizer)		R		--	7	--	%	
Reflective Contrast Ratio		Cr		--	20	--	%	
Color gamut of CF		NTS		--	60	--	%	
Response time	Rising	T _R +T _F		--	30	50	msec	
	Falling							
Color Filter Chromaticity	White	W _X		0.248	0.288	0.328		Chromaticity measuring machine: CFT-01. Reference Only
		W _Y		0.272	0.312	0.352		
	Red	R _X		0.425	0.465	0.505		
		R _Y		0.286	0.326	0.366		
	Green	G _X		0.277	0.317	0.357		
		G _Y		0.458	0.498	0.538		
	Blue	B _X		0.135	0.175	0.215		
		B _Y		0.075	0.115	0.155		
Viewing angle	Hor.	Θ _L	CR>10	60	80	--		
		Θ _R		60	80	--		
	Ver.	Θ _U		60	80	--		
		Θ _D		60	80	--		
		Option View Direction		Wide angle				

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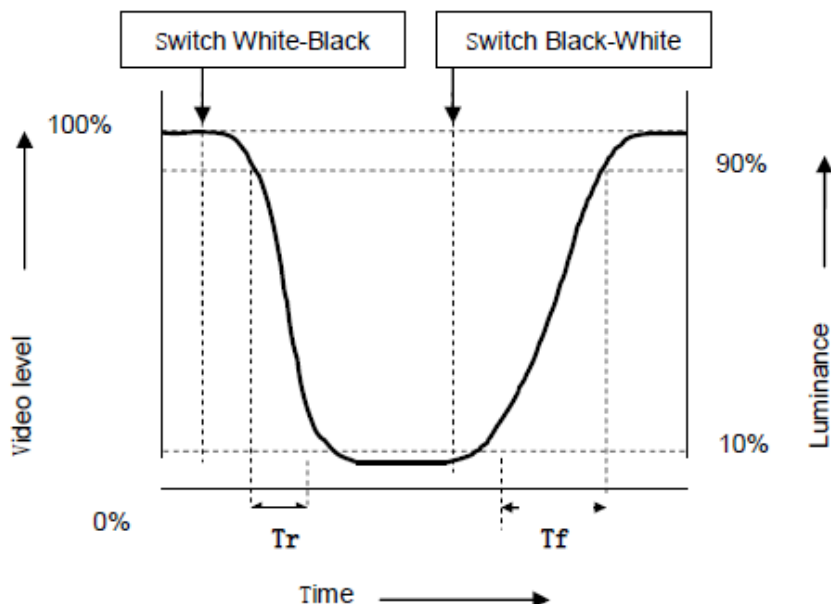
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[2] Response Time(Tr、 Tf)

The rise time ‘Tr’ is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time ‘Tf’ is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



[3] Contrast ratio (Cr)

The contrast ratio (Cr), measured on a module, is the ratio between the luminance (L_w) in a full white area (R=G=B=1) and the luminance (L_d) in a dark area (R=G=B=0):

$$Cr = \frac{L_w}{L_d}$$

ISO9000

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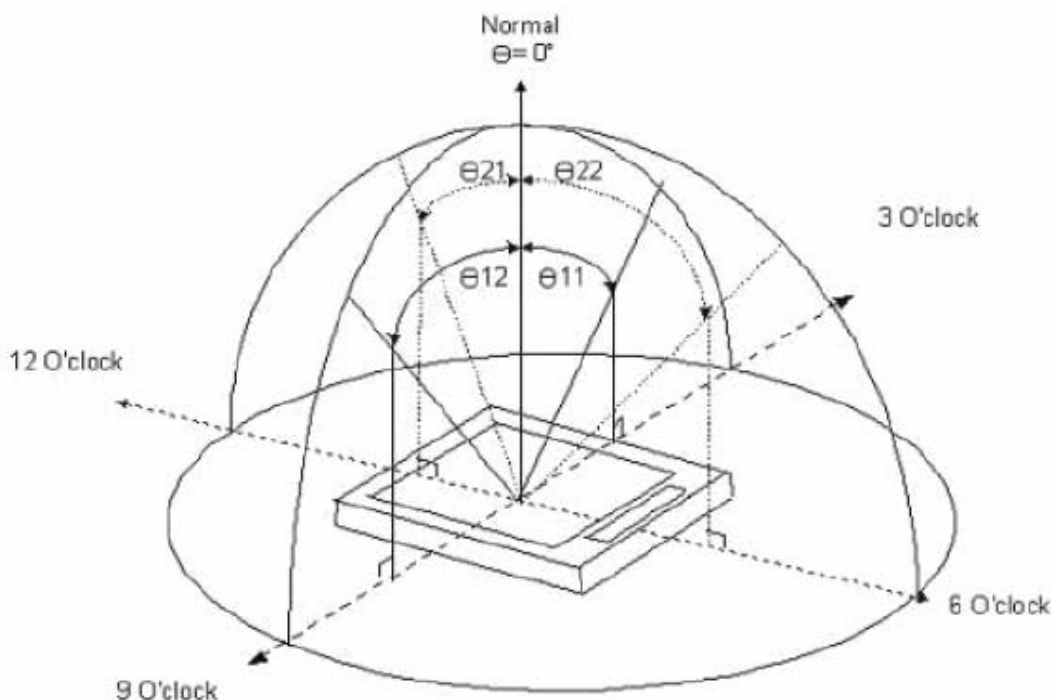
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[4]Viewing angle diagram



[5] Definition of color gamut

Measuring machine:CFT-01. NTSC'S Primaries: R(x,y,Y)、G(x,y,Y)、 B(x,y,Y).

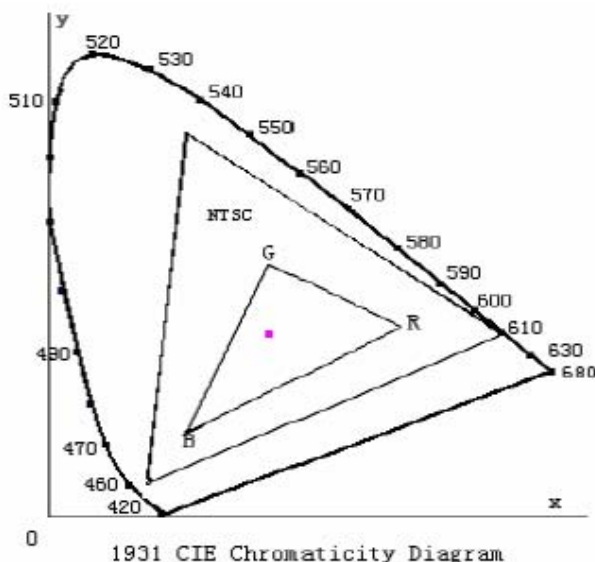


Fig. 1931 CIE chromaticity diagram

$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

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5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCC	-0.3	4.6	V
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCC	2.5	3.3	3.6	V	
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.3		
Normal mode Current consumption	I _{VCC+IOVCC}	--	20	40	mA	
Level input voltage	V _{IH}	0.7 IOVCC	-	IOVCC	V	
	V _{IL}	GND	-	0.3 IOVCC	V	
Level output voltage	V _{OH}	0.8 IOVCC	-	IOVCC	V	
	V _{OL}	GND	-	0.2 IOVCC	V	

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5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 6 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	15	20	--	mA	
Forward Voltage	V_F	--	18.6	--	V	
LCM Luminance	L_v	65	115	--	cd/m ²	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

SNote (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

$T_a=25\pm3\text{ }^{\circ}\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at $T_a=25^{\circ}\text{C}$ and $I_L=20\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 20mA. The constant current driving method is suggested.



B/L Circuit

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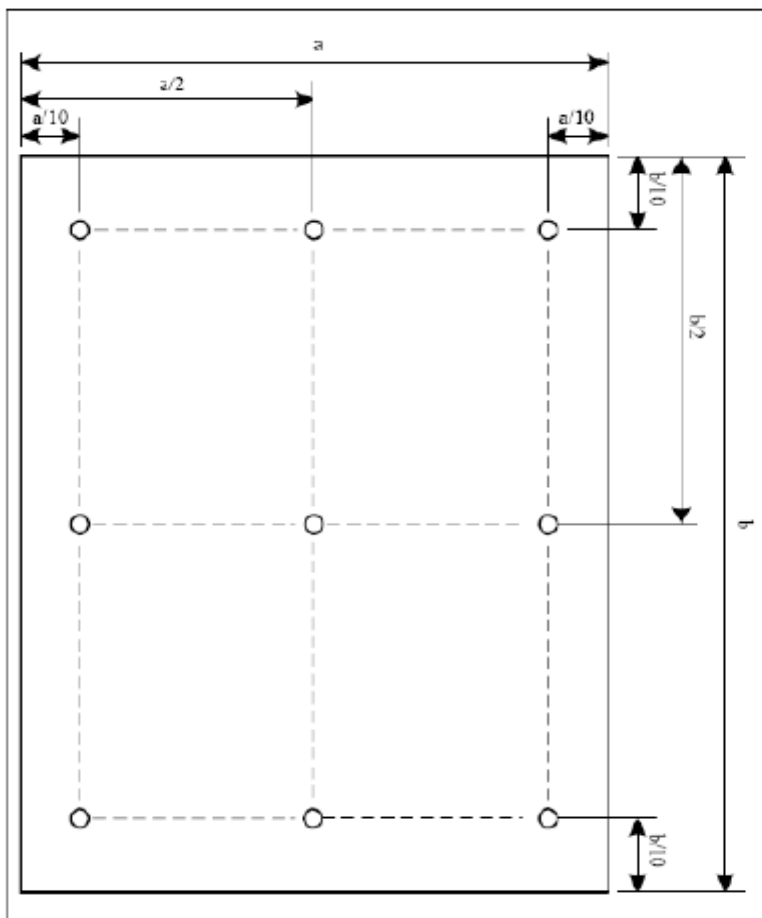
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NOTE 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

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6. AC Characteristic

6.1 Serial Interface Characteristics (3-Pin Serial)

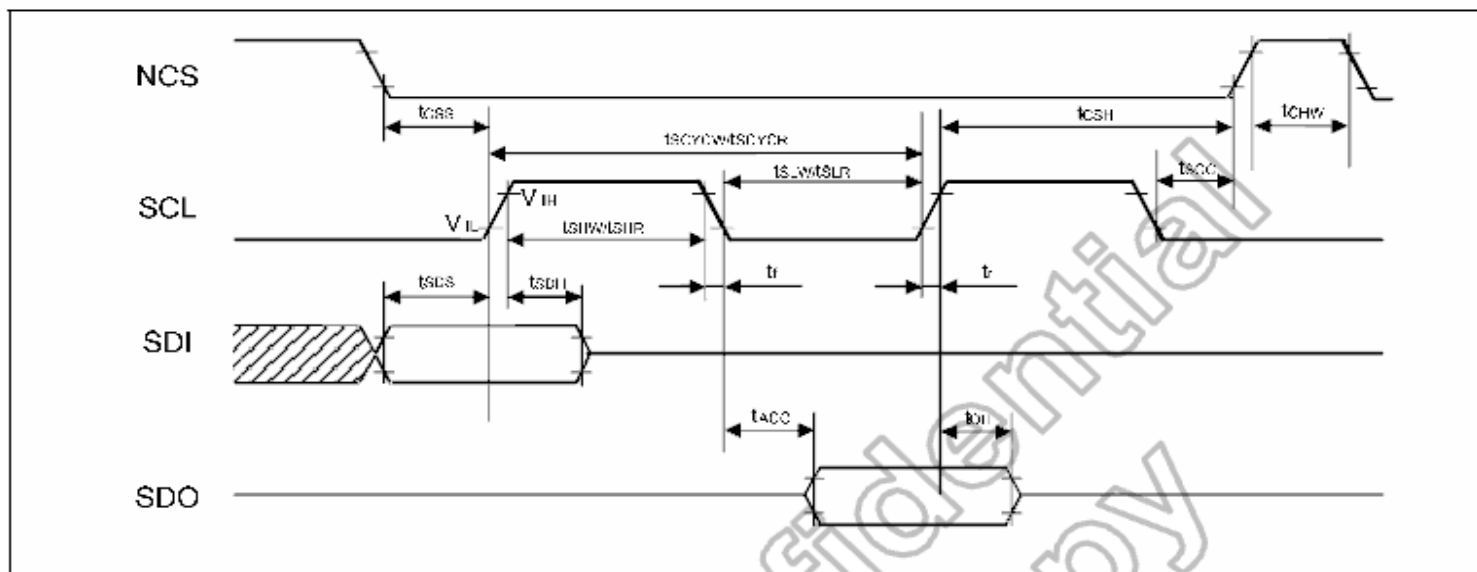


Figure 8.1: 3-pin Serial Interface Characteristics

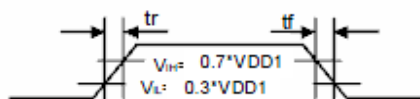
(VSSA=VSSD=0V, VDD1=1.65V to 1.95V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, $T_A = -30$ to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write)	t_{SCYCW}	SCL	80	-	-	ns
SCL "H" pulse width (Write)	t_{SHW}		30	-	-	
SCL "L" pulse width (Write)	t_{SLW}		30	-	-	
Data setup time (Write)	t_{SDS}	SDI	10	-	-	ns
Data hold time (Write)	t_{SDH}		10	-	-	
Serial clock cycle (Read)	t_{SCYCR}	SCL	150	-	-	ns
SCL "H" pulse width (Read)	t_{SHR}		60	-	-	
SCL "L" pulse width (Read)	t_{SLR}		60	-	-	
Access time	t_{acc}	SDO For maximum $C_L=30\text{pF}$ For maximum $C_L=8\text{pF}$	10	-	60	ns
Output disable time	t_{OH}	SDO For maximum $C_L=30\text{pF}$ For maximum $C_L=8\text{pF}$	15	-	100	ns
SCL to Chip select	t_{SCC}	NCS	30	-	-	ns
NCS "H" pulse width	t_{CHW}	NCS	60	-	-	ns
NCS-SCL time (write)	t_{CSS}	NCS	30	-	-	ns
NCS-SCL time (write)	t_{CSH}		30	-	-	
NCS-SCL time (Read)	t_{CSS}	NCS	60	-	-	ns
NCS-SCL time (Read)	t_{CSH}		65	-	-	

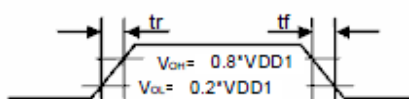
Note: The input signal rise time and fall time (t_r , t_f) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Input Signal Slope



Output Signal Slope



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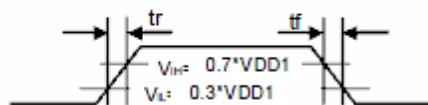
(VSSA=VSSD=0V, VDD1=1.95V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write)	t _{SCYCW}	SCL	80	-	-	ns
SCL "H" pulse width (Write)	t _{SHW}		30	-	-	
SCL "L" pulse width (Write)	t _{SLW}		30	-	-	
Data setup time (Write)	t _{SDS}	SDI	10	-	-	ns
Data hold time (Write)	t _{SDH}		10	-	-	
Serial clock cycle (Read)	t _{SCYCR}	SCL	150	-	-	ns
SCL "H" pulse width (Read)	t _{SHR}		60	-	-	
SCL "L" pulse width (Read)	t _{SLR}		60	-	-	
Access time	t _{ACC}	SDO For maximum C _L =30pF For maximum C _L =8pF	5	-	60	ns
Output disable time	t _{OH}	SDO For maximum C _L =30pF For maximum C _L =8pF	8	-	100	ns
SCL to Chip select	t _{SCC}	NCS	30	-	-	ns
NCS "H" pulse width	t _{CHW}	NCS	60	-	-	ns
NCS-SCL time (write)	t _{CSS}	NCS	30	-	-	ns
NCS-SCL time (write)	t _{CSH}		30	-	-	
NCS-SCL time (Read)	t _{CSS}	NCS	60	-	-	ns
NCS-SCL time (Read)	t _{CSH}		65	-	-	

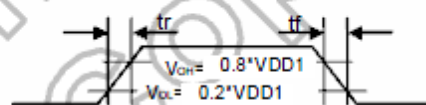
Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Input Signal Slope



Output Signal Slope





6.2 RGB Interface Characteristics

Vertical Timings for RGB I/F

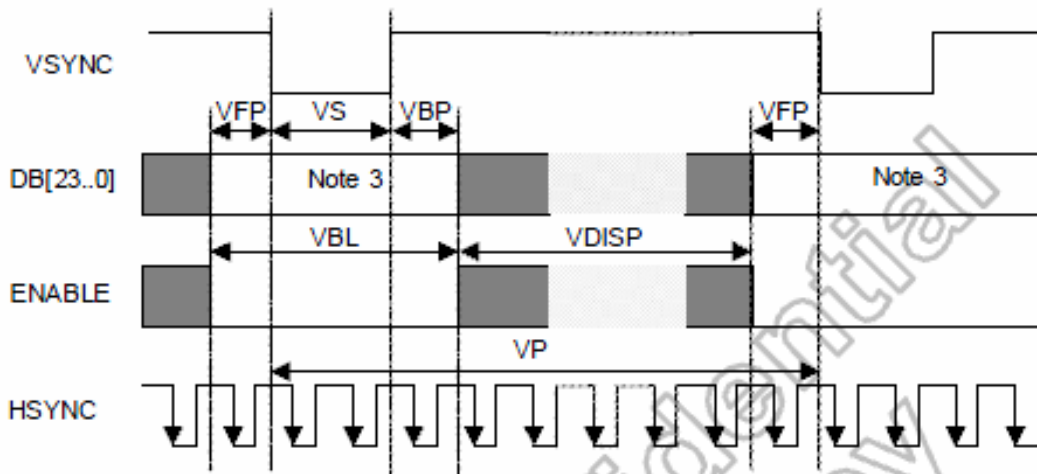


Figure 8.2: Vertical Timings for RGB I/F

(Resolution=480x854, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	860	-	864	Line
Vertical low pulse width	VS	-	2	-	4	Line
Vertical front porch	VFP	-	2	-	4	Line
Vertical back porch	VBP	-	2	-	4	Line
Vertical data start point	-	VS+VBP	4	-	8	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	10	Line
Vertical active area	-	VDISP	-	854	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(4) VRR must keep from 50Hz to 70Hz when adjust other items

(Resolution=480x800, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	806	-	810	Line
Vertical low pulse width	VS	-	2	-	4	Line
Vertical front porch	VFP	-	2	-	4	Line
Vertical back porch	VBP	-	2	-	4	Line
Vertical data start point	-	VS+VBP	4	-	8	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	10	Line
Vertical active area	-	VDISP	-	800	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(4) VRR must keep from 50Hz to 70Hz when adjust other items

Table 8.5: Vertical Timings for RGB I/F

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Horizontal Timings for RGB I/F

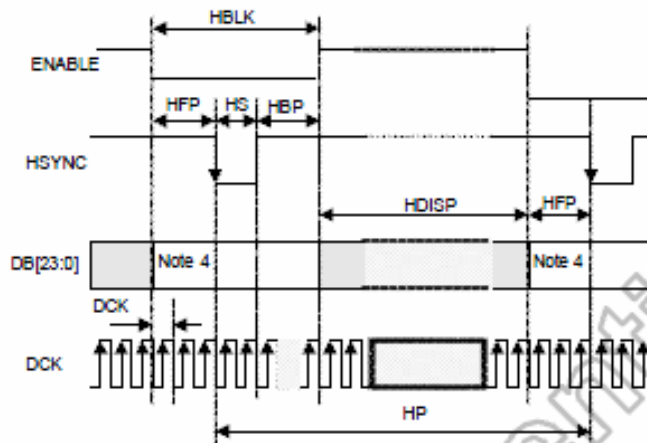


Figure 8.3: Horizontal Timing for RGB I/F

(Resolution=480x854, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, $T_A = -30$ to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note ⁽³⁾	504	-	568	DCK
HS low pulse width	HS	-	5	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal data start point	-	HS+HBP	19	-	83	DCK
			700	-	-	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	DCK
Horizontal active area	HDISP	-	-	480	-	DCK
Pixel clock frequency	DCK	VRR = Min. 50Hz	21.6	-	34.3	MHz
When RGB I/F is running		- Max. 70Hz	29.1	-	46.2	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by $0.30 \times VDD1$ for low state and $0.70 \times VDD1$ for high state.

(3) HP is multiples of eight DCK.

(4) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(5) VRR must keep from 50Hz to 70Hz when adjust other items.

(Resolution=480x800, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, $T_A = -30$ to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note ⁽³⁾	504	-	568	DCK
HS low pulse width	HS	-	5	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal data start point	-	HS+HBP	19	-	83	DCK
			700	-	-	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	DCK
Horizontal active area	HDISP	-	-	480	-	DCK
Pixel clock frequency	DCK	VRR = Min. 50Hz	20.3	-	32.2	MHz
When RGB I/F is running		- Max. 70Hz	31	-	49.2	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by $0.30 \times VDD1$ for low state and $0.70 \times VDD1$ for high state.

(3) HP is multiples of eight DCK.

(4) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(5) VRR must keep from 50Hz to 70Hz when adjust other items.

Table 8.6: Horizontal Timings for RGB I/F

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General Timings for RGB I/F

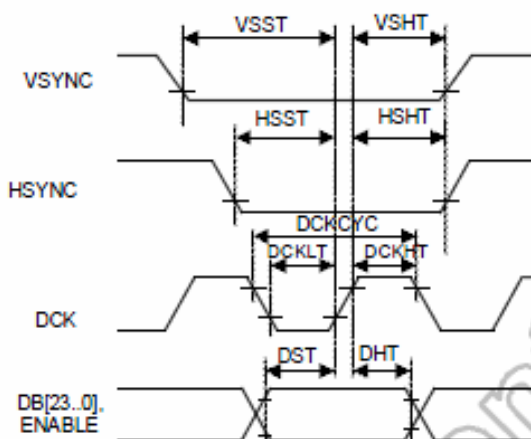


Figure 8.4: General Timings for RGB I/F

(Resolution=480x854, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. Setup time	VSST	-	5	-	-	ns
Vertical sync. Hold time	VSH	-	5	-	-	ns
Horizontal sync. Setup time	HSST	-	5	-	-	ns
Horizontal sync. Hold time	HSH	-	5	-	-	ns
Pixel clock cycle When RGB I/F is running	DCKCYC	VRR = Min. 50 Hz Max. 70 Hz	29.1 ⁽³⁾	-	46.2 ⁽⁴⁾	ns
Pixel clock low time	DCKLT	-	5	-	-	ns
Pixel clock high time	DCKHT	-	5	-	-	ns
Data setup time DB[23:0]	DST	-	5	-	-	ns
Data Hold time DB[23:0]	DHT	-	5	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.

(3) 34.3 MHz

(4) 21.6 MHz

(Resolution=480x800, VSSA=VSSD=0V, VDD1=1.65V to 3.3V, VDD2=2.5 to 3.3V, VDD3=2.5 to 3.3V, T_A = -30 to 70°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. Setup time	VSST	-	5	-	-	ns
Vertical sync. Hold time	VSH	-	5	-	-	ns
Horizontal sync. Setup time	HSST	-	5	-	-	ns
Horizontal sync. Hold time	HSH	-	5	-	-	ns
Pixel clock cycle When RGB I/F is running	DCKCYC	VRR = Min. 50 Hz Max. 70 Hz	31 ⁽³⁾	-	49.2 ⁽⁴⁾	ns
Pixel clock low time	DCKLT	-	5	-	-	ns
Pixel clock high time	DCKHT	-	5	-	-	ns
Data setup time DB[23:0]	DST	-	5	-	-	ns
Data Hold time DB[23:0]	DHT	-	5	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.

(3) 32.2MHz

(4) 20.3MHz

Table 8.7: General Timings for RGB I/F

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6.3 Reset Timing

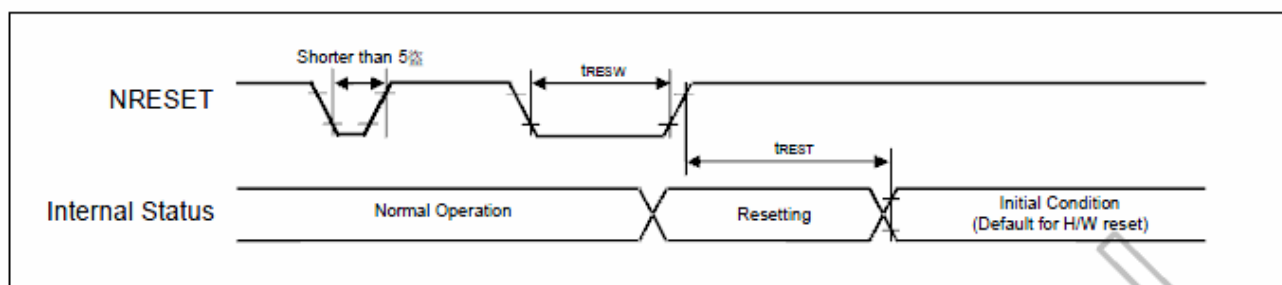


Figure 8.10: Reset Input Timing

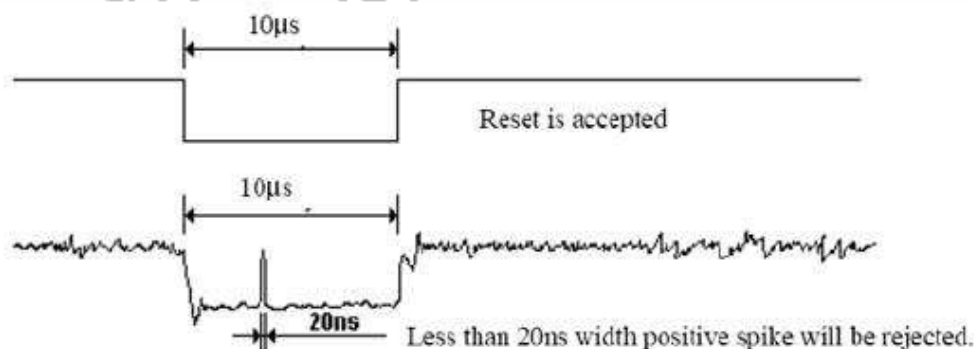
Symbol	Parameter	Related Pins	Min.	Typ.	Max.	Note	Unit
tRESW	Reset low pulse width ⁽¹⁾	NRESET	10	-	-	-	µs
tREST	Reset complete time ⁽²⁾	-	-	-	5	When reset is applied during Sleep In mode	ms
		-	-	-	120	When reset is applied during Sleep Out mode	ms

Table 8.18: Reset Timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
- (3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown below:



- (5) When Reset is applied during Sleep In Mode.
- (6) When Reset is applied during Sleep Out Mode.
- (7) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

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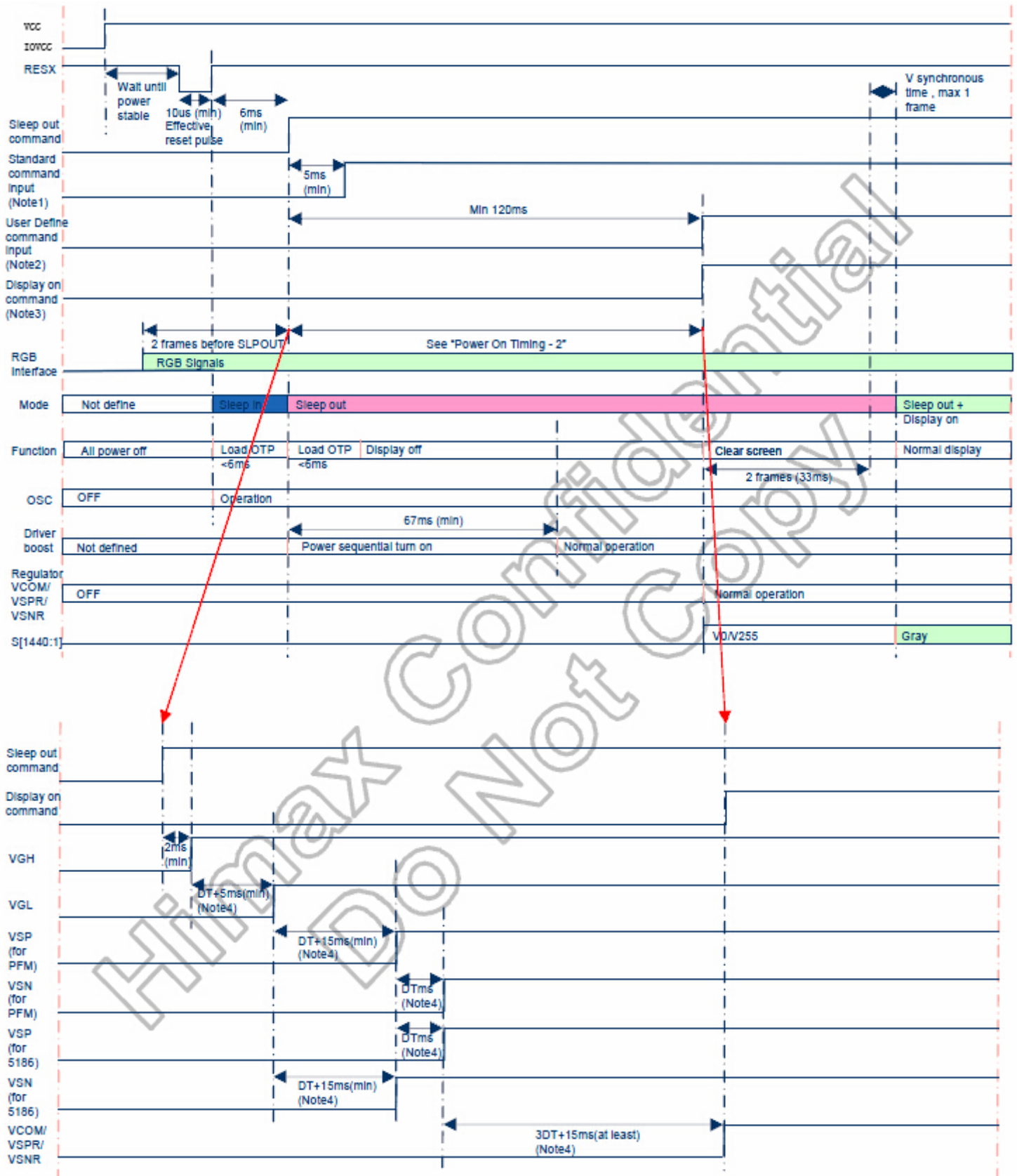
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6.4 Power On/Off Timing



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- Note1:**
“Standard” command except “01h” & “10h” command must wait 5ms after “Sleep out” command then can be sent. “01h” & “10h” command must wait 100ms after “Sleep out” command then can be sent.
- Note2:**
“User Define” command must wait 100ms after “Sleep out” command then can be sent. “B9h” command must be sent first then other command can be sent after “B9h” command.
- Note3:**
“Display on” command must send after “User Define” command or at the same time.
- Note4:**
DT[0]: Delay time of power on and power off sequence.

DT1	DT0	Delay time of power on and power off sequence on
0	0	5ms
0	1	10ms
1	0	15ms
1	1	20ms

Default DT=5ms

Figure 8.11: Power On Timing

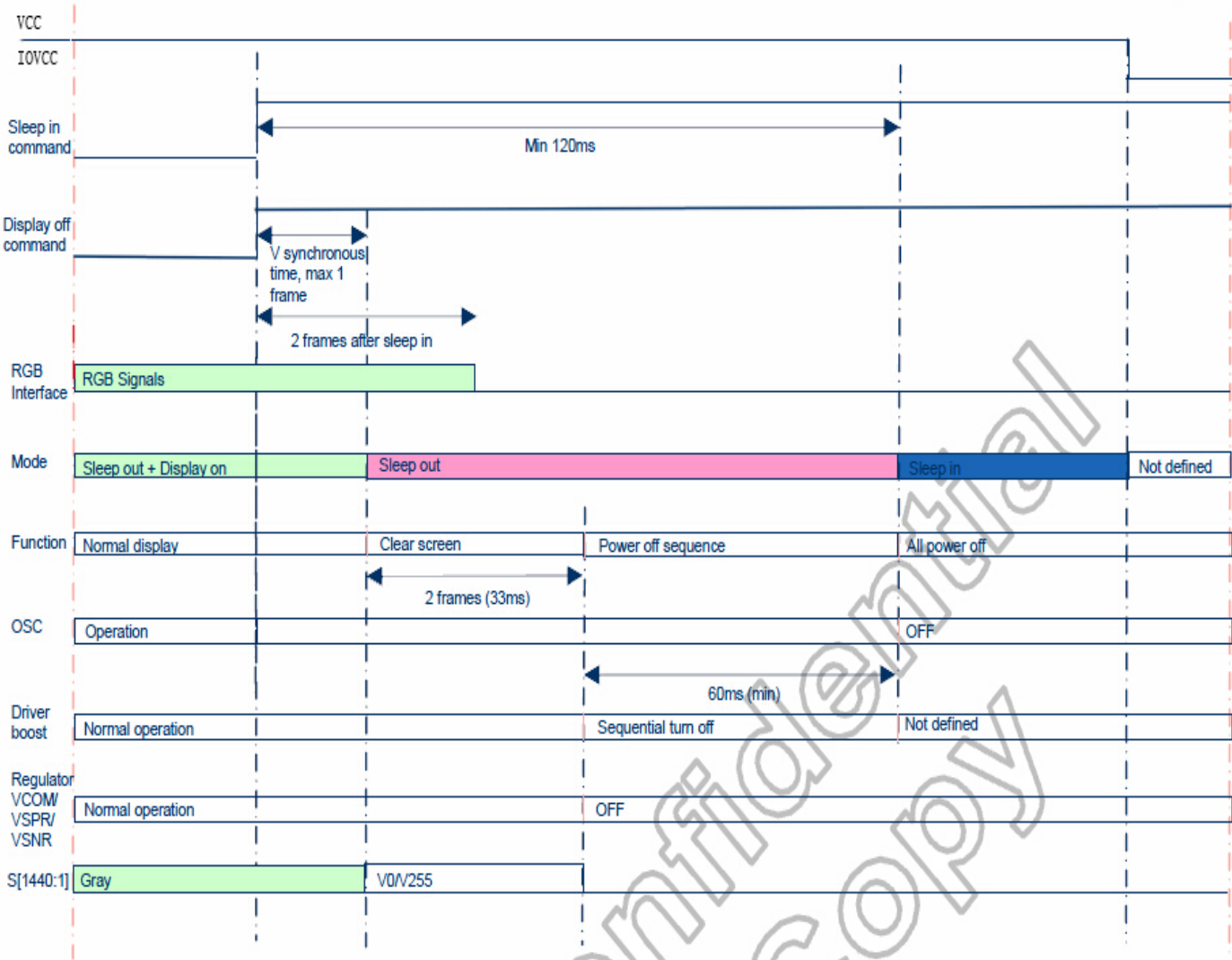


Figure 8.12: Power Off Timing



7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

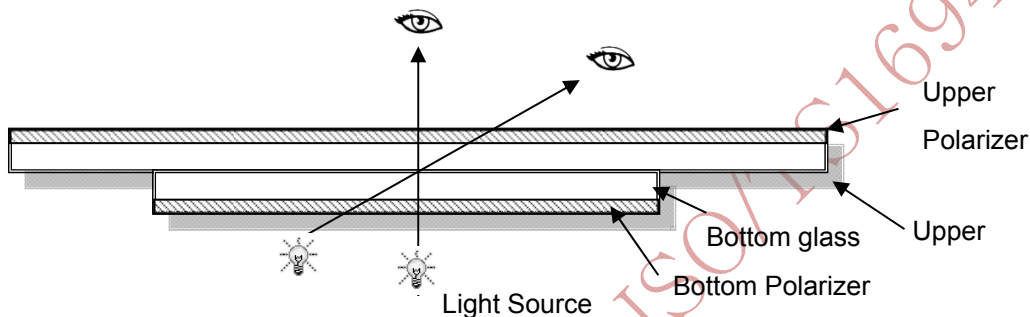
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

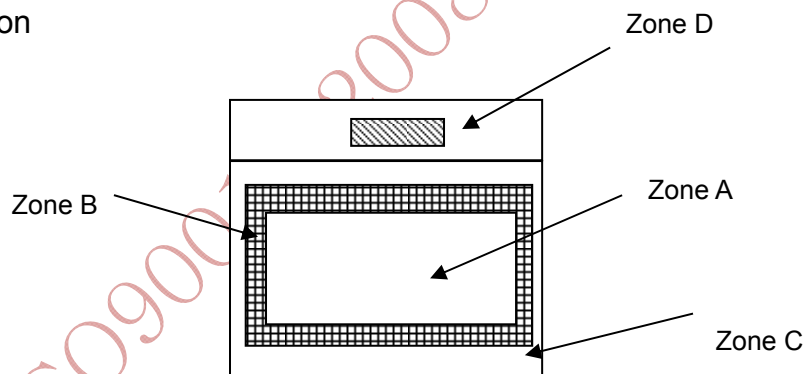
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note: As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

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7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

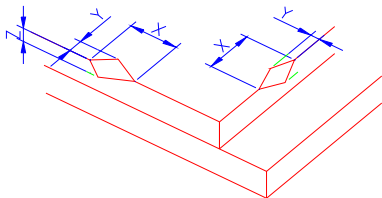
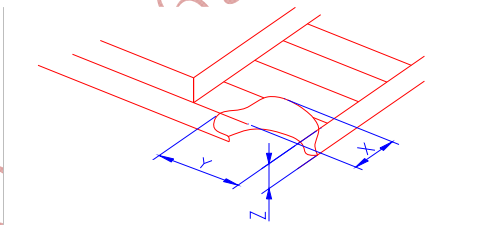
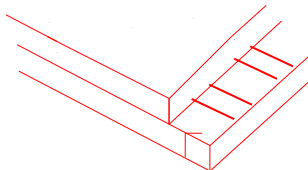
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot, Dim spot, Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	



7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							

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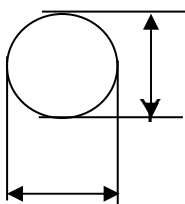
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2.0

Spot defect



X

$$\Phi = (X + Y) / 2$$

① light dot (LCD/TP/Polarizer black/white spot, light dot, pinhole, dent, stain)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.10$	Ignore		
$0.10 < \Phi \leq 0.25$			
$0.25 < \Phi \leq 0.3$			
$\Phi > 0.35$			

② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.1$	Ignore		
$0.10 < \Phi \leq 0.25$			
$0.25 < \Phi \leq 0.3$			
$\Phi > 0.35$			

③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		
$0.3 < \Phi \leq 0.5$			
$\Phi > 0.5$			

④ Pixel bad points (light dot, Dim dot, color dot)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.1$	Ignore		
$0.15 < \Phi \leq 0.25$			
$\Phi > 0.3$			

⑤ Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		
$0.3 < \Phi \leq 0.4$			
$0.4 < \Phi \leq 0.5$			
$\Phi > 0.5$			

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3.0	Line defect (LCD/TP /Polarizer backlight black/white line, scratch, stain)	Width(mm)	Length(m m)	Acceptable Qty		
				A	B	C
		$\Phi\leq0.05$	Ignore	Ignore		Ignore
		$0.05<W\leq0.06$	$L\leq3.0$	$N\leq2$		
		$0.07<W\leq0.08$	$L\leq2.0$	$N\leq1$		
$0.08<W$	Define as spot defect					
4.0	Electronic Comp onents SMT	Not allow missing parts, solderless connection, cold solder joint, mis match, The positive and negative polarity opposite				
5.0	Display color& B rightness	1. Color: Measuring the color coordinates, The measurement standar d according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measu rement standard according to the datasheet or Samples.				
6.0	LCD Mura	By 5% ND filter invisible.				

6.0	RTP Related	TP film • bubble/ accidented spot				
			Size Φ (mm)	Acceptable Qty		
				A	B	C
			$\Phi \leq 0.1$	Ignore		Ignore
			$0.1 < \Phi \leq 0.2$	3 (distance $\geq 10\text{mm}$)		
			$0.25 < \Phi \leq 0.3$	2		
$\Phi > 0.35$	0					

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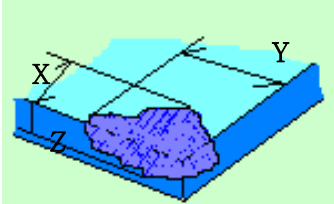
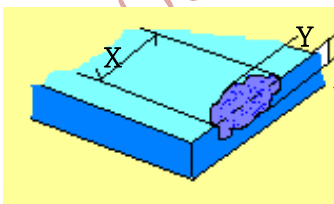
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NO MOQ

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			<table><tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr><tr><th>A</th><th>B</th><th>C</th></tr><tr><td>$\Phi \leq 0.05$</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr><tr><td>$0.05 < W \leq 0.06$</td><td>$L \leq 3.0$</td><td colspan="2">$N \leq 2$</td></tr><tr><td>$0.07 < W \leq 0.08$</td><td>$L \leq 2.0$</td><td colspan="2">$N \leq 1$</td></tr><tr><td>$0.08 < W$</td><td colspan="4">Define as spot defect</td></tr></table>	Width(mm)	Length(mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.05$	Ignore	Ignore		Ignore	$0.05 < W \leq 0.06$	$L \leq 3.0$	$N \leq 2$		$0.07 < W \leq 0.08$	$L \leq 2.0$	$N \leq 1$		$0.08 < W$	Define as spot defect			
Width(mm)	Length(mm)	Acceptable Qty																											
		A	B	C																									
$\Phi \leq 0.05$	Ignore	Ignore		Ignore																									
$0.05 < W \leq 0.06$	$L \leq 3.0$	$N \leq 2$																											
$0.07 < W \leq 0.08$	$L \leq 2.0$	$N \leq 1$																											
$0.08 < W$	Define as spot defect																												
		Assembly deflection	beyond the edge of backlight $\leq 0.2\text{mm}$																										
		Bulge (undulation included)	The ITO film plumped below 0.40mm, it's ok. 																										
		Newton Ring	Newton Ring area $> 1/3$ TP area NG Newton Ring area $\leq 1/3$ TP area OK																										



		TP corner broken X : length Y : width Z : height	<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$X \leq 3\text{mm}$</td><td>$Y \leq 3\text{mm}$</td><td>$Z < \text{COVER thickness}$</td></tr></table> *Circuitry broken is not allowed.	X	Y	Z	$X \leq 3\text{mm}$	$Y \leq 3\text{mm}$	$Z < \text{COVER thickness}$	
X	Y	Z								
$X \leq 3\text{mm}$	$Y \leq 3\text{mm}$	$Z < \text{COVER thickness}$								
		TP edge broken X : length Y : width Z : height	<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>$X \leq 4\text{mm}$</td><td>$Y \leq 2\text{mm}$</td><td>$Z < \text{COVER thickness}$</td></tr></table> * Circuitry broken is not allowed.	X	Y	Z	$X \leq 4\text{mm}$	$Y \leq 2\text{mm}$	$Z < \text{COVER thickness}$	
X	Y	Z								
$X \leq 4\text{mm}$	$Y \leq 2\text{mm}$	$Z < \text{COVER thickness}$								

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

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8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non- operation)	-30℃,30 min ↔ 80℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

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NO MOQ

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9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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10. Packing

---TBD-----

ISO9001 : 2008 ISO/TS16949 : 2009

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