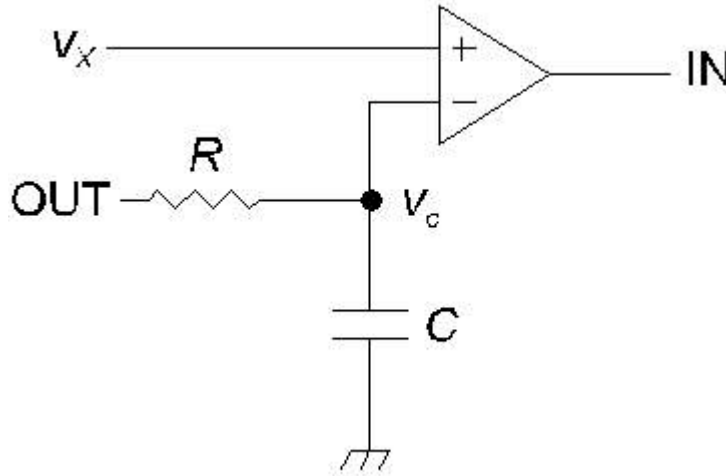


Simple μ C-Based ADCs -- Part II

by Dennis L Feucht

Microcontrollers (μ Cs) often contain a comparator that can implement a precise ADC with the addition of only an external resistor and capacitor. The technique is to implement a charge-balancing, or Σ - Δ (Δ - Σ) ADC. The basic scheme uses a comparator which outputs μ C input bit IN and requires one μ C output bit, OUT. The circuit is shown below.



In μ C software, the ADC routine is best implemented as an interrupt routine, driven by a timer of period t_{INT} , the interrupt period. In the circuit above, the ADC reference voltage is the μ C supply ($V_R = V_{CC}$). This assumes that the μ C has CMOS output bits, so that the outputs for negligible current are near the rails:

OUT bit CMOS levels: $\begin{cases} 0 \rightarrow 0 \text{ V (ground)} \\ 1 \rightarrow V_{CC} \end{cases}$

If greater accuracy than V_{CC} is required, instead of driving R directly from OUT, use it to switch accurate analog switches between reference ground (for 0) and an accurate V_R (for 1). If the OUT-bit voltage levels are close enough to the rails, then an accurate V_{CC} can be supplied as the reference.

Σ - Δ RC Constraint for n -Bit Accuracy

The charge-balance voltage waveform on the capacitor is a constant voltage with a small up-down exponential ripple riding on it, at the frequency of the OUT switching. If this varying voltage becomes too large, the ADC will not be linear enough for n -bit conversion. The larger the RC time constant, the smaller the ripple. How large must RC be to ensure n bits of linearity?

The ripple voltage, $\Delta v_C = v_H - v_L \leq V_{LSB} = 2^{-n} \cdot V_R$, and

$$\frac{\Delta v_C}{v_H} = 1 - \frac{v_L}{v_H} = 1 - e^{-t_{INT}/RC}$$

Where, v_H and v_L are the maximum and minimum of v_C . At full-scale, $v_H = V_R$ and

$$2^{-n} \geq 1 - e^{-t_{INT}/RC}$$

or,

$$R \cdot C \geq \frac{t_{INT}}{\ln(1-2^{-n})^{-1}} \cong 2^n \cdot t_{INT}, n \gg 1$$

For $t_{INT} = 1$ ms, and $n = 8$ bits, then $R \cdot C \geq 256$ ms. For $n = 10$, $R \cdot C \geq 1.024$ s. The allowable measurement rate is comparable to DMMs.

Σ - Δ Algorithm

The ADC algorithm, coded as part of the interrupt routine, sets or clears OUT to keep $v_C = v_X$. In other words, charge balance is maintained on C so that $\Delta q = 0$. This can be expressed using $\Delta q = i \cdot \Delta t$, where $i = v/R$:

$$\frac{V_R - v_X}{R} \cdot N_X = \frac{v_X}{R} \cdot (N - N_X)$$

or,

$$\frac{N_X}{N} = \frac{v_X}{V_R},$$

where, N is the number of t_{INT} cycles during the measurement. After N intervals, the measurement ends, and the N_X accumulated during this measurement interval is related to v_X by N and V_R :

$$v_X = \left(\frac{V_R}{N} \right) \cdot N_X$$

N is a software parameter and $V_R = V_{CC}$ of the μC . Each interrupt, the following routine is executed:

If IN = 1: OUT \leftarrow 1; increment N_X
 If IN = 0: OUT \leftarrow 0

At the end of the measurement, after N interrupts (or intervals of t_{INT}), then execute the following routine:

measured $N_X \leftarrow N_X$
 Reset $N_X \leftarrow 0$

Unmatched R_U and R_L

A refinement that can be brought to the minimalist ADC is to account for different resistance values in series with the OUT switches. Let R_U be the series resistance when OUT = 1 (high) and R_L when it is 0 (low).

Then:

$$\frac{V_R - v_X}{R_U} \cdot N_X = \frac{v_X}{R_L} \cdot (N - N_X)$$

Given the two switch resistance values, the measured voltage, as a fraction of the reference voltage is:

$$\frac{v_X}{V_R} = \frac{\left(\frac{R_L}{R_U} \right) \cdot N_X}{N - \left(\frac{R_L}{R_U} - 1 \right) \cdot N_X}$$

This equation presents the onerous μC task of division, despite the pre-calculated constant, R_L/R_U . This refinement is best left for DSPs, which usually facilitate division. As μC s become like DSPs, this improvement becomes feasible to implement.

Auto-Calibration

A more elegant method of producing an accurate measurement without external reference switching can be applied to systems in which multiple channels are multiplexed into the ADC. If two additional MUX inputs are available and the ADC is linear, two-point calibration can be applied. Two reference voltages, which can be 0 V and V_R are applied to the ADC, resulting in $N_X(0 \text{ V}) = N_0$ and $N_X(V_R) = N_R$. A plot of v_X versus N_X will then have two known points on it, corresponding to the known input voltages. The equation for the calibration line is:

$$v_X = \left(\frac{V_R - V_{os}}{N_R - N_0} \right) \cdot N_X + V_{os}$$

where, the expression in parentheses is the slope of the line. In general, the offset voltage, V_{os} , can be of either polarity, requiring negative N_X . To get around this, two precision resistors forming a divider from V_R can provide instead a known accurate voltage of $\alpha \cdot V_R$, where α is the attenuation ratio of the divider. For this more general case, the equation of the line can be written by equating slope expressions:

$$\frac{v_X - \alpha \cdot V_R}{N_X - N_\alpha} = \frac{V_R - \alpha \cdot V_R}{N_R - N_\alpha}$$

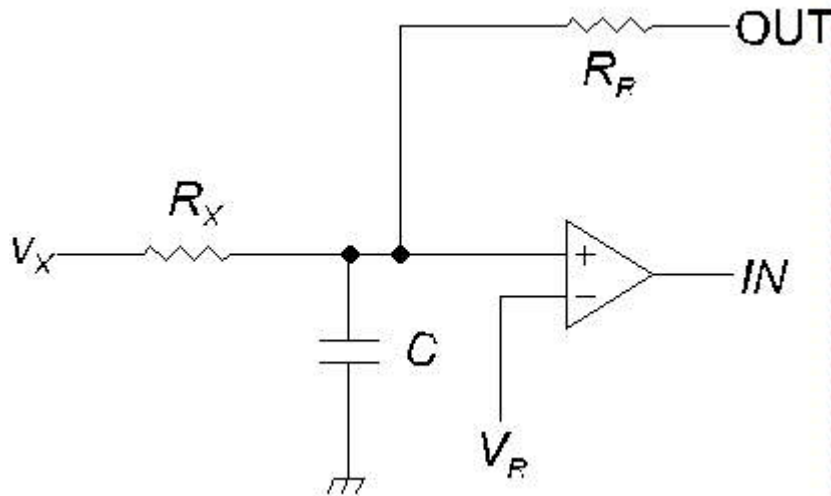
Solving for v_X ,

$$v_X = \left[\left(\frac{N_X - N_\alpha}{N_R - N_\alpha} \right) \cdot (1 - \alpha) + \alpha \right] \cdot V_R = [m \cdot (1 - \alpha) + \alpha] \cdot V_R$$

By making $\alpha = 1/2$, then m must be divided by two, a right-shift instruction. To add $1/2$ to it, increment m before right-shifting. The resulting number is the fraction of V_R that is v_X .

Inverting Σ - Δ ADC

An inverting Σ - Δ converter uses one additional resistor, as shown below.



The RC time constants must still be much greater than t_{INT} , a low OUT is 0 V, and a high level is $V_{CC} = \alpha \cdot V_R$. Charge balance on the capacitor is maintained by the ADC algorithm, keeping $V_C = V_R$. This results in $\Delta Q = 0 \text{ C}$, or:

$$\frac{v_X - V_R}{R_X} \cdot N + \frac{V_{CC} - V_R}{R_R} \cdot N_X = \frac{V_R}{R_R} \cdot (N - N_X)$$

or,

$$\frac{v_X}{V_R} = \frac{R_X}{R_R} \cdot \left(1 - \alpha \cdot \frac{N_X}{N}\right) + 1$$

For $R_X = R_R$, and $\alpha = 2$, then:

$$\frac{v_X}{V_R} = 2 \cdot \left(1 - \frac{N_X}{N}\right)$$

The following chart summarizes the transfer function:

N_X	v_X
0	$2 \cdot V_R = V_{CC}$
$N/2$	V_R
N	0 V

The interrupt routine for the ADC is:

If IN = 1: OUT \leftarrow 0; increment N_X

If IN = 0: OUT \leftarrow 1

At the end of the measurement, after N interrupts (N intervals of t_{INT}), then execute:

measured $N_X \leftarrow N_X$

Reset $N_X \leftarrow 0$

Closure

These minimal-component ADCs are often adequate for slow, low- to medium-precision, μ C-based ADC requirements. Besides few components, other advantages of the Σ - Δ ADC is that it does not need an anti-aliasing filter or a sample & hold circuit preceding its input. Its integrating function reduces noise bandwidth of the measurement. It is an optimal solution for many μ C-based applications.

The inverting ADC input circuit could be extended to have a second-order, cascaded RC filter using the same software routine, with a total of 4 external resistors and 2 capacitors. This adumbration is left to the imagination of the reader. With sufficiently low t_{INT} , which is achievable on faster μ Cs and DSPs, high precision can be attained with a medium-performance comparator.

