ESP8266

Hardware Design Guidelines

Version 2.4

Espressif Systems

About This Guide

This document provides product information of ESP8266EX series, including ESP8266EX chip, ESP-LAUNCHER development board and ESP8266EX modules.

Release Notes

Date	Version	Release Notes
2015.12	V1.3	Initial release.
2016.01	V1.4	Update Section 1.5.2, Section 1.5.3 and Section 1.6.
2016.06	V1.5	Update Section 3.1.
2016.07	V1.6	Update Section 2.1.
2017.01	V2.0	Updated the minimum voltage of ESP8266EX to 2.5V; Updated Table 1-1.
2017.04	V2.1	Updated the chip's output impedance from 50Ω to 39+j6 Ω; Added a note that the size of ESP-LAUNCHER's Flash1 and Flash2 is 32 Mbit; Updated Section 1.4.5.
2017.06	V2.2	Updated Section 1.4.2.
2018.04	V2.3	Updated the name of the document from "ESP8266 System Description" to "ESP8266 Hardware Design Guidelines"; Updated all the figures in the document; Updated Section 1.4 Schematic Checklist; Updated Chapter 3 ESP8266EX Module.
2018.12	V2.4	Updated description in Section 1.4.2 about reset; Updated formatting.

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1. ESP8266EX

1.1. Overview

Espressif's ESP8266EX delivers a highly integrated Wi-Fi SoC solution to meet the continuous demand for efficient power usage, compact design and reliable performance in the industry.

With its complete and self-contained Wi-Fi networking capabilities, ESP8266EX can perform either as a standalone application, or as a slave to a host MCU. When ESP8266EX hosts an application, it promptly boots up from the external flash. The integrated high-speed cache optimizes the system's performance and memory.

Also, ESP8266EX can be applied to any micro-controller design as a Wi-Fi adaptor through SPI/SDIO or I2C/UART interfaces.

Besides the Wi-Fi functionalities, ESP8266EX also integrates an enhanced version of Tensilica's L106 Diamond series 32-bit processor and on-chip SRAM. It can be interfaced with external sensors and other devices through the GPIOs, resulting in low development cost at early stage and minimum footprint. Software Development Kit (SDK) provides sample codes for various applications.

ESP8266EX integrates antenna switches, RF balun, power amplifier, low-noise receive amplifier, filters and power management modules. The compact design minimizes the PCB size and the external circuitry.

ESP8266EX enables sophisticated features, such as:

- Fast switching between sleep and wake-up modes for efficient energy use;
- Adaptive radio biasing for low-power operation;
- Advanced signal processing;
- Spur cancellation;
- Radio co-existence mechanisms for common cellular, Bluetooth, DDR, LVDS, LCD interference mitigation.

Figure 1-1 shows the functional blocks of ESP8266EX.

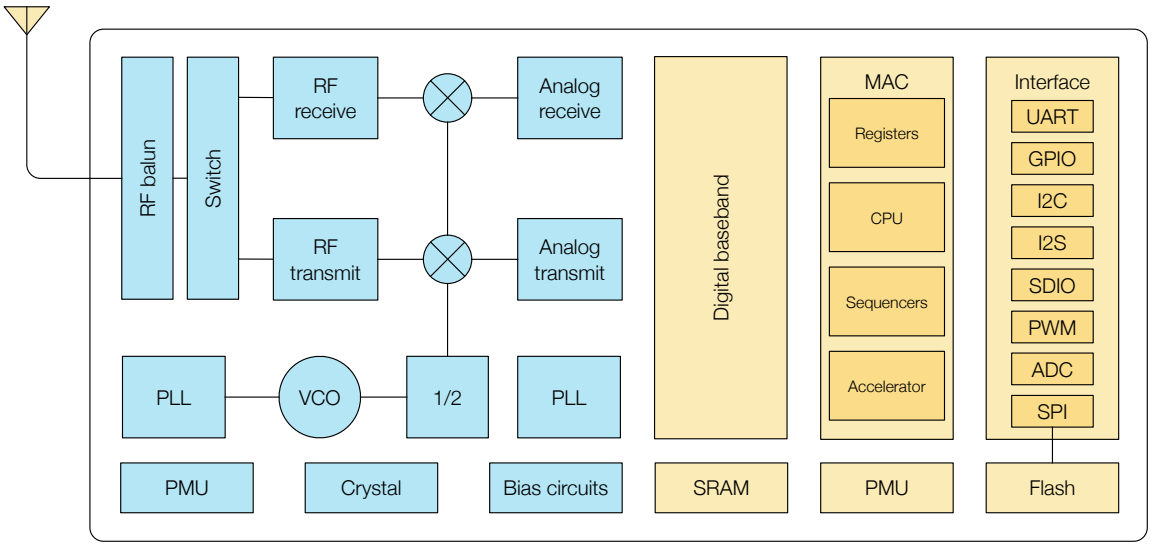

Figure 1-1. ESP8266EX Block Diagram

1.2. Specifications

Table 1-1. ESP8266EX Specifications

Categories	Items	Parameters
Wi-Fi	Standard	FCC/CE/TELEC/SRRC
	Protocols	802.11 b/g/n/e/i
	Frequency Range	2.4G ~ 2.5G (2400M ~ 2483.5M)
	Tx power	802.11 b: +20 dBm
		802.11 g: +17 dBm
		802.11 n: +14 dBm
	Rx Sensitivity	802.11 b: -91 dBm (11 Mbps)
		802.11 g: -75 dBm (54 Mbps)
		802.11 n: -72 dBm (MCS7)
	Antenna	on-board, external, IPEX connector, ceramic chip
Hardware	Peripheral interface	UART/SDIO/SPI/I2C/I2S/IR Remote Control
		GPIO/PWM
	Operating voltage	2.5V ~ 3.6V
	Operating current	Average: 80 mA
	Operating temperature range	-40°C ~ 125°C
	Storage temperature range	-40°C ~ 125°C

Categories	Items	Parameters
	Package size	QFN32-pin (5 mm x 5 mm)
	External interface	N/A
Software	Wi-Fi mode	Station/SoftAP/SoftAP+Station
	Security	WPA/WPA2
	Encryption	WEP/TKIP/AES
	Firmware upgrade	UART Download/OTA (via network)
	Software development	SDK for customized development/cloud server development
	Network Protocols	IPv4, TCP/UDP/HTTP/FTP
	User configuration	AT Instruction Set, Cloud Server, Android/ iOS app

1.3. Pin Definitions

The pin layout for the 32-pin QFN package is illustrated in Figure 1-2.

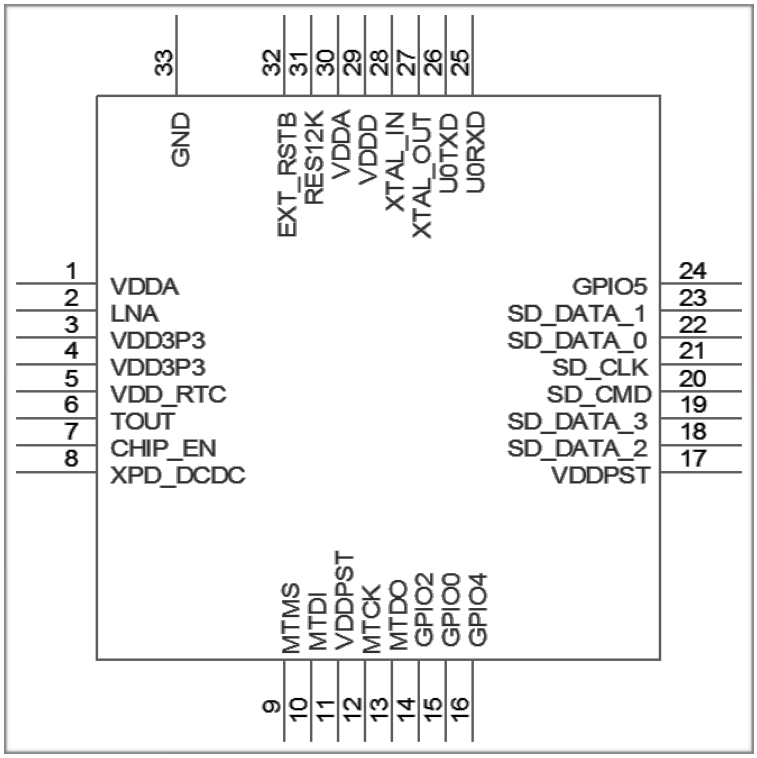

Figure 1-2. ESP8266EX Pin Layout

Table 1-2 lists the definitions and functions of each pin.

Table 1-2. ESP8266EX Pin Definitions

Pin	Name	Type	Function
1	VDDA	P	Analog Power 2.5V ~ 3.6V
2	LNA	I/O	RF antenna interface Chip output impedance=39+j6 Ω. It is suggested that users retain the π-type matching network which matches the antenna.
3	VDD3P3	P	Amplifier Power 2.5V ~ 3.6V
4	VDD3P3	P	Amplifier Power 2.5V ~ 3.6V
5	VDD_RTC	P	NC (1.1V)
6	TOUT	I	ADC pin. It can be used to test the power-supply voltage of VDD3P3 (Pin3 and Pin4) and the input power voltage of TOUT (Pin 6). However, these two functions cannot be used simultaneously.
7	CHIP_EN	I	Chip Enable High: On, chip works properly Low: Off, small current consumed
8	XPD_DCDC	I/O	Deep-sleep wakeup (need to be connected to EXT_RSTB); GPIO16
9	MTMS	I/O	GPIO 14; HSPI_CLK
10	MTDI	I/O	GPIO 12; HSPI_MISO
11	VDDPST	P	Digital/IO Power Supply (1.8V ~ 3.3V)
12	MTCK	I/O	GPIO 13; HSPI_MOSI; UART0_CTS
13	MTDO	I/O	GPIO 15; HSPI_CS; UART0_RTS
14	GPIO2	I/O	UART Tx during flash programming; GPIO2
15	GPIO0	I/O	GPIO0; SPI_CS2
16	GPIO4	I/O	GPIO 4
17	VDDPST	P	Digital/IO Power Supply (1.8V ~ 3.3V)
18	SDIO_DATA_2	I/O	Connects to SD_D2 (Series R: 200Ω); SPIHD; HSPIHD; GPIO 9
19	SDIO_DATA_3	I/O	Connects to SD_D3 (Series R: 200Ω); SPIWP; HSPIWP; GPIO 10
20	SDIO_CMD	I/O	Connects to SD_CMD (Series R: 200Ω); SPI_CS0; GPIO 11
21	SDIO_CLK	I/O	Connects to SD_CLK (Series R: 200Ω); SPI_CLK; GPIO 6
22	SDIO_DATA_0	I/O	Connects to SD_D0 (Series R: 200Ω); SPI_MSIO; GPIO 7
23	SDIO_DATA_1	I/O	Connects to SD_D1 (Series R: 200Ω); SPI_MOSI; GPIO 8

Pin	Name	Type	Function
24	GPIO5	I/O	GPIO 5
25	U0RXD	I/O	UART Rx during flash programming; GPIO 3
26	U0TXD	I/O	UART Tx during flash progamming; GPIO 1; SPI_CS1
27	XTAL_OUT	I/O	Connects to crystal oscillator output, can be used to provide BT clock input
28	XTAL_IN	I/O	Connects to crystal oscillator input
29	VDDD	P	Analog Power 2.5V ~ 3.6V
30	VDDA	P	Analog Power 2.5V ~ 3.6V
31	RES12K	I	Serial connection with a 12 kΩ resistor and connect to the ground
32	EXT_RSTB	I	External reset signal (Low voltage level: Active)

📖 ***Note:***

GPIO2, GPIO0, and MTDO are configurable on PCB as the 3-bit strapping register that determines the booting mode and the SDIO timing mode.

1.4. Schematic Checklist

The highly-integrated design of ESP8266EX reduces the number of components required. Besides ESP8266EX, less than 10 resistors and capacitors, one crystal oscillator and one SPI flash are needed to make a complete module with wireless communication capability.

The following is a detailed description of ESP8266EX schematics, and the layout design which ensures optimum functionality.

The complete circuit diagram of ESP8266EX is illustrated in Figure 1-3.

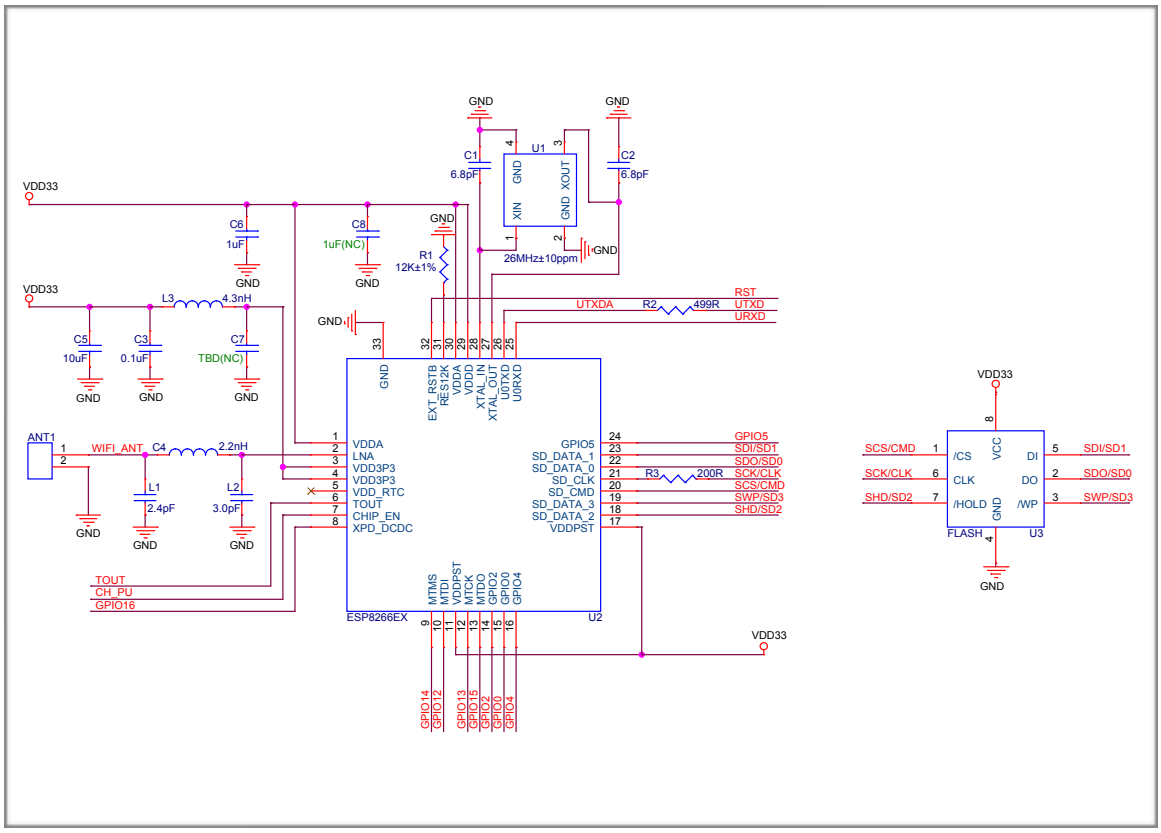

Figure 1-3. ESP8266EX Schematics

The ESP8266EX schematics include seven aspects:

- Power supply
- Power-on sequence and reset
- Flash
- Crystal oscillator
- RF
- External resistor
- UART

1.4.1. Power Supply

1.4.1.1. Digital Power Supply

ESP8266EX has two digital pins for power supply, Pin11 and Pin17. For digital power supply, there is no need to add additional filter capacitors. The operating voltage range of digital power supply pins is 1.8V ~ 3.3V.

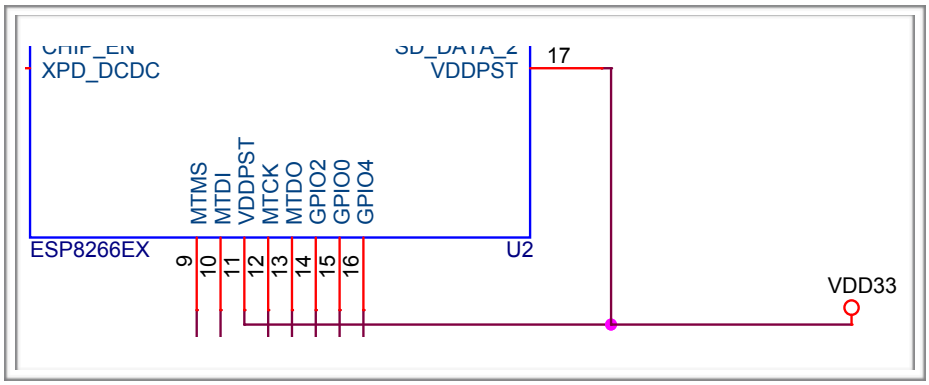

Figure 1-4. ESP8266EX Digital Power Supply Pins

1.4.1.2. Analog Power Supply

ESP8266EX has five analog pins for power supply, including Pin1, Pin3, Pin4 that are the power supply for internal PA and LNA; and Pin29, Pin30 for the internal PLL. The operating voltage for analog power supply pins is 2.5V ~ 3.6V.

Note that the power supply channel might be damaged due to the sudden increase of current when ESP8266EX is transmitting analog signals. Therefore, an additional 10 µF capacitor with a 0603 or 0805 package is needed to match the 0.1 µF capacitor.

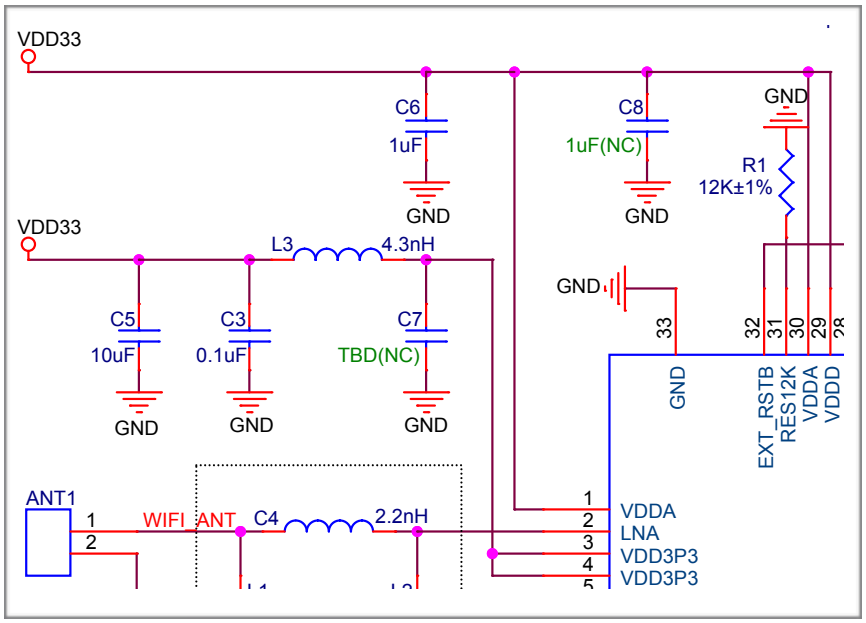

Figure 1-5. ESP8266EX AVDD

📖 **Note:**

- *ESP8266EX's EMC is in conformity with FCC and CE requirements. There is no need to add ferrite beads in the analog power-supply circuit.*
- *When using a single power supply, the recommended output current is 500 mA.*
- *It is suggested that users add an ESD tube at the power entrance.*

1.4.2. Power-on Sequence and Power Reset

1.4.2.1. Power-on Sequence

ESP8266EX uses a 3.3V system power supply. The chip should be activated after the power rails have stabilized. This is achieved by delaying the activation of CH_EN (Pin7) by time T after the 3.3V rails have been brought up. The recommended delay time (T) is given by the parameter of the RC circuit. For reference design, please refer to Figure ESP-WROOM-02 Peripheral Schematics in the *ESP-WROOM-02 Datasheet*.

> ⚠ **Notice:**
>
> *If CHIP_EN is driven by a power management chip, then the power management chip controls the ESP8266EX power state. When the power management chip turns on/off Wi-Fi through the high/low level on GPIO, a pulse current may be generated. To avoid level instability on CHIP_EN, an RC delay (R=10 kΩ, C=100 nF) circuit is required.*

1.4.2.2. Reset

Pin32 EXT_RSTB serves as the reset pin of ESP8266EX. This pin contains an internal pull-up resistor and is active low. To avoid resets caused by external interference, we recommend that you keep the PCB trace of EXT_RSTB as short as possible, and add an RC circuit at the EXT_RSTB pin.

Pin7 CHIP_EN serves as the enable pin of ESP8266EX. In this case, ESP8266EX powers off when this pin is held low. Pin7 CHIP_EN also serves as the reset pin of ESP8266EX. In this case, ESP8266EX reboots when the input level of this pin is below 0.6 V and lasts for at least 200 µs.

We recommend that you use CHIP_EN, instead of EXT_RSTB, to reset the chip.

> ⚠ **Notice:**
>
> *CHIP_EN cannot be left floating.*

1.4.3. Flash

The demo flash used on ESP8266EX is an SPI Flash with 2-MB ROM in an SOP8 (208 mil) package. Pin21 SD_CLK is connected to the flash CLK pin together with a 0402 resistor in serial connection, which reduces the drive current and eliminates external interruption. The initial resistance of the resistor is 200Ω.

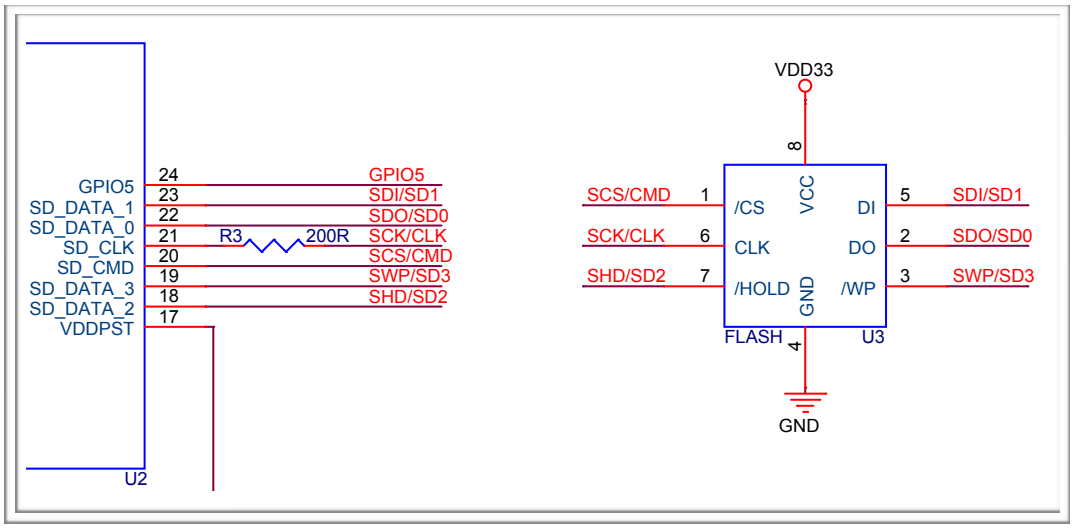

Figure 1-6. ESP8266EX Flash

1.4.4. Crystal Oscillator

ESP8266EX can support 40 MHz, 26 MHz and 24 MHz crystal oscillators. The accuracy of crystal oscillators should be ± 10 PPM, and the operating temperature range should be between -20°C and 85°C.

Please select the right type of crystal oscillator that is used in the ESP Flash Download Tool. In circuit design, capacitors C1 and C2, which are connected to the ground are added to the input and output terminals of the crystal oscillator respectively. The values of the two capacitors can be flexible, ranging from 6 pF to 22 pF. However, the specific capacitive values of C1 and C2 depend on further testing of and adjustment to the overall performance of the whole circuit. The crystal precision should be ±10 PPM.

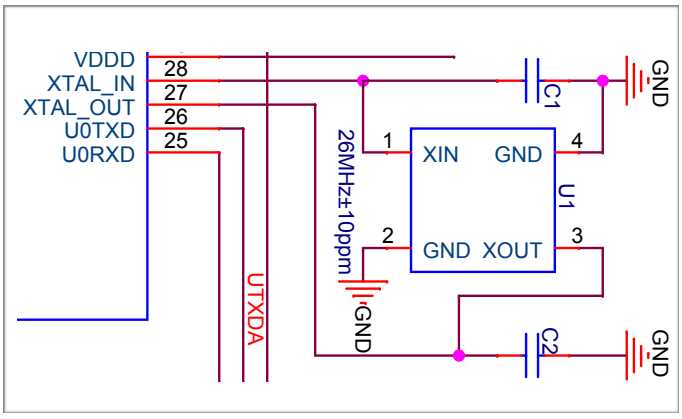

Figure 1-7. ESP8266EX Crystal Oscillator

⚠ Notice:

Defects in the craftsmanship of the crystal oscillators (for example, high frequency deviation and unstable working temperature) may lead to the malfunction of ESP8266EX, resulting in the decrease of overall performance.

1.4.5. RF

The impedance of the ESP8266 PA output end is (39+j6)Ω, so the matched impedance is (39-j6)Ω (from antenna to the chip).

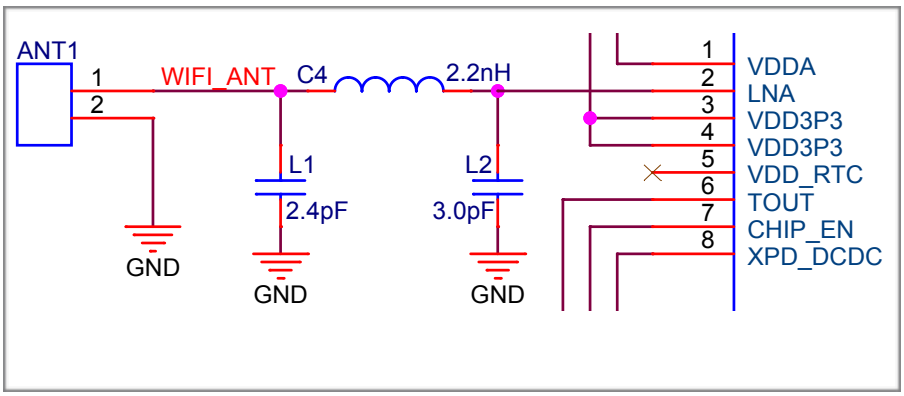

Figure 1-8. ESP8266EX RF

1.4.6. External Resistor 12K

An external ground resistor should be connected o the ERS12K pin (Pin31). The ground resistor requires high accuracy when controlling the bias current. An accuracy of 12K ± 1% is recommended.

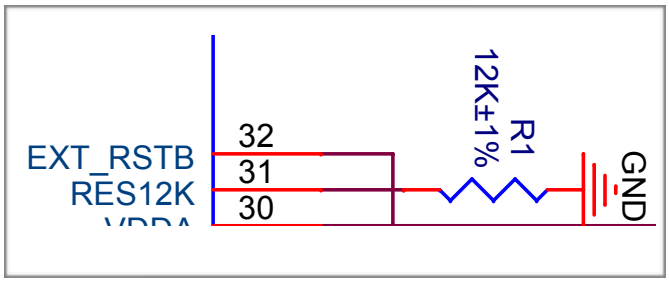

Figure 1-9. ESP8266EX External Resistor

1.4.7. UART

Users need to connect a 499Ω resistor to the U0TXD line in order to suppress the 80 MHz harmonics.

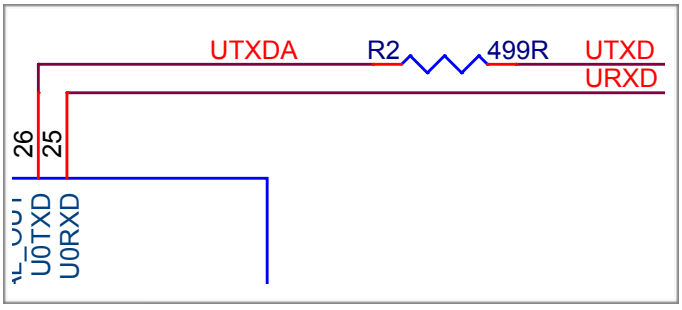

Figure 1-10. ESP8266EX UART

1.5. Slave SDIO/SPI

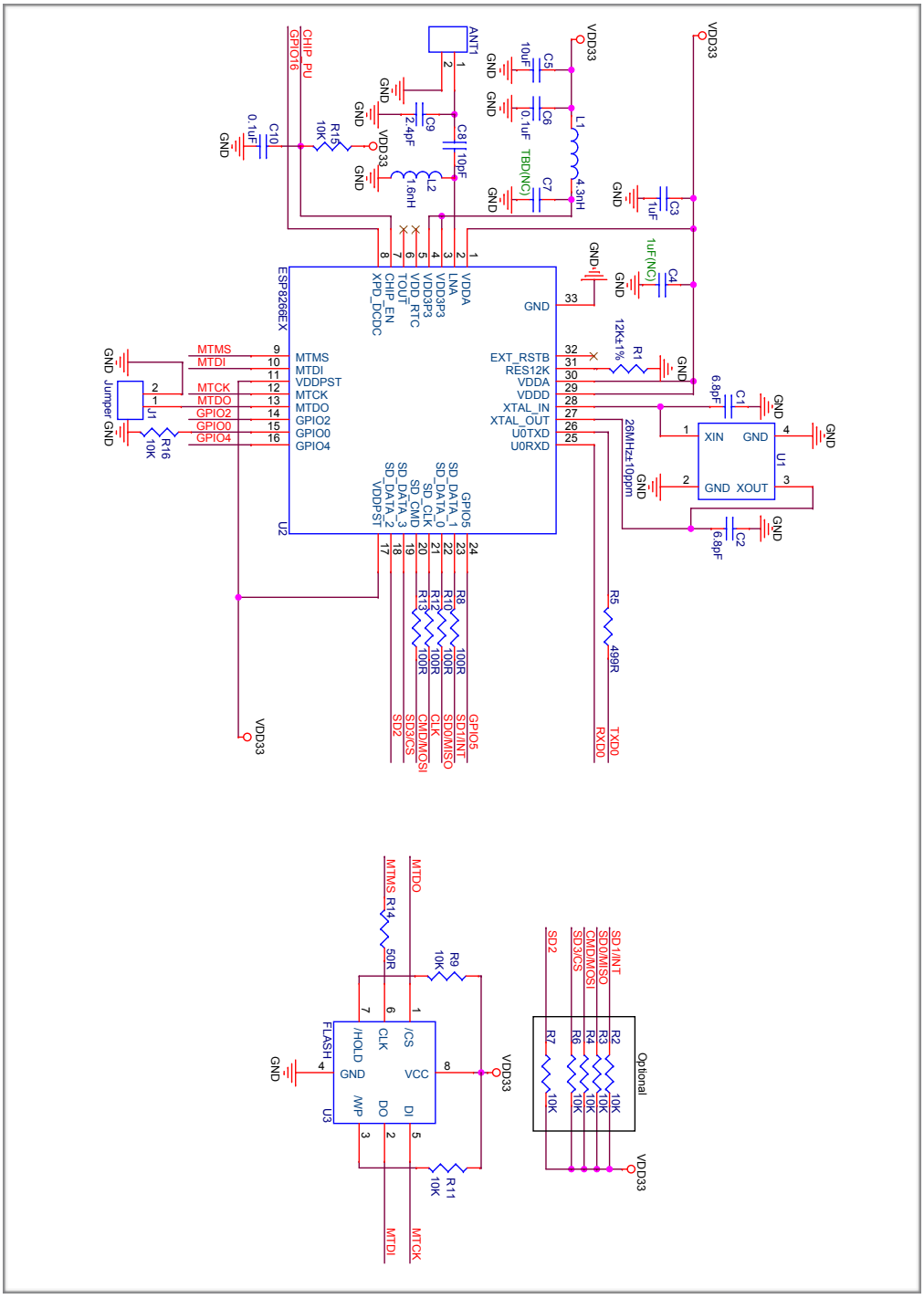

Figure 1-11. Schematics of ESP8266EX as a Slave SDIO

📖 **Note:**

- *Please refer to the design of ESP-WROOM-S2 for further details.*
- *UART Download Mode: Jumper J1 short circuit.*
- *SDIO Boot Mode: Jumper J1 open circuit.*
- *If the external host CPU's SDIO or SPI interface has been pulled up, the optional pull-up resistor can be omitted.*

1.6. PCB Layout Design

The chapter introduces the ESP8266EX PCB layout design by using the ESP8266EX as an example. The PCB layout design guidelines are applicable to cases when

- the ESP8266EX module functions as a standalone device, and when
- the ESP8266EX functions as a salve device.

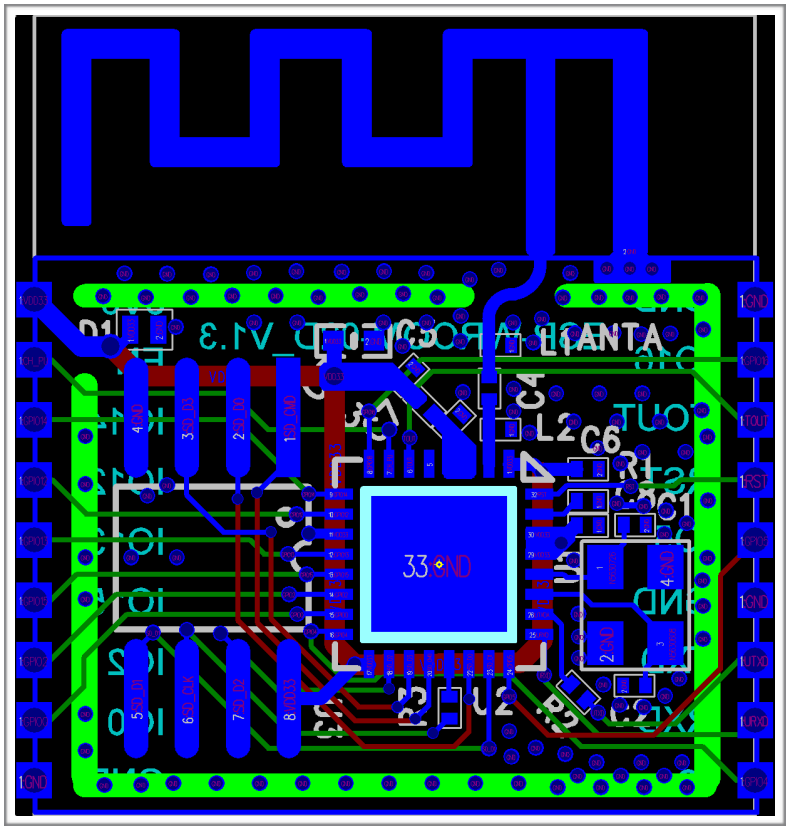

Figure 1-12. ESP8266EX PCB Layout

1.6.1. General Principles of PCB Layout Design

The PCB has four layers:

- The first layer is the TOP layer for signal lines and components.
- The second layer is the GND layer, where no signal lines are laid to ensure a complete GND plane.

- The third layer is the POWER layer where only power lines can be placed. It is acceptable to place some signal lines under unavoidable circumstances.
- The forth layer is the BOTTOM layer. Only signal lines can be laid. Placing components on this layer is not recommended.

Below are the suggestions for a two-layer PCB design.

- The first layer is the TOP layer for signal traces and components.
- The second layer is the BOTTOM layer, where power traces are routed. Placing any components on this layer is not recommended. Do not route any power or signal traces under or around the RF and crystal oscillator, and so that there is a complete GND plane, which is connected to the Ground Pad at the bottom of the chip.

1.6.2. Positioning a ESP32 Module on a Base Board

If users adopt on-board design, they should pay attention to the layout of the module on the base board. The interference of the base board on the module's antenna performance should be reduced as much as possible.

It is recommended that the PCB antenna area of the module be placed outside the base board while the module be put as close as possible to the edge of the base board so that the feed point of the antenna is closest to the board.

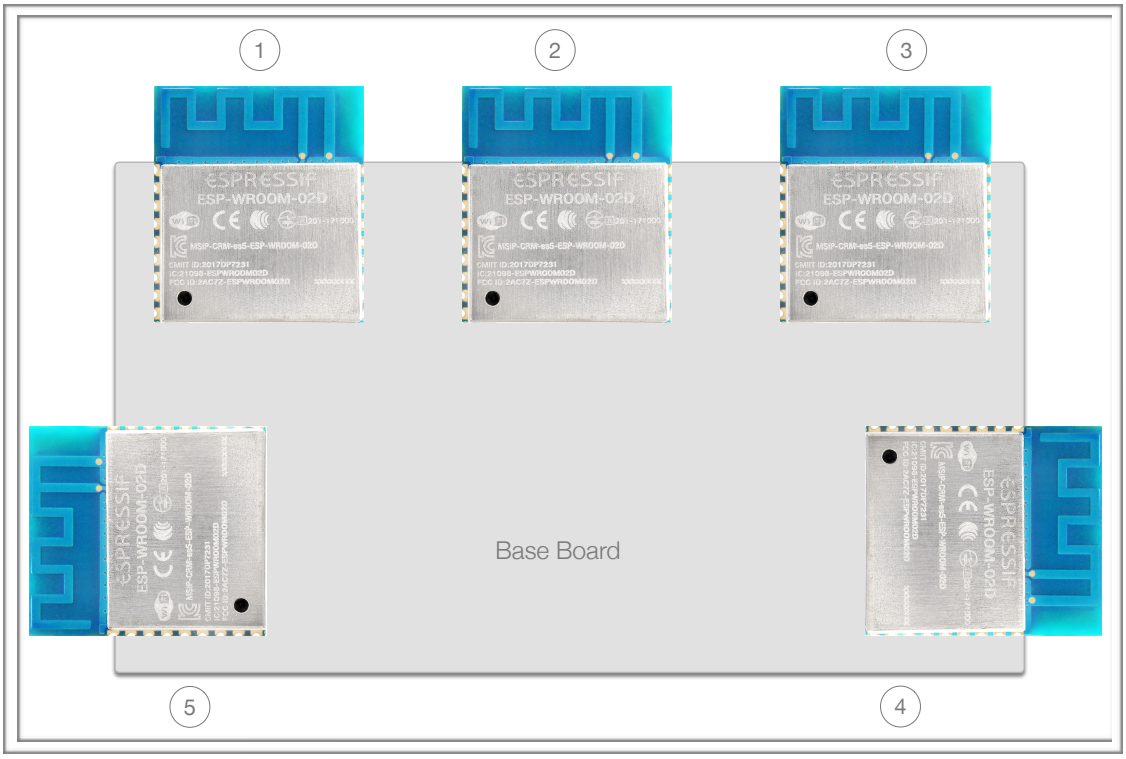

Figure 1-13. ESP32 Module Antenna Position on Base Board

> 📖 **Note:**
>
> *As is shown in Figure 1-13, the recommended position of ESP32 module on the base board should be:*
>
> - *Position 3: Highly recommended;*
> - *Position 4: Recommended;*
> - *Position 1, 2, 5: Not recommended.*

If the positions recommended are not suitable, please make sure that the module is not covered by any metal shell. The antenna area of the module and the area 15 mm outside the antenna should be kept clean, (namely no copper, routing, components on it) as shown in Figure 1-14:

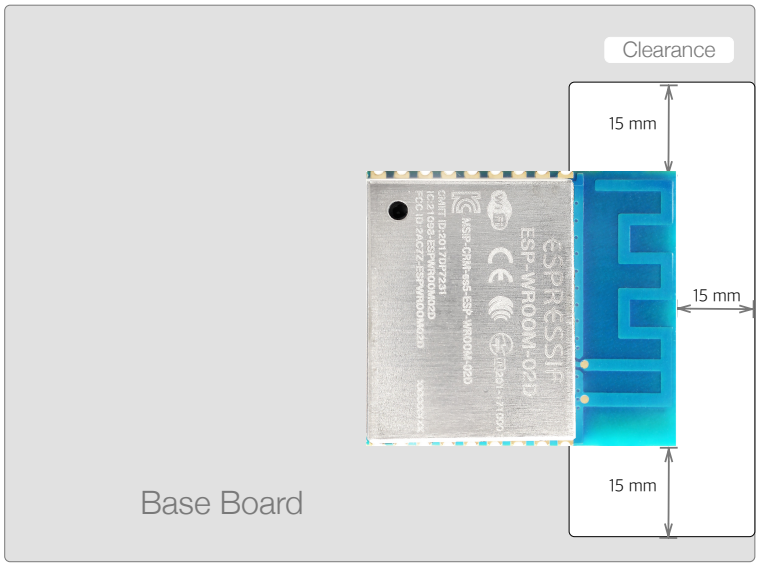

Figure 1-14. Keepout Zone for ESP8266 Module's Antenna on the Base Board

1.6.3. Standalone ESP8266EX Module

1.6.3.1. Power Supply Design

The 3.3V power lines are highlighted in yellow in Figure 1-15. The width of the power lines should be greater than 15 mil.

Before power traces reach the analog power-supply pins (Pin1、3、4、28、29), a 10 μF capacitor is required, which can work in conjunction with the 0.1 μF capacitor. A C circuit and an L circuit should be added to the power supplies of Pin3 and Pin4. As Figure 1-15 shows, C5 (10 μF capacitor) is placed by the 3.3V stamp hole; C7, L3 and C7 are placed as close as possible to the analog power-supply pin. Note that all decoupling capacitors should be placed close to the power pin, and ground vias should be added adjacent to the ground pin for the decoupling capacitors to ensure a short return path.

Power lines should be placed on the third layer. When the power lines reach the pins of the chipset, vias are needed so that the power lines can go through the layers and connect to the pins of the chipset on the TOP layer. The diameter of the via holes should exceed the

width of the power lines and the diameter of the drill should be 1.5 times that of the radius of the vias.

The center ground pad at the bottom of the chip should be connected to ground plane through at least 9 ground vias.

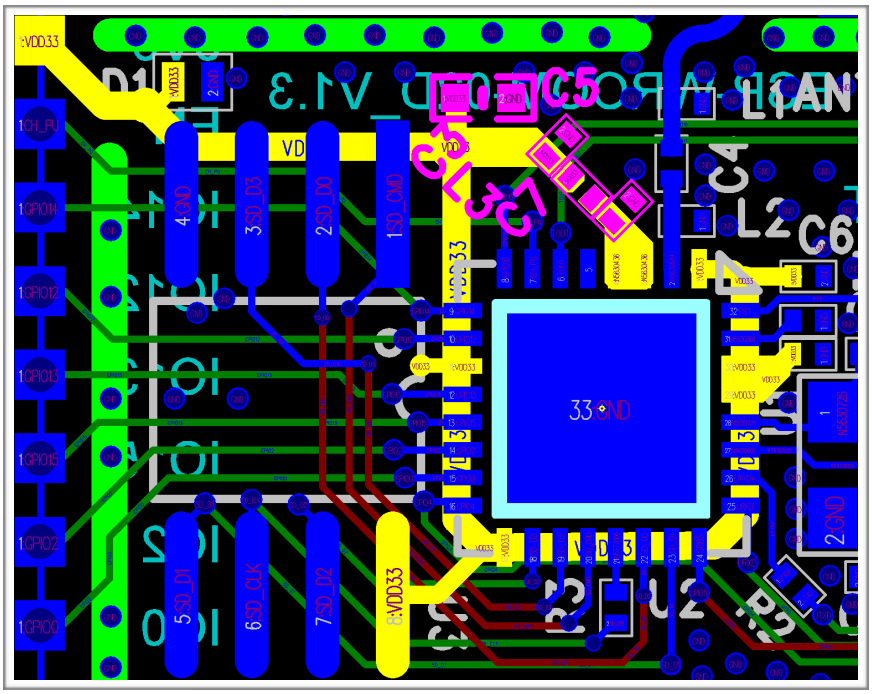

Figure 1-15. ESP8266EX PCB Layout

1.6.3.2. Crystal Oscillator Design

The crystal oscillator should be placed as close to the XTAL pins as possible (without the traces being too long). However, the crystal cannot be placed too close to the chip to prevent the crystal from interfering with the chip, as Figure 1-15 shows. The recommended distance is 0.8 mm (see Figure 1-16). However, the crystal cannot be too close to the chip to prevent the crystal from interfering with the chip. The recommended distance is 0.8mm (see Figure 1-16). It is good practice to use via stitching around the clock trace for low ground-plane impedance.

There should be no vias on the input and output traces, which means the traces cannot cross layers. In addition, the input and output traces should not be routed over one another, not even on different layers.

Place the input and output bypass capacitors on the near left or right side of the chip. Do not place them on the traces.

Do not route high-frequency digital signal lines under the crystal oscillator. It is best not to route any signal line under the crystal oscillator. The larger the copper area on the top layer is, the better. As the crystal oscillator is a sensitive component, do not place any magnetic components nearby that may cause interference, for example, power-switching converter components or unshielded inductors.

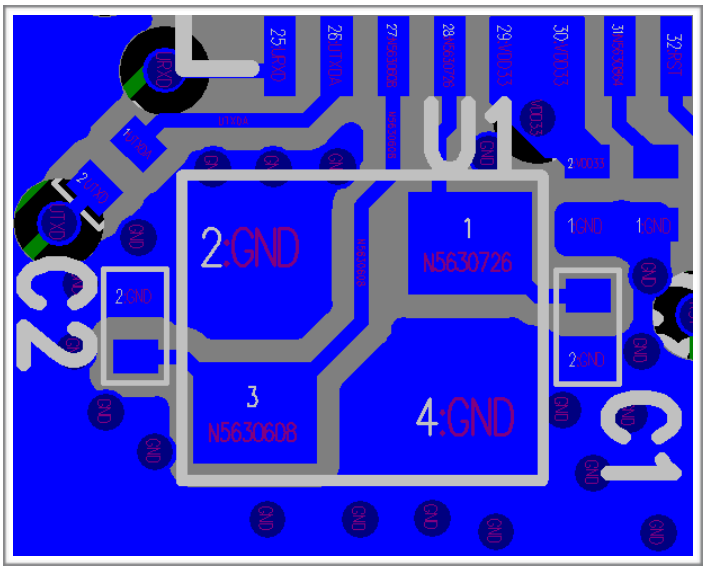

Figure 1-16. ESP8266EX Crystal Oscillators

1.6.3.3. RF Design

The characteristic RF impedance is 50Ω. The ground plane should be complete. The RF trace should be as short as possible with dense ground via stitching around it for isolation. The width of RF lines should be as short as possible and there should be dense vias stitched around.

π-type matching circuitry should be reserved on the RF trace and placed close to the RF Pin2. The components of the π-matching network should be placed in the same direction (see Figure 1-17).

There should be no vias for the RF trace. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.

There should be no RF routing around the high-frequency signal lines.

The RF antenna should be set away from high-frequency transmitting devices, such as crystal oscillators, DDR, and certain high frequency clocks (SDIO_CLK, etc.). Besides, the USB ports, USB-to-UART signal chips, UART signal lines (including traces, vias, test points, headers, etc.) must be placed as far away from the antenna as possible. The UART signal line is packaged and ground shielding is added.

For PCB onboard antenna design please refer to Type-A version by Espressif. If there are power traces near the antenna, the power traces and antenna must be isolated with GND copper.

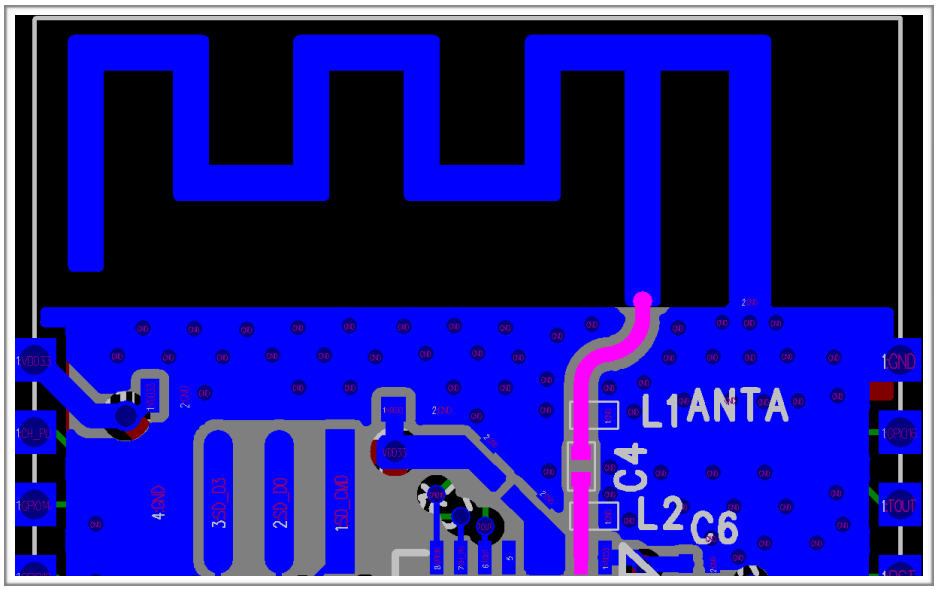

Figure 1-17. ESP8266EX RF Design

1.6.4. ESP8266EX as a Slave Device

When ESP8266EX works as a slave device in a system, users need to pay more attention to signal integrity in the PCB design. It is important to keep ESP38266EX away from the interferences caused by the complexity of the system and an increased number of high-frequency signals. We use the mainboard of a PAD or TV Box as an example here to provide guidelines for the PCB layout and design.

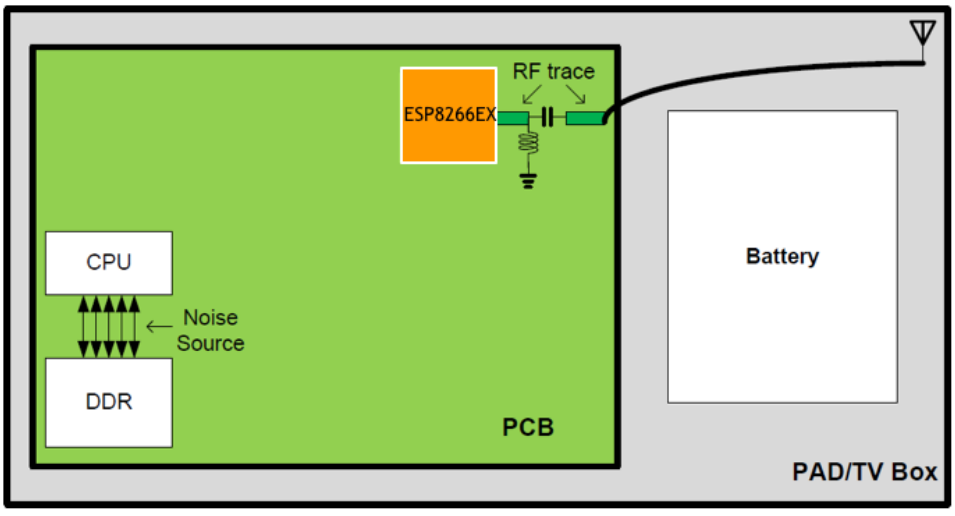

Figure 1-14. PCB/TV Box Layout

The digital signal between the CPU and the DDR is the major producer of high-frequency noise and interferes with Wi-Fi radio from the air. Below are the key points when designing the PCB layout:

- As shown in Figure 1-14, ESP8266EX should be placed near the edge of the PCB and away from the CPU and DDR, the main high-frequency noise sources. The

distance between the chip and the noise sources decreases the interference and reduces the coupled noise.

- It is suggested that a 100Ω~200Ω series resistor is added to the six signal traces when ESP8266EX communicates with the CPU via SDIO to decrease the drive current and any interferences, and also to eliminate the sequencing problem caused by the inconsistent length of the SDIO traces.
- On-board PCB antenna is not recommended, as it receives much interference and coupling noise, both of which impact the RF performance. We suggest that you use an external antenna which should be directed away from the PCB board via a cable, in order to weaken the high frequency interference with Wi-Fi.
- The high-frequency signal traces between the CPU and associated memory should be routed strictly ac- cording to the routing guidelines (please refer to the DDR trace routing guidelines). CLK and data/addr lines should be laid underground.
- The GND of the Wi-Fi circuit and that of other high-power devices should be separated and connected through wires if there are high-power components, such as motors, in the design.
- The antenna should be kept away from high-frequency noise sources, such as LCD, HDMI, Camera Sensor, USB, etc.

1.6.5. Typical Layout Problems and Solutions

- **Q: The current ripple is not large, but the Tx performance of RF is rather poor.**

Analysis:

Ripple has a strong impact on the performance of RF Tx. It should be noted that ripple must be tested when ESP8266EX is in the normal working mode. The ripple increases when the power gets high. Generally, the ripple should be <80 mV when sending 11n MCS7 packets, and <120 mV when sending 11b packets.

Solution:

Add a 10-µF filter capacitor to the branch of source circuit (ESP8266EX AVDD pin). The 10-µF capacitor should be adjacent to the VDDA pin.

- **Q: The power ripple is small, but the Tx performance is poor.**

Analysis:

The RF Tx performance can be affected not only by power ripples, but also by the crystal oscillator itself. Poor quality and big frequency offsets (more than ±40 ppm) of the crystal oscillator decrease the RF Tx performance. The crystal oscillator clock may be corrupted by other interfering signals, such as high-speed output or input signals. Besides, sensitive components or radiation components, such as inductors and antennas, may also decrease the RF performance.

Solution:

This problem is caused by improper layout and can be solved by re-layout. See Section 1.5 for details.

- **Q: When ESP8266EX sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.**

Analysis:

The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna.

Solution:

Match the antenna's impedance with the reserved π-type circuit on the RF trace, so that the resistance from the RF pin to the antenna approaches (39-j6)Ω.

- **Q: TX performance is not bad, but the Rx sensitivity is low.**

Analysis:

Good Tx performance indicates proper RF impedance matching. External coupling to the antenna can affect the Rx performance. For instance, the crystal oscillator signal harmonics could couple to the antenna. If ESP8266EX serves as slave device, there will be other high-frequency interference sources on the board, which may affect the Rx performance.

Solution:

Keep the antenna away from crystal oscillators. Do not route high-frequency signal traces close to the RF trace.

1.7. PCB Layout Design

1.7.1. UART to Wi-Fi Smart Device

The two UART interfaces are defined in Table 1-3.

Table 1-3. Pin definitions of UART Interfaces

Category	Pin definition	Function
UART0	(Pin 25) U0RXD+ (Pin 26) U0TXD	Receive and transmit user's data packages.
UART1	(Pin 14) GPIO2 (U1TXD)	Print information.

AT instruction and examples are provided here: *http://www.espressif.com/en/support/download/documents?keys=&field_type_tid%5B%5D=14*

Application example: ESP8266EX development board (please see Chapter 2).

1.7.2. Sensor

ESP8266EX can be used for developing sensor products by using the I2C interface. The

I2C works in the master mode and can connect to multiple sensors. The slave devices are identified through the addressing mode, as each slave device has a unique address.

The sensor products send real-time data to ESP8266EX via the I2C interface, and ESP8266EX uploads the data to the server wirelessly. Users can acquire information from the server through the mobile app when their mobile phones connect to the internet.

1.7.3. Smart Light

ESP8266EX can be used for developing such smart home products as smart light by using the PWM and infrared interfaces. The three PWM interfaces control red, blue, and green LEDs respectively. The minimal PWM duty ratio is 1/214. In addition, the infrared interface allows specific control on LEDs, such as reset, power on/off, color switch, etc.

1.7.4. Smart Plug

ESP8266EX can be used for developing smart plug products. The GPIOs control the power switch through the high/low-level switch and connection/disconnection of relay. A smart plug requires three modules: 220V to 3.3V power conversion module, ESP8266EX Wi-Fi module and relay control module.

2. ESP-LAUNCHER

2.1. Overview

Espressif provides ESP8266EX development board—ESP-LAUNCHER for quick configuration and further development. The size of the board is 46 mm x 78.5 mm (see Figure 2-1).

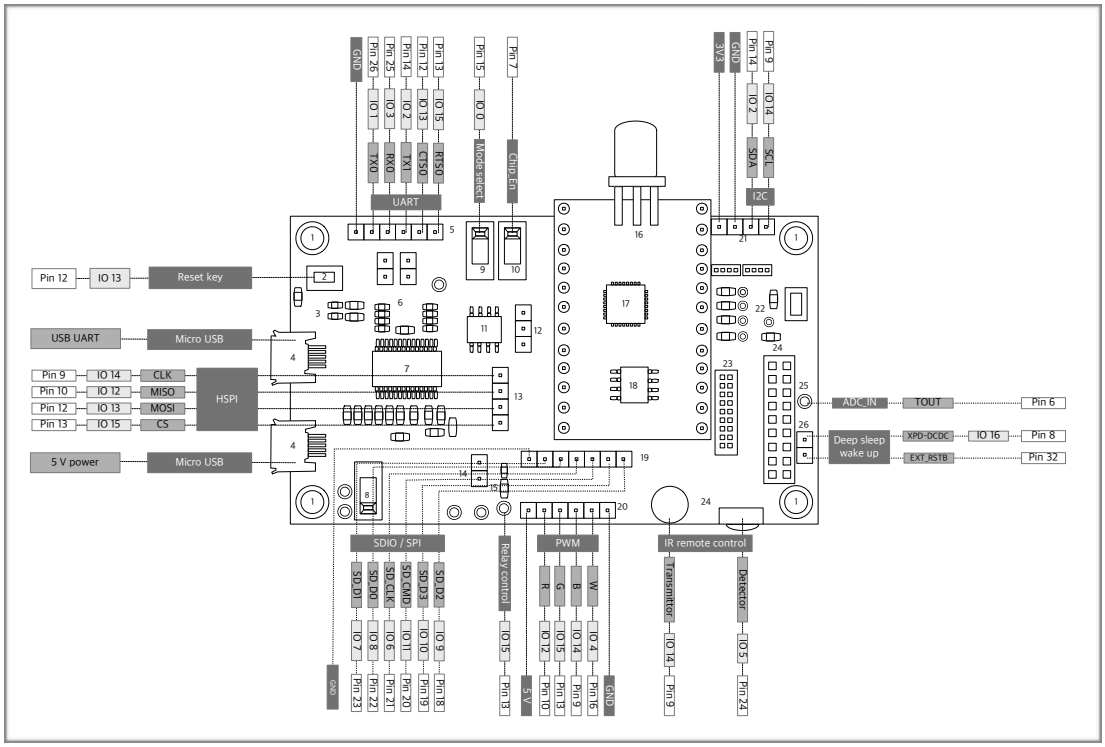

Figure 2-1. ESP-LAUNCHER

1	Chip positioning hole	8	5V power switch	15	Relay control	22	Undefined LED and buttons
2	Reset Button	9	IO0 control	16	SMA ANT	23	1.27 mm pin header
3	Wi-Fi LED, Link LED	10	CH_EN switch	17	Test board	24	2.0 mm pin header
4	Micro USB: USB-UART, 5V power	11	Flash2: HSPI	18	Flash1: SPI	25	ADC_IN
5	UART	12	CS of Flash2	19	SDIO/SPI	26	Deep-sleep wakeup
6	UART SWAP	13	HSPI	20	IR_T, IR_R		
7	USB-UART chip	14	3.3 V power	21	I2C		

2.2. Modules and Interfaces

ESP-LAUNCHER can be configured through USB serial or Wi-Fi connection. The modules/ interfaces integrated on the development board are described in Table 2-1 and 2-2.

Table 2-1. ESP-LAUNCHER Module Description

Module	Functional description
Micro USB interface	There are two USB interfaces. Both can be used as a 5V power supply or for serial communication (2-1-4).
Power supply	The USB interface provides 5V power supply which can be converted to 3.3V through a DC-to-DC converter. An LED light indicates the power, and a header pin is used for testing the power current.
Slide switch	Three slide switches are used for the 5V power supply (2-1-8), GPIO0 voltage level switch (2-1-9) and chip enable pin CH_EN (2-1-10), respectively. When the switches are toggled to the outer side, the voltage level is high, while when the switches are toggled to the inner side, the voltage level is low. • For the 5V power switch: - Toggled to the inner side, the board is powered on; - Toggled to the outer side, the board is powered off. • For the GPIO0 Control: - Toggle to the inner side, the UART download mode is enabled and users can download firmware with ESP Flash Download Tool; - Toggle to the outer side, the Flash boot mode is enabled and the UART debug tool can be used for debugging.
Reset Key	SW1 is connected to MTCK (GPIO13) for application reset and clearing the Wi-Fi configuration (2-1-2). SW2 is not defined (2-1-22).
Indicator light	• Red light (D2) indicates Wi-Fi work status (2-1-3). • Blue (D3) indicates communication with server (2-1-3) • Green light (D1) indicates relay switch control (2-1-15) • Blue light (D11) and red light (D10) indicate Rx and Tx work status, respectively (2-1-7) • Red light (D12) indicates a 5V power supply (2-1-8) • D4/13/14/16 are not defined (2-1-22).
Jumper	• J82: It needs to be shorted by a jumper, so that the 3.3V power supply can be channeled into other circuits. It can also be used to test the power current (2-1-14). • J3: CS of HSPI flash. HSPI flash is disabled when the two upper pins are shorted by a jumper. HSPI flash is enabled when the two lower pins are shorted by a jumper (2-1-12). • J14 and J67: Short-circuit J14 to connect GPIO13 to U0CTS. Short-circuit J67 to connect GPIO15 to U0RTS (2-1-6). • J77: Short-circuit J77 to connect GPIO16 to EXT_RSTB for Deep-sleep wake up (2-1-26).
Interfaces	UART, HSPI, SDIO/SPI, I2C, ADC_IN, GPIO16, relay control, PWM and IR TX/RX
Flash	• 32-Mbit Flash1 (mounted on the test board): Flash1 is connected to the chip via the SPI interface. Currently, Flash1 is used when the chip is working in the Wi-Fi standalone mode. R9 and R85 can be used for the CS of Flash1. By default, Flash1 is enabled (2-1-18). • 32-Mbit Flash2 (mounted on the baseboard): Flash2 is connected to the chip via the HSPI interface. HSPI is used in SIP mode. For the ESP-LAUNCHER, when ESP8266EX works as a slave device, it connects to the host MCU via the SPI interface that is defined in SDIO specifications. HSPI is connected to Flash2. J3 can be used for the CS of Flash2 (2-1-11).

Module	Functional description
Test modules	There are multiple modules that can be connected to the ESP-LAUNCHER for testing and development, through the 1.27mm double-row pin headers (2-1-23) and 2.00 mm double-row pin headers (2-1-24). Please note that module pins should be connected to their corresponding pins on the board. Besides, only one module at a time can be used.

Table 2-2 lists the function description of ESP-LAUNCHER.

Table 2-2: ESP-LAUNCHER interfaces

Interfaces	Function description
HSPI	It can interface SPI flash (Flash2), display screen, MCU, etc (2-1-13).
SDIO/SPI	It can interface flash, host MCU, display screen, etc (2-1-19).
PWM	Currently the PWM interface has four channels, and users can extend the channels as needed. The PWM interface can be used to control LED lights, buzzers, relays, motors, etc (2-1-20).
IR	The functionality of the infrared remote control interface can be implemented via software programming. NEC coding, modulation and demodulation are used by this interface. The frequency of the modulated carrier signal is 38 KHz (2-1-24).
ADC	The interface is used to test the power supply voltage of VDD3P3 (pin3 and pin4), as well as the input voltage of TOUT (pin6). It can also be used in sensors (2-1-25).
I2C	It can interface sensors and display screens with 2.54 mm or 1.27 mm pin headers (2-1-21).
UART	UART0: U0TXD, U0RXD, MTDO (U0RTS), MTCK (U0CTS) UART1: GPIO2 (U1TXD) It can interface other UARTdevices (2-1-5).
	• For firmware downloading: U0TXD+U0RXD or GPIO2+U0RXD • For communication: UART0: U0TXD, U0RXD, MTDO(U0RTS), MTCK(U0CTS) • For debugging: UART1_TXD (GPIO2) can be used to print debugging information.
	By default, UART0 will output some printed information when the device is powered on. For the applications that are sensitive to this feature, users can exchange the pins of UART during system initialization, that is, exchange U0TXD, U0RXD with U0RTS, U0CTS. R1/3/5/7 should not be mounted with other components, while R2/4/6/8 can be mounted with other components. J14 and J67 should be shorted.
Relay control terminal	It is used to control, with an indicator light, the on-and-off switch of the relay in a smart plug application (2-1-15).

To use the SDIO/SPI interfaces on ESP-LAUNCHER, please follow the steps below:

1. Move the 0R at R85 to R9, and then disable the flash on the ESP_Test Board;
2. Short-circuit the two lower pins on J3 with a jumper to enable HSPI flash;
3. Remove C8 (next to the Reset key on the left of the PCB);

4. Remove R58 on the PCB and disconnect GPIO14 with the infrared transmitting tube;
5. Remove the pull-down resistor R29 of MTDO/IO15 (next to J11);
6. When downloading firmware, pull the IO15/CS at J11 to low level and toggle the switch of GPIO0 inwards to enable UART Download mode;
7. When downloading is completed, release IO15/CS to enable SDIO Boot mode;
8. Connect SDIO/SPI at J5 to host for communication.

2.3. Schematics

2.3.1. Interfaces

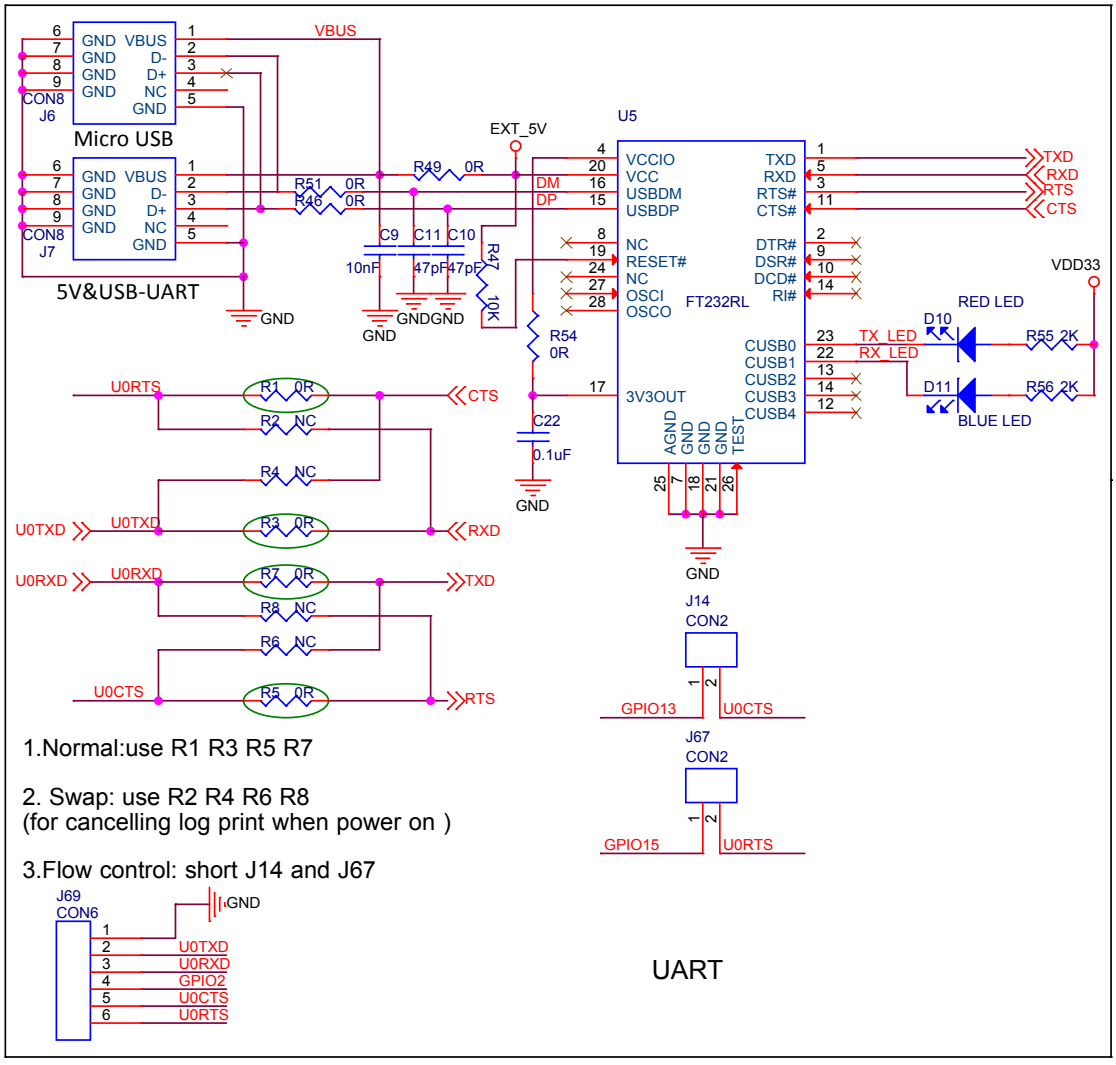

Figure 2-2. ESP-LAUNCHER Interface

2.3.2. 5V Power Supply

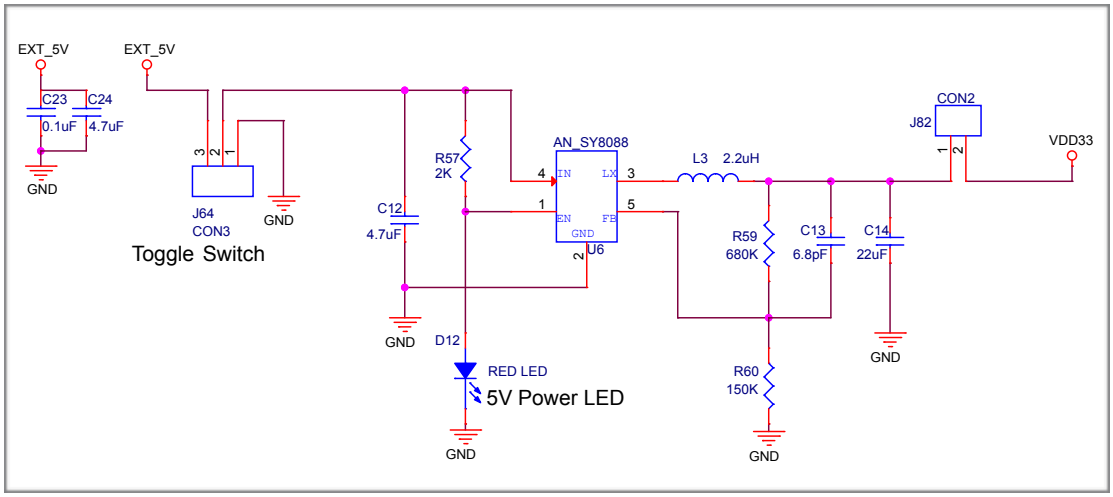

Figure 2-3. ESP-LAUNCHER 5V Power Supply Schematics

2.3.3. Test Module

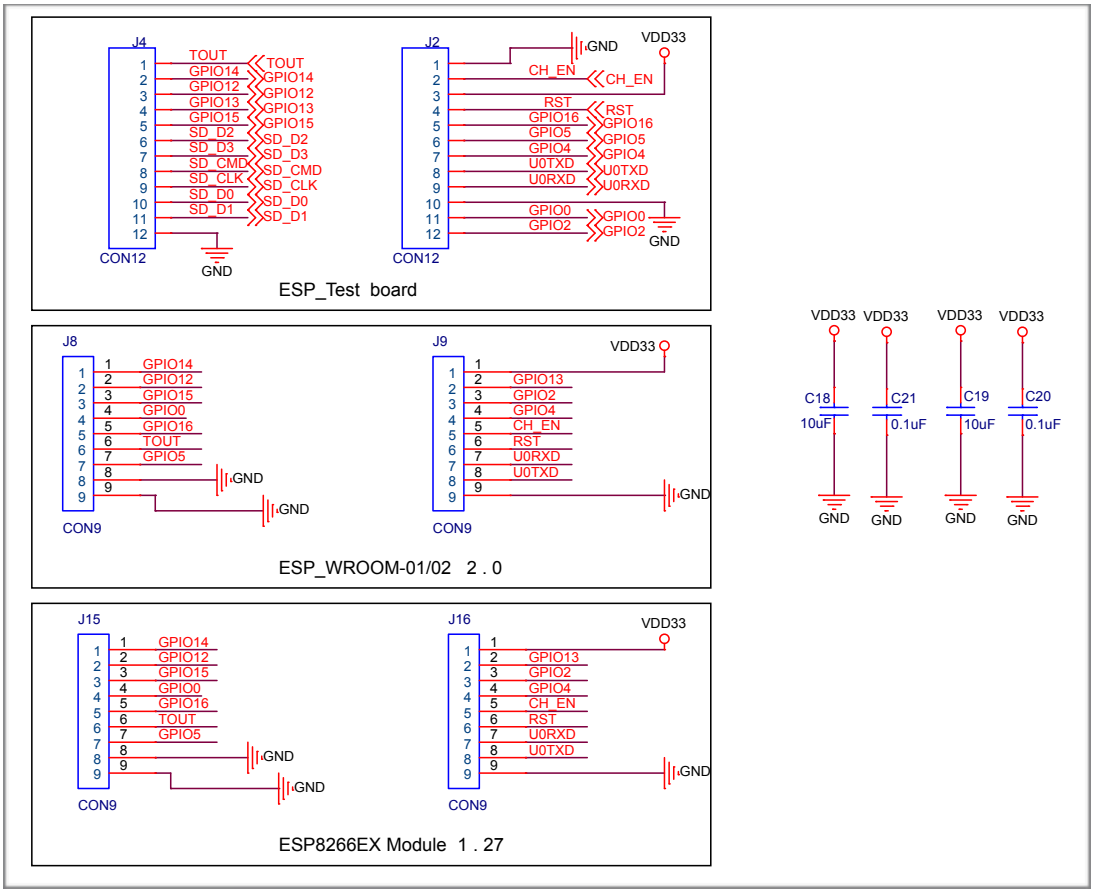

Figure 2-4. ESP-LAUNCHER Test Module Schematics

2.4. Test Board

A test board is embedded in ESP-LAUNCHER, as shown in Figure 2-5. The external size of the test board is 20 mm x 31 mm. A 2-dBi SMA antenna or other testing equipment can be connected to the test board via the SMA antenna connector. The 2.54 mm pin headers makes test and development easy and convenient when using a breadboard.

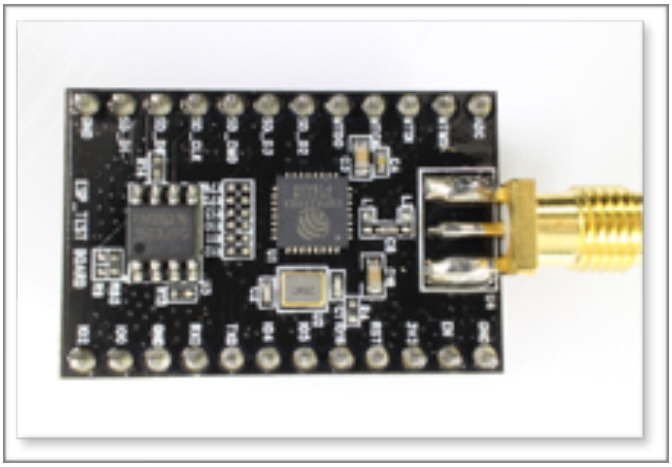

Figure 2-5. ESP-LAUNCHER Test Board

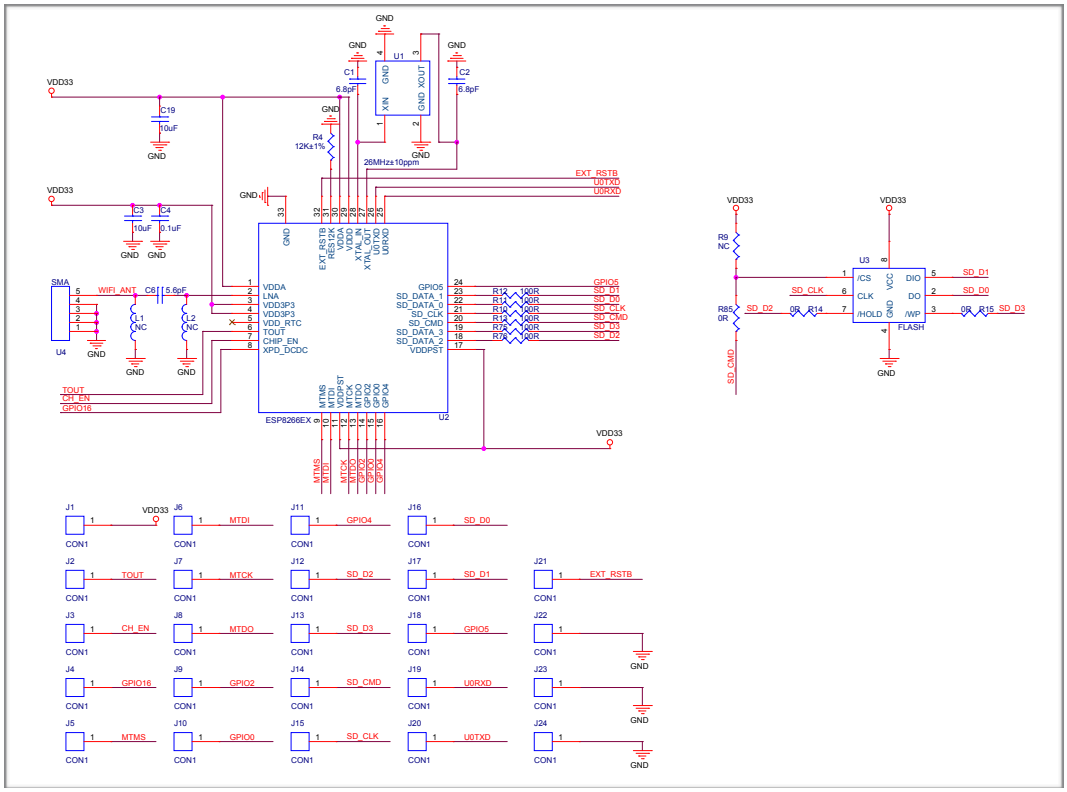

Figure 2-6. ESP-LAUNCHER Test Board Schematics

3. ESP8266EX Module

Espressif provides two types of modules, the SMD module (ESP-WROOM-02) and the DIP module (ESP-WROOM-01). The modules have been improved to achieve the optimum RF functionality. It is recommended that users use these modules for testing or further development.

3.1. ESP-WROOM-S2

The module size is 16±0.2 mm x 23±0.2 mm x 3±0.15 mm (see Figure 1-1). The flash used on this module is a 2-MB SPI flash connected to HSPI, with a package size of SOP 8-150 mil. The gain of the on-board PCB antenna is 2 dBi.

The ESP-WROOM-S2 works as the SDIO/SPI slave with the SPI speed of up to 8 Mbps.

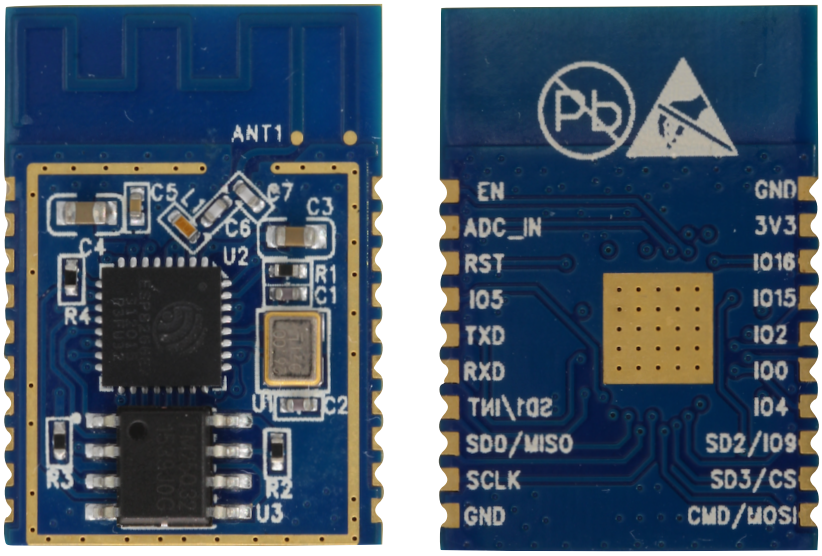

Figure 3-1. ESP-WROOM-S2 Module

For details of ESP-WROOM-S2, please refer to *ESP-WROOM-S2 Datasheet*.

3.2. ESP-WROOM-02

The module size is (18±0.2) mm x (20±0.2) mm x (3±0.15) mm. The type of flash used on this module is an SPI flash with a package size of SOP 8-150 mil. The gain of the on-board PCB antenna is 2 dBi.

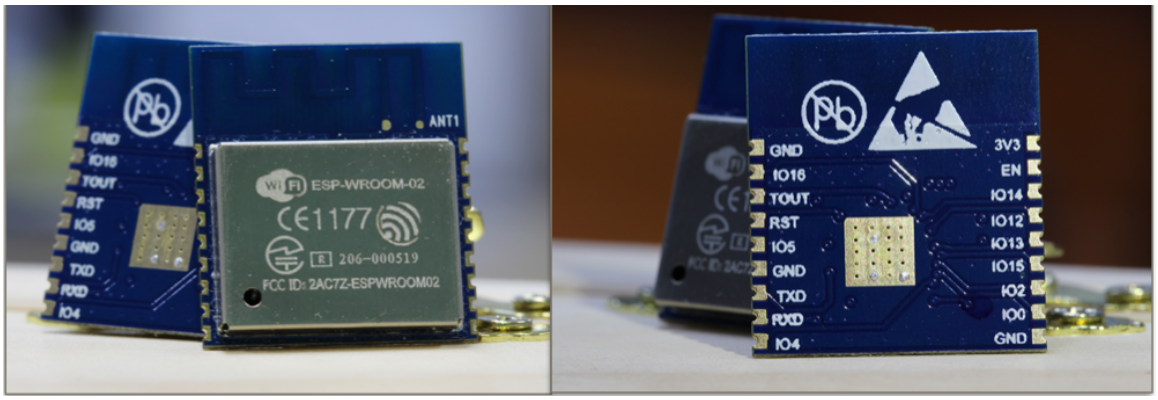

Figure 3-2. ESP-WROOM-02 Module

For details of ESP-WROOM-S2, please refer to *ESP-WROOM-02 Datasheet*.

3.3. ESP-WROOM-02D/ESP-WROOM-02U

The module size of ESP-WROOM-02D is (18±0.2) mm x (20±0.2) mm x (3±0.15) mm. The type of flash used on this module is an SPI flash with a package size of SOP 8-150 mil. The gain of the on-board PCB antenna is 3 dBi.

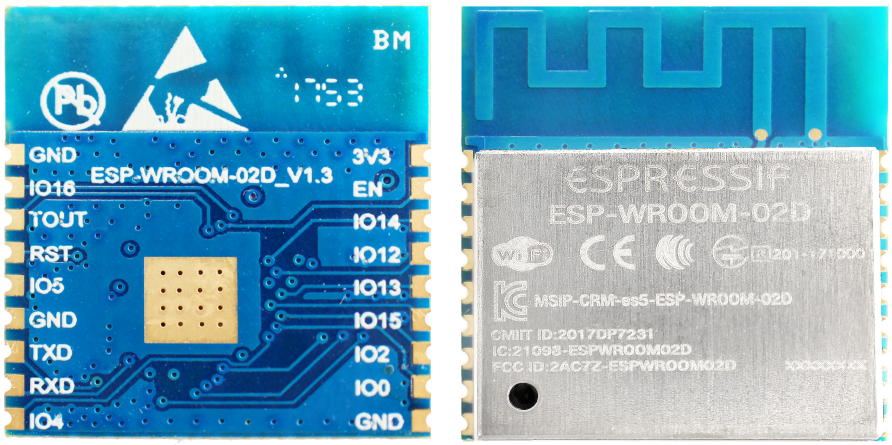

Figure 3-3. ESP-WROOM-02D Module

The module size of ESP-WROOM-02U is (18±0.1) x (14.3±0.1) x (3.2±0.1) mm. The type of flash used on this module is an SPI flash with a package size of SOP 8-150 mil. ESP-WROOM-02U integrates a U.FL connector and has no onboard antenna.

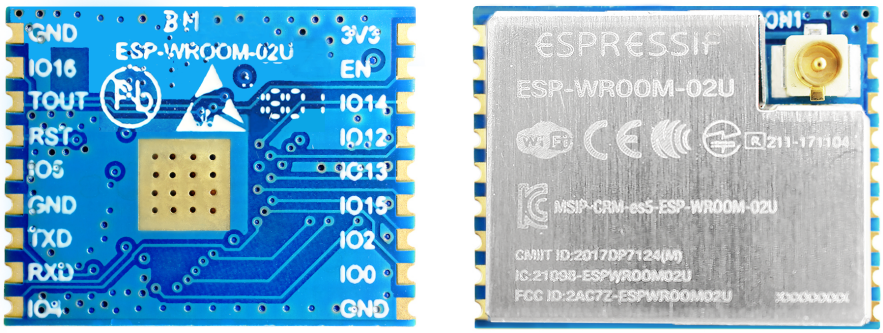

Figure 3-4. ESP-WROOM-02U Module

For detailed information on ESP-WROOM-02D/ESP-WOOM-02U, please refer to *ESP-WROOM-02D/ESP-WROOM-02U Datasheet*.

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