NEC

Using the VRC4171A Graphics Display Controller with the VR41xx Evaluation Board

Application Note

August 1999

Description

The VR41xx™ 32-/64-bit MIPS® RISC microprocessors are members of NEC's VR4100™ family of devices for Windows® CE handheld computer applications. The VRC4171™ companion chip for the VR41xx contains a PC Card™ controller, additional general-purpose I/Os, and an LCD graphic display controller. This application note explains operation of the VRC4171A's LCD graphic display controller and connection of graphic displays to the VR41xx evaluation board.

Features

- Color screen up to 64K shades (1, 2, 5, 6, 8,16 bits/pixel)
- Monochrome screen up to 16 gray scales (1, 2, 4 bits/pixel)
- On-chip color palette RAM (256 x 18 bits) and on-chip hardware cursor (32 x 32 x 2)
- Standard resolutions up to 640 x 480 for 16-bit color
- 600 x 800 for 8-bit color
- STN, DSTN, and TFT LCD panels
- Analog CRT interface (D/A converter required for analog CRT and analog TFT)

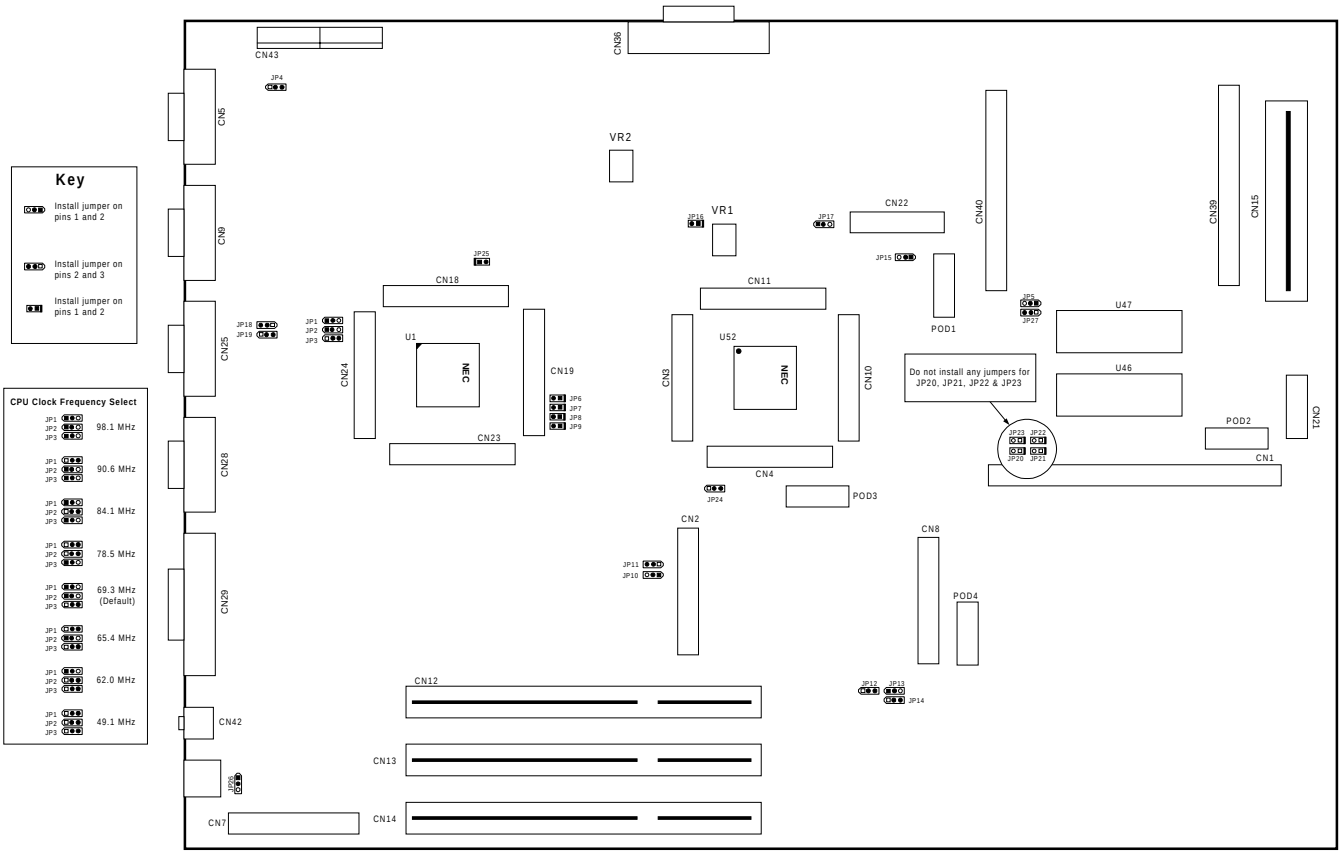
The evaluation board includes an on-board digital-to-analog (D/A) converter for analog TFT and CRT interfaces, 44-pin LCD panel connector (N36), and four voltages for LCD panel power (Table 1).

Table 1. LCD Voltages

Voltage	Description	Jumper	Setting	Selection
PANVDD	LCD panel buffer type	JP15	1-2	3.3-volt buffer
			2-3	5-volt buffer
PANBKL		N/A	N/A	12 volts (fixed)
PANVEE	LCD panel VEE bias voltage control	JP16	IN	Positive VEE (default)
				15 to 25 volts adjustable
				Use VR1 for adjustment
PANVBB	LCD panel VBB bias voltage control	JP16	OUT	Adjustable to –18 volts
				Use VR2 for VBB adjustment

Note: See Figure 1 for jumper and resistor locations.

Figure 1. Evaluation Board

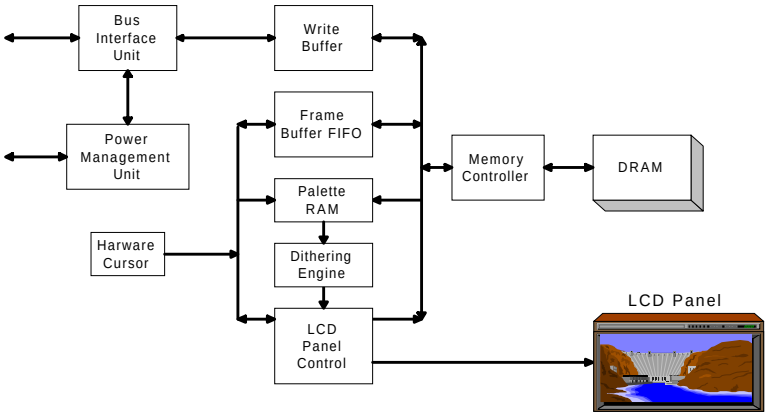


UNB4111 Evaluation Board Jumper Settings Rev. 2.1d

LCD Controller

The LCD controller is designed to work with a variety of STN and TFT color or monochrome LCD panels. It consists of seven fundamental blocks (Figure 2).

Figure 2. LCD Block Diagram



1. The **bus interface unit** performs all handshaking between the system bus and the internal registers, memory write buffers, and power management unit.

2. The **write buffer** enables memory write accesses to the frame buffer to occur between the processor system bus and the frame buffer DRAM without large latencies. The write buffer is designed to match the peak bandwidth of both the processor bus and the frame buffer DRAM.

3. The **frame buffer FIFO** separates the data read from the frame buffer memory during an active scan. The memory controller generates the address and controls the timing and access to the DRAM.

4. The **palette RAM** contains the color palette used for color display (Table 2). It is organized as 256 addresses by 18 bits (6 bits each for red, green, and blue color).

5. The **dithering engine** is used for color STN panels to provide the appearance of more colors by modulating the data as it is being written to the panel during a frame of refresh.

6. The **LCD panel controller** functions as the timing generator for the memory read cycles to the frame buffer FIFO and the data write cycles to the LCD panel. It provides the fundamental scanning synchronization timing signals such as frame and line synchronization and retrace timing.

7. The **hardware cursor** function causes a 32 x 32-pixel by two-color cursor image to appear as an overlay on top of the frame buffer during display time. The hardware cursor interfaces to the memory for the cursor data and to the LCD panel control to switch the data output to the display. The hardware cursor data is stored in off-screen memory in the upper 512 bytes of the frame buffer. When displaying the pixels in the cursor area, the output from the frame buffer data is switched to the output of the cursor data

Graphics Display Data

Table 2. TFT Panel Specifications

Color	Pin Name	Panel Name
RED	VUD_5	RED 5 (MSB)
	VUD_	RED 4
	VUD_	RED 3
	VUD_	RED 2
	VUD_	RED 1
	VUD_	RED 0 (LSB)
GREEN	VLD_3	GREEN 5 (MSB
	VLD_2	GREEN 4
	VLD_1	GREEN 3
	VLD_0	GREEN 2
	VUD_	GREEN 1
	VUD_	GREEN 0 (LSB)
BLUE	TFTD_17	BLUE 5 (MSB
	TFTD_16	BLUE 4
	VLD_7	BLUE 3
	VLD_6	BLUE 2
	VLD_5	BLUE 1
	VLD_4	BLUE 0 (LSB)

The graphics display data is stored in the LCD frame buffer memory and written to the frame buffer memory with a linear address. The display data is read out of the frame buffer by the LCD controller using the starting address and offset registers. This data is then clocked out to the LCD panel using a shift clock with timing based on the value in the horizontal and vertical control registers.

The pixel format used in 8-bit-per-pixel data is an address look-up table (LUT), most commonly referred to as the *color palett* . The 8-bit pixel data is used as an address into the palette RAM. For each address, a specific value of red, green, or blue is read out to the display (6 bits for each color and 18 bits total).

For formats of 5 and 6 bits per pixel, the upper used address bits are available for use as segments that make multiple simultaneous palettes available. This feature allows applications to switch palettes by reloading the on-chip palette, resulting in smoother transitions between applications that may only use a subset of the 256 color address locations available. For 1-, 2-, and 4-bit-per-pixel formats, color registers 0 through 3 are used as a pseudo-palette.

The 16-bit-per-pixel format is a direct color format. Table 3 shows 5-6-5 format, but a 5-5-5 format is also supported.

Table 3. 16-Bit 5-6-5 Pixel Format

High Byte											Low Byte				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4	3	2	1	0	5	4	3	2	1	0	4	3	2	1	0
RED					GREEN						BLUE				

To map 16-bit pixel data to an 18-bit TFT panel, R0 and B0 must output logic 0 to the panel. The origin of the frame buffer is in the upper left of the display area(Table 4)

Table 4. Frame Buffer Pixel Organization

Pixel 00, Pixel 01	Pixel 639
Pixel 640	
Pixel 153000	Pixel 153599

Table 5. Tested LCD Modules

Panel Type	Vendor	Model No.	Reference	Display Format	Active Viewing Area
STN color	Sharp	LM32C04P	Table 8	320 x 240	5.5"
	Kyocera	KCB6424ASTT	Table 14	640 x 240	6.5”
	ALPS	LFH8P4021A	Table 9	240 x 320	3.8”
STN monochrome	ALPS	LRH9J504XA	Table 11	320 x 240	3.8"
DSTN color	Kyocera	KCS6448MSTT-X1	Table 13	640 x 480	7.2”
	Sharp	LM64C21P	Table 15	640 x 480	8.0”
DMTN monochrome	Sharp	LM4Q30TA	Table 16	320 x 240	4.7”
FSTN monochrome	Samsung	UG-24U01-WGT3-B	Table 18; Table 19	240 x 320	3.8”
TFT color	Sharp	LQ039Q2DS01	Table 20	320 x 240	3.8”
	Sharp	LQ64D431	Table 21	640 x 480	10.4”
	NEC	NL6448AC20-06	Table 22	640 x 480	6.5”
	NEC	NL6448AC33-18	Table 23	640 x 480	10.4"
	NEC	NL6448AC33-18A	Table 23	640 x 480	10.4
	NEC	NL6448AC33-24	Table 23	640 x 480	10.4
	NEC	NL6448AC33-27	Table 23	640 x 480	10.4”
	NEC	NL8060AC26-04	Table 24	800 x 600	10.4”

Graphics Registers

The registers listed inTable 6 andTable 7 must be programmed for proper graphic display. The first two registers belong to the VR4111; all others belong to the VRC4171A LCD control registers.

Table 6. VRC4171A Graphics Registers

Registers	Offset Address	Module Type/Resolution				
		TFT, CRT (Note 1)	DSTN (Note 2)	DMTN (Note 3)	FSTN (Note 4)	HR-TFT (Note 4)
		640x48 Color	640x48 Color	320x240 Mono	240x320 Mono	320x240 Color
Gmode (VR41xx)	AB000002	1	1			1
VCLK, MCLK Divider (VR41xx)	BB0005FE	1808	1810	—	1828	1A30
Panel Select	AA800000	5	6	48	48	5
LCD Panel Control	AA800002	607 (Note 5)	05 (Note 6)	2	2	40
Power Mode Control	AA800004	xxxx	xxxx	xxxx	—	—
MCLK Enable	AA800006	1	1	1	1	1
VCLK Enable	AA800008	1	1	1	1	1
Video FIFO/ Memory Interface	AA80000A	12	8	08	8	8
Pixel Adjustment/ Vertical Half	AA80000C	F0	F0	F0	A0	F0
Reserved	AA80000E	xxxx	xxxx	Xxxx	Xxxc	xxxx
Horizontal Display	AA800010	4F5B	4F63 (Note 7)	2731	1E27	2731
Horizontal Retrace	AA800012	5C52	6157	2F2B	2220	312A
Vertical Display Total	AA800014	1DF	1DF	EF	13F	F0
Vertical Display End	AA800016	20C	20C	FF	14F	10
Vertical Retrace Start	AA800018	1EA	1EA	F1	142	FA
Vertical Retrace End	AA80001A	2	8	385	2	C
Starting Address	AA80001C	0	0	0	0	0
Offset/Screen Width	AA80001E	A0	50	14	F	50

Notes:
1. 256-color, 8 bpp: NEC NL6448AC33-18/18a/24 (640 x 480 CRT) and NEC NL6448AC20-06
2. Kyocera KCS6448MSTT-X1; Sharp LM64C21P (8 bpp
3. Sharp LM4Q30TA (4 bpp
4. Samsung UG-24U01-WGHT3-B (4 bpp; do not use 1 bpp)
5. 64K true color and 16 bpp chosen for mode.
6. 256-color, 8 bpp chosen for mode.
7. 0x4F5F, 0x0054, 1E0, 1E4, 1E4: alternative board settings for DSTN panels
8. Select 0x8 for two chips of 16-bit memory x 1M locations.
9. Select 0x10 for one chip of 16-bit memory x 256K locations.
10. Sharp LQ039Q2DS01 320x 240 HR-TFT.

Table 7. VRC4171A Graphics Registers (continued)

Registers	Offset Address	Module Type/Resolution				
		STN (Note 1) 320x24 Mono	STN (Note 2) 320x24 Color	STN (Note 3) 240 x 320 Color	STN (Note 4) 640x240 Color	TFT, CRT (Note 5) 800x600 Color
Gmode (VR41xx)	AB000002	1	1	1	1	1
VCLK, MCLK Divider (VR41xx)	BB0005FE	1A18	1A08	1A08	1A10	1000
Panel Select	AA800000	8	46	46	46	5
LCD Panel Control	AA800002	0	5	5	5	E05 (Note 2)
Power Mode Control	AA800004	xxxx	xxxx	1	1	xxxx
MCLK Enable	AA800006	1	1	1	1	1
VCLK Enable	AA800008	1	1	1	1	1
Video FIFO/ Memory Interface	AA80000A	8	8	8	8	8
Pixel Adjustment/ Vertical Half	AA80000C	F0	F0	A0	78	12C
Reserved	AA80000E	xxxx	xxxx	xxxx	xxxx	xxxx
Horizontal Display	AA800010	2831	2731	1D27	4F63	637
Horizontal Retrace	AA800012	2F2B	2F2B	2420	6157	716B
Vertical Display Total	AA800014	EF	EF	13F	EF	25
Vertical Display End	AA800016	FF	FF	14F	FF	27
Vertical Retrace Start	AA800018	F1	F1	142	F1	26
Vertical Retrace End	AA80001A	2	385	0x0	8	2
Starting Address	AA80001C	0	0	0	0	0
Offset/Screen Width	AA80001E	14	50	IE	50	64

Notes:
1. ALPS Sharp LRH9J50XA
2. Sharp LM32C04P
3. ALPS LFH8P4021A
4. Kyocera KCB6424ASTT
5. NEC NL8060AC20-04
6. Select 0x8 for two chips of 16-bit memory x 1M locations.
7. Select 0x10 for one chip of 16-bit memory x 256K locations.

LCD Connections

The following tables provide information about connection of various LCD models to the NEC VR41xx evaluation board.

Table 8. Sharp LM32C04P Panel Specifications(5-Volt SSTN)

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0			23	NC		
2	VD_L1			24	GND	14	VSS
3	VD_L2			25	FLM		
4	VD_L3			26	DTMG		
5	VD_L4			27	LP	2	LP
6	VD_L5			28	PANVEE	8	VEE
7	VD_L6			29	NC		
8	VD_L7			30	PANVBB		
9	VD_U0	10	D0	31	PANBLK		
10	VD_U1	11	D1	32	PANVDD	7	VDD
11	VD_U2	12	D2	33	*DTMG		
12	VD_U3	13	D3	34	GND	19	VSS
13	VD_U4	15	D4	35	LOCLK		
14	VD_U5	16	D5	36	GND		
15	VD_U6	17	D6	37	VPBIAS	6	DISP
16	VD_U7	19	D7	38	VPLCD		
17	GND	3	VSS	39	PANVDD		
18	SCK	4	XCK	40	PANVDD		
19	GND	5	VSS	41	NC		
20	NC			42	TFTD16		
21	GND	9	VSS	43	NC		
22	FLM	1	YD	44	TFTD17		

Note: Recommended inverter: Sharp. model no. LQ0J04

Table 9. ALPS LFH8P4021A Panel Specifications (V_{DD} = 3.3 V)

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0			23	NC		
2	VD_L1			24	GND	19	VSS
3	VD_L2			25	FLM		
4	VD_L3			26	DTMG		
5	VD_L4			27	LP	13	LOAD
6	VD_L5			28	PENVEE		
7	VD_L6			29	NC		
8	VD_L7			30	PENVBB		
9	VD_U0	2	FPD0	31	PENBLT		
10	VD_U1	3	FPD1	32	PENVDD	15	VDD
11	VD_U2	4	FPD2	33	*DTMG		
12	VD_U3	5	FPD3	34	GND	24	VSS
13	VD_U4	6	FPD4	35	NC		
14	VD_U5	7	FPD5	36	GND		
15	VD_U6	8	FPD6	37	VPBIAS	18	/D.OFF
16	VD_U7	9	FPD7	38	VPLCD		
17	GND	1	VSS	39	PENVDD	16	VDD
18	SCLK	11	CP	40	PENVDD		
19	GND	10	VSS	41	GNDC		
20	NC			42	TFTD16		
21	GND	12	VSS	43	PAN5BL		
22	FLM	14	FRAME	44	TFTD17		

Notes: **1.** Recommended inverter: Tamura Corporation
2. 240 x 320 color STN LCD handwriting device
3. External circuitry requires pin 17, VADJ, of the LFH8P4021 panel to adjust the voltage between 0 and 3 volts.

Table 10. Handwriting Device Terminal Function

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V_{SS}	7	D5	13	LOAD	19	V_{SS}
2	D0	8	D6	14	FRAME	20	YU
3	D1	9	D7	15	V_{DD}	21	XL
4	D2	10	V_{SS}	16	V_{DD}	22	YD
5	D3	11	CP	17	VADJ	23	XR
6	D4	12	V_{SS}	18	/D. OFF	24	V_{SS}

Table 11. ALPS LRH9J504XA Panel Specifications (V_{DD} = 2.7 to 5.5 V)

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0			23	NC		
2	VD_L1			24	GND		
3	VD_L2			25	FLM		
4	VD_L3			26	DTMG		
5	VD_L4			27	LP	7	LOAD
6	VD_L5			28	PENVEE	3	VEE
7	VD_L6			29	NC		
8	VD_L7			30	PENVBB		
9	VD_U0	17	D0	31	PEN+12V		
10	VD_U1	16	D1	32	PENVDD	4	VDD
11	VD_U2	15	D2	33	*DTMG		
12	VD_U3	14	D3	34	GND	8	VSS
13	VD_U4			35	LOCLK		
14	VD_U5			36	GND		
15	VD_U6			37	VPBIAS		
16	VD_U7			38	VPLCD		
17	GND	6	VGND	39	PENVDD		
18	SCK	11	CP	40	PENVDD		
19	GND			41	NC		
20	NC			42	TFTD16		
21	GND			43	NC		
22	FLM	5	FRAME	44	TFTD17		

Table 12. ALPS LCD Panel Terminal Functions

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V5	7	LOAD	13	V3
2	V2	8	VSS	14	D3
3	VEE	9	DF	15	D2
4	VDD	10	/D. OFF	16	D1
5	FRAME	11	CP	17	D0
6	VGND	12	V4	18	NC

Note: Refer to the ALPS panel specification for additional information and to Figure 3 for additional circuitry.

Figure 3. Additional Circuitry for the ALPS LRH9J504XA Panel

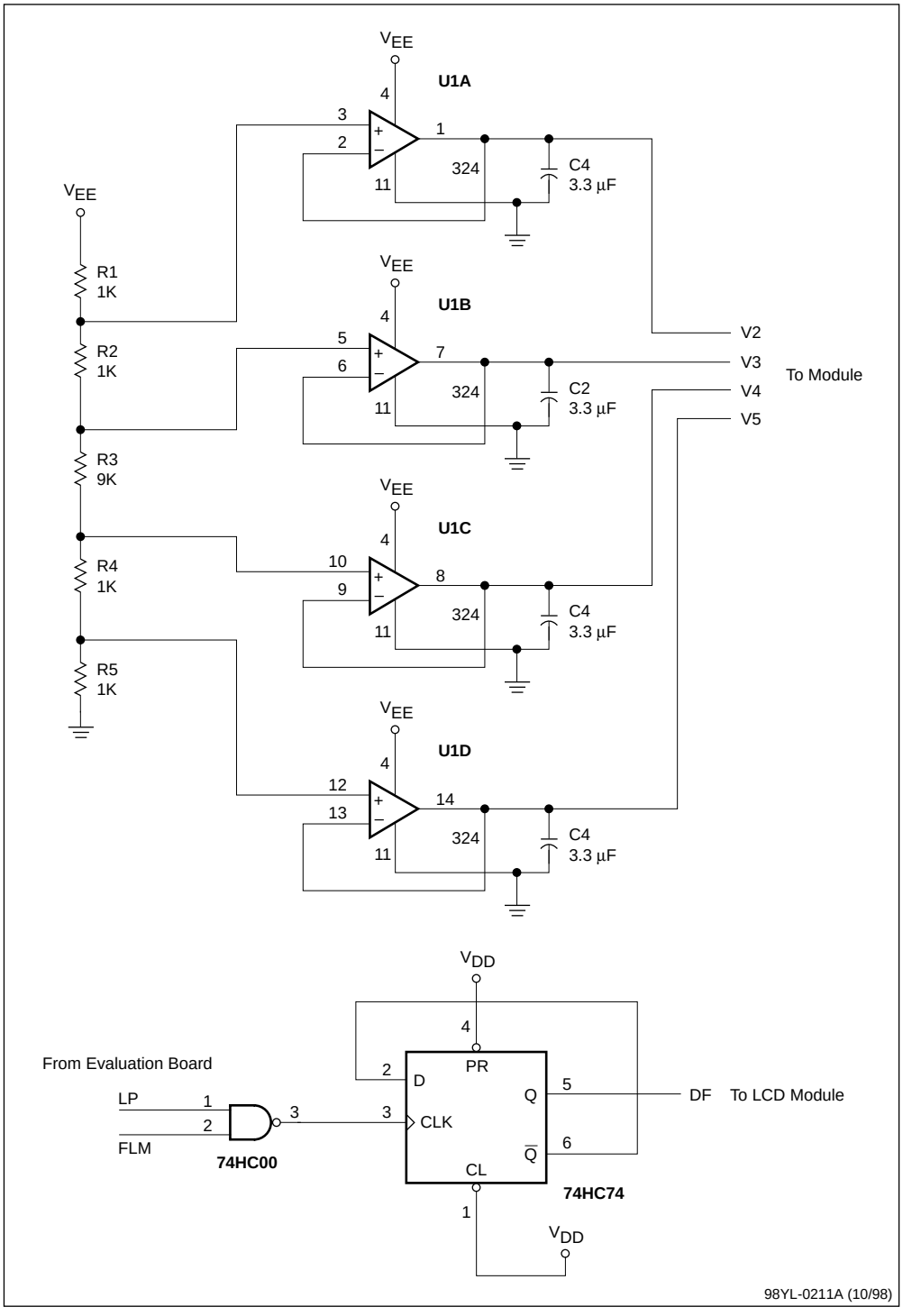


Table 13. Kyocera KCS6448MSTT-X1 Panel Specifications (5-Volt DSTN)

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0	11	LD0	23	NC		
2	VD_L1	13	LD1	24	GND	21	VSS
3	VD_L2	17	LD2	25	FLM		
4	VD_L3	19	LD3	26	DTMG		
5	VD_L4	1	LD4	27	LP	6	LOAD
6	VD_L5	3	LD5	28	PANVEE		
7	VD_L6	5	LD6	29	NC		
8	VD_L7	7	LD7	30	PANVBB		
9	VD_U0	28	HD0	31	PANBLK		
10	VD_U1	26	HD1	32	PANVDD	14	VDD
11	VD_U2	24	HD2	33	*DTMG		
12	VD_U3	22	HD3	34	GND	27	VSS
13	VD_U4	23	HD4	35	LOCLK		
14	VD_U5	25	HD5	36	GND	30	VSS
15	VD_U6	29	HD6	37	VPBIAS	18	DISP
16	VD_U7	31	HD7	38	VPLCD		
17	GND	2	VSS	39	PANVDD	16	VDD
18	SCK	10	CP	40	PANVDD		
19	GND	8,9	VSS	41	NC		
20	NC			42	TFTD16		
21	GND	15	VSS	43	NC		
22	FLM	4	YD	44	TFTD17		

Notes: **1.** 7.2-inch viewing area
2. Recommended inverter: Hitachi Media Electronics model no. PH-BLC08-K2
3. Refer to the LCD and inverter specifications for additional information.

Table 14. Kyocera KCB6424ASTT Panel Specifications (3.3-Volt STN)

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0			23	NC		
2	VD_L1			24	GND	21	VSS
3	VD_L2			25	FLM		
4	VD_L3			26	DTMG		
5	VD_L4			27	LP	2	LP
6	VD_L5			28	PANVEE		
7	VD_L6			29	NC		
8	VD_L7			30	PANVBB		
9	VD_U0	9	D0	31	PENBLT		
10	VD_U1	10	D1	32	PANVDD	5	VDD
11	VD_U2	11	D2	33	*DTMG		
12	VD_U3	12	D3	34	GND	19	VSS
13	VD_U4	13	D4	35	NC		
14	VD_U5	14	D5	36	GND		
15	VD_U6	15	D6	37	VPBIAS	4	DISP
16	VD_U7	16	D7	38	VPLCD		
17	GND	6	VSS	39	VENVDD		
18	SCLK	3	XCK	40	PENVDD		
19	GND	8	VSS	41	NC		
20	NC			42	TFTD16		
21	GND			43	NC		
22	FLM	1	YD	44	TFTD17		

Notes: **1.** 640 x 240 color single-scan STN.
2. Recommended inverter: Kyocera PH-BL08-K2

Table 15. Sharp LM64C21P Panel Specifications (5-Volt STN)

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0	11	DL0	23	NC		
2	VD_L1	13	DL1	24	GND	21	VSS
3	VD_L2	17	DL2	25	FLM		
4	VD_L3	19	DL3	26	DTMG		
5	VD_L4	1	DL4	27	LP	6	LP
6	VD_L5	3	DL5	28	PANVEE		
7	VD_L6	5	DL6	29	NC		
8	VD_L7	7	DL7	30	PANVBB		
9	VD_U0	28	DU0	31	PANBLK		
10	VD_U1	26	DU1	32	PANVDD	14	VDD
11	VD_U2	24	DU2	33	*DTMG		
12	VD_U3	22	DU3	34	GND	27	VSS
13	VD_U4	23	DU4	35	LOCLK		
14	VD_U5	25	DU5	36	GND	30	VSS
15	VD_U6	29	DU6	37	VPBIAS	18	DISP
16	VD_U7	31	DU7	38	VPLCD		
17	GND	2	VSS	39	PANVDD	16	
18	SCK	10	XCK	40	PANVDD		
19	GND	8,9	VSS	41	NC		
20	NC			42	TFTD16		
21	GND	15	VSS	43	NC		
22	FLM	4	YD	44	TFTD17		

Notes: **1.** 8-inch active viewing area
2. Recommended inverter: Xentek, Inc. model no. LS380
3. Refer to the LCD module specifications for inverter specifications and additional circuitry.

Table 16. Sharp LM4Q30TA LCD Panel Specifications

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0			23	NC		
2	VD_L1			24	GND		
3	VD_L2			25	FLM		
4	VD_L3			26	DTMG		
5	VD_L4			27	LP	2	CP1
6	VD_L5			28	PENVEE	6	Note
7	VD_L6			29	NC		
8	VD_L7			30	PENVBB		
9	VD_U0	7	D0	31	PEN+12V		
10	VD_U1	8	D1	32	PENVDD	4	VDD
11	VD_U2	9	D2	33	*DTMG		
12	VD_U3	10	D3	34	GND		
13	VD_U4			35	LOCLK		
14	VD_U5			36	GND		
15	VD_U6			37	VPBIAS		
16	VD_U7			38	VPLCD		
17	GND	5	GND	39	PENVDD	11	ENAB
18	SCK	3	CLK	40	PENVDD		
19	GND			41	NC		
20	NC			42	TFTD16		
21	GND	12	GND	43	NC		
22	FLM	1	S	44	TFTD17		

Note: Refer to the LCD module specifications for additional information and to Figure 4 for additional circuitry.

Table 17. Sharp LM4Q30TA Panel Terminal Functions

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	S	Scan start	7	D0	Display data
2	CP1	Input data latch	8	D1	Display data
3	CLK	Clock	9	D2	Display data
4	VDD	Power supply V_{DD} (+3.3V)	10	D3	Display data
5	GND	Ground	11	ENAB	Data enable
6	VEE	Power supply V_{EE} (13 to 22V)	12	GND	Ground

Figure 4. Connection of the LM4Q30TA to the VRC4171

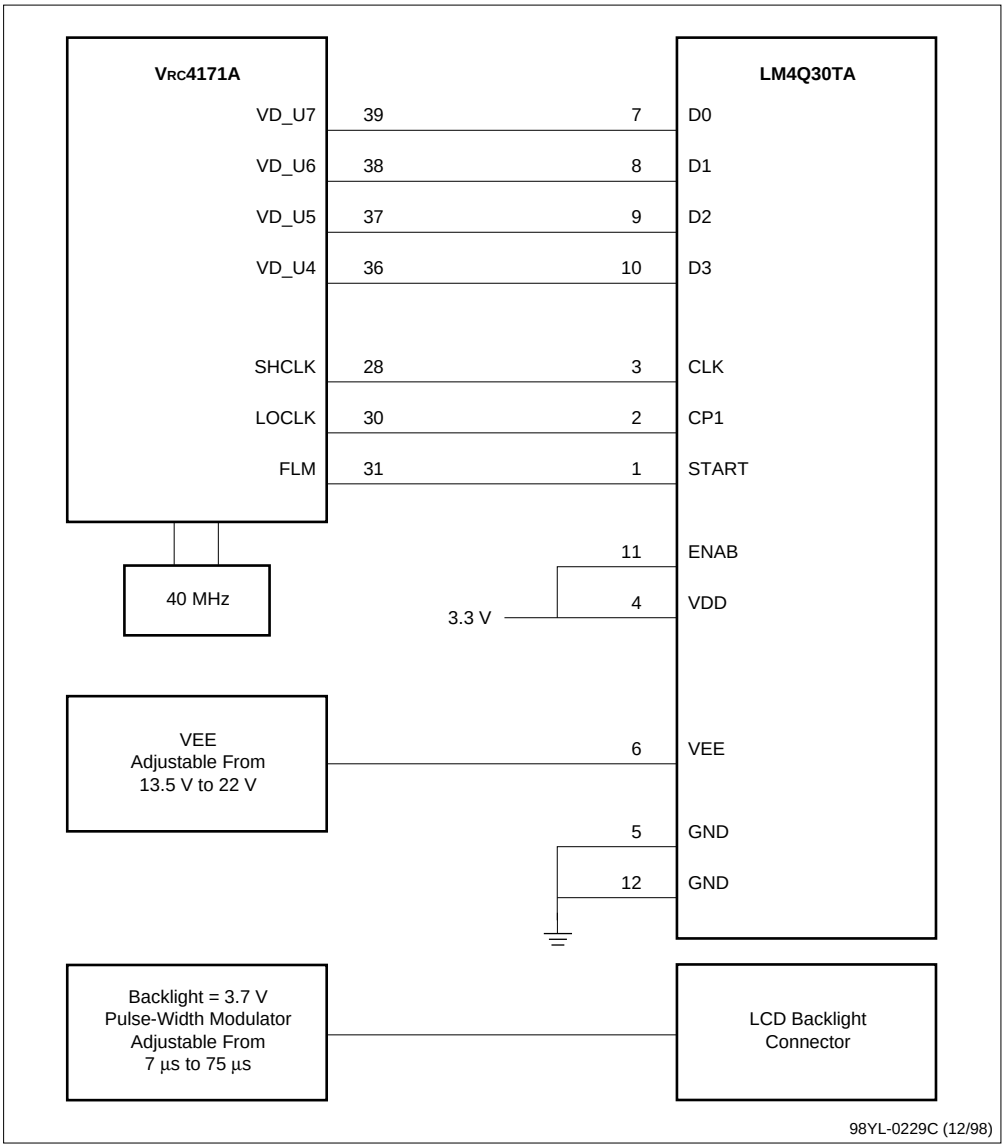


Table 18. Samsung UG-24U01-WGHT3-B LCD Panel Specifications

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0			23	NC		
2	VD_L1			24	GND		
3	VD_L2			25	FLM		
4	VD_L3			26	DTMG		
5	VD_L4			27	LP	2	CP1
6	VD_L5			28	PENVEE	6	Note
7	VD_L6			29	NC		
8	VD_L7			30	PENVBB		
9	VD_U0	7	D0	31	PEN+12V		
10	VD_U1	8	D1	32	PENVDD	4	VDD
11	VD_U2	9	D2	33	*DTMG		
12	VD_U3	10	D3	34	GND		
13	VD_U4			35	LOCLK		
14	VD_U5			36	GND		
15	VD_U6			37	VPBIAS		
16	VD_U7			38	VPLCD		
17	GND	5	GND	39	PENVDD	11	ENAB
18	SCK	3	CLK	40	PENVDD		
19	GND			41	NC		
20	NC			42	TFTD16		
21	GND	12	GND	43	NC		
22	FLM	1	S	44	TFTD17		

Note: Refer to the LCD module specification for additional information and to Figure 5 fo additional circuitry.

Table 19. Samsung UG-24U01-WGHT3-B Panel Terminal Functions

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	VSS	Ground	13	D0	Display data
2	FLM	Frame Start	14	D1	Display data
3	CL1	Data Latch Pulse	15	D2	Display data
4	VSS	Ground	16	D3	Display data
5	CL2	Data Shift Pulse	17	VSS	Ground
6	VSS	Ground	18	X2	Touch screen signal
7	/D.OFF	Display off	19	Y1	Touch screen signal
8	M	AC for LCD driving	20	Y1	Touch screen signal
9	VDD	Power supply, V_{DD}	21	Y2	Touch screen signal
10	VSS	Ground	22	VSS	Ground
11	VEE	Power supply, V_{EE}	23	EL-VCC	Backlight power, 3.3V
12	VSS	Ground	24	El-ON	EL control signal

Figure 5. Additional Circuitry for the Samsung UG-2401-WGHT3-B LCD Module

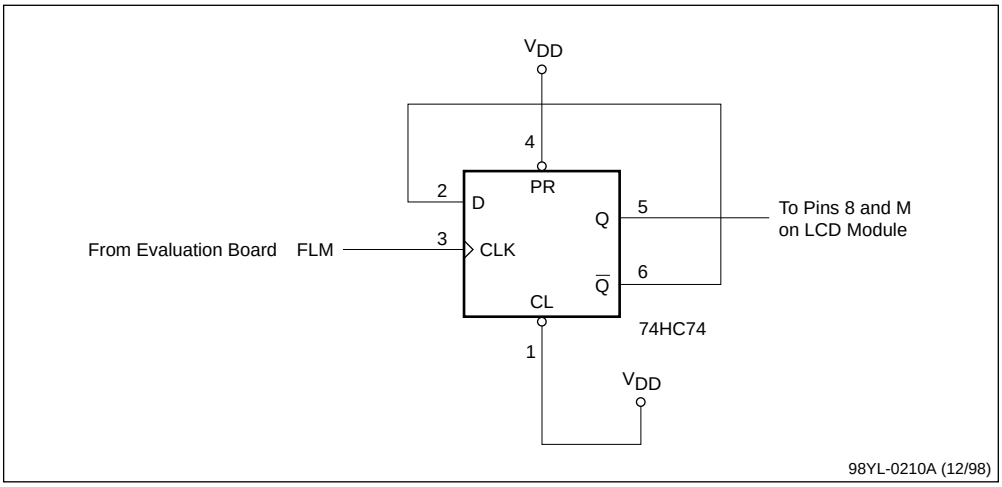


Table 20. Sharp LQ039Q2DS01 Panel Specifications

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0	15	G2	23	NC		
2	VD_L1	16	G3	24	GND	19	GND
3	VD_L2	17	G4	25	FLM		
4	VD_L3	18	G5	26	DTMG	27	DE
5	VD_L4	20	B0	27	LP	3	Hsync
6	VD_L5	21	B1	28	PENVEE		
7	VD_L6	22	B2	29	NC		
8	VD_L7	23	B3	30	PENVBB		
9	VD_U0	6	R0	31	PENBLT		
10	VD_U1	7	R1	32	PENVDD	28	VCC
11	VD_U2	8	R2	33	*DTMG		
12	VD_U3	9	R3	34	GND	26	GND
13	VD_U4	10	R4	35	LP		
14	VD_U5	11	R5	36	GND		
15	VD_U6	13	G0	37	VPBIAS		
16	VD_U7	14	G1	38	VPLCD		
17	GND	1	GND	39	PENVDD	29	VCC
18	SCK	2	CK	40	PENVDD		
19	GND	5	GND	41	NC		
20	NC			42	TFTD16	24	B4
21	GND	12	GND	43	NC		
22	FLM	4	Vsync	44	TFTD17	25	B5

Notes: **1.** ASIC board from Sharp is required.
2. Pin assignment is to the Sharp ASIC board.
3. Refer to the LCD module specification for additional information

Table 21. Sharp LQ64D341 Panel Specifications (5-Volt TFT)

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0	15	G2	23	NC		
2	VD_L1	16	G3	24	GND	19	GND
3	VD_L2	17	G4	25	FLM		
4	VD_L3	18	G5	26	DTMG	27	ENAB
5	VD_L4	20	B0	27	LP	3	Hsync
6	VD_L5	21	B1	28	PANVEE		
7	VD_L6	22	B2	29	NC		
8	VD_L7	23	B3	30	PANVBB		
9	VD_U0	6	R0	31	PANBLK		
10	VD_U1	7	R1	32	PANVDD	28, 29	VDD
11	VD_U2	8	R2	33	*DTMG		
12	VD_U3	9	R3	34	GND	26	GND
13	VD_U4	10	R4	35	LOCLK		
14	VD_U5	11	R5	36	GND		
15	VD_U6	13	G0	37	VPBIAS		
16	VD_U7	14	G1	38	VPLCD		
17	GND	1	GND	39	PANVDD		
18	SCK	2	CK	40	PANVDD		
19	GND	5	GND	41	NC		
20	NC			42	TFTD16	24	B4
21	GND	12	GND	43	NC		
22	FLM	4	Vsync	44	TFTD17	25	B5

Notes: **1.** Ground pin 31, R/L, on the LCD module connector.
2. Connector pin 30, U/D, on the LCD module connector to pin 32, PENVDD, on the 44-pin connector.
3. Recommended inverter: Xentek, Inc. model no. LS460

Table 22. NEC NL6448AC20-6 Panel Specifications (5-Volt TFT)

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0	15	G2	23	NC		
2	VD_L1	16	G3	24	GND	19	GND
3	VD_L2	17	G4	25	FLM		
4	VD_L3	18	G5	26	DTMG	27	DE
5	VD_L4	20	B0	27	LP	3	Hsync
6	VD_L5	21	B1	28	PANVEE		
7	VD_L6	22	B2	29	NC		
8	VD_L7	23	B3	30	PANVBB		
9	VD_U0	6	R0	31	PANBLK		
10	VD_U1	7	R1	32	PANVDD	28	VCC
11	VD_U2	8	R2	33	*DTMG		
12	VD_U3	9	R3	34	GND	26	GND
13	VD_U4	10	R4	35	LOCLK		
14	VD_U5	11	R5	36	GND		
15	VD_U6	13	G0	37	VPBIAS		
16	VD_U7	14	G1	38	VPLCD		
17	GND	1	GND	39	PANVDD	29	VCC
18	SCK	2	CK	40	PANVDD		
19	GND	5	GND	41	NC		
20	NC			42	TFTD16	24	B4
21	GND	12	GND	43	NC		
22	FLM	4	Vsync	44	TFTD17	25	B5

Notes:
1. 6.5-inch active viewing area
2. Recommended inverter: built-in
3. Ground pin 31, DPS (Display Signal Select signal), for normal position
4. High for 180-degree reversed position.
5. Refer to the LCD module specifications for additional information.
6. The information inTable 16 is for 6-bit interface mode. Refer to the LCD module specifications for information about 4-bit interface mode.
7. Pin 30 on the LCD module is no connection.

Table 23. NEC NL6448AC33-18/18A/24/27 Panel Specifications (3.3-Volt TFT)

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0	15	G2	23	NC		
2	VD_L1	16	G3	24	GND	19	GND
3	VD_L2	17	G4	25	FLM		
4	VD_L3	18	G5	26	DTMG	27	DE
5	VD_L4	20	B0	27	LP	3	Hsync
6	VD_L5	21	B1	28	PENVEE		
7	VD_L6	22	B2	29	NC		
8	VD_L7	23	B3	30	PENVBB		
9	VD_U0	6	R0	31	PENBLT		
10	VD_U1	7	R1	32	PENVDD	28	VCC
11	VD_U2	8	R2	33	*DTMG		
12	VD_U3	9	R3	34	GND	26	GND
13	VD_U4	10	R4	35	LP		
14	VD_U5	11	R5	36	GND		
15	VD_U6	13	G0	37	VPBIAS		
16	VD_U7	14	G1	38	VPLCD		
17	GND	1	GND	39	PENVDD	29	VCC
18	SCK	2	CK	40	PENVDD		
19	GND	5	GND	41	NC		
20	NC			42	TFTD16	24	B4
21	GND	12	GND	43	NC		
22	FLM	4	Vsync	44	TFTD17	25	B5

Notes: **1.** Recommended inverter: supplied by NEC
2. 10.4-inch viewing area
3. Refer to LCD module specifications for information about backlight power connections.
4. Pins 30 and 31 on the module are N/C.
5. Refer to the LCD module specifications for additional information.

Table 24. NEC NL8060AC26-04 Panel Specifications (3.3-Volt TFT)

44-Pin Connector		LCD Module Connector		44-Pin Connector		LCD Module Connector	
Pin No.	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**	**Pin No.**	**Symbol**
1	VD_L0	21	G2	23	NC		
2	VD_L1	23	G3	24	GND	8	GND
3	VD_L2	24	G4	25	FLM		
4	VD_L3	25	G5	26	DTMG	37	DE
5	VD_L4	29	B0	27	LP	4	Hsync
6	VD_L5	30	B1	28	PANVEE		
7	VD_L6	31	B2	29	NC		
8	VD_L7	33	B3	30	PANVBB		
9	VD_U0	9	R0	31	PAN+12V		
10	VD_U1	10	R1	32	PANVDD	38	VCC
11	VD_U2	11	R2	33	*DTMG		
12	VD_U3	13	R3	34	GND	12	GND
13	VD_U4	14	R4	35	LOCLK		
14	VD_U5	15	R5	36	GND		
15	VD_U6	19	G0	37	VPBIAS		
16	VD_U7	20	G1	38	VPLCD		
17	GND	3	GND	39	PANVDD	39	VCC
18	SCK	2	DCLK	40	PANVDD	40	VCC
19	GND	6	GND	41	NC		
20	NC			42	TFTD16	34	B4
21	GND	7	GND	43	NC		
22	FLM	5	Vsync	44	TFTD17	35	B5

Notes:
1. 10.4-inch active viewing are
2. Recommended inverter: Xentek, Inc. LS460
3. Pins 1, 3, 6, 7, 8, 12,16,17,18, 22, 26, 27, 28, 32, 36 are grounded on the module.
4. All ground pins on the module are connected to the frame of the module.
5. Pin 41 on the module (MODE) is the timing mode select pin. H = fixed mode, L=DE mode. Refer to the LCD module specification for additional information.
6. Refer to the inverter specifications for more information about connecting the inverter.

Example Program to Exercise the LCD Panels

```
//  Look for updated versions of this software at "www.nec.com"
/*****************************************
      TFT VGA PANEL INITIALIZE PROGRAM for 16 bits per pixel
*****************************************/
/* Define LCD register */
#define PANEL_SELECT                    0x0
#define PANEL_CONTROL                   0x1
#define POWER_CONTROL                   0x2
#define MCLK_ENABLE                     0x3
#define VCLK_ENABLE                     0x4
#define VIDEO_CONTROL                   0x5
#define PIXEL_ADJUST                    0x6

#define HDISP_CONTROL                   0x8
#define HRET_CONTROL                      9
#define VDISPE_CONTROL                   10
#define VDISP_CONTROL                    11
#define VRETS_CONTROL                    12
#define VRETE_CONTROL                    13
#define START_ADDRESS                    14
#define VIDEO_OFFSET                     15

// Vrc4171 Companion Chip to drive LCD panels and PC Card interfaces
#define CC_BASE 0xAA800000
#define FRAME_BUFFER 0xAA000000
short *DST_MEM;
short *CC_init_ptr;
short *GMODE_init_ptr;
short *PANEL_init_ptr;
char *LED7SEG = (char *) 0xb600ffa0;  // New address on 4102 board. an FPGA change from 4101
short *TERMINAL_LSR = (short *) 0xB600FFCA; // LSR register bit 0 is Receive Data Ready bit.

void crlf(void)
{
       print("\r\n");
}

short char_available(void)
{
       if ( *TERMINAL_LSR & 0x01) return (1);
       else return(0);
}

Fill16bppScreen(
short x,  // number of pixels to offset in the Horizontal direction from Left side of screen
short y,  // number of pixels to offset in the Vertical direction from the Top down
short Width,  // Size of Fill in the Horizontal direction
short Height, // Size of Fill in the Vertical direction
short ScreenWidth,  // LCD panel screen width in pixels 640 or 320 short color)
{
      long i,j;
//    print(" Call FillScreen !\n");
      DST_MEM = (short *) FRAME_BUFFER;   // Start from Beginning of Buffer
      DST_MEM += x+(ScreenWidth*(y+Height));  // add in the x & y offsets
//    print(" DST_MEM initial value "); putnum(DST_MEM); print("  "); crlf();
```

```
//    Loop, filling bottom line of rectangle first, then line above the bottom
          for(i=Height; i>0; i--){
             for(j=0; j<(Width+1); j++){
                *( (short *)(DST_MEM +j)) = color;
          }
          DST_MEM -= ScreenWidth; //DST_MEM didnt change just minus 640 to get previous line
      }
}
int panel_read_out(void)
{
  int k01,index1;
      print ("  LCD Panel Registers Read out!"); crlf();
      for(k01=0; k01 < 0x20 ; k01+=2)   // print index array in short 16 bit format
      {
      putnum((unsigned short *)(CC_BASE+k01));  print(" -> ");  putnum(*((unsigned
short*)(CC_BASE+(k01)))); crlf();
      }
      return(1);
}
int generic_register_out(unsigned short *BASE_PTR, long  count)
{
  int k01,index1;
      for(k01=0; k01 < (count<<1) ; k01+=2)   // print index array in short 16 bit format half
word addresses
      {
putnum((unsigned short *)(BASE_PTR+k01));  print(" -> ");  putnum(*((unsigned short
*)(BASE_PTR+(k01)))); crlf();
      }
      return(1);
}
//  Program to initialize the CRT screen 640 x 480 pixels and/or TFT LCD 640 x 480 panel size
//  Then fill screen with a ROSE color background and 5 rectangles of solid
//  color.   Green, Yellow, Red, Blue, & Black.  Continue repeating until a
//  key is pressed.

int vr_main(void)
{
      LED7SEG = (char *) 0xb600ffa0;// initialize the address again;
      *LED7SEG = 0x01; // Show start of Program

      CC_init_ptr = (short *) 0xb40005fe; //Set CC top register address
      GMODE_init_ptr = (short *) 0xab000002; //Set GMODE register address
      PANEL_init_ptr = (short *) 0xaa800000; //Set LCD register address

      print(" TFT VGA  Initialize for 16 bits per pixel format "); crlf();

       *CC_init_ptr = 0x1a08; //initially 1000h after reset, set the clock speed
*GMODE_init_ptr = 0x0001;// 1 write true data values, 0 write inverted data bus values

      PANEL_init_ptr[PANEL_SELECT]       =0x0005;     //0000h register
      PANEL_init_ptr[PANEL_CONTROL]      =0x0607;     //002h register 16 bits per pixel
      //PANEL_init_ptr[POWER_CONTROL]    =0000;       //0004h register !!Careful Power up LCD
voltages in strict order!!
      PANEL_init_ptr[MCLK_ENABLE]        =0x0001;     //0006h register
      PANEL_init_ptr[VCLK_ENABLE]        =0x0001;     //0008h register VCLK_ENABLE
      PANEL_init_ptr[VIDEO_CONTROL]      =0x0008;     //000Ah register VIDEO_CONTROL
```

```
      PANEL_init_ptr[PIXEL_ADJUST]       =0x00f0;     //000Ch register PIXEL_ADJUST
      PANEL_init_ptr[HDISP_CONTROL]     =0x4f5b;      //0010h register was 4f63
      PANEL_init_ptr[HRET_CONTROL]      =0x5C52;      //0012h register
      PANEL_init_ptr[VDISPE_CONTROL]    =0x01df;      //0014h register
      PANEL_init_ptr[VDISP_CONTROL]     =0x020c;      //0016h register
      PANEL_init_ptr[VRETS_CONTROL]     =0x01ea;      //0018h register
      PANEL_init_ptr[VRETE_CONTROL]     =0x0002;      //001Ah register
      PANEL_init_ptr[START_ADDRESS]     =0x0000;      //001Ch register
      PANEL_init_ptr[VIDEO_OFFSET]      =0x00a0;      //001Eh register 16 bits per pixel

      *LED7SEG = 0x02; // Show start of Program

      if (0 == PANEL_init_ptr[POWER_CONTROL]                          )
      {
      PANEL_init_ptr[POWER_CONTROL]=(short) 4;        //0004h register
      delay(300000);  print(" delay 1 \r\n");
      PANEL_init_ptr[POWER_CONTROL]=(short) 6;        //0004h register
      delay(300000);  print(" delay 2 \r\n");
      PANEL_init_ptr[POWER_CONTROL]=(short) 7;        //0004h register
      delay(300000);  print(" delay 3 \r\n");
      PANEL_init_ptr[POWER_CONTROL]=(short) 0xF ;     //Turn on the Back light too
      }
      else print(" TFT power is already on ");
      print(" TFT VGA 16 BITS PER PIXEL panel is now on! \r\n");
      *LED7SEG = 0x99; // Show end of Program
      panel_read_out();   // Dump the LCD panel registers
      generic_register_out((short *)0xAB000002,(long) 1);
      generic_register_out((short *)0xB40005FC,(long) 2);
      while(1)
    {
      if ((PANEL_init_ptr[01] & 0x0F)==0x7)   // checking AA800002 for bits per pixel size
          {
//     fill_16bpp(0xEA9C);
Fill16bppScreen(0,0,640,480,640,0xE19C); //Fill screen with single Rose Color background
Fill16bppScreen(120,80,240,240,640,0x06e0); //write a single Green square offset in the center
Fill16bppScreen(20,200,80,140,640,0xF7C0); //write a single Yellow square offset in the center
Fill16bppScreen(400,300,180,140,640,0xE800); //write a single Red square offset in the center
Fill16bppScreen(400,100,180,140,640,0x001f); //write a single Blue square offset in the center
Fill16bppScreen(120,340,240,40,640,0x0000); //write a single Black square offset in the center
}
      if (char_available())  // Check for a Key Hit received from the Terminal!
{
              print(" Thank you for observing the Vrc4171 demonstration! ");
              exit(1);
          }

       delay(200000);
      }

}
```

Header Files for the LCD Panel Drivers

```
/******** IMPORTANT SETTINGS *********/
#define       FBBPP           8

// Only one can be defined. These are only used in this file.
// Or you can "set CDEFINES=-DPANEL_TYPE -DFBBPP=X"
// in your compilation environment window to specify
// these variables.

//#define       CRT640                          1
#define       SHARP_TFT640            1
//#define       KYOCERA_DSTN640 1
//#define       SHARP_STN320              1
//#define       ALPS_STN320                     1
//#define       NEC_TFT320                      1
/******** IMPORTANT SETTINGS *********/

/* register init code, which should be done in boot code
 * should no longer needed in driver
 */
#define TEMP_CODE       1

#define BPP_MASK        0xFFF8

/* For calc. DispDrvr_cdwStride */
#if FBBPP==15
      #define         NUM_BPP 16
#else
      #define         NUM_BPP FBBPP
#endif

/* For GPE and lcd register values */
#if FBBPP==1
  #define               GPEBPP                  gpe1Bpp
  #define               REG_BPPBITS             0
#endif
#if FBBPP==2
  #define               GPEBPP                  gpe2Bpp
  #define               REG_BPPBITS             1
#endif
#if FBBPP==4
  #define               GPEBPP                  gpe4Bpp
  #define               REG_BPPBITS             2
#endif
#if FBBPP==8
  #define               GPEBPP                  gpe8Bpp
  #define               REG_BPPBITS             5
#endif
```

```
#if FBBPP==15
  #define               GPEBPP                  gpe16Bpp
  #define               REG_BPPBITS             6
#endif
#if FBBPP==16
  #define               GPEBPP                  gpe16Bpp
  #define               REG_BPPBITS             7
#endif

/
*************************************************************
*/
//  VAL_PANEL_CONTROL 'S bpp NEED NOT BE DEFINE; it will be
ignored
//   It will be calculated in program using FBBPP.
// VALUE OF VIDEO_OFFSET WILL BE CALCULATED IN PROGRAM using
SCREEN_WIDTH.

//
============================================================
====//
#ifdef SHARP_TFT640
#define CRT640  1
#endif

#ifdef CRT640 /* crt, Sharp TFT*/
#ifdef REG_VAL_DEFINED
 #error More than 1 panel/mode defined!
#endif
#define REG_VAL_DEFINED 1
#define SCREEN_WIDTH    640
#define SCREEN_HEIGHT   480

#define VAL_CLK_DIV                 0x1808
#define VAL_PANEL_SELECT    0x0005
#define VAL_PANEL_CONTROL   0x0600
#define VAL_MCLK_ENABLE     0x0001
#define VAL_VCLK_ENABLE     0x0001
#define VAL_VIDEO_CONTROL   0x0008
#define VAL_PIXEL_ADJUST    0x00F0
#define VAL_HDISP_CONTROL   0x4F5B
#define VAL_HRET_CONTROL    0x5C52
#define VAL_VDISPE_CONTROL  0x01DF
#define VAL_VDISP_CONTROL   0x020C
#define VAL_VRETS_CONTROL   0x01EA
#define VAL_VRETE_CONTROL   0x0002
#define VAL_START_ADDRESS   0x0000
#endif
```

```
//
================================================================
====//
#ifdef KYOCERA_DSTN640

#ifdef REG_VAL_DEFINED
 #error More than 1 panel/mode defined!
#endif
#define REG_VAL_DEFINED 1
#define SCREEN_WIDTH            640
#define SCREEN_HEIGHT   480

#define VAL_CLK_DIV                     0x1810
#define VAL_PANEL_SELECT                0x0006
#define VAL_PANEL_CONTROL               0x0000
#define VAL_MCLK_ENABLE                 0x0001
#define VAL_VCLK_ENABLE                 0x0001
#define VAL_VIDEO_CONTROL               0x0008
#define VAL_PIXEL_ADJUST                0x00F0
#define VAL_HDISP_CONTROL               0x4F63
#define VAL_HRET_CONTROL                0x6157
#define VAL_VDISPE_CONTROL              0x01DF
#define VAL_VDISP_CONTROL               0x020C
#define VAL_VRETS_CONTROL               0x01EA
#define VAL_VRETE_CONTROL               0x0008
#define VAL_START_ADDRESS               0x0000
#endif


//
================================================================
====//
#ifdef SHARP_STN320 /* Sharp STN*/
#ifdef REG_VAL_DEFINED
 #error More than 1 panel/mode defined!
#endif
#define REG_VAL_DEFINED 1
#define SCREEN_WIDTH    320
#define SCREEN_HEIGHT   240

#define VAL_CLK_DIV                             0x1A08
#define VAL_PANEL_SELECT                0x0046
#define VAL_PANEL_CONTROL               0x0000
#define VAL_MCLK_ENABLE                 0x0001
#define VAL_VCLK_ENABLE                 0x0001
#define VAL_VIDEO_CONTROL               0x0008
```

```
#define VAL_PIXEL_ADJUST                0x00F0
#define VAL_HDISP_CONTROL               0x2731
#define VAL_HRET_CONTROL                0x2F2B
#define VAL_VDISPE_CONTROL              0x00EF
#define VAL_VDISP_CONTROL               0x00FF
#define VAL_VRETS_CONTROL               0x00F1
#define VAL_VRETE_CONTROL               0x0385
#define VAL_START_ADDRESS               0x0000
#endif

//
================================================================
====//
#ifdef ALPS_STN320
#ifdef REG_VAL_DEFINED
 #error More than 1 panel/mode defined!
#endif
#define REG_VAL_DEFINED 1
#define SCREEN_WIDTH    320
#define SCREEN_HEIGHT   240

#define VAL_CLK_DIV                             0x1818
#define VAL_PANEL_SELECT                0x0008
#define VAL_PANEL_CONTROL               0x0000
#define VAL_MCLK_ENABLE                 0x0001
#define VAL_VCLK_ENABLE                 0x0001
#define VAL_VIDEO_CONTROL               0x0008
#define VAL_PIXEL_ADJUST                0x00F0
#define VAL_HDISP_CONTROL               0x2831
#define VAL_HRET_CONTROL                0x2F2B
#define VAL_VDISPE_CONTROL              0x00EF
#define VAL_VDISP_CONTROL               0x00FF
#define VAL_VRETS_CONTROL               0x00F1
#define VAL_VRETE_CONTROL               0x0002
#define VAL_START_ADDRESS               0x0000
#endif

//
================================================================
====//
#ifdef NEC_TFT320
#ifdef REG_VAL_DEFINED
 #error More than 1 panel/mode defined!
#endif
#define REG_VAL_DEFINED 1
#define SCREEN_WIDTH    320
#define SCREEN_HEIGHT   240
```

```
#define VAL_CLK_DIV                             0x1830
#define VAL_PANEL_SELECT                0x0005
#define VAL_PANEL_CONTROL               0x0400
#define VAL_MCLK_ENABLE                 0x0001
#define VAL_VCLK_ENABLE                 0x0001
#define VAL_VIDEO_CONTROL               0x0008
#define VAL_PIXEL_ADJUST                0x00F0
#define VAL_HDISP_CONTROL               0x2731
#define VAL_HRET_CONTROL                0x312A
#define VAL_VDISPE_CONTROL              0x00F0
#define VAL_VDISP_CONTROL               0x0106
#define VAL_VRETS_CONTROL               0x00F4
#define VAL_VRETE_CONTROL               0x000C
#define VAL_START_ADDRESS               0x0000
#endif

//
================================================================
====//



/* Some error checks */
#ifndef REG_VAL_DEFINED
 #error No panel/mode defined!
#endif
```

NEC

Some of the information contained in this document may vary from country tocountry. Before using any NEC product in your application, please contact a representative from the NEC office in your country to obtain a list of authorized representatives and distributors who can verify the following:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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