GROUNDING IN HIGH SPEED SYSTEMS

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The importance of maintaining a low impedance large area ground plane is critical to practically all analog circuits today, especially at high speeds. The ground plane not only acts as a low impedance return path for high frequency currents but also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuits susceptibility to external EMI/RFI is also reduced.

All IC ground pins should be soldered directly to the ground plane to minimize series inductance. Power supply pins should be decoupled to the ground plane using low inductance ceramic surface mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1mm. Ferrite beads may be also required.

The ground plane allows the impedance of PCB traces to be controlled, and high frequency signals can be terminated in the characteristic impedance of the trace to minimize reflections when necessary.

Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers and vias. Nevertheless, as much area as possible should be preserved, and at least 75% should remain. After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated ground "islands." IC ground pins located in a ground "island" have no current return path to the ground plane.

The best way of minimizing ground impedance in a multicard system is to use another PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the mother card. The PCB connector should have at least 30-40% of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities: (1) The backplane ground plane can be connected to chassis ground at numerous points, thereby diffusing the various ground current return paths. (2) The ground plane can be connected to a single system "star ground" point (generally at the power supply).

The first approach is often used at very high frequencies and where the return currents are relatively constant. The low ground impedance is maintained all the way through the PC boards, the backplane, and ultimately the chassis. It is critical that good electrical contact be made where the grounds are connected to the sheet metal chassis. This requires self-tapping sheet metal screws or "biting" washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

In other systems, especially high speed ones with large amounts of digital circuitry, it is highly desirable to physically separate sensitive analog components from noisy digital components. It is usually desirable to use separate

ground planes for the analog and the digital circuitry. On PCBs which have both analog and digital circuits, there are two separate ground planes. These planes should not overlap in order to minimize capacitive coupling between the two. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The arrangement shown in Figure 7.26 illustrates that the two planes are kept separate all the way back to a common system "star" ground, generally located at the power supplies. The connections between the ground planes, the power supplies, and the "star" should be made up of multiple bus bars or wide copper brads for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental DC voltage from developing between the two ground systems when cards are plugged and unplugged.

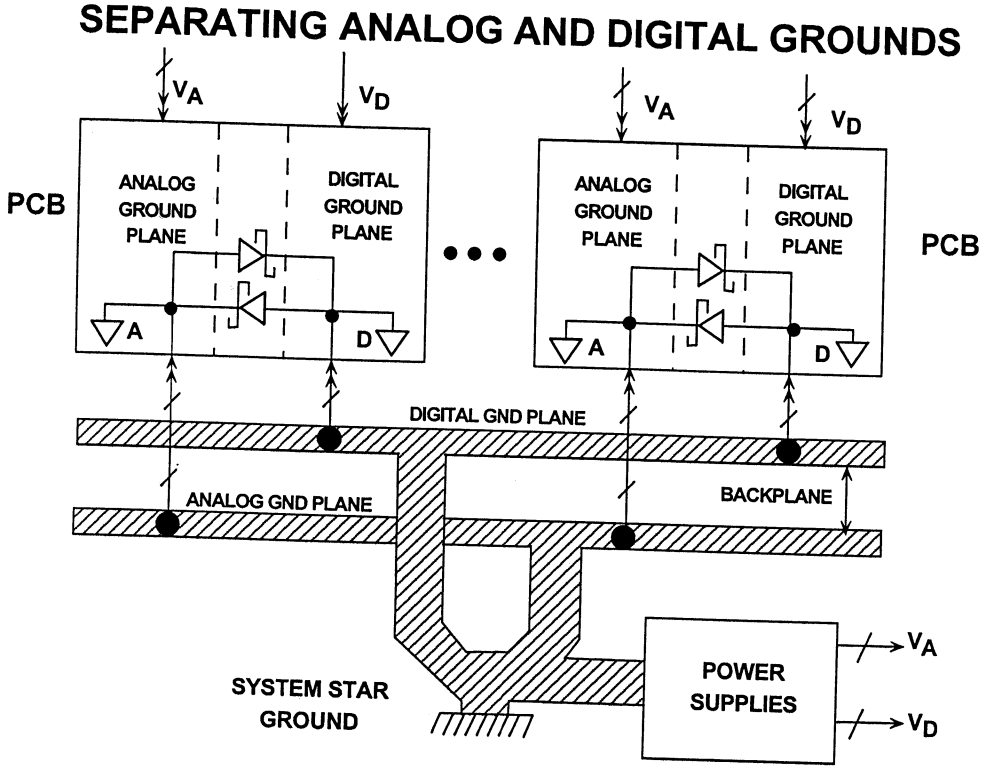

Figure 7.26

Sensitive analog components such as amplifiers and voltage references are referenced and decoupled to the analog ground plane. *The ADCs and DACs (and even some mixed-signal ICs) should be treated as analog components and also grounded and decoupled to the analog ground plane.* At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in Figure 7.27 will help to explain this seeming dilemma.

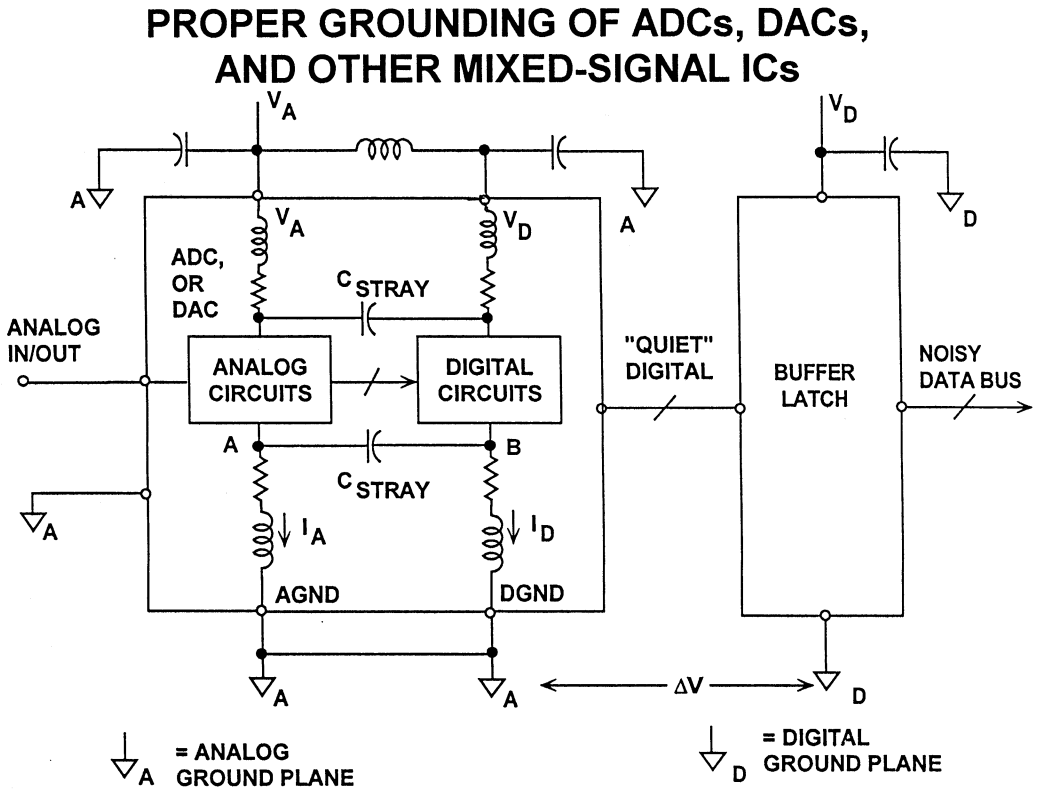

Figure 7.27

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 7.27 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance.

The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system.

It is true that this arrangement will inject a small amount of digital noise on the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter input/or output does not drive a large fanout (they normally can't by design). Minimizing the fanout on the converter's digital port will also keep

the converter logic transitions relatively free from ringing, and thereby minimize any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Figure 7.27. The internal digital currents of the converter will return to ground through the V_D pin decoupling capacitor (mounted as close to the converter as possible) and will not appear in the external ground circuit. It is always a good idea (as shown in Figure 7.27) to place a buffer latch adjacent to the converter to isolate the converter's digital lines from any noise which may be on the data bus. Even though a few high speed converters have three-state outputs/inputs, this isolation latch represents good design practice.

The buffer latch and other digital circuits should be grounded and decoupled to the digital ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter.

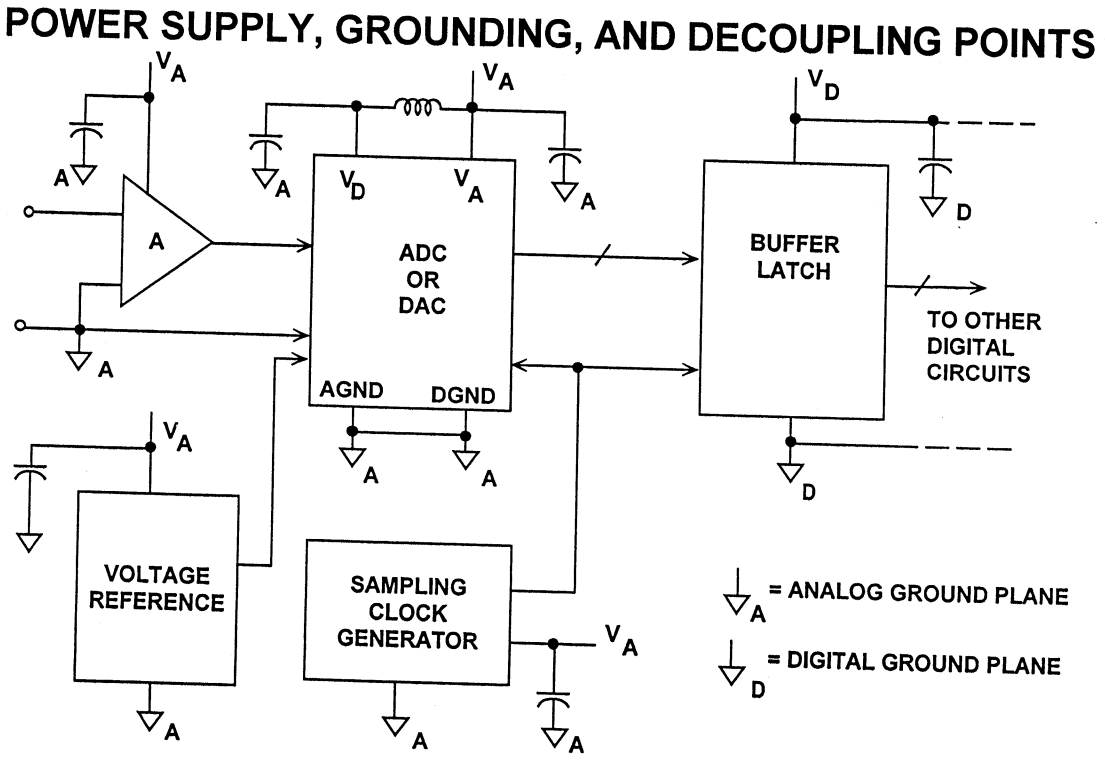

Figure 7.28

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

The sampling clock generation circuitry should also be grounded and heavily-decoupled to the analog ground plane. As previously discussed, phase noise on the sampling clock produces degradation in system SNR.

A low phase-noise crystal oscillator should be used to generate the ADC sampling clock, because sampling clock jitter modulates the input signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

Ideally, the sampling clock generator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multi-purpose system clock which is generated on the digital ground plane. If it is passed between its origin on the digital ground plane to the ADC on the analog ground plane, the ground noise between the two planes adds directly to the clock and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics. This can be remedied somewhat by transmitting the sampling clock signal as a differential one using either a small RF transformer or a high speed differential driver and receiver as shown in Figure 7.29. The driver and receiver should be ECL to minimize phase jitter. In either case, the original master system clock should be generated from a low phase noise crystal oscillator.

It is evident that noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

If a ground plane is used, as it should in be most cases, it can act as a shield where sensitive signals cross. Figure 7.30 shows a good layout for a data acquisition board where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

SAMPLING CLOCK DISTRIBUTION FROM DIGITAL TO ANALOG GROUND PLANES

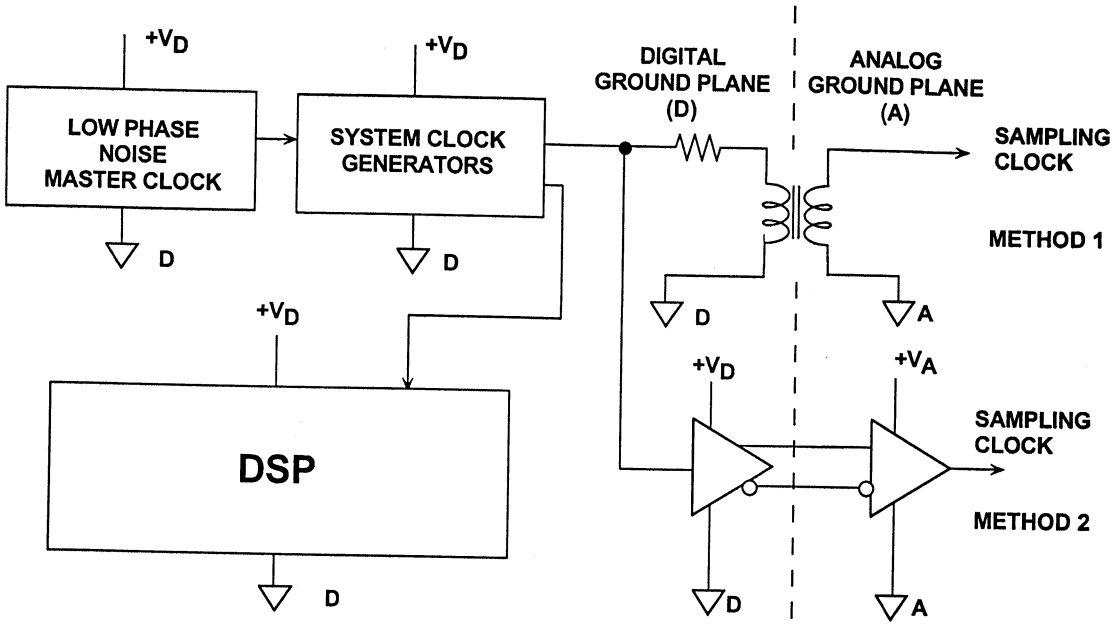

Figure 7.29

A PC BOARD LAYOUT SHOWING GOOD SIGNAL ROUTING

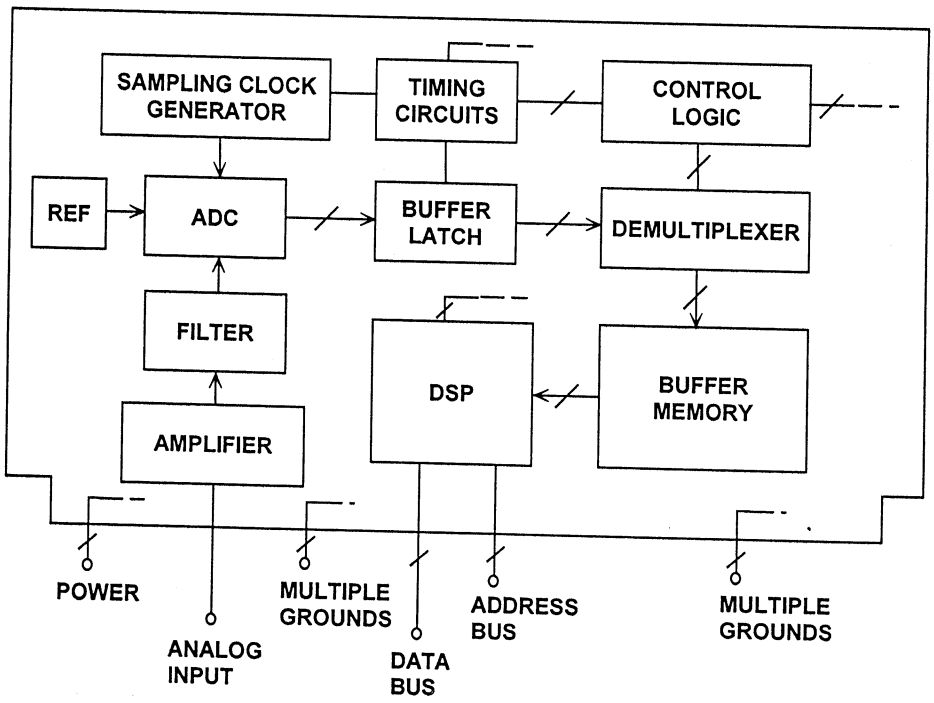

Figure 7.30

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mOhms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.