DESIGNING EMITTER FOLLOWERS

Bob, G4FHU, works mainly on the hf bands using cw or rtty. Despite taking early retirement last year he finds little enough time to "get on the air" in competition with other hobbies such as computers and piano and the dreaded grass cutting that is the result of moving from London to the country.

Boyhood short wave listening was interrupted by the second world war and post-war service as a radio mechanic in the Royal Signals. Then, after graduation, five years in the electronics industry was followed by 28 in polytechnics running and teaching in degree and HND courses in electrical and electronic engineering.

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Introduction

Single transistor voltage follower circuits are very widely used and look very simple, but their design is often careless and their performance not what might be expected. Elementary books tend to end before the crucial problems are reached, while advanced texts rarely give clear practical advice.

A simple but effective design sequence is offered here, together with the results of some practical measurements that show what can happen in typical circuits. As a foretaste of these, glance at Fig 11 to see how input resistance can vary and remain negative over most of the amateur radio frequency range; then look at Fig 5 to see how a low frequency waveform can be damaged by a bad choice of bias.

Although the focus is mainly upon bipolar emitter followers, the same methods can be extended easily to the design of field effect source followers. It is assumed that the reader is already familiar with the well-known virtues of such circuits that *can* be obtained if the signal amplitude and frequency are small enough, ie high input resistance, low output resistance, nearly unity voltage gain.

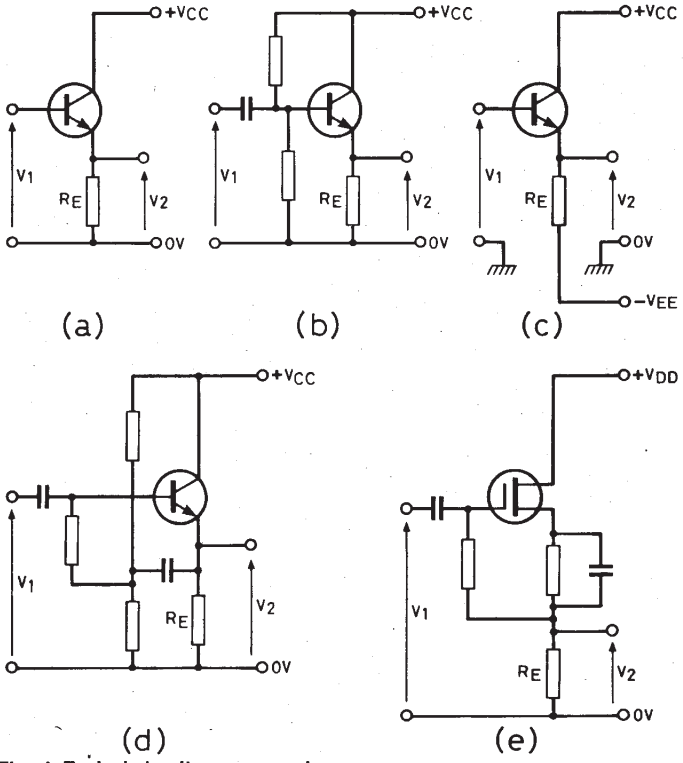


Fig 1. Typical circuit arrangements

Choosing a practical bias circuit

Some of the most useful circuit arrangements are shown in Fig 1; the best and simplest is that in 1(a), but this only works if the direct voltage that happens to be associated with the input signal is nearly enough right to set the desired dc (bias) conditions. To keep the bias indepedent of the signal source, 1(b) is often employed, or when supply rails of both polarities are available the arrangement of 1(c) is very convenient.

To offset the reduction of input resistance by shunt bias resistors, a kind of "bootstrap" circuit is sometimes used, such as in 1(d). For really high input resistance in low frequency applications a fet is preferable, as for example in 1(e).

Choosing the bias levels

In all the circuits mentioned so far, the emitter (or source) resistor R_E is the only "load" at the output side, and in this practically rather limited case the bias levels are easily decided. The essential starting point is to specify the amplitude of the largest signal to be handled and the minimum voltage to be maintained across the transistor. To cover all cases, let us assume that

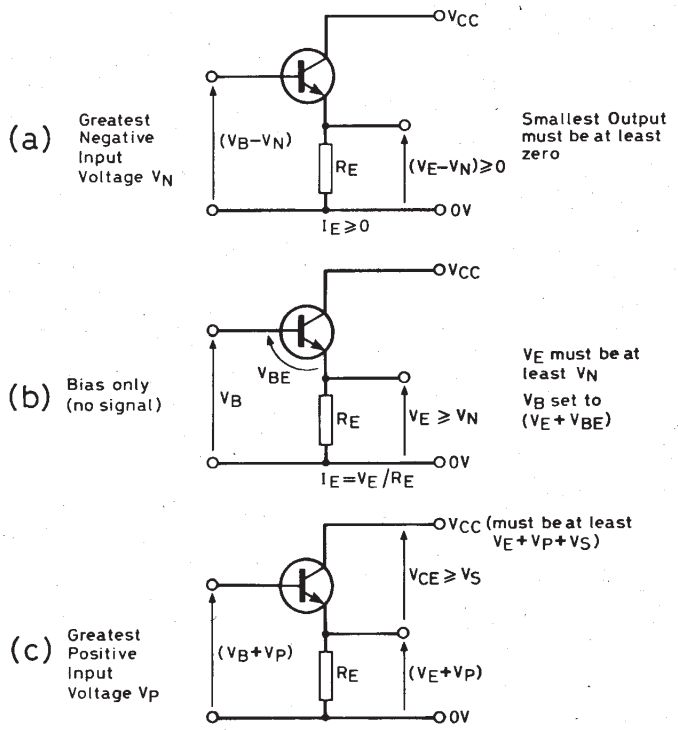


Fig 2. Choosing bias levels. *(a)* Greatest negative input voltage V_N. Smallest output voltage must be at least zero. *(b)* Bias only (no signal). V_E must be at least V_N. V_B set to $(V_E + V_{BE})$. *(c)* Greatest positive input voltage V_P. V_{CC} must be at least $(V_E + V_P + V_S)$

*13 Mill Drove, Bourne, Lincs PE10 9BX.

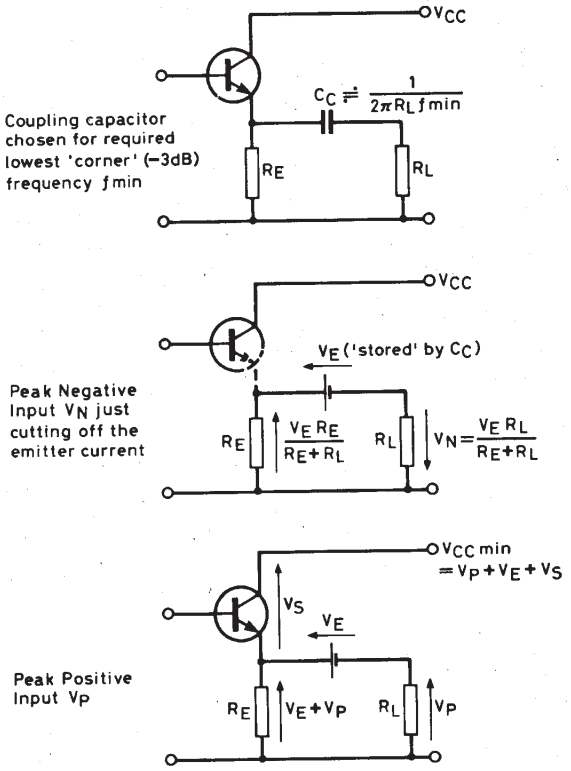


Fig 3. Effects of ac coupling the load. *(a)* Coupling capacitor chosen for required lowest "corner" (−3dB) frequency f_{min}. *(b)* Peak negative input voltage V_N just cutting off the emitter current. *(c)* Peak positive input voltage V_P

the input signal has a positive peak voltage V_P and a (possibly) different negative peak voltage V_N.

The minimum transistor voltage (V_{CEmin} or V_{DSmin}) should be at least about 0·7V to keep a bipolar out of saturation and, for a fet at least a couple of volts will be needed to keep in the pinch-off operating region. Let's call this minimum voltage V_S. Fig 2 shows how these combine with the dc bias levels V_B, V_E, I_E and the supply voltage V_{CC}, and how they relate to extreme conditions.

The best that any transistor can do to follow a big negative peak is to switch off entirely, so the greatest negative peak output swing is equal to V_E, and we must choose V_E safely larger than V_N. For positive peak inputs there must be sufficient supply voltage V_{CC} to allow "headroom", ie $V_{CC} = V_E + V_S + V_P$ is the absolute minimum satisfactory supply voltage. The no-signal emitter current is $I_E = V_E/R_E$, and the corresponding static power dissipation in the transistor is $I_E (V_{CC} - V_E)$. These factors override the predictions that can be made by small signal equivalent circuit analysis (especially those based upon small signal output resistance).

A more common practical circuit that couples the signal but not the bias level to an external load R_L is shown in Fig 3(a), and the ac coupling via a capacitor has a profound effect upon the bias level required. This is summarized in Fig 4, and explained in more detail in Appendix A. The ac-coupled load resistance R_L now becomes more difficult to drive when large signals are present (and "large" may mean only a volt or less in some cases). The crucial factor is the ratio $K = R_E/R_L$, and this is the horizontal axis in Fig 4. Look first at the extremes: if the ratio K is too small, the emitter current has to be enormous; if K is high, the collector supply voltage has to be very much larger than the signal amplitude. Suppose, for example, that an emitter follower is required to drive a diode modulator with the following specification: Power level +6dBm, input resistance 50Ω (this demands a peak signal voltage of 630mV and a peak signal current of 12·6mA). If K is chosen as 4, say, then V_E = 3·15V and I_E = 15·75mA. Then, if the minimum transistor voltage is chosen as V_S = 2V the minimum supply voltage will be V_{CC} = 5·78V. The emitter resistance R_E is $V_E/I_E = K.R_L$ = 200Ω.

If the above procedure is omitted, the resulting waveform distortion can be quite severe. A bad case is illustrated by the photographed waveforms of Fig 5. The two upper waveforms superimposed show an input sinusoid and the corresponding distorted waveform across the 470Ω emitter resistor R_E. The lower waveform is that across the 47Ω load resistor R_L, and the true zero for all plots is marked by the unused 500mV/div cro channel which is one division from the bottom of the screen.

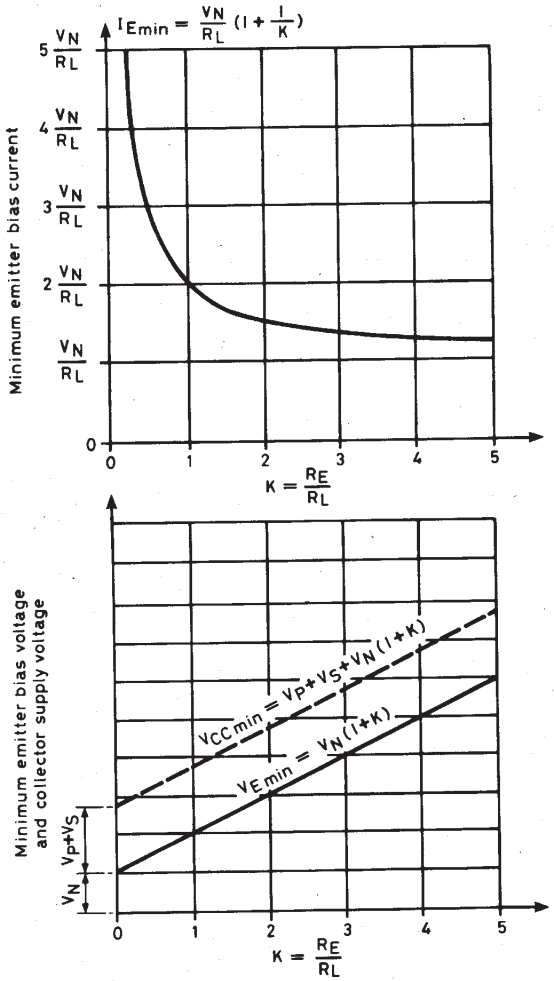


Fig 4. Minimum bias levels for an emitter follower. *(a)* Minimum emitter bias current. *(b)* Minimum emitter bias voltage and supply voltage

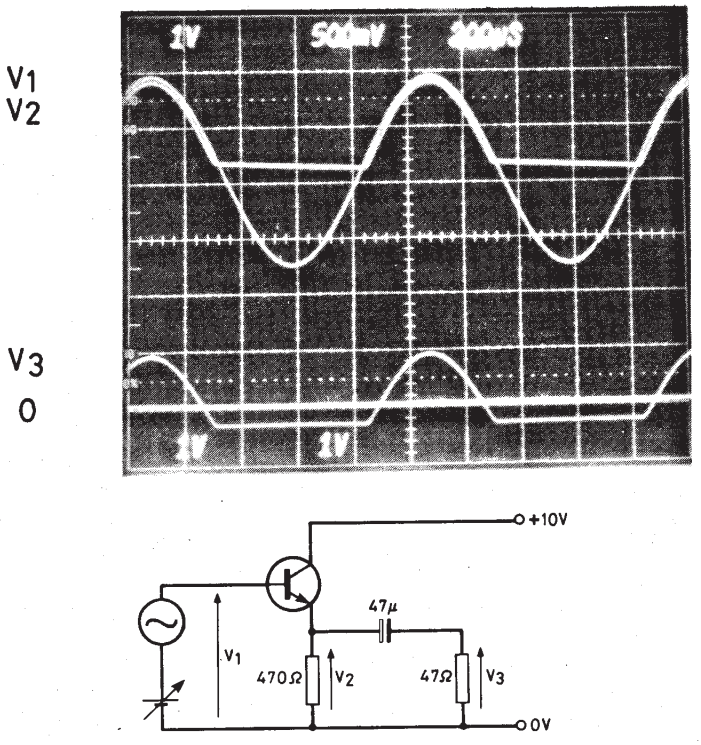
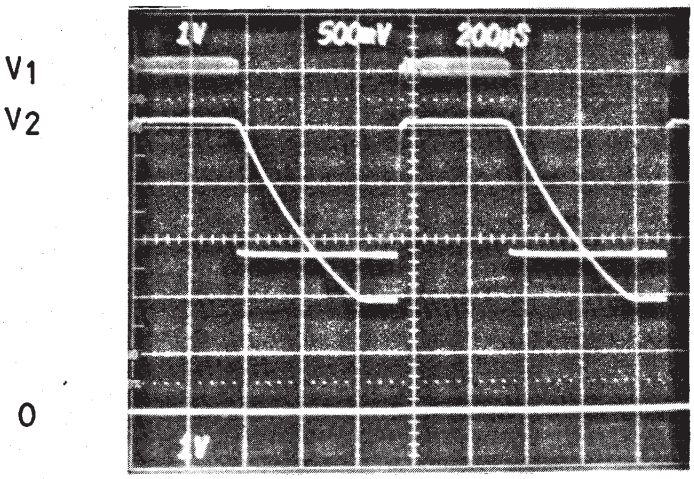


Fig 5. One effect of badly-chosen bias levels. Output is lower waveform

Load capacitance and slewing rate

Followers often have to cope with significant load capacitance. This is most likely to occur when the load is fed via a screened cable and when the load does not terminate the cable in its characteristic impedance. In even the most simple arrangement there will be *some* load capacitance, including that of wiring, pcb tracks and the transistor junctions. So the follower really works into a load that we might simplify to a resistance R_2 in parallel with a capacitance C_2. The design for slewing rate will be no more precise than the estimate of the total load capacitance.

If the time constant C_2R_2 is too large it will prevent the output voltage falling fast enough. A deliberately slowed down example is shown in Fig 6 in which a 1μF capacitor was put across a 470Ω emitter resistor while 1kHz pulses were being handled by an emitter follower.



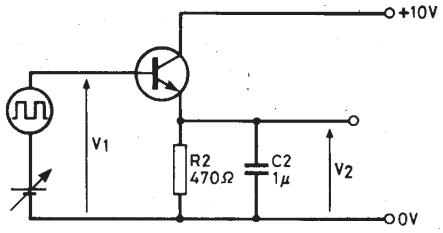


Fig 6. Slewing rate reduced by added load capacitance

There is not likely to be a serious limitation for positive slewing because the load capacitance can be charged rapidly by transistor current, but in the negative-going direction performance is likely to be much worse, and the most important limitation. The greatest rate of change in the negative direction occurs if I_E is suddenly reduced to zero: greatest negative slewing rate = $I_E/C_2 = V_E/(C_2R_2)$. For example, $I_E = 1mA$, $C_2 = 20pF$ gives a slewing rate of 50V/μs. If the load R_L is separate and ac coupled to R_E, $R_2 = R_ER_L/(R_E + R_L)$.

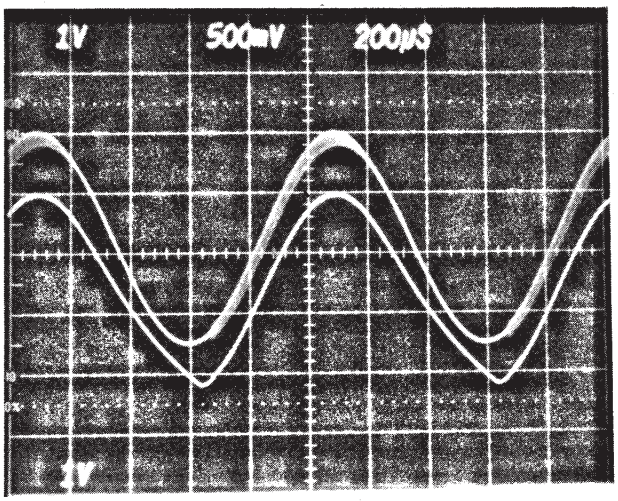


Fig 7. Slewing rate just inadequate, causing distortion of output (lower) waveform

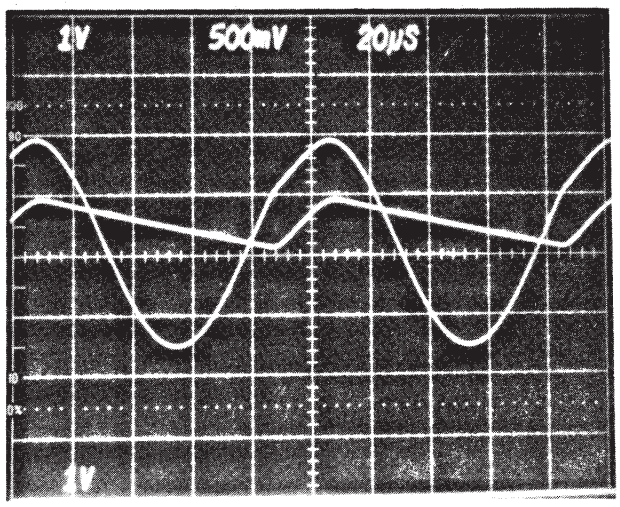


Fig 8. Slewing rate totally inadequate. Output approaching that of a peak detector circuit

For most amateur radio designs we are interested in meeting the slewing rate requirement for an hf sine waveform, and that is given by $2\pi f$ times the peak voltage; eg a 1V peak signal at 10MHz "slews" at a maximum rate of nearly 63V/μs. If the slewing rate is inadequate, the output waveform will distort. In Fig 7 this problem is beginning to show where the emitter (lower) waveform has the characteristic sharpened corner caused by slew-rate limiting. The upper waveform is the input signal. In Fig 8 the problem has become absurdly exaggerated by an increase in frequency, and the output waveform is more typical of an amplitude detector than of a voltage follower!

High frequency input impedance

Predicting when the input resistance will go negative.

One of the best-known oscillator circuits looks exactly like a follower with capacitance added at the output and with an inductor across its input. Such a Colpitts oscillator is shown in Fig 9. Even if no capacitors are deliberately included, unavoidable stray and device capacitances remain. So a follower is always a potential oscillator and it can easily become one.

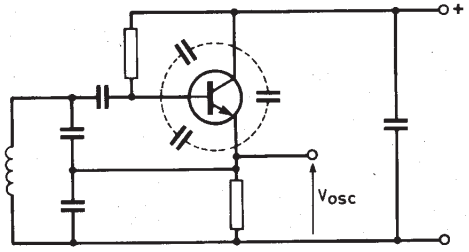


Fig 9. Colpitts oscillator

By happy mischance, during waveform photography for this article a nearby vhf radio emitted sounds of interference, and it was noticed that waveforms (such as Figs 6 and 7) were blurred at the same time as the interference was heard. The emitter follower under test was oscillating at vhf.

Very thorough hf design needs sophisticated software and, more of a problem, a lot of data to feed in to the calculations. So the tendency is to skip it altogether. This is a pity because the simplest of all hf transistor models for calculation can give useful predictions (see Fig 10 and Appendix B). The only transistor data needed are I_E, h_{fe} and either f_{beta} or f_T (or, for a fet, g_m and interelectrode capacitances).

Access to a Hewlett Packard 4192A impedance analyser gave an opportunity to see if simple calculations of hf performance had any value, and the answer is yes (at least up to the 13MHz limit of measurements possible with this instrument). With a BC108 emitter follower and a 2N5459 source follower it was found that the analysis gave approximate but useful predictions in respect of input capacitance and resistance. The gain predictions were sensible but not tested with any precision on this occasion.

Some typical results for effective parallel input resistance R_{in} and capacitance C_{in} are shown in Figs 11 to 14. The curves show the computer predictions and the circles are practically measured values. The main

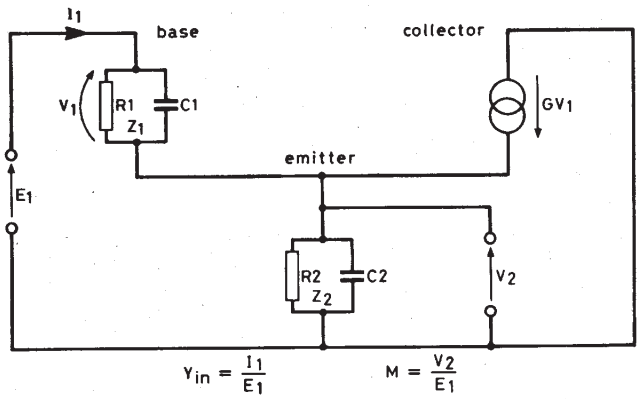


Fig 10. Simplest transistor circuit model for hf

feature, at first sight, is the remarkable variation of R_{in} with frequency. It dashes off to infinity at some critical frequency, reappearing from minus infinity and thereafter approaches zero from the negative side as frequency increases. The algebra suggests, and the calculations confirm, that a rough estimate of the critical frequency can be made as:

$$f_{crit} = \sqrt{f_E f_{beta}} \quad \text{..... see Appendix B .....} \quad (10)$$

To cope with the negative input resistance and prevent unwanted oscillation, it may be necessary to shunt the input with positive resistance **lower** in magnitude than the offending negative resistance. Since the latter gets smaller as frequency rises, it may also be necessary to "kill" the follower action at vhf by adding some series resistance at the input or a lossy ferrite bead.

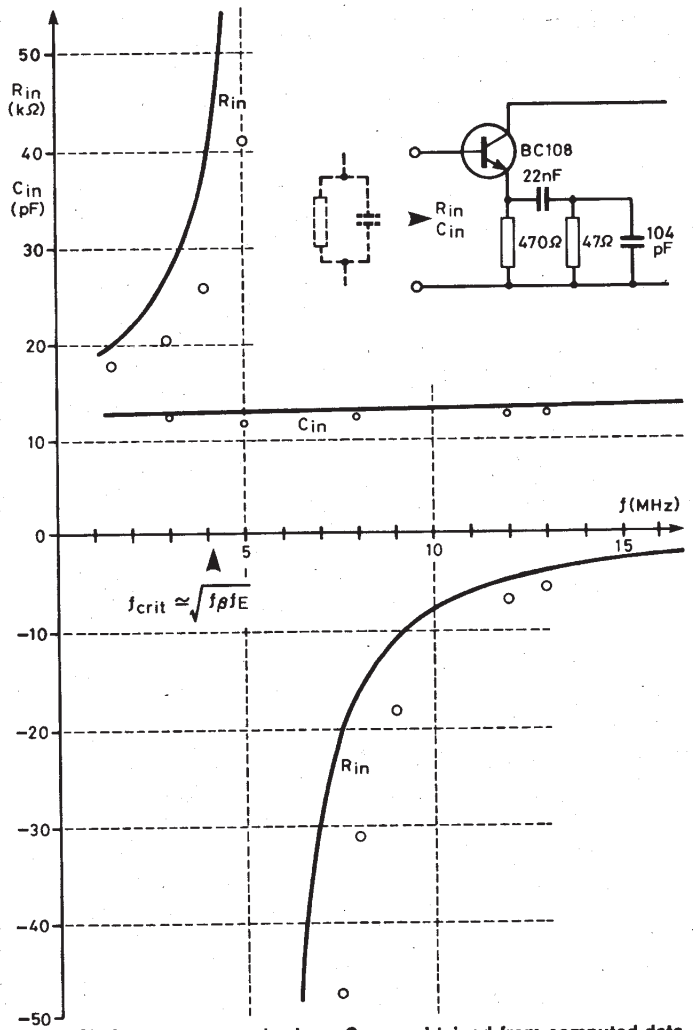


Fig 11. Circles are measured values. Curves obtained from computed data. $f_{crit} = \sqrt{f_{beta}\, f_E}$ is approximate predicted frequency at which R_{in} reverses sign

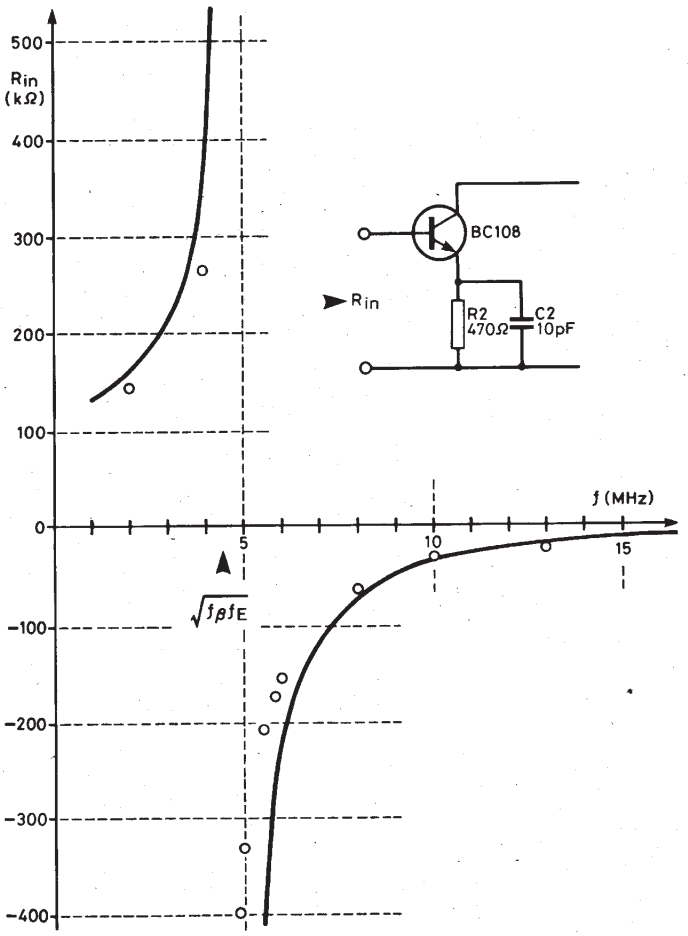


Fig 12. Showing how quite a small capacitance across the load has an important effect upon input resistance

Input capacitance

Follower input capacitance appears to be a well-behaved function of frequency, and one is inclined to dismiss it as of no great importance. This

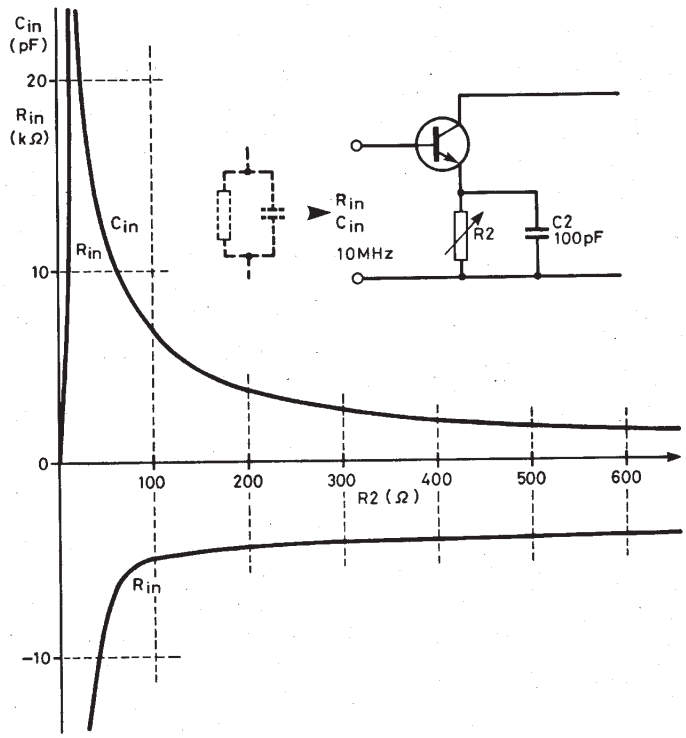


Fig 13. How load resistance affects R_{in} and C_{in}

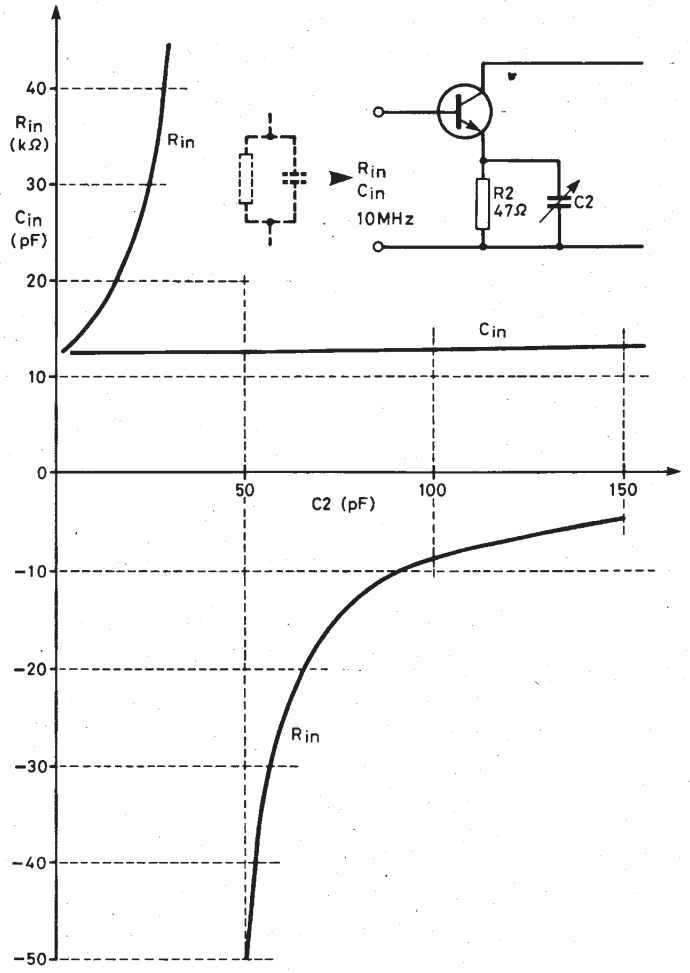
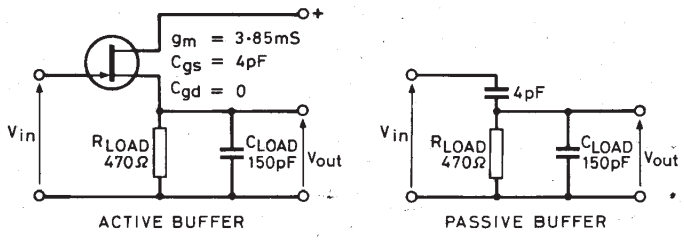


Fig 14. How load capacitance affects R_{in} and C_{in}

could be misleading on those occasions when a follower is a vital buffer in an unusually-sensitive part of the system, such as a master oscillator.

The most interesting feature of a buffer amplifier is the way in which its input impedance is affected by changes in the impedance of its load. To make this clearer for an emitter follower, the load resistance and capacitance were separately varied in computation. Typical results are shown in Figs 13 and 14. Note that: input capacitance is most affected by load resistance changes; input resistance is most affected by load capacitance changes.



R_{LOAD} (Ω)	C_{LOAD} (pF)	f (MHz)	Voltage gain Vout/Vin		Input capacitance (pF)		Input resistance (kΩ)	
			Active	Passive	Active	Passive	Active	Passive
470	150	0·5	0·64	0·006	1·44	3·995	−1600	+13000
470	150	1·0	0·64	0·011	1·49	3·982	−408	+4050
470	150	3·0	0·58	0·021	1·90	3·932	−54·6	+1070
470	150	5·0	0·50	0·024	2·40	3·913	−26·3	+831
470	150	10·0	0·34	0·025	3·21	3·900	−14·4	+730
370	150	10·0	0·33	0·025	3·19	3·904	−15·3	+591
470	50	10·0	0·56	0·063	1·98	3·787	−16·3	+119

Fig 15. Active and passive buffer circuits compared. (The passive buffer is merely the 4pF capacitor!)

Followers as buffer stages

Using these ideas and the computer program provided, an estimate can be made of the buffering action of a follower in its most common role of protecting a sensitive circuit from load changes. Instead of just hoping for the best, one can predict the kind of changes in input resistance and capacitance likely to be caused by changes in load resistance and capacitance, and can ensure that the desired signal levels can be handled.

It is always worth keeping in mind that a passive network, ie using no transistors at all, can offer very effective and predictable performance as a buffer. If the signal input is a lot bigger than is really needed, a simple potential divider can give excellent performance. A typical case is shown in Fig 15 where a humble 4pF capacitor is used as the buffer and its performance compared with that of a source follower. Apart from the reduction in signal level, the passive circuit is an excellent buffer.

It is possible to use the program for such passive circuits by choosing appropriate circuit parameters and by "turning off" the transistor simply by setting its $g_m = G$ to zero. Predictions should be good because they no longer involve the complexity of transistor action.

```
1 R1=1333
2 R2=50
3 C1=239
4 C2=150
5 G=200
100 REM Alter lines 1-5 as required. Units are Ohm, pF, mS
110 REM Emitter or Source Follower---G4FHU Program on RML480Z
120 G1=1/R1
130 G2=1/R2
140 H=6.28318
150 G=G/1000
160 PRINT"f MHz","V Gain","Angle","Cin pF","Rin Ohm"
170 FOR I=1 TO 13
180   READ F
190   W=H*F*1E-6
200   A=G+G1:B=W*C1:C=A+G2:D=W*(C1+C2)
210   P=G1*G2-W*W*C1*C2
220   Q=W*(C1*G2+C2*G1)
230   M=SQR((A*A+B*B)/(C*C+D*D))
240   N=ATN(B/A)-ATN(D/C)
250   Y=SQR((P*P+Q*Q)/(C*C+D*D))
260   J=P*C+Q*D:K=Q*C-P*D:L=C*C+D*D
270   R=L/J
280   S=K/(L*W)
290   N=N*360/H
300   PRINT F,M,N,S,R
310 NEXT I
320 PRINT
330 PRINT"R1=";R1,"R2=";R2,"C1=";C1,"C2=";C2,"gm=";G*1000
340 DATA.01,.02,.05,.1,.2,.5,1,2,5,10,20,50,100
350 REM----------Essential Program ends here----------
1000 RESTORE
1010 INPUT"1 = END       2 = Set up new conditions";X
1020 IF X=1 THEN 1280
1030 IF X=2 THEN 1050
1040 GOTO1000
1050 INPUT"1 = Bipolar    2 = FET";X
1060 IF X=1 THEN 1090
1070 IF X=2 THEN 1230
1080 GOTO1050
1090 INPUT"input the current gain hfe";H1
1100 INPUT"which do you have ?  1 = fT      2 = fbeta";X
1110 IF X=1 THEN 1140
1120 IF X=2 THEN 1170
1130 GOTO 1100
1140 INPUT"fT in MHz";F1
1150 F2=F1/H1
1160 GOTO 1180
1170 INPUT"fbeta in MHz";F2
1180 INPUT"Ie, emitter bias current (mA)";I1
1190 R1=25*H1/I1
1200 C1=1000000/(H*F2*R1)
1210 G=40*I1
1220 GOTO 1260
1230 INPUT"FET gm in mS (mA/V)";G
1240 INPUT"FET Cgs (pF)";C1
1250 R1=1E+9
1260 INPUT"Effective Load R2,C2  (Ohm,pF)";R2,C2
1270 GOTO 100
1280 END
```

Summary

When designing an emitter or source follower, the crucial requirements are that the output signal should move far enough and fast enough and that the input resistance and capacitance are predictable. The methods shown make this possible without much effort and with no need for unusual data.

To minimise the effort required, the complex algebra has been cut off at the point where a computer program is the most effective means of evaluation (that is why, for example, Appendix A ends before explicit

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expressions for C_{in} and R_{in} are reached). For use once only there is no need to set up any of the program from line 1000 onwards, but for tackling a lot of calculations this extra part will prove worthwhile.

Appendix A

With R_L ac coupled via a capacitor, the greatest possible negative peak voltage output occurs when I_E is suddenly cut off so that the bias voltage V_E stored on the capacitor is shared by resistors R_E and R_L. The output V_N is the partial voltage across R_L which is:

$$V_N = V_E R_L/(R_E+R_L) \quad \text{See Fig 3(b)} \quad (1)$$

Also, when the signal is at the other extreme, ie positive:

$$V_P = V_{CC}-V_S-V_E \quad \text{See Fig 3(c)} \quad (2)$$

The quantities V_N, V_P and R_L are already specified by the design requirements. V_s can be chosen above an unavoidable minimum. It is not obvious from (1) and (2) how we may choose V_{CC}, V_E and R_E, but with some rearrangement:

$$K = R_E/R_L \quad (3)$$

$$V_E = V_N(1+R_E/R_L) = V_N(1+K) \quad (4)$$

$$I_E = V_E/R_E = V_N(1+K)/R_L \quad (5)$$

$$V_{CC} = V_P + V_E + V_S = V_P + V_S + V_N(1+K) \quad (6)$$

These minimum values are plotted in Fig 4, which makes much clearer how one can trade one decision against another by choosing the resistance R_E to set the ratio $K = R_E/R_L$.

Appendix B

Using the circuit model of Fig 10.

Voltage gain

$$M = V_2/E_1 = V_2/(V_1+V_2) = Z_2(I_1+GV_1)/[V_1+(I_1+GV_1)Z_2] \quad (7)$$

$$V_1 = I_1Z_1 \; ; \; Y_1 = (1/R_1)+jwC_1 \; ; \; Y_2 = (1/R_2)+jwC_2 \quad (8)$$

$$M = (Y_1+G)/(Y_1+Y_2+G) = [(G_1+G)+jwC_1]/[(G_1+G_2+G)+jw(C_1+C_2)] \quad (9)$$

$$\text{M magnitude} = \sqrt{[(G_1+G)^2+(wC_1)^2]/[(G_1+G_2+G)^2+w^2(C_1+C_2)^2]} \quad (10)$$

Input admittance

$$Y_{in} = 1/Z_{in} = I_1/E_1 = (E_1-V_2)Y_1/E_1 = Y_1(1-M) \quad (11)$$

$$Y_{in} = (1/R_{in})+jwC_{in} = Y_1Y_2/(Y_1+Y_2+G) \quad (12)$$

$$Y_{in} = [(G_1G_2-w^2C_1C_2)+jw(C_1G_2+C_2G_1)]/[(G_1+G_2+G)+jw(C_1+C_2)] \quad (13)$$

Critical frequency

(at which R_{in} rises to infinity and returns from minus infinity)

$$f_{crit} = 1/[2\pi\sqrt{T_1T_2-(T_1+T_2)T_3}] \quad (14)$$

where $T_1 = C_1R_1$, $T_2 = C_2R_2$, $T_3 = (C_1+C_2)/(G_1+G_2+G)$ (15)

also $f_{beta} = 1/[2\pi T_1]$ and we may define $f_E = 1/[2\pi T_2]$ (16)

The quantity f_E is that at which the emitter circuit impedance falls by 3dB below its dc value. (R_2 is R_E and R_L in parallel and C_2 is the total capacitance across the output.)

If $G >> (G_1+G_2)$ then a useful approximation is:

$$f_{crit} = 1/[2\pi\sqrt{T_1T_2}] = \sqrt{f_E f_{beta}} \quad (17)$$

This rough estimate of f_{crit} seems to hold well if the answer is not too many times larger than f_{beta}, ie if C_2R_2 is a significant time constant.

Appendix C

For the bipolar predictions the parameters $R_1 = h_{ie}$ and $G = g_m$ were established in a separate dc test, and $C_1 = C_{be}$ was deduced indirectly from a measurement of h_{fe} at 200MHz. In normal design one would not go to that trouble but use estimates as follows:

$$G = g_m = 40\,I_E \quad \text{result in ms (milli-Siemens) if } I_E \text{ in mA} \quad (18)$$

$$R_1 = h_{ie} = h_{fe}/g_m \quad (19)$$

$$f_{beta} = f_T/h_{fe} \text{ and } C_1 = C_{be} = 1/(2\pi R_1 f_{beta}) \quad (20)$$

A fet will have a gate-source resistance that is unknown but very high. In a program it can be set to, say, 1E9 to serve as infinity (some machines insist on the format 1E+9 by the way). The fet values $C_1 = C_{gs}$ and $G = g_m$ will normally be a lot less than the corresponding bipolar figures and the most obvious results are a much higher input resistance, but a much lower frequency at which it becomes negative. The voltage gain is also noticeably lower. □