



This diagram illustrates the hardware architecture for an ov7670 camera interface. The system is composed of several key components:

- Clocking Wizard (clk\_wiz\_0):** Receives the system clock (sys\_clock) and an input (i\_0) to generate three clock outputs (clk\_out1, clk\_out2, clk\_out3).
- Debounce (debounce\_0):** A simple debouncer that takes an input (i\_0) and produces a clean clock signal (clk).
- ov7670\_controller\_0:** The central interface to the camera. It receives the clean clock (clk) and a reset signal (resend). It outputs control signals (sioc, siod, reset, pwn, xclk) to the camera and status signals (config\_finished).
- POWER\_ON\_RESET\_CONTROLLER\_1\_0:** Manages the power-on reset logic, receiving a reset signal and outputting NOT\_RESET\_OUT.
- AL422B\_WRITE\_0 and AL422B\_READ\_0:** These blocks handle the AL422B camera's write and read operations. They interface with external memory (MEM\_FILLED\_0) and control signals (NOT\_WE\_0, NOT\_WRST\_0, NOT\_OE\_0, NOT\_RRST\_0, NOT\_RE\_0).
- ov7670\_capture\_0:** Captures the camera's output. It receives the camera's clock (pclk), resolution (rez\_160x120, rez\_320x240), vsync, href, and d[7:0] signals. It outputs a 11-bit data stream (dout[11:0]) to the Block Memory Generator and an Address\_Generator\_0.
- Block Memory Generator (blk\_mem\_gen\_0):** Provides BRAM\_PORTA and BRAM\_PORTB for data storage and retrieval.
- Address\_Generator\_0:** Generates addresses for the Block Memory Generator based on the camera's resolution and vsync signals.
- VGA\_0:** Converts the camera's output into a standard VGA format. It receives the camera's clock (CLK25), resolution (rez\_160x120, rez\_320x240), and blanking signals (Nblank, activeArea, Nsync). It outputs Hsync, Vsync, and RGB signals.
- RGB\_0:** Processes the VGA signals to produce the final video output: R\_0[3:0], G\_0[3:0], B\_0[3:0], Hsync\_0, and Vsync\_0.