CEL California Eastern Laboratories

AN1035

Design Considerations for a Ku-Band DRO in Digital Communication Systems

ABSTRACT

This application note will review the process by which Dielectric Resonator Oscillator (DRO) designers choose their oscillator's topology and devices based on performance requirements, real estate constraints and manufacturing yields concerns. DROs are attractive microwave sources because of their high Q, low phase noise, good output power and high stability versus temperature. They represent a good compromise of costs, size, and performance compared to alternative signal sources such as cavity oscillators, microstrip oscillators or multiplied crystal oscillators.

Using the local oscillator of a Ku-Band Low Noise Block (LNB) in a Digital Direct Broadcast System (DDBS) application as a practical example, this article will demonstrate a DRO design at 11.25 GHz with one of NEC's new super low cost plastic package MESFETs. The required system specifications as well as the design's performance will be presented. The paper then discusses choosing an appropriate device and how phase noise parameters are included in the nonlinear model. Upon reviewing basic DRO topologies and focusing on a reflection type oscillator, the paper proceeds with a linear and nonlinear simulation using HP-EEsof's SERIES IV to accurately predict the DRO performance. Measured results and practical "on the bench optimization" methods will then be considered. Finally, as cost is of paramount importance to designers of commercial products, a total cost summary of

the parts for the DRO and mechanical assembly will be presented. While the design proposed might not yield the optimum design solution for all DBS applications, it does introduce a few important DRO design techniques that can be applied to other high frequency communication systems.

SPECIFICATIONS

In a DDBS system application, the DRO must exhibit low phase noise in order to meet the digital modulation scheme and Bit Error Rate (BER) requirements. It also must have minimal frequency drift over temperature to keep the receiver locked into the selected channel and should provide enough output power to directly drive the mixer downconverter (usually a diode ring or an active GaAs FET mixer). Because the DC supply is usually supplied through the IF feed from an indoor unit, voltage requirements are usually not a constraint with as much as 8 V available from the system. However, current draw remains a limitation and needs to be set to the lowest value that will allow meeting the output power specifications. Finally, DBS applications drive the need for a design that is both compact and light since the LNB will be a small outdoor unit located at the focal point of an antenna through a light supportive pole. These last needs were met by using 0603 (60 mils by 30 mils components) SMT technology components and by laying out the components within a tightly enclosed cavity. These choices resulted in a .950" by 0.750" by 0.500" final design that also includes the metal

PARAMETER	UNITS	SPECIFICATION	SIMULATION	MEASURED PERFORMANCE
Supply Voltage	(V)	8 ± 0.25	6.0	6.0 ± 0.25
Supply Current	(mA)	20 ± 2.5	18	18
Operating Frequency Range	(GHz)	11.25	11.25	11.25
Output Power (50 ohms)	(dBm)	7 ± 2.5	7.2	6.5
Phase Noise at 1 KHz	(dBC/Hz)	-58	-61.3	-62.8
Phase Noise at 10 KHz	(dBC/Hz)	-80	-91.3	-89.4
Phase Noise at 30 KHz	(dBC/Hz)	-90	-	-97.6
Phase Noise at 100 KHz	(dBC/Hz)	-100	-120.4	-112.3
Phase Noise at 1 MHz	(dBC/Hz)	-120	-131.2	-130.0
Freq. pushing (V$_{CC}$ = 6 V ± 0.25 V)	(KHz)	±800 max	Not simulated	±200
Freq. pulling (VSWR = 2.0:1 at all phases)	(MHz)	±2	Not simulated	±1
Harmonics	(dBC)	-40 min	-20 min	-50 min
Spurious	(dBC)	-80 min	N/A	-80 min
Output impedance (in a 50 Ω system)	N/A	VSWR ≤ 2.0:1	Not simulated	VSWR ≤ 1.5:1 (With Buffer)
Operating temperature	(°C)	-55 to +80	Not simulated	-55 to +80
Temperature stability	(MHz)	±2	Not simulated	±700 KHz

Table 1. Digital DBS DRO: Goal, simulation and test results.

cavity, the tuning screw and output connectors. The enclosed **Table 1** summarizes the design goals, simulated performance and final laboratory results.

DEVICE CHOICE AND CHARACTERISTICS

Designers of high volume commercial products share common goals: high performance, small size, low costs and high manufacturing yields. When choosing a device, the choices are many: Silicon Bipolars, Si MOSFETs, GaAs FETs or Gunn/IMPATT diodes [1]. In all cases, to achieve a clean oscillation and good phase noise performance, the criteria should include a low noise figure and enough loop gain at the maximum operating junction temperature and under large signal conditions. The silicon bipolar is a natural for low noise oscillators due to its well-characterized and repeatable parameters and an intrinsic excellent phase noise performance. However, for any good steady oscillating operation, a good rule of thumb is to use a transistor with a f_T at least two to three times the operating frequency. These conditions would require medium output power silicon transistors with a f_T between 23 and 35 GHz. Such devices, currently under development, are not yet readily available for high volume manufacturing. However, DRO designs up to X-Band are now easily attainable with a silicon solution. Because of similar high frequency requirement, Si MOSFETs are better suited choices at lower frequencies. Gunn and IMPATT diodes make excellent very high frequency devices (50 GHz and above), but their high phase noise, need for careful mechanical design and very low power efficiency make them an unsuitable choice for high volume consumer applications. This elimination process leaves the GaAs FETs the most suitable device to meet the **Table 1** specifications because they naturally exhibit a very high f_T, a good loop gain and enough output power in Ku-Band and up to 25 GHz.

To meet the needs of Ku-Band oscillator designers, NEC developed the NE72218, a new epitaxial grown, recessed gate GaAs MESFET that provides high performance and low phase noise for oscillators up to 14 GHz. Housed in a single SOT-343, 1.25 x 2 mm four pin surface mount plastic package, this component is ideally suited for high volume, high density SMT assembly. With a high I_{DSS} rank, the NE72218 can also offer enough output power under different biases to drive most Ku-Band mixers even where a resistive buffer has been added. Finally, NEC optimized its ion implantation technology to minimize the device's flicker noise and provide the lowest 1/f noise performance currently available with GaAs devices. This parameter will directly impact the DRO's phase noise performance.

DEVICE NONLINEAR MODEL DEVELOPMENT

The choice of a nonlinear model for a FET is determined by evaluating the DC characteristics of the device and comparing these measured characteristics to characteristics of available nonlinear models. Different models implement the DC I-V curve equations differently [8]. For the device under consideration, NEC's NE72218, it was determined Triquint's Own Model (TOM) would best represent the I-V curves because the MESFET showed an almost linear increase in drain current with increasing drain voltage at lower gate voltages and an approximately constant drain current with respect to increasing drain voltage at higher gate voltages.

The first step in the extraction process is to extract DC model parameters so the model reflects the measured I-V curves. From **Table 2**, the main DC parameters affecting the I-V curves are VTO, ALPHA, BETA, GAMMADC, Q, DELTA, RG and RS. A good fit to the AC data cannot be achieved until a good DC fit is obtained. When the model accurately predicts the device's DC characterization, AC parameters can then be adjusted. The TOM model parameters that most affect the AC prediction of the model are GAMMA, TAU, CDS, CGSO, CDSO, RG, RS and the package parasitics (see **Figure 1**) Once the DC and AC performance of the model is satisfactory, the model can be optimized to fit measured power and noise data (including 1/f noise), where applicable.

Model parameters typically affect more than one type of simulation response. The value of a parameter that results in the model providing the best S-parameter fit may not provide the best fit to measured noise data across a wide range of biases and frequencies. California Eastern Laboratories develops nonlinear models to fit the widest range of biases, frequencies and applications as possible. There is usually a trade-off in device model performance when developing this type of model. In general, the DC and AC parameter prediction is approximately equivalent. Then, depending on the targeted application of the device, either the power or the noise performance of the device model is optimized. Sometimes the AC performance of the model is slightly degraded to improve the power or noise prediction of the model. However, the parameters AF and KF are the only model parameters which affect 1/f noise prediction and no compromises to the AC performance need to be made.

Device model extraction results

The device model for the NE72218 was extracted over the following ranges:

DC: Vds=0V to 5V, Vgs=0V to -1.4V
AC: Vds=2V to 4V, Id=10mA to 40mA,
    frequency=0.5GHz to 18GHz
1/f : Vds=3V, Id=30mA and Vds=3V, Id=40mA.

Figure 1 and **Table 2** presents the final device model and **Figures 2-5** compare the results of the extracted device model to the measured data. S-parameter comparisons (**Figures 2-5**) are shown at the desired DRO bias of Vds=4V, Ids=20mA. **Figure 6a,b** shows the measured and modeled 1/f noise at Vds=3V, Ids=30mA and Vds=3V, Ids=40mA.
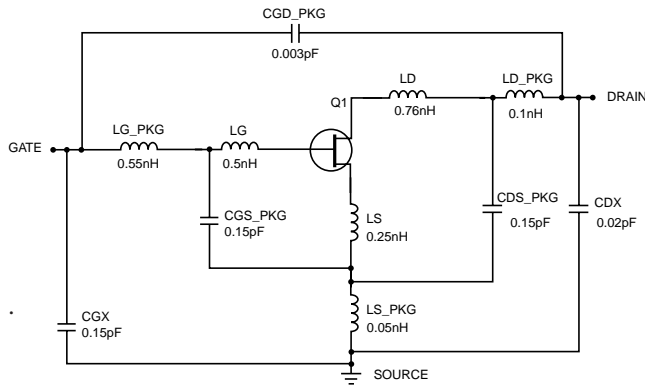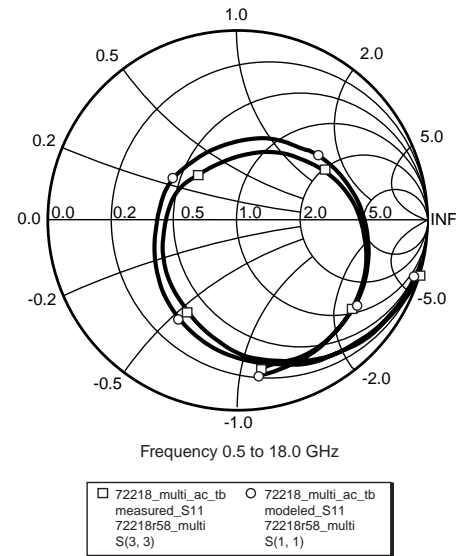
Figure 1.   NEC NE72218 Nonlinear Model Schematic

Frequency 0.5 to 18.0 GHz

□ 72218_multi_ac_tb measured_S11 72218r58_multi S(3, 3)	○ 72218_multi_ac_tb modeled_S11 72218r58_multi S(1, 1)

Figure 2. NEC NE72218 Measured vs. Modeled S11

LIBRA PARAMETER	PARAMETER VALUE	DEFINITION
VTO	-1.8065	Nonscaleable portion of the threshold voltage
VTOSC	0	Scaleable portion of the threshold voltage
ALPHA	2.5	Current saturation parameter
BETA	0.0396	Transconductance parameter or coefficient
GAMMA	0.072	AC drain pull coefficient
GAMMADC	0.03	DC drain pull coefficient
Q	1.8	Power law exponent
DELTA	0.3	Output feedback coefficient
VBI	1	Built-in gate potential
IS	1e-14	Gate junction reverse saturation current
N	1.3	Gate junction ideality factor
RIS	0	Source end channel resistance
RID	0	Drain end channel resistance
TAU	4e-12	Transit time under gate
CDS	0.27e-12	Drain-source capacitance
RDB	5000	Dispersion source output impedance
CBS	1e-10	Dispersion source capacitance
CGSO	0.85e-12	Zero bias gate-source junction capacitance
CGDO	0.055e-12	Zero bias gate-drain junction capacitance
DELTA 1	0.3	Capacitance saturation transition voltage parameter
DELTA 2	0.3	Capacitance threshold transition voltage parameter
FC	0.5	Coefficient for forward bias depletion capacitance
VBR	Infinity	Gate-drain junction reverse bias breakdown voltage
RD	4	Drain ohmic resistance
RG	10	Gate ohmic resistance
RS	4	Source ohmic resistance
RGMET	0	Gate metal resistance
KF	2e-10	Flicker noise coefficient
AF	1.5	Flicker noise exponent
XTI	3	Temperature exponent for saturation current
EG	1.43	Energy gap or band gap voltage
VTOTC	0	VTO temperature coefficient
BETATCE	0	BETA exponential temperature coefficient
FFE	1	Flicker noise frequency exponent

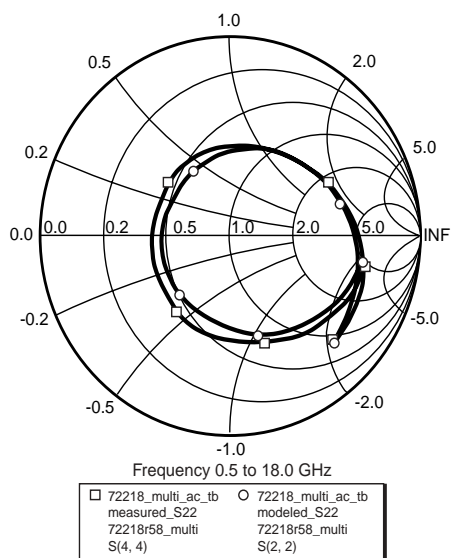Table 2. Triquint's own model (TOM) parameters for the NE72218 nonlinear model

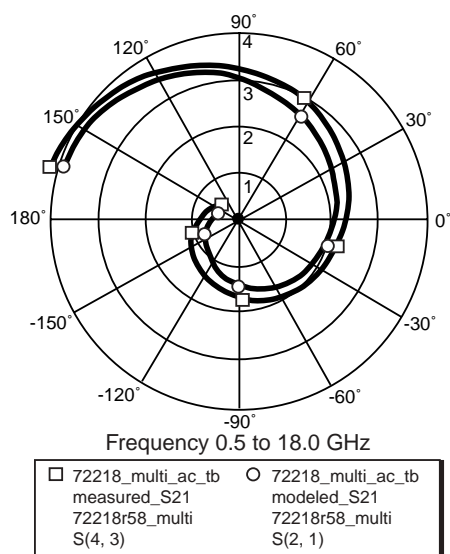Figure 3. NEC NE72218 Measured vs. Modeled S22

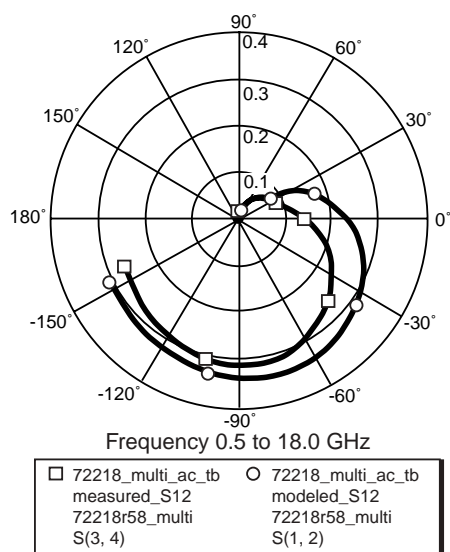Figure 4. NEC NE72218 Measured vs. Modeled S21

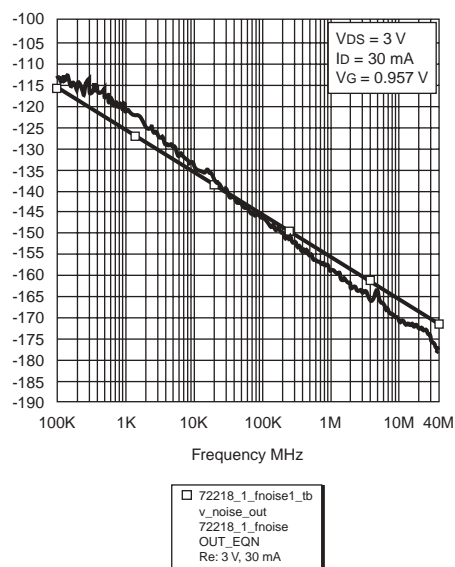
Figure 5. NEC NE72218 Measured vs. Modeled S12
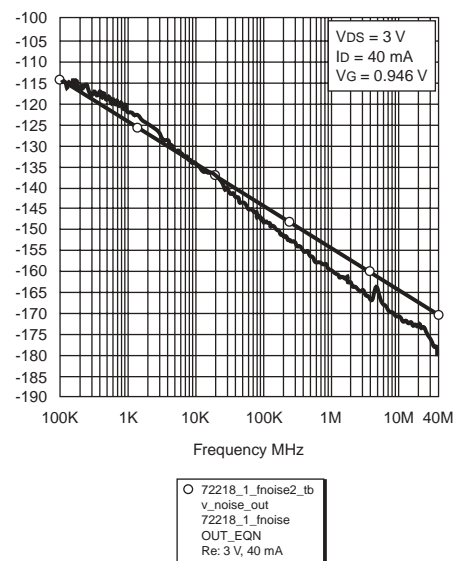

Figure 6a. NEC NE72218 Measured vs. Modeled 1/f Noise

Figure 6b. NEC NE72218 Measured vs. Modeled 1/f Noise

CHOICE OF TOPOLOGY

There are essentially four different classes of DROs that can be designed: Reaction, transmission, parallel-feedback and reflection DROs. A reaction DRO is a free running oscillator with enough appropriate feedback to oscillate in the desired frequency range. The frequency of oscillation is then stabilized with a Dielectric Resonator (DR) on the output. Because of the design method, this oscillator usually has a high spurious content and does not provide low phase noise [4]. The parallel-feedback and the transmission DRO uses the DR between two transmission lines to provide the frequency selective loop feedback between the input and the output of an amplifier design. Usually, these two configurations do not allow too much adjustment during on-the-bench tuning and are generally complex to model with a simulator. Because of the tight enclosure required in LNB designs, most DROs display some level of feedback within the cavity. In most cases, however, that effect is both undesired and rarely simulated. Finally, the reflection type DRO uses the concept of negative resistance in which the resonator is placed near a terminated microstrip line connected to the input port of an unstable amplifier. Near its resonant frequency, the dielectric resonator reflects power back to the amplifier, causing an oscillation build-up between the two components that can be tapped into. In this configuration, the coupling between the resonator and the transmission line is easier to model and spurious oscillations are more readily avoided. **Figure 7** shows the topology that will be used for this DRO design.
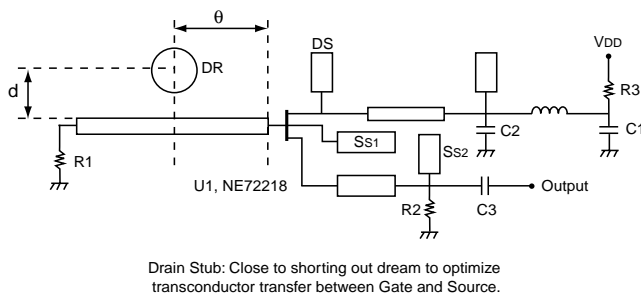

Drain Stub: Close to shorting out dream to optimize transconductor transfer between Gate and Source.

Figure 7. DRO Schematic

DRO DESIGN THEORY

General Electrical Considerations

The two most challenging aspects of the design will be to meet the low phase noise specifications and the frequency stability over temperature. Studying Leeson's equation [3] provides some insight into the factors that affect the phase noise of an oscillator. These parameters are studied in depth in reference [5]. However the important rules of thumb that should be remembered to optimize this design for low phase noise are:

• Maximize the loaded Q (Q_L) of the tuned circuit. This goal will be achieved with a very high Q unloaded dielectric resonator that will only be lightly coupled to the circuit to limit loading effects.

• Choose a device with a low flicker noise. The 1/f noise characteristic of the NE72218 (**Figure 6**) makes this device a prime choice for the application.

• Maximize the power at the input of the oscillator (High P_{avs}). A light coupling of the DR will ensure that most of the circuit's available power is stored in the DR and available at the FET's gate.

In addition, the phase noise is also dominated by Signal to Noise Ratio at the input (SNR_I) which depends on the noise figure of the active device and on the P_{avs} (power available from the source). Consequently, design rules that make good Low Noise Amplifiers (LNAs) also apply to low phase noise oscillators. Usually, a typical oscillator runs at about 20% efficiency, however, this achievement also depends on how much output power is tapped out of the circuit. A higher output power means higher efficiency, however, this will reduce the circuit's loaded Q, which in turn degrades the phase noise performance. A light output coupling will increase phase noise but reduce the power available to drive the rest of the system. With this trade-off in mind, this particular circuit was set to achieve 5% efficiency to provide a minimum of 6 dBm output power over temperature.

Negative Resistance Amplifier

The most common use of GaAs FET amplifiers at Ku-Band is in the common source configuration. However, without feedback elements, the common source FET transistor does not make a very good oscillator because of its small feedback capacitance from input to output (C_{GD0}=0.055 pF) when compared to other capacitance values in the FET.

Therefore, to generate the required output to input feedback, the design will use a common drain configuration. This structure is very unstable and makes excellent oscillators by using the internal capacitance feedback of the transistor (C_{GS0}= 0.85 pF) instead of external feedback. This configuration will reverse the normal output with respect to ground since the drain will provide the RF grounding and all signals will be referenced to that port. By choosing the appropriate drain open stub length (DS in **Figure 7**), the designer will determine the frequency at which the series negative resistance will be generated on the gate's reflection port. That port should be set to a quarter wavelength at the desired frequency of oscillation. Selecting the correct reactance at the source (Ss1) maximizes the magnitude of the reflection coefficient at the gate terminal. Adjusting these two parameters will provide the required amount of negative resistance at the needed frequency. Adjusting the output matching network and the amount of output coupling (C3) will drive the output power and loaded Q (and therefore the phase noise) of the oscillator. As the amplitude of the oscillation increases, the active devices start saturating, and magnitude of the negative resistance decreases until it is equal to the equivalent resistance presented by the DR at the resonant frequency. For a steady state oscillation to occur, the following condition needs to be met in the input reference plane of the active device:

$$\mathbf{\Gamma}_{in} * \mathbf{\Gamma}_R = 1 \qquad\qquad (1)$$

Where $\mathbf{\Gamma}_{in}$ is the return loss provided by the puck coupled with the transmission line and $\mathbf{\Gamma}_R$ is the greater than 1 reflective coefficient exhibited by the negative resistance amplifier. Consequently, for a given amplifier circuit, the designer will need to adjust the puck coupling both in term of phase (how far the puck should be from the FET) and strength of the coupling (how far the puck should be from the transmission line). Eventually, the oscillator should achieve under steady state oscillation, a loop phase and amplitude of 0 and 1 respectively. Therefore, the next task is to synthesize the gate load by coupling the resonating structure.

Choosing the Puck

As mentioned earlier, the Dielectric Resonator is key to the performance of the oscillator in that it defines the Q of the circuit and locks the frequency. The high unloaded Q (Q_0) results in the super low noise performance and is defined by both dielectric loss tangent of the material and the environmental losses. Recent developments in ceramic material technology have resulted in performance improvements including Q_0 as high as 12,000 at 12 GHz and small controllable temperature coefficients. With proper temperature compensation, nearly constant frequency over temperature can be achieved. This parameter also depends on both the characteristics of the FET's S-Parameters over temperature and the cavity's mechanical expansion coefficient. Finally, the last important parameter defining the DR is the dielectric constant which ultimately determines the resonator dimensions as well as the cavity (and circuit design) dimensions. At present, commercially available temperature stable DR materials exhibit dielectric constants of about 36 to 40. These dielectric resonators also come in different forms and modes, however, the cylindrical shape transverse electric (TE) mode has been widely accepted as the most advantageous one. Numerous references are available describing the advantages of different ratio in height (H) and diameter (D) from dielectric resonator manufacturers [7]. However, a choice of H/D = 0.4 is recommended to avoid spurious modes oscillations and achieve and optimal Q_0.

Coupling the Puck

Choosing the right DR for the application is key to meeting the DRO's specifications, however, fitting use of the puck is as equally important to the DRO's performance. Because of the series negative resistance of the FET in its feedback circuit, the puck is coupled in series to the circuit through a 50Ω line and used in a band reject filter mode. At the desired frequency, the puck will reflect any incoming power back to the FET producing a build-up between the active device and the DR. Coupling between the microstrip and the resonator is accomplished by orienting the resonator's magnetic momentum perpendicular to the microstrip plane at a distance d (**Fig-**

ure 7). The position of the resonator relative to the transmission line determines the oscillator's stability, output power and phase noise. As will be seen in the next sections, optimum positioning can be tricky but is greatly aided by linear and nonlinear simulations. Adjusting d increases or decreases the amount of coupling. A higher coupling provides more output power and robustness of oscillation build-up, however, it reduces the loaded Q and therefore the phase noise performance. A lower coupling will improve phase noise but reduces the output power, and under certain circumstances, the oscillator could fail to start oscillating. Therefore, when designing a low noise oscillator, the compromise will be to set the distance d small enough that the oscillator will always start (under both quick and slow turn-on and at all temperatures) and provides enough power, but large enough to get high loaded Q and low phase noise. Finally, as more energy is stored in the DR, the temperature characteristics of the DRO more closely follow that of the DR. Consequently, a lighter coupling will also provide more control of the LO drift over temperature. The phase relationship of the puck to the active device is as equally critical to efficiently creating an oscillation build-up. The electrical length (θ) (**Figure 7**) representing the physical distance between the FET and the puck's plane of reference will determine how fast and stable the build-up will occur, driving both output power and phase noise performance.

Mechanical Considerations

In a DRO, the electrical layout is only one aspect of the oscillator design. Mechanical interests also highly influence the local oscillator's performance. The cavity's size and height have loading effects on the LO which can reduce the phase noise performance and create an unwanted frequency drift over temperature. Under best conditions, the DR would be free to resonate in free space, but because of obvious real estate consideration, the LO needs to be constrained within a shielded cavity. References [4] and [7] analyze in depth the effects of enclosed cavities, and rules-of-thumb dictate that in order for the cavity to have a reasonable thermal and loading effects, the cavity should be at least three pucks high and three puck's diameter wide. This height requirement is one reason most DRO designers prefer to set their DR on a stand-off, so that the housing or PCB on which the DR usually rests does not affect the resonator's performance. The PCB material's mechanical integrity also needs careful consideration because of LO drift over temperature and long term aging effects, especially if the cavity is resting on the PCB. For example, Rogers 4003 material is hard enough to allow only minimum frequency aging while providing a low tangent loss at 12 GHz. This low insertion loss provides for a low noise figure performance as well as a high Q for the circuit. However, other low loss materials such as Teflon mesh compound do not have the same mechanical integrity and the PCB thickness has a tendency to change over time. Although this has little bearing in an amplifier design, in an oscillator, the cavity and ground plane relations will slowly change over

time, providing a slow LO drift or aging effect that could obsolete the LNB after a few years. Finally, the fine tuning and adjustment of the DRO will be set through a tuning screw that will increase the DR's resonant frequency as it closes the electrical field above the puck. This should provide as much 80 MHz of tuning range. However, it is important to notice that tuning the frequency with a tuning screw is achieved at the cost of reduction in both unloaded Q and temperature stability. This increase in temperature stability is due to the increasing slope of the tuning curve as the metal plate gets closer to the DR surface. Therefore, if no more than about 10 MHz of loading can be achieved, the design will provide a good compromise between adjustment for manufacturing variations and high performance.
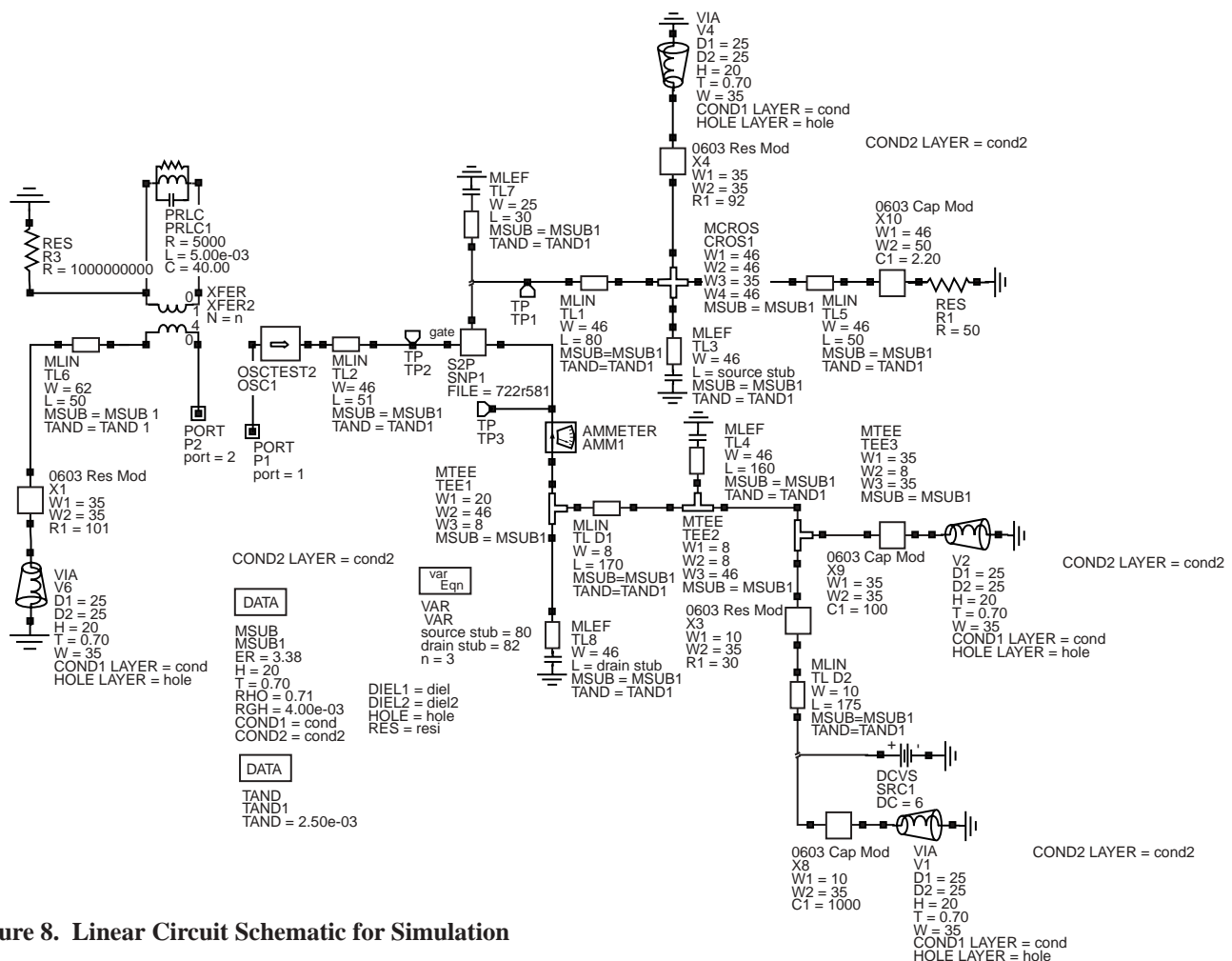
LINEAR CIRCUIT SIMULATION

With the DRO topology elected, designers will first create a first approximation design by using the Touchstone formatted s-parameter files (*.s2p) in a linear simulation. Although its is understood that an oscillator is a saturated circuit that behaves nonlinearly under steady state operation, a linear simulation will provide a good initial circuit layout before fine tuning the design in the nonlinear simulator.

The linear simulation can be used to develop the matching network, determine the appropriate resonator model, and find the appropriate reactive elements that will affect the circuit's performance.

For both simulations, considerable care must be taken to account for the many components and board parasitics in the simulation. At Ku-band, 0.5 nH of parasitic can amount to up to a 40Ω impedance. Therefore, an accurate simulation resulting in a minimum of board tuning in the laboratory can only be achieved through careful modeling of all components utilized by the design, including:

1. Using models for the 0603 resistors and capacitors that include parasitics. Most manufacturers of such components now provide an accurate high frequency model.
2. Carefully modeling transmission lines (lengths and widths), especially in regard to impedance steps, crosses and open stubs with capacitive effects.
3. Using an accurate model of the board characteristics including loss tangent effects and metal deposition thickness.
4. Utilizing via holes and via pads instead of perfect grounds where appropriate.

The final linear simulation circuit utilized is provided in **Figure 8.**

Figure 8. Linear Circuit Schematic for Simulation

Dielectric Resonator Model

The resonator is modeled as a parallel resistor-inductor-capacitor where the value of L and C are adjusted to provided the proper resonant frequency (11.25GHz) and Q factor (**Figure 8**).

The resonant frequency is defined as

$$f_0 = \frac{1}{2\pi \sqrt{LC}}$$

with L and C the modeling equivalent inductive and capacitive elements of the resonator.

The Q is defined as:

$$Q_0 = 2\pi \, \frac{\text{Maximum energy stored}}{\text{Energy dissipated per cycle}}$$

also defined for simulation purpose into the following formula: $Q_0 = \frac{\omega_0}{2} \, \frac{d\phi}{d\omega}$

where ω_0 is the resonant frequency:

$\omega_0 = 2\pi f_0$ and ϕ is the phase of the resonator impedance.

For a parallel resonator at resonance,

$$Q_0 = \frac{R}{L\omega_0} \quad \text{because} \quad \frac{d\phi}{d\omega} = \frac{2R}{L} \quad \text{at resonance.}$$

Therefore, the value of R defines the DR's unloaded Q_0. The more frequency selective the resonator, the larger the derivation and the better the phase noise. Also, off resonance, this derivative diminishes, causing the Q to decrease. Such a resonator model is also provided by Trans-Tech through their program DR which also assists in choosing the right DR part number dependant on the cavity size and required tuning range. In the model, the DR is then coupled to the 50 Ω transmission line through a transformer where the ratio (n) simulates the coupling coefficient β (distance d). When β (or n) is adjusted, the increased or decreased coupling is characterized by the insertion loss of the band stop filter as seen in **Figure 9.** This coupling coefficient will eventually be fine tuned in the nonlinear simulation to minimize the phase noise while keeping an appropriate output power, but initially should be set so that the filter's insertion loss is less than the reflection gain provided by the active device on the gate port (-1.5 dB versus +3.1 dB in **Figure 9**). **Figure 10** also shows the coupled DR's reflection coefficient in the DR plane of reference in a Smith chart to be compared to the FETs' reflection coefficient. Notice that both angles were set to 0° to set the overall loop phase to 0° as well.
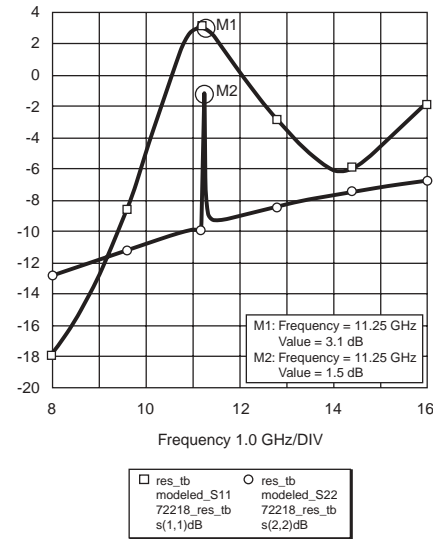

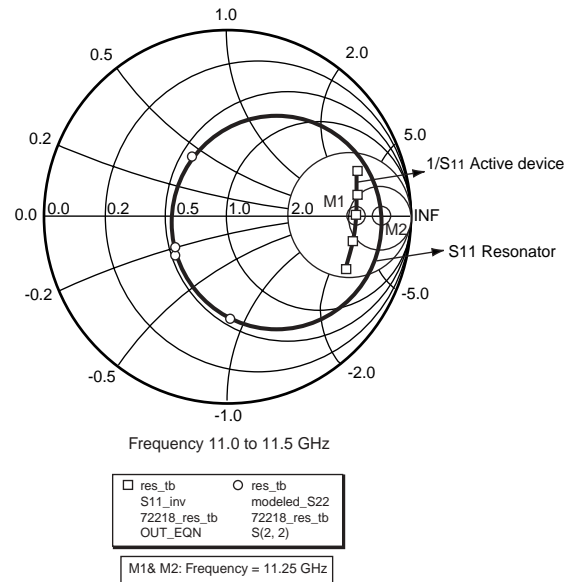**Figure 9. DR and FET Insertion Losses from Linear Circuit Simulation**

Figure 10. DR and FET Reflection Coefficients from Linear Circuit Simulation

Dielectric Resonator Positioning

Once the Dielectric Resonator is modeled (in terms of the parallel RLC network), physical placement of the puck on the board needs to be simulated. This is achieved through the transformer (XFER2) where transform ratio n defines the amount of coupling and through the 50 Ohm transmission line TL2 which introduces the desired amount of phase and adjusts the loop phase. The first location approximation will be done under small signal conditions. However, as the device saturates and its S-Parameters change accordingly, a refinement will be conducted for best output power and phase noise performance during the nonlinear simulation.

Negative Resistance Modeling

From the negative resistance amplifier section, we know that the common drain amplifier should be set so that:
• Its drain will be AC shorted at the frequency of interest providing the required feedback to unstabilize the FET. This is done through TL8, an open stub on the drain that is close to a λ/4 length. The stub is also isolated from the DC supply with a high impedance λ/4 line (TL D1) followed by another λ/4 open stub (TL4). Adjusting TL8 will mostly move the negative resistance peak up and down in frequency. Its length was adjusted so that the maximum negative resistance occurred at 11.25 GHz (**Figure 11**).
• The source reactance will define the amount of negative resistance at the gate. This is achieved by adjusting TL3 in conjunction with the oscillator output network (matched to 50 Ω) and the self-biasing network (X4). TL3 was adjusted to provide about +3 dB gate reflection coefficient but could be increased to provide a higher return gain. However, too much return gain could provide unwanted spurious oscillation due to the non-perfect return loss of the 50 Ω load shorting the gate beyond the DR's placement. The short open stub TL7 models the second source pin of the four pin FET device.
• It will provide a negative resistance on the gate port and a good output match into 50 Ohms.
• The phase delay of the transmission line θ needs to be set to 0 so that (1) condition is respected and a steady state oscillation occurs.

In actuality and for a better understanding of the simulation, designers will consider the parameter $1/S_{11}$ of the active device, since we are interested in $\Gamma_{in} * \Gamma_R \geq 1$ and therefore in

making sure that $\Gamma_{in} \geq \dfrac{1}{\Gamma_R} = \dfrac{1}{S_{11}}$ and that the phase re-

lation is equal to 0° at f_0. These two relations are easily seen in **Figure 10**, where clearly both reflection coefficients have a 0° phase relation and the magnitude relation is respected under small signal conditions. As signal builds-up, $|S11|$ will decrease and both $|1/S_{11}|$ (M1) and the resonator's refection (M2) will merge at the desired frequency where steady state will be reached.
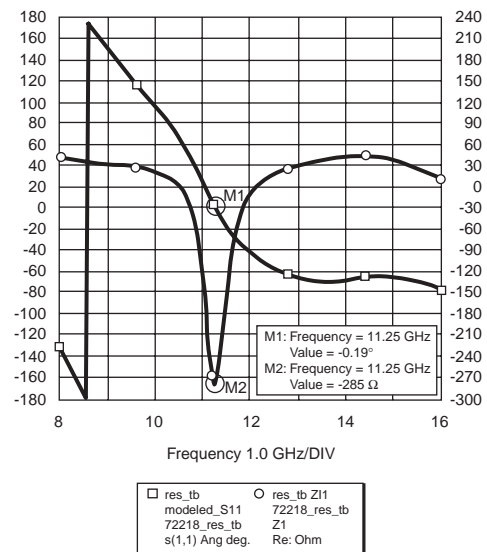

Figure 11. FET Negative Resistance from Linear Circuit Simulation

NONLINEAR CIRCUIT SIMULATION

After tuning the matching circuit and determining the proper resonator model, the nonlinear model can be substituted for the *.s2p file and used to simulate and optimize the phase noise and power performance of the circuit. It should be noted that accurate and complete modeling of the biasing network is needed at this point to ensure the model will more closely predict the actual circuit. The final circuit for the DRO nonlinear simulation is shown in **Figure 12.**

The HP-EEsof Libra simulator simulates the performance of an oscillator in three steps:
1. The simulator looks for the frequency of oscillation,
2. The power output of the oscillator is computed, and
3. The phase noise is calculated.

Difficulties in successfully simulating the oscillator circuit are typically encountered in steps (1) and (2). However, if the linear circuit has been properly optimized for negative resistance, step (1) should result in an oscillation frequency close to that for which the circuit was designed and only small adjustments to the resonator model should be needed. It is more likely problems will be encountered in step (2) and the simulator will be unable to converge on the oscillator's output power. If this problem is encountered, the following steps may help convergence problems:
1. Change the Q of the resonator circuit by varying the R of the parallel RLC,
2. Vary the coupling of the resonator by varying the N of the transformer, or
3. Vary the source and drain stub lengths.
Once convergence is achieved, the above parameters can be modified in small increments to achieve the circuit performance while still ensuring convergence.

Using the schematic of **Figure 12**, the simulator predicted the results shown in **Figures 13** and **14**. Compared to the measured performance (**Table 1**), it can be seen the simulation was useful in predicting actual circuit behavior.

Figure 12. **Nonlinear Circuit Schematic for Simulation**

Figure 13. **Phase Noise, Power, and Bias from the Nonlinear Circuit Simulation**

Figure 14. **Power Harmonics from the Nonlinear Circuit Simulation**

CIRCUIT TESTING

Upon achieving satisfying results with the simulation and choosing the appropriate circuit values for the different components, a prototype board was constructed and tested for compliance with the proposed specifications. When turned on, the DRO exhibited a lower than expected output power (+2 dBm) and the tuning range (via the tuning screw) was less than the preferred 100 MHz minimum range, even after optimizing the puck placement. This was due to non-optimal length of the two tuning stubs (Source and Drain). Decreasing the length of the drain stub by about 20 mils brought back the oscillator's center frequency to 11.25 GHz, slightly increased the output power and provided the required tuning range. Decreasing the source stub granted the expected output power (6.5 dBm). During that process, no tuning element values (capacitor or resistors) had to be modified and it was also verified that the oscillator would not have spurious oscillations at undesired frequencies by removing the puck. If an oscillation occurs without the resonator, it means that the FET provides too much gain or the circuit has too much indirect feedback. Such spurious oscillation has a loading effect on the circuit and seriously reduces the DRO's phase noise performance. Self-oscillation problem can also result from a poor 50 Ω termination on the gate. If at any frequencies, the return loss of the termination is less than the device's reflection gain, a spurious oscillation will occur. Therefore, it is important to ensure a good match throughout the frequency range where the device exhibits high reflection gain. In the presented design, this was achieved in reducing the inherent parasitics of the SMT resistors by paralleling two 100 Ω. For a more comprehensive testing, all spurious oscillation testing also has to be run at low temperatures, since under such thermal conditions, GaAs devices have more gain and a higher propensity to self-oscillate.

Once basic oscillation conditions were reached, and the two start-up conditions (slow, with a power supply and fast by clipping the supply on) were verified, the phase noise performance was investigated and the puck placement optimized. Although it usually is a time consuming and tedious activity, it is also fairly straightforward. The puck is first moved along the 50 Ω transmission line to optimize output power, fairly close to the line (to provide a strong coupling). If the active circuit has been centered at the proper frequency, the maximum output power will occur when the loop gain is 0° and the puck will be optimally placed in regards to its distance to the FET. Once that location is defined, the puck will be moved within that place of reference closer or away from the line. This will reduce the output power, but will increase the loaded Q of the DRO and dramatically improve phase noise. The compromise is then to be far enough to get the absolute best phase noise, but close enough to get some decent output power and always be able to start the oscillator (again under both start-up conditions). When this is optimized, the design should be able to provide an adequate tuning range to accommodate manufacturing yields and fallout, and a limited power varia-

tion over the specified temperature range. If the output power drops significantly (3 dBm or more) at high temperature, the design is bound to experience high attrition during production due to some DROs not oscillating at high temperature, the puck's coupling should be increased. If coupling does not provide the required phase noise, the source stub can be adjusted to provide more reflection gain, at the expense of a potential spurious oscillation, and the puck location optimization should be started again from the beginning.

Figure 15 presents the layout of the DRO that was tested, and **Figures 16a,b,c and 17** presents the measured output power and phase noise performance that was achieved. As can be reviewed in **Table 1**, these results matched quite well the simulated performance and meet all of the design's specifications. **Table 3** provides the part list for the DRO's assembly and the total approximate cost that would be expected for this circuit.
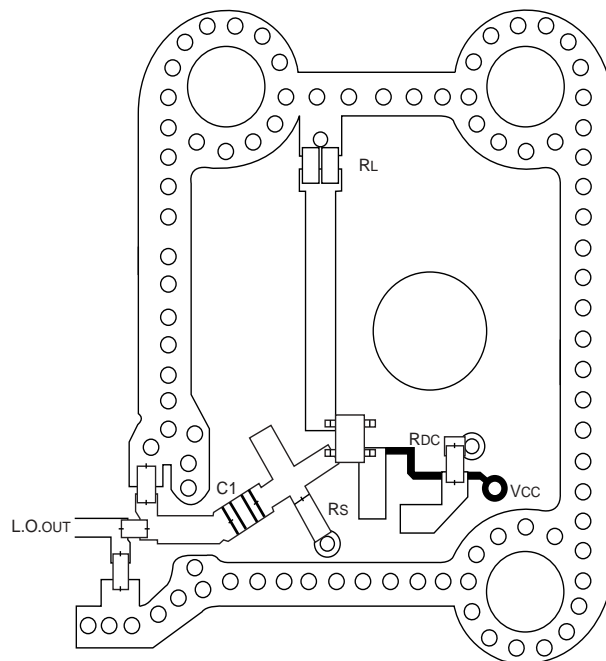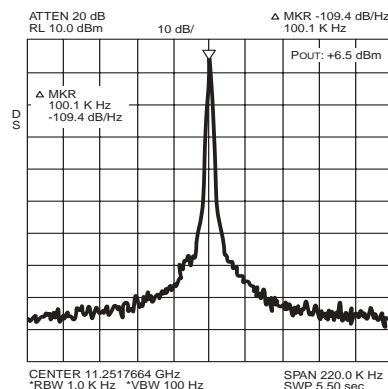

Figure 15. NE72218 DRO Layout
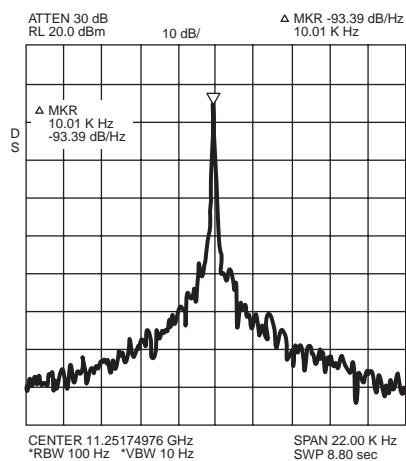

Figure 16a. DRO Measured Output Performance

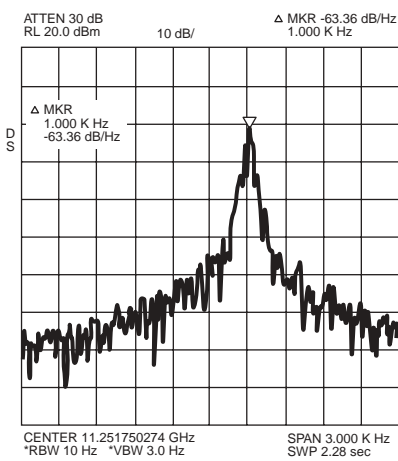**Figure 16b. DRO Measured Output Performance**

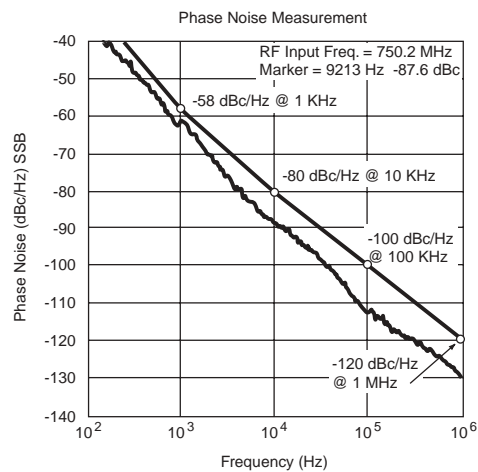**Figure 16c. DRO Measured Output Performance**

Figure 17. DRO Measured Phase Noise Performance
Versus Minimum Specifications

REFERENCE DESIGNATOR (Refer to Figure 7)	DESCRIPTION	APPROXIMATE COST in $ (100K QUANTITIES)
U1	NE72218 GaAs MESFET microwave transistor (NEC)	0.60
DR1	11.25 GHz. dielectric resonator, (Trans-Tech Inc.)	0.70
C1	1000 pF SMT chip capacitor, 0603 package	0.02
C2	100 pF SMT chip capacitor, 0603 package	0.02
C3	2.2 pF SMT chip capacitor, 0603 package	0.02
R1 (2 in parallel)	101 ohm chip resistor, 0603 package	0.010
R2	92 ohm chip resistor, 0603 package	0.005
R3	30 ohm chip resistor, 0603 package	0.005
PCB1	0.020 thick double sided Rogers 4003 printed circuit board	0.5
CAVITY1	Metal cavity with tuning screw	1.00
	Total parts cost (approximate)	2.88

Table 3. DRO Billing of Materials.

SUMMARY

This application note has demonstrated a DRO design at 11.25 GHz using one of NEC's new super low cost GaAs MESFETs. The required performance specifications were presented. Leeson's phase noise equation was then discussed to develop some rules of thumb for low noise DRO design. HP-EEsof's Series IV was then used to predict and optimize the DRO performance. Measured results and practical "on the bench optimization" was then pursued. The result was a DRO that met all the specification goals for a typical DBS application. In general, the design of any DRO requires tradeoffs between phase noise, output power, tuning range and frequency stability. By applying the design techniques presented in this applications note and understanding how resonant circuits are affected by different factors, designers can quickly design a DRO that is customized to their requirements. The NE72218 is an excellent choice for DRO because of good microwave performance at low power biasing, compact packaging, low cost and NEC's consistent processes. A very compact DRO was presented that would cost just under $3.00 in 100K quantities for high volume manufacturing.

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