

RECORDS OF REVISION

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SPEC No.	Date	NO.	PAGE	SUMMARY	NOTE
LCY-07071	2007. 11. 21		_	_	1 st Issue
CY-07071A	2007. 12. 18		8	Table6-1 Common electrode driving signal part	2 nd Issu
				Remark part was modified	
			9	Table7-2 [caution] Turn off part : REVV -> REV	
			10	Table7-3 VLED remark part : [Note7-11] added	
				(By customer request)	
			12	Table7-5 Gate part Start pulse frequency part :	
				Symbol was modified Fsp -> fsp	
			17	Table9-1 Surface reflectance remarks part	
				[Note9-8] -> [Note9-9]	
			24	Packing form(carton size, Total mass of one	
				carton)	
			29	Fig3-1 Tcf / Tcr position was changed.	
		,			

TFT-LCD MODULE

LQ088K9LA02

DEVICE SPECIFICATIONS

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(1) Summary

This TFT-LCD module is a color active matrix LCD module incorporating amorphous silicon TFT. An outline of the module is given in Table 4-1.

(2) Features

•SHARP SM-LCD panel and LED Backlight is adopted in this module.

- •6bit RSDS™ *(Reduced Swing Differential Signaling) interface is adopted in this module.
- ·Utilizes a panel with a 8:3 aspect ratio, which makes the module suitable for use in wide-screen systems.
- •The 8.8 screen produces a high resolution image that is composed of 614,400 pixels elements in a stripe arrangement.
- •Graphics and texts can be displayed on a 1280×3×480 dots panel with 262,144 colors by supplying 18 bit data signals(6 bit/color).
- ·This module features both transmissive and reflective display technology.
- ·Wide viewing field angle technology is employed.(The most suitable viewing angle is in the All directions.)
- ·Viewing angle control technology is employed.
- •By adopting an active matrix drive, a picture with high contrast is realized.
- •Reduced reflection as a result of low reflection black matrix and an AG(antiglare)AR(antireflection) top polarizer.
- •By COG method, realized a slim, lightweight, and compact module.
- •Transparent intensity is raised by adoption of the rate LCD panel of a high aperture, a high transparently color filter, and a high transparently polarizing plate.
- •An inverted video display in the vertical and horizontal directions is possible.
- * RSDS™ is a trademark of National Semiconductor Corporation.

(3) Structure and Outline dimensions

Outline dimensions of the module are given in Fig.1.

Structure of the TFT-LCD module is given in Fig.2.

This TFT-LCD module is composed of the color TFT-LCD panel, driver ICs, FPC, frame, shielding front case, shielding back case and LED backlight unit.(LED circuit to drive the backlight is not built into this module.)

(4) Mechanical specifications

Table4-1

Parameter	Specifications	Units	Remarks
Screen size (Diagonal)	22.35 [8.8″]	cm	
Active area	209.28(W) × 78.48(H)	mm	
Display format	1280 × RGB(W) × 480(H)	dots	
Dot pitch	0.0545(W) × 0.1635(H)	mm	
Pixel configuration	R,G,B Stripe configuration		
Display mode	Normally black		
Outline dimension	231.6(W) × 94.7(H) × 11.25(D)	mm	[Note4-1]
Mass	Max 320	g	

[Note4-1]Typical values are shown.

For detailed measurements and tolerances, please refer to Fig.1. (Projection portions, Backlight harness, FPC are excepted.)

(5) I/O terminal name and functions

5-1) TFT-LCD panel driving part

	Source par		Recommended connector : Hi	
Pin No.	, ,		Description	Remarks
1	CS	_	CS Signal input	
2	VCOM	—	COM Signal input	
3	GND	_	Ground	
4	VLS	—	Power supply source part	
5	SPOI	i/o	Source Start Pulse Input signal	[Note5-3]
6	X0P	i	Data Input signal(X0P)	[Note5-6]
7	XON	i	Data Input signal(X0N)	[Note5-6]
8	X1P	i	Data Input signal(X1P)	[Note5-6]
9	X1N	i	Data Input signal(X1N)	[Note5-6]
10	X2P	i	Data Input signal(X2P)	[Note5-6]
11	X2N	i	Data Input signal(X2N)	[Note5-6]
12	LP	i	Source data transfer signal	
13	GND	_	Ground	
14	СКР	i	Source clock signal(CKP)	
15	CKN	i	Source clock signal(CKN)	
16	VL	i	Gammer reference power supply	[Note5-5]
17	VH	i	Gammer reference power supply	[Note5-5]
18	VP2	i	Power supply of gray image	
19	VN2	i	Power supply of gray image	
20	REV	i	Polarity reversing signal of LCD output	
21	LBR	i	Setting signal of horizontal display position.	[Note5-3]
22	VCCS	—	Power supply of Source part	[Note5-1]
23	YOP	i	Data Input signal(Y0P)	[Note5-6]
24	YON	i	Data Input signal(Y0N)	[Note5-6]
25	Y1P	i	Data Input signal(Y1P)	[Note5-6]
26	Y1N	i	Data Input signal(Y1N)	[Note5-6]
27	Y2P	i	Data Input signal(Y2P)	[Note5-6]
28	Y2N	i	Data Input signal(Y2N)	[Note5-6]
29	GND	[Ground	
30	ZOP	i	Data Input signal(Z0P)	[Note5-6]
31	ZON	i	Data Input signal(Z0N)	[Note5-6]
32	Z1P	i	Data Input signal(Z1P)	[Note5-6]
33	Z1N	i	Data Input signal(Z1N)	[Note5-6]
34	Z2P	i	Data Input signal(Z2P)	[Note5-6]
35	Z2N	i	Data Input signal(Z2N)	[Note5-6]
36	GND		Ground	
37	SPIO	i/o	Source Start Pulse output signal	[Note5-3]

Table5-1-A(sequel)

Pin No.	Symbol	i/o	Description	Remarks
38	OPEN	_	Non connection	
39	N.C.	_	Non connection	
40	OPEN	_	Non connection	
41	N.C.	_	Non connection	
42	OPEN	_	Non connection	
43	N.C.	_	Non connection	
44	OPEN	_	Non connection	
45	OPEN	_	Non connection	
46	N.C.	_	Non connection	
47	OPEN	_	Non connection	
48	N.C.	—	Non connection	
49	OPEN	_	Non connection	
50	N.C.	_	Non connection	

2	OPEN	—	Non connection	
3	GND	—	Ground	
4	MODE1	i	Output mode setting signal 1 of gate driver	[Note5-2]
5	MODE2	i	Output mode setting signal 2 of gate driver	[Note5-2]
6	R/L	i	Setting signal of horizontal display position.	[Note5-3]
7	CLS	i	Gate Shift Clock Pulse Input	
8	SPS	i	Gate Start Pulse Input	
9	XDON	i	Gate Output Enable Signal Input	[Note5-4]
10	VCCG	—	Gate driver power supply	[Note5-1]
11	OPEN	_	Non connection	
12	VDD	_	Gate VDD Power Input	
13	OPEN	_	Non connection	
14	GND	_	Ground	
15	OPEN	_	Non connection	
16	GND	—	Ground	
17	OPEN	—	Non connection	
18	СОМ	i	COM Signal input	
19	OPEN	—	Non connection	
20	CS	i	CS Signal input	

[Note5-1] VCCS and VCCG can input same level voltage.

[Note5-2] The mode of the gate driver output can be selected by setting MODE1 and MODE2. Table5-2

MODE1	MODE2	Output mode		
Hi	Hi	Normal mode(1 line writing)		
Lo	Hi Out of use			
Hi	Lo	2 line simultaneous writing mode		
Lo	Lo Lo All output terminals is fixed at the VEE leve			

*Refer to "[caution] Notes when power supply is turned on." in 7-1).

*Refer to Fig.5-2.

*Please set the signal voltage level when use the Rueko DCC.

MODE1=Hi, MODE2=Lo

Caution) Lo=GND , Hi=VCCG

[Note5-3] Setting signal of horizontal and vertical display position

	R/L	LBR	SPOI	SPIO
Normal displayed	Lo	Hi	Input mode	Output mode
Right/Left reverse mode	Lo	Lo	Output mode	Input mode
Up/Down reverse mode	Hi	Hi	Input mode	Output mode
Right/Left & Up/Down reverse mode	Hi	Lo	Output mode	Input mode

Caution) Hi=VCCS , Lo=GND(0V)

*Please set the signal voltage level when use the Rueko DCC.

R/L=Lo , LBR=Hi

[Note5-4] XDON signal controls all the GATE output signals.

Table5-3

XDON	Function
Lo	At the normally use
Hi	all the GATE output signals are VDD level.

Caution) Lo=GND , Hi=VCCG

Caution) The setting of XDON=Hi might momentarily generate current surge.

[Note5-5] Please set the following.

VH = 5.3V, VL = GND (0V)

[Note5-6] Refer to (8), Table8-1, Fig8-1.

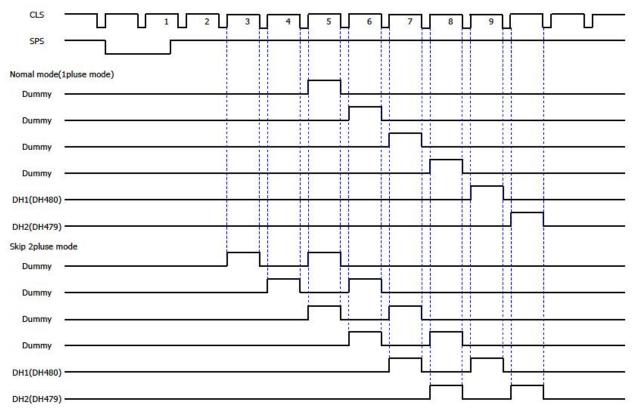


Fig.5-2 Gate output timing

5-2) LED Backlight system driving part

Table5-4 Recommended connector : Hirose FH28E-20S-0.5SH

Table 5-4	Recommen	ILLEU CUTITIECTOL - THIOSE FLIZOF-203-0.3311	
Pin No.	Symbol	Description	Remarks
1	A1	LED power supply input (+)	Anode side
2	A1	LED power supply input (+)	Anode side
3	A2	LED power supply input (+)	Anode side
4	A2	LED power supply input (+)	Anode side
5	N.C.	OPEN	
6	N.C.	OPEN	
7	C1	LED power supply input 1 ($-$)	Cathode side 1
8	C1	LED power supply input 1 ($-$)	Cathode side 1
9	C2	LED power supply input 2 $(-)$	Cathode side 2
10	C2	LED power supply input 2 ($-$)	Cathode side 2
11	C3	LED power supply input 3 $(-)$	Cathode side 3
12	C3	LED power supply input 3 $(-)$	Cathode side 3
13	C4	LED power supply input 4 $(-)$	Cathode side 4
14	C4	LED power supply input 4 ($-$)	Cathode side 4
15	N.C.	Open	
16	TH	Sensor(+)	Terminal for temperature sensor
17	TH_G	Sensor(-)	Terminal for temperature sensor
18	PH_V	Open	
19	PH_G	Open	
20	PH_O	Open	

(6) Absolute maximum ratings

Teble6-1

Teble6-1						GND=0V
Para	meter	Symbol	MIN	MAX	Unit	Remark
Power supply	Analog	VLS	-0.3	+6.0	V	Ta=25 ℃
of source part	Digital	VCCS	-0.3	+4.3	V	11
Power supply	·	VDD	-0.3	+35.0	٧	II .
of gate part	t	VCCG	-0.3	+6.0	٧	11
		VEE	-20	+0.3	V	11
		VDD-VEE	-0.3	+35.0	V	"
Input signal	Digital	VID	-0.3	VCCS(G)+0.3	V	" ,[Note6-1]
	Analog	VIA	-0.3	VLS+0.3	V	" ,[Note6-2]
Common electroc	ledriving signal	VCOM	-20	+35.0	٧	<i>" ,</i> VCOM <35Vp-р
Power supply of I	LED Back Light	ILED	-	0.4	А	11
Storage temp	erature	Tstg	-40	+95	°C	[Note6-3,4,7]
Operating ten	nperature	Topr1	-40	+85	°C	[Note6-3,4,5,7]
(LCD panel surface)						
Operating ten	nperature	Topr2	-40	+85	°C	[Note6-6]
(Ambient tem	perature)					

[Note6-1] SPOI, SPIO, X0P~X2N, Y0P~Y2N, Z0P~Z2N, LP, CKP, CKN, REV, LBR, MODE1, MODE2, R/L, SPS, CLS, XDON [Note6-2] VH、VL、VP2、VN2

[Note6-3] This rating applies to all parts of the module and should not be exceeded. Operating temp: -40 to -31 °C, does not provide a correct image on the LCD, but no damage of the display function will occur.

[Note6-4] Maximum wet-bulb temperature is 49 °C . Avoid dew condensation on the module. Otherwise electrical current leaks will occur, and it cannot meet the specifications.

[Note6-5] The operating temperature guarantees only operation of the circuit. For contrast, speed of response, and other factors related to display quality are determined in the circumstances

with Ta=+25 °C.

[Note6-6] Ambient temperature when the backlight is lit (reference value).

At a temperature specified by the application LED current must be reduced in order to keep the agreed panel operating temperature of +85°C(max)

[Note6-7] Refer to Table 15-1.

(7) Electrical characteristics

7-1) TFT-LCD panel driving section

Table7-1 Recommended operating conditions

Table7-1 Recoi	lable/-1 Recommended operating conductors													
Para	ameter		Symbol	MIN	TYP	MAX	Unit	Remarks						
Power supply	Analog		VLS	+5.2	+5.3	+5.4	V							
of source driver	Digital		VCCS	+3.0	+3.3	+3.6	V	[Note7-1]						
Power supply	ाना	Hi	VDD	+14.5	+15.0	+15.5	V							
of gate driver	driving	Lo	VEEDC	-11.5	-12.0	-12.5	V	VEEDC Bias						
			VEEAC		VCOMAC		Vp-p	[Note7-2]						
	Logic	Hi	VCCG	+3.0	+3.3	+3.6	V	[Note7-1]						
			VDD-VEE	_	· _	+33V	V							
Power supply of	gray imag	е	VH,Vp2,VN2	0	_	VLS	V							

[Note7-1] VCCS and VCCG can input same level voltage.

[Note7-2] This is must be made into common electrode driving signal, this phase, and this amplitude.

Para	meter	Symbol	MIN	TYP	MAX	Unit	Remarks					
Input voltage	Hi input	VIHS	0.8×VCCS		VCCS	V	[Neto7 2]					
of source part	Lo input	VILS	GND —		0.2×VCCS	V	[Note7-3]					
	Hi input	VIHRSDS	70	200		mV						
	Lo input	VILRSDS	—	-200	-70 mV		[Note7-4]					
	RSDS standard voltage range	VCOM RSDS	GND+0.1	1.2	VCC-1.2	V	[NOLE) -4]					
Input current	Hi input	IIHS1	-60	_		μA	[Note7-5]					
of source part	Lo input	IILS1			60	μA	[Noter-5]					
Input voltage	Hi input	VIHG	0.8×VCCG	_	VCCG	V	[Note7-6]					
of gate part	Lo input	VILG	GND	<u> </u>	0.2×VCCG	V						
Input current	Hi input	IIHG	2.0	—		μA	VI≕GND,[Note7-7]					
of gate part	Lo input	IILG	_	_	2.0	μA	VI=VCCG,[Note7-8]					
Common electrode	AC component	COM AC	_	±4.2	±5.0	V						
driving signal	DC component	COM DC	+0.5	—	+2.5	V	[Note7-9]					
CS driving signal	AC component	VCSAC	_	VCOM AC		V	[Note7-10]					
	DC component	VCSDC	_	VCOM DC		V						

Table7-2 Electric characteristic

* The supply voltage condition is a range in Table 7-1.

[caution] Notes when power supply is turned on.

Please do a power supply on and the power-off in the following order. And, please input the signal after turning on all power supplies.

Turn on ~~ VCCS,VCCG $\rightarrow~$ Logic signal $\rightarrow~$ VLS $\rightarrow~$ VEE , VDD $\rightarrow~$ REV $\rightarrow~$ MODE1,MODE2 ~

Turn off $VLS \rightarrow REV \rightarrow XDON 1H \text{ output} \rightarrow MODE1, 2 \rightarrow VDD, VEE \rightarrow Logic signal \rightarrow VCCS, VCCG$

At the terminals of MODE1/MODE2 signals, input low voltage when applying the power supply, and

hold low voltage for more than 2 vertical synchronous terms after VDD rises completely.

Then, either or both of them should hold high voltage until the power supply is turned off.

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GND=0V, Ta=25 °C

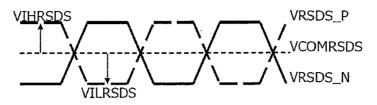
Ta=-40 °C ~+95 °C

[Note7-3] SPIO, SPOI, LP, LBR, REV

[Note7-4] X0P~X2N,Y0P~Y2N,Z0P~Z2N,CKP,CKN

Please refer to the following for VIHRSDS, VILRSDS, and VCOMRSDS.

RSDS Single end wave form



VRSDS_P:Wave form on P side of single end VRSDS_N:Wave form on N side of single end

[Note7-5] Apply the each terminals of SPIO, SPOI, LS, LBR, REV, X0P~X2N,Y0P~Y2N,Z0P~Z2N,CKP,CKN.

[Note7-6] CLS, SPS, MODE1, MODE2, XDON

[Note7-7] Apply the each terminal of CLS, SPS, MODE1, MODE2, XDON.

[Note7-8] Apply the each terminal of CLS, SPS.

[Note7-9] Please switch polarity of amplitude VCOMAC by center value of amplitude that is VCOMDC for every one level scan and every one vertical scan. Moreover, please adjust VCOMDC so that contrast becomes the maximum and a flicker becomes the minimum for every module.

[Note7-10] This is must be made into common electrode driving signal, this phase, and this amplitude.

7-2) LED backlight unit driving section

Table7-3

Ta=25℃

Parameter	symbol	MIN	ТҮР	MAX	UNIT	Remark
Input Voltage	VLED	21.0	24.8	26.9	V	ILED=0.320A, [Note7-11]
Current consumption	ILED		0.320		A	
PWM Frequency	fL		150		Hz	[Note7-11]
Power consumption	WLED	_	7.6		w	
Specification of LED-Type						
Detection of defect LEDs		by current				

[Note7-11] This value is reference value. Please refer to your LED backlight driving circuit.

7-3) LED Monitoring interface

Temperature Sensor Thermister Type : TH11-3T223GT made by MITSUBISHI MATERIALS CORPORATION

Table7-4				(Referei	nce data)
Temperature	R-Thermistor	Remark	Temperature	R-Thermistor	Remark
°C	kΩ (AVE)		°C	kΩ (AVE)	
-	-		40	11.93	
-40	568.60		50	8.165	
-30	326.60		60	5.71	
-20	193.90		70	4.07	
-10	115.10	[Note7-12]	80	2.96	[Note7-12]
0	69.41		90	2.19	
10	42.97		100	1.65	
20	27.32		110	1.26	
30	17.83		120	0.97	

[Note7-12] The above-mentioned value is a characteristic value of the thermally sensitive resistor unit at LED backlight off. Please confirm the characteristic in the state of the product when using it.

7-4) AC characteristics of input signals

AC characteristics of input signals are shown in Fig3-1, Fig3-2

ParameterSymbolMINTYPMAXUnitTerminalOperating Clock frequencyfck60MHzHigh level clock widthTowh66nsLow level clock widthTowh66nsClock rise timeTcr5nsClock rise timeTcr5nsStart pulse set up timeTsup3nsStart pulse set up timeTsup6nsStart pulse set up timeTsup3nsStart pulse set up timeTsup3nsStart pulse set timeTsup3nsStart pulse set timeTsup3nsStart pulse set up timeTsup5nsLP pulse hold timeTsup5nsLP pulse field timeTsup5nsLP pulse hold timeThip6nsLP pulse field timeTsup1/fckns1/fckIP pulse field timeTsup5nsLP pulse field timeTsup5nsIP pulse field timeTsup5nsIP pulse field timeTsup5nsIP pulse field timeTsup1	Table	e7-5			V	CCS、VCCG=3.	3V,VLS≕5.3\	/,GND=0V,Ta=25°C
Image: set of the se		Parameter	Symbol	MIN	ТҮР	MAX	Unit	Terminal
Low level clock width Towl 6 ns CKP CKN Clock rise time Tcr 5 ns CKN Clock fall time Tcf 5 ns CKN Start pulse set up time Tsupp 3 ns Start pulse set up time Tsupp 6 ns Start pulse full time full time ns Inter 1 1 full time ns Inter Inter ns Inter Inter Inter ns Inter ns Inter Inter		Operating Clock frequency	fck		—	60	MHz	
Low level clock width Tcw 6 ns CKN Clock rise time Tcr 5 ns Clock fall time Tcf 5 ns Start pulse set up time Tsusp 3 ns Start pulse hold time Thsp 2 ns CKP rise time Tcksp 6 ns Start pulse fall time Tspck 3 ns Start pulse fall time Tspck 3 ns LP pulse fact pulse width Twp 1 2 Tcwh() LP pulse start pulse width Twp 1 ns LP LP pulse frequency flp fsp ns .20*-x2N, VOP-x2N LP pulse frequency fcb		High level clock width	Tcwh	6	-	-	ns	
Clock rise time Tcr 5 ns Clock fall time Tcf 5 ns Start pulse set up time Tsusp 3 ns Start pulse hold time Thsp 2 ns Ns Start pulse hold time Thsp 2 ns Ns CKP rise time Tcksp 6 ns Start pulse fall time Tspck 3 ns Start pulse fall time Tspck 3 ns LP pulse fall time Tspck 3 ns LP pulse set up time Tsup 5 ns LP pulse set up time Tsup 5 ns LP pulse frequency flp - fsp ns Data hold time Thd 2 ns z0P-x2N/0P-x2N <		Low level clock width	Tcwl	6			ns	
Start pulse set up timeTsusp3nsStart pulse hold timeThsp2nsStart pulse hold timeTcksp6nsCKP rise timeTcksp6nsStart pulse rise timeTspck3nsStart pulse vidthTwsp12Tcwh())LP pulse set up timeTsulp5nsLP pulse hold timeThlp6nsLP pulse hold timeThlp6nsLP pulse hold timeThlp6nsLP pulse hold timeThlp6nsLP pulse frequencyfipfspnsLP pulse frequencyfipfspnsData set up timeTsud3nsData hold timeThd2nsData hold timeThd2nsClock rise timeTrd100nsClock pulse widthTwi500nsClock fall timeTfdnsClock fall timeTfdnsStart pulse frequencyfsp6065HzStart pulse hold timeThsp300ns<		Clock rise time	Tcr			5	ns	CICIN
Start pulse hold timeThsp2nsCKP rise time - Start pulse rise timeTcksp6nsSPOI ,SPIO [Note7-9]Start pulse rise timeTcksp6nsSPOI ,SPIO [Note7-9]Start pulse rise timeTspck3nsStart pulse widthTwsp12Tcwh()LP pulse set up timeTsulp5nsLP pulse hold timeThlp6nsLP pulse hold timeThlp6nsLP pulse hold timeThlp6nsLP pulse frequencyfipfspHzLP pulse frequencyfipfspnsData set up timeTsud3nsData hold timeThd2nsClock rulse widthTwi500nsClock rulse widthTwi500nsClock fall timeTrd100nsClock rulse widthTwi500nsClock fall timeTrdnsStart pulse frequencyfsp6065HzStart pulse frequencyfspnsStart pulse hold timeThsps300nsStart pulse		Clock fall time	Tcf			5	ns	
Teg BigCKP rise time Start pulse rise time → CKP rise timeTcksp6nsSPOI , SPIO [Note7-9]Start pulse fall time → CKP rise timeTspck3nsNsNote7-9]Start pulse widthTwsp12Tcwh(l)Note7-9]NsNote7-9]LP pulse set up timeTsulp5nsNsNote7-9]LP pulse hold timeThip6nsLPLP pulse frequencyflpfspnsLPLP pulse frequencyflpfspnsLPLP pulse start pulse set up timeTsud3nsLPData set up timeTsud3nsz0P~X2N,Y0P~Y2NData hold timeThd2nsz0P~X2N,Y0P~Y2NData hold timeThd2nsz0P~X2N,Y0P~Y2NClock rise timeTrclnsz0P~Z2NClock rise timeTrclnsz0P~Z2NClock fall timeTfclnsset up timeStart pulse frequencyfsp6065HzStart pulse set up timeTsups300nsStart pulse hold timeThsp300nsStart pulse fall timeTfsp100ns <td></td> <td>Start pulse set up time</td> <td>Tsusp</td> <td>3</td> <td></td> <td></td> <td>ns</td> <td></td>		Start pulse set up time	Tsusp	3			ns	
$ \begin{array}{ c c c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		Start pulse hold time	Thsp	2		_	ns	
Start pulse widthTwsp12Tcwh(1)LP pulse set up timeTsulp5nsLP pulse hold timeThlp6nsHigh level LP pulse widthTwlp1/fckmsLPLP pulse frequencyflpfspHzLP pulse start pulse set up timetLSLP1/fcknsLPData set up timeTsud3nsZOP~Z2N/OP~Y2NData hold timeThd2nsZOP~Z2NOperating Clock frequencyfcls100nsCLSClock rulse widthTwl500µsClock rulse widthTrd100nsClock rulse widthTrdnsCLSClock rulse widthTrdnsSCLSClock rulse widthTrdnsSCLSStart pulse frequencyfsp60655HzStart pulse frequencyfspnsSPSStart pulse hold timeThsps300nsStart pulse fall timeTfsp100nsStart pulse fall timeTfsp100nsVCOM signal hold timeThcom0µsVCOM signal hold timeThcom0µs	part		Tcksp	6	_	—	ns	-
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Source		Tspck	3	—	_	ns	[]
$\begin{tabular}{ c c c c c c } \hline LP pulse hold time & Th lp & 6 & - & - & ns \\ \hline $High level LP$ pulse width & Twlp & 1/fck & - & - & ns \\ \hline LP pulse frequency & flp & - & fsp & - & Hz \\ \hline LP pulse start pulse set up time & TLSLP & 1/fck & - & - & ns \\ \hline $Data set up time & Tsud & 3 & - & - & ns \\ \hline $Data hold time & Thd & 2 & - & ns \\ \hline $Data hold time & Thd & 2 & - & ns \\ \hline $Data hold time & Thd & 2 & - & ns \\ \hline $Data hold time & Thd & 2 & - & ns \\ \hline $Data hold time & Thd & 2 & - & ns \\ \hline $Clock pulse width & Twl & 500 & - & - & \mus \\ \hline $Clock rulse width & Twl & 500 & - & - & \mus \\ \hline $Clock rulse width & Twl & 500 & - & - & \mus \\ \hline $Clock rulse width & Twl & 500 & - & - & \mus \\ \hline $Clock fall time & Tfcl & - & - & 100 & ns \\ \hline $Clock fall time & Tfcl & - & - & ns \\ \hline $Start pulse frequency & fsp & - & 60 & 65 \\ \hline $Start pulse set up time & Tsups & 100 & - & - & ns \\ \hline $Start pulse set up time & Tsups & 100 & - & - & ns \\ \hline $Start pulse hold time & Thsps & 300 & - & - & ns \\ \hline $Start pulse rise time & Trsp & - & - & 100 & ns \\ \hline $VCOM signal set up time & Tsucom & 4 & - & - & \mus \\ \hline $VCOM signal hold time & Thcom & 0 & - & - & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & \mus \\ \hline $VCOM signal rise time & Trcom & - & - & 2 & - & 1 \\ \hline $VCOM signal rise time & Trcom & - & - & - & 2 & - & 1 \\ \hline $VCOM signal rise time & Trcom & - & - & - & 2 $		Start pulse width	Twsp	1		2	Tcwh(l)	
High level LP pulse widthTwip1/fcknsLPLP pulse frequencyflpfspHzLP pulse start pulse set up timetLSLP1/fcknsData set up timeTsud3nsX0P~X2N,Y0P~Y2NData hold timeThd2ns,Z0P~Z2NOperating Clock frequencyfcls100ns,Z0P~Z2NClock pulse widthTwi500µsClock rise timeTrcl100nsCLSClock fall timeTfclnsStart pulse frequencyfspStart pulse frequencyfsp6065HzStart pulse set up timeTsups100nsStart pulse hold timeThps300nsStart pulse fall timeTfsp100nsSPSStart pulse fall timeTfsp100nsVCOM signal set up timeTsucom4µsVCOM signal hold timeThcom0µsVCOM signal rise timeTrcom100ns		LP pulse set up time	Tsulp	5			ns	
$ \begin{array}{ c c c c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		LP pulse hold time	Thlp	6			ns	-
LP pulse Start pulse set up time tL SLP 1/fck ns Data set up time Tsud 3 ns X0P~X2N,Y0P~Y2N Data hold time Thd 2 ns ,Z0P~X2N,Y0P~Y2N Data hold time Thd 2 ns ,Z0P~Z2N Operating Clock frequency fcls 100 ns CLS Clock pulse width Twl 500 µs ,CLS Clock rise time Trcl 100 ns ,CLS Clock fall time Tfcl 100 ns ,CLS Start pulse frequency fsp 60 65 Hz ,SPS Start pulse set up time Tsusps 100 ns ,SPS ,SPS Start pulse hold time Thsps 300 ns ,SPS Start pulse fall time Tfsp 100 ns ,SPS VCOM signal set up time Tsucom 4		High level LP pulse width	Twlp	1/fck			ns	LP
Data set up timeTsud3nsX0P~X2N,Y0P~Y2NData hold timeThd2ns,ZDP~Z2NDerating Clock frequencyfcls250kHzClock pulse widthTwl500 μ sClock rise timeTrcl100nsClock fall timeTfcl100nsClock fall timeTfclnsCLSStart pulse frequencyfsp6065HzStart pulse set up timeTsups100nsStart pulse hold timeThsps300nsStart pulse fall timeTfsp100nsVCOM signal set up timeTsucom4 μ sVCOM signal hold timeThcom0 μ sVCOM signal rise timeTrcom μ sVCOM		LP pulse frequency	flp		fsp	·	Hz	
Data hold timeThd2ns,Z0P~Z2NOperating Clock frequencyfcls250kHzClock pulse widthTwl500µsClock rise timeTrcl100nsClock fall timeTfcl100nsClock fall timeTfcl100nsStart pulse frequencyfsp60655HzStart pulse set up timeTsusps100nsStart pulse hold timeTfsp300nsStart pulse frequencyfsp100nsStart pulse hold timeTfspnsStart pulse hold timeTfspnsStart pulse frequencyfsp100nsVCOM signal set up timeTfsp100nsVCOM signal hold timeThcom0µsVCOM signal rise timeTrcomµsCS		LP pulse Start pulse set up time	tLSLP	1/fck			ns	
Upperating Clock frequencyfcls $ 250$ kHzClock pulse widthTwl 500 $ \mu$ sClock rise timeTrcl $ 100$ nsClock fall timeTfcl $ 100$ nsStart pulse frequencyfsp $ 60$ 65 HzStart pulse set up timeTsusps 100 $ -$ nsStart pulse hold timeThsps 300 $ -$ nsStart pulse rise timeTrsp $ 100$ nsStart pulse fall timeTfsp $ 100$ nsVCOM signal set up timeTsucom 4 $ \mu$ sVCOM signal hold timeThcom 0 $ \mu$ sVCOM signal rise timeTrcom $ 2$ μ sVCOM signal rise timeTrcom $ 2$ μ s		Data set up time	Tsud	3	—	<u> </u>	ns	XOP~X2N,YOP~Y2N
Clock pulse widthTwl500µsCLSClock rise timeTrcl100nsClock fall timeTfcl100nsClock fall timeTfcl100nsStart pulse frequencyfsp6065HzStart pulse set up timeTsusps100nsStart pulse hold timeThsps300nsStart pulse rise timeTrsp100nsSPSStart pulse fall timeTfsp100nsVCOM signal set up timeTsucom4µsVCOM signal hold timeThcom0µsVCOM signal nise timeTrcom2µsVCOM			Thd	2			ns	,ZOP~Z2N
UnderstandClock rise timeTrcl100nsCLSClock fall timeTfcl100nsClock fall timeTfcl100nsStart pulse frequencyfsp6065HzStart pulse set up timeTsusps100nsstartStart pulse hold timeThsps300nsSPSStart pulse rise timeTrsp100nsSPSStart pulse fall timeTfsp100nsVCOM signal set up timeTsucom4µsVCOMVCOM signal rise timeThcom0100CS			fcls		-	250	kHz	
$\frac{1}{100} = \frac{1}{100} = \frac{1}$		Clock pulse width	Twl	500	—		μs	CLS
Image grow growStart pulse frequencyfsp6065HzStart pulse set up timeTsusps100nsStart pulse hold timeThsps300nsStart pulse rise timeTrsp100nsStart pulse fall timeTfsp100nsVCOM signal set up timeTsucom4µsVCOM signal hold timeThcom0µsVCOM signal rise timeTrcom2µsVCOM		Clock rise time	Trcl			100	ns	
BOther pulse inside insid	art	Clock fall time	Tfcl		_	100	ns	
Start pulse hold timeThsps300nsSPSStart pulse rise timeTrsp100nsStart pulse fall timeTfsp100nsVCOM signal set up timeTsucom4 μ sVCOM signal hold timeThcom0 μ sVCOM signal rise timeTrcom2 μ s	te pi	Start pulse frequency	fsp	-	60	65	Hz	
Start pulse rise time Trsp 100 ns Start pulse fall time Tfsp 100 ns VCOM signal set up time Tsucom 4 µs VCOM signal hold time Thcom 0 µs VCOM VCOM signal rise time Trcom 2 µs CS	Ga	Start pulse set up time	Tsusps	100			ns	
Start pulse fall time Tfsp - - 100 ns VCOM signal set up time Tsucom 4 - - µs VCOM signal hold time Thcom 0 - - µs VCOM VCOM signal rise time Trcom - - 2 µs CS		Start pulse hold time	Thsps	300		—	ns	SPS
VCOM signal set up timeTsucom4µsVCOM signal hold timeThcom0µsVCOMVCOM signal rise timeTrcom2µsCS		Start pulse rise time	Trsp	<u> </u>	—	100	ns	
VCOM signal hold timeThcom0µsVCOMVCOM signal rise timeTrcom2µsCS		Start pulse fall time	Tfsp		_	100	ns	
VCOM signal rise time Trcom 2 µs CS		VCOM signal set up time	Tsucom	4	—	-	μs	
		VCOM signal hold time	Thcom	0	·	_	μs	VCOM
VCOM signal fall time Tfcom 2 µs		VCOM signal rise time	Trcom			2	μs	CS
		VCOM signal fall time	Tfcom		—	2	μs	

Table7-5

VCCS、VCCG=3.3V,VLS=5.3V,GND=0V,Ta=25°C

[Note7-9] The rising pulse in CKP is existed only 1 time during Hi period (Twsp) on start pulse.

7-5) Timing characteristics of input signals

Please refer to special DCC specifications of the separate volume for the timing characteristic when special DCC is used.

7-6) Electric power consumption

Tab	07-6
Iau	167-0

Tuble? 0							10 - 25 C
Paramet	ter	symbol	Voltage conditions	Min	Тур	Max	Unit
Current for	Analog	ILS	VLS=+5.3V		30	45	mA
source driver	Digital	ICCS	VCCS,VCCG=+3.3V	_	28	40	mA
Current for	Hi	IDD	VDD=+15.0V	_	0.5	1	mA
gate driver	Lo	IEE	VEEAC = -12.0	_	60	90	mA
	Logic	ICCG	VEEDC=8.4Vp-p	_	0.2	0.5	mA

*Conditions

Driving conditions:

 $\mathsf{fck}{=}\mathsf{42MHz}$, $\mathsf{fcls}{=}\mathsf{30kHz}$, $\mathsf{fsp}{=}\mathsf{60Hz}$, Normal displayed

Display pattern:

Vertical stripe pattern alternating 21 gray scale (GS21) with 42 gray scale (GS42) every 1 dot.

7-7) Input Data Signals and Display Position on the screen



D1,DH1	D2,DH1	D3,DH1		D1280,DH1
D1,DH2	D2,DH2		-	
D1,DH3				
		R	G B	
D1,DH480				D1280,DH480

Ta = 25°C

(8) Input signals, basic display color and gray scale of each color

Table8-1

									0 d ow lovel veltage 1 dich lovel veltage											
	Colors &					[Data s		0 :Low level voltag				e 1 :High level voltage							
_	Gray scale	Gray Scale	R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
	Black	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	—	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
B	Green	—	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
asic	Cyan	—	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Basic color	Red	_	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
r	Magenta	_	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	_	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	_	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	仓	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of red	仓	\downarrow				r					``	r						L I		
ile o	Û	\rightarrow				\mathbf{k}						\mathbf{k}						\mathbf{k}		
f red	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Û	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	仓	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
àray	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Scal	仓	\checkmark																		
Gray Scale of green	Û	\downarrow				\mathbf{k}						\mathbf{k}						\mathbf{k}		
gree	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
'n	Û	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	仓	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Gray	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
/ Sca	仓	\downarrow																		
Gray Scale of blue	Û	\downarrow							\downarrow				\downarrow							
f blu	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
e	٦.igiicei ب	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
L			-		-		-		-	-		-	-	-	-		_			

Each basic color can be displayed in 64 gray scales from 6 bit data signals. According to the combination of total 18 bit data signals, the 262,144-color display can be achieved on the screen.

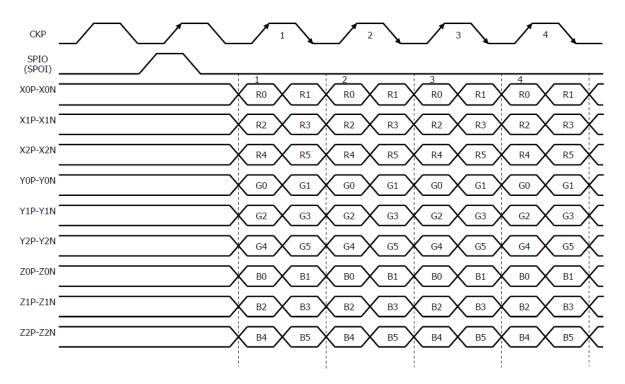


Fig.8-1 Timing Diagram

(9) Optical characteristics

Table9-1

Ta=25°C

Table9-1						r		
Pa	rameter	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
		θ11,θ12	20degree	80	150	_		[Note9-1,2]
Viewir	ng angle range	θ21, θ22	60degree	15	25	—		CR value
		CRmax	Optimal	220	360	_		[Note9-2]
			(Ta=25°C)		25		0/	
Contr	ast ratio	-	θ=0°,Ta=80°C	_	-25	—	%	[Note9-2,3]
		-	θ=0°,Ta=60°C	_	-15		%	[Note9-2,3]
		-	θ=0°,Ta=-10°C	_	-10	—	%	[Note9-2,3]
		-	θ=0°,Ta=-30°C		-25	-	%	[Note9-2,3]
Respo	nse		$\theta = 0^{\circ}, B \rightarrow W$	_	8	10	ms	[Note9-4]
Time	Ta=25℃	τ r(B-L10)	$\theta = 0^{\circ}, B \rightarrow L10$	_	45	70	ms	[Note9-4]
*		τ d	$\theta = 0^{\circ}, W \rightarrow B$	_	5	10	ms	[Note9-4]
*with		τ d(L16-L10)	$\theta = 0^{\circ}, L16 \rightarrow L10$	_	13	20	ms	[Note9-4]
O/S drivir	Ta=0℃	τr_0	θ=0°,B→W	_	13	20	ms	[Note9-4]
unvi	ig	τ r ₀ (B-L10)	θ=0°,B→L10	—	135	180	ms	[Note9-4]
		τ d ₀	θ=0°,₩→B	_	15	20	ms	[Note9-4]
		τ d ₀ (L16-L10)	$\theta = 0^{\circ}$,L16 \rightarrow L10	_	20	50	ms	[Note9-4]
_	Ta=-20℃	τ r ₋₂₀	θ=0°,B→W	_	70	100	ms	[Note9-4]
ode		τ r ₋₂₀ (B-L10)	θ=0°,B→L10	—	440	590	ms	[Note9-4]
Ē		τ d ₋₂₀	θ=0°,₩→B	_	55	70	ms	[Note9-4]
Transmissive mode		τ d ₋₂₀ (L16-L10)	$\theta = 0^{\circ}$,L16 \rightarrow L10	_	130	210	ms	[Note9-4]
simis	Та=-30 °С	τ r ₋₃₀	θ=0°,B→W	—	190	250	ms	[Note9-4]
rans		τ r ₋₃₀ (B-L24)	θ=0°, B→L24	—	600	770	ms	[Note9-4]
F		τ d ₋₃₀	θ=0°,₩→B	_	140	180	ms	[Note9-4]
		τ d ₋₃₀	$\theta = 0^{\circ}$,L24 \rightarrow L16	_	235	340	ms	[Note9-4]
		(L24-L16)						
White	e luminance	Lw	$\theta = 0^{\circ}$	210	240	_	cd/m ²	[Note9-5,6]
Black	luminance	Lb	$\theta = 0^{\circ}$	_	—	1.2	cd/m ²	[Note9-5,6]
Unifor	nity of luminance	-	θ=0°	77	81	-	%	[Note9-5,6,7]
Gamm	าล	-	Value at L31	1.83	-	2.55		[Note9-12]
White	chromaticity	Х	θ=0°	0.270	0.300	0.330		[Note9-5,6]
		Y	θ=0°	0.290	0.320	0.350		[Note9-5,6]
Red c	hromaticity	Х	θ=0°	0.502	0.542	0.582		[Note9-5,6]
		Y	θ=0°	0.287	0.327	0.367		[Note9-5,6]
Green	chromaticity	Х	$\theta = 0^{\circ}$	0.290	0.330	0.370		[Note9-5,6]
	/	Y	θ=0°	0.532	0.572	0.612		[Note9-5,6]
Blue o	hromaticity	X	θ=0°	0.107	0.147	0.187		[Note9-5,6]
	2	Y	θ=0°	0.073	0.113	0.153		[Note9-5,6]
	C chromaticity		θ=0°	0.242	0.312	0.382		
BLACK	CHIOMAULITY	X Y	$\theta = 0^{\circ}$	0.242	0.312	0.348		[Note9-5,6] [Note9-5,6]
NTOC				0.200			<u> </u>	[110169-2,0]
NTSC	ratio	-	$\theta{=}0^{\circ}$	-	45	-	%	

Tab	le9-1 (sequel)							Ta=25℃
	Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
	Viewing angle range	θ11,θ12	20degree	3	4.5	-		[Note9-1,8]
		θ21, θ22	40degree	2	3			[140163-1,0]
	Contrast ratio	CR _{ref}	$\theta = 0^{\circ}$,Optimal	3	5	_		[Note9-1,8]
	Response Time	$\tau r_{ref} + \tau d_{ref}$	B→W/W→B	_	20	—	ms	[Note9-4]
	Reflection ratio	Rf	θ=0°		3.8		%	[Note9-9]
	White chromaticity	Х	$\theta = 0^{\circ}$	0.269	0.319	0.369		
e l		Y	θ=0°	0.299	0.349	0.399		
pom	Red chromaticity	Х	θ=0°	0.405	0.455	0.505		
tive		Y	θ=0°	0.220	0.270	0.320		
Reflective mode	Green chromaticity	Х	θ=0°	0.210	0.260	0.310		[Nata0 10]
8		Y	θ=0°	0.397	0.447	0.497		[Note9-10]
	Blue chromaticity	Х	θ=0°	0.126	0.176	0.226		
		Y	θ=0°	0.117	0.167	0.217		
	BLACK chromaticity	Х	θ=0°	0.171	0.241	0.311		
		Y	θ=0°	0.121	0.191	0.261		
	NTSC ratio	-	θ=0°	-	22	-	%	
	Surface reflectance	SRf		-	0.6	-	%	[Note9-9]
LED) lifetime +25°C		continuation	10000		_	Hour	[Note9-11]

*The measurement data of above optical characteristics are measured 30 minutes after lighting the B/L. they are measured in a dark room or an equivalent state by the method shown in the following figure.

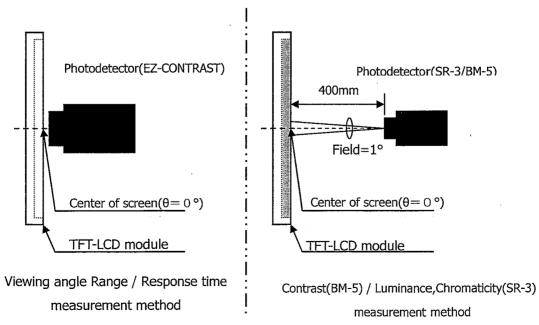
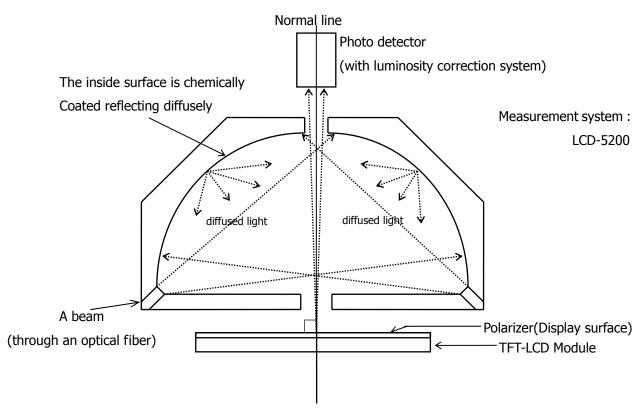


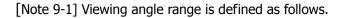
Fig.9-1 Optical characteristics measurement method (Transmissive mode)

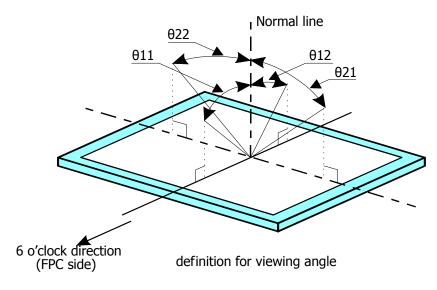
T-LLO 1 /



Contrast / Viewing angle Range / Response time measurement method

Fig.9-2 Optical characteristics measurement method (Reflective mode)





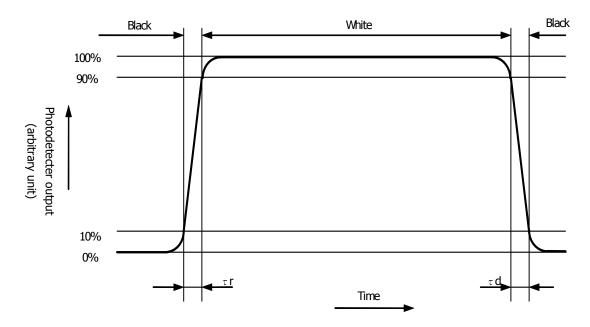
[Note 9-2] Contrast ratio is defined as follows:

[Note 9-3] The change rate by the ambient temperature of the contrast is defined as follows.

It is a change rate against the CR value of $25^\circ\!\mathrm{C}$ in ambient temperature of the module.

[Note 9-4] Response time is defined as follows:

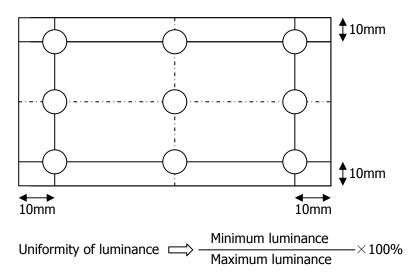
Response time is obtained by measuring the transition time of photo detector output, when input signals are applied so as to make the area "black" to and from "white".



[Note 9-5] LED driving condition is refer to Table7-3.

[Note 9-6] Measured on the center area of the panel at a viewing cone 1-degree by TOPCON luminance meter SR-3.(After 30 minutes operation)

[Note 9-7] Uniformity of luminance is measured in the measurement part shown in the figure below. The measurement part is "O" symbol it shown.



[Note 9-8] Contrast ratio of reflection mode is defined as follows:

[Note 9-9] Reflectance is defined as follows

[Note 9-10] It is assumed that chromaticity of the light source is (x=0.313,y=0.329). The measuring system is CM-2002(with the unit reflecting diffusely) made by MINOLTA co., ltd.

[Note 9-11] LED life is the time when the Brightness level of the panel surface doesn't become equal or less than 50% of the brightness of the initial value on the following conditions.

* LED driving condition is refer to Table7-3. PWM dimming 100%~5%(Ta=25°C)

[Note 9-12] When you adjust the power supply voltage level and signal voltage level to the following set value .

VLS= $5.3V \pm 0.05V(5.25V \sim 5.35V)$, VCOMAC= $8.4Vp-p \pm 0.1Vp-p(8.3Vp-p \sim 8.5Vp-p)$

(10) Mechanical characteristics

10-1) External appearance

No significant defects permitted. (See Fig. 1)

10-2) Panel toughness

The panel should not be broken, when press to the center of the panel by 30N power using smooth surface with 15mm diameter.

Caution: If the pressure is added on the active area of the panel over the long time, even if the pressure is very small weight , the functional damage might occur in the panel.

10-3) I/O connector performance

A) Input/output connectors to control the LCD module

÷

- 1) Applicable Connector : FH28-50S-0.5SH (HIROSE)
- 2) FPC flexibility

Slit on the film cover lay coat part of one side printing

If it had been tested bending under radius nothingness and bending angle

180degrees, the FPC should not be cut.

(It should be bend by hand and only at once).

B) Input/output connector of LED backlight driving circuit

2

- 1) Applicable Connector : FH28E-20S-0.5SH (HIROSE)
- 2) FPC flexibility

Slit on the film cover lay coat part of one side printing

If it had been tested bending under radius nothingness and bending angle

180degrees, the FPC should not be cut.

(It should be bend by hand and only at once).

(11) Display quality

The display quality of the color TFT-LCD module is controlled by the Incoming Inspection Standard.

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(12) Handling instruction of TFT-LCD module

12-1) Handling of FPC

TFPC can be bent only in the input part straight wiring part.

②Please do not hang the LCD module from the FPC or do not apply excessive force to FPC.

③Please do not impact on the part equipped with parts of FPC.

12-2) Installation of TFT-LCD module

- ①When assembling the TFT-LCD module, ensure module is fixed in its natural flat plane, and avoid stressing the module causing it to twist or wrap.
 - Do not apply pressure to the module from the user application (user push-buttons etc.) since this may distort the display images.
- ②Remove all electrical power before connecting or disconnecting the module FPCs.
- ③Be sure to connect the metallic shielding cases of the module and the GND of the LED B/L driving circuit surely.

(4) The sensor hall on the back of the module is a part that dust especially enters easily. Please the process design the equipment and design the structure so that dust should not invade after the built-in time and building in.

12-3) Precautions in mounting

①Polarizer adhesion the surface of the LCD is made of a soft material and should be handled carefully to avoid damage. Protection sheet is applied on the LCD top surface to safeguard the polarizer against scratches and dirt. It is recommended to remove the protection sheet immediately before use, taking care to avoid static electric charges.

②Precautions in removing the protection sheet

A) Work environment

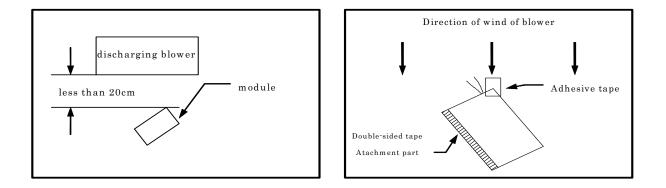
When the protection sheet is removed off, static electricity may cause dust to stick to the polarizer surface. To avoid this, the following working environment is desirable.

a) Floor : Conductive treatment of $1M\Omega$ or more on the tile.

(conductive mat or conductive paint on the tile)

- b) Clean room free form dust and with an adhesive mat on the doorway
- c) Advisable humidity:50%~70% Advisable temperature:15 °C~27 °C
- d) Workers shall wear conductive shoes, conductive work clothes, conductive gloves and an earth band.
- B) Working procedures
 - a) Direct the air of discharging blower in downward to ensure that module is blown sufficiently. Keep the distance between module and discharging blower within 20 cm.
 - b) Attach adhesive tape to the protection sheet part near discharging blower so as to protect polarizer against flaw.
 - c) Remove the protection sheet , pulling adhesive tape slowly to your side.

- d) On removing off the protection sheet, pass the module to the next work process to prevent the module to get dust.
- e) Method of removing dust from polarizer
- ·Blow off dust with N2 blower for which static electricity preventive measure has been taken.
- ·Since polarizer is vulnerable, wiping should be avoided if necessary.
- However, please wipe it carefully with the cloth for a lens wipe when it is necessary to wipe the surface.



③When metal part of the TFT-LCD module (shielding case) soiled, wipe it with soft dry cloth.

- (4) The LCD used in the module is made of glass. If drop the module or bump it on hard surface, the LCD should be broken. Please handle with care.
- ⑤Since CMOS LSI is used in this module, take care of static electricity and earth your body when handling the module.
- 12-4) Caution of product design
 - ①Protect the LCD module from water/salt-water by the waterproof cover, etc.
 - ②Please implement electromagnetic shielding measures to prevent interference from radiated emissions originating from the module, which could affect peripheral appliances.

12-5) Other

- (1) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours. Liquid crystal is deteriorated by ultraviolet rays.
- ②Store the module at a temperature near the room temperature. At lower than the rated storage temperature, liquid crystal solidifies, causing the panel to be damaged. At higher than the rated storage temperature, liquid crystal turns into isotropic liquid and may not recover.
- ③If LCD panel breaks, there may be a possibility that the liquid crystal escapes from the panel. Since the liquid crystal is hazardous, do not put it into the eyes or mouth. When liquid crystal sticks to hands, feet or clothes, wash it out immediately with soap.
- ④Be sure to adjust DC bias voltage of common electrode driving signal(VCOM DC) in the state of the last product. When not adjusted, it becomes the cause of a deterioration of display quality.
- ⑤Observe all precautionary requirements of general electronic components.

(13) Packing form

a) Maximum number of cartons for stacking	: 7
b) Package quantity in one carton	: 20pcs
c) carton size	:594×379×246(H)
d) Total mass of one carton	:8.6kg

13-2) Carton keeping conditions

Environments

Temperature	:	0~40°C	
Humidity	:	60%RH or less(at 40°C)	
Atmosphere	:	No dew condensation at low temperature and high humidity. Harmful gas such as acid or alkaline that corrodes electronic components or wires, must not be avoided.	
Storage periods	:	Max of approx 3 months	
Opening of	:	In order to prevent the LCD module from breakdown by electrostatic	
the package charges, please control the humidity over 50%RH and open the package			
		taking sufficient countermeasures against electrostatic charges, such as	
		earth, etc.	

(14) Other

14-1) Indication of the lot number

The lot number is shown on a label. Attached location is shown in Fig.1 (Outline Dimensions).

Indicated contents of the label :

 LQ088K9LA02
 OOOOOOOO

 Model name
 lot number

contents of lot No. the 1st figure production year (ex. 2007 : 7) the 2nd figure production month 1,2,3,...,9,X,Y,Z the 3rd \sim 8th figure serial No. 000001 \sim the 9th figure revision marks A,B,C...

14-2) RoHS

This TFT-LCD module is RoHS compliant products.

14-3) Instructions for disposing of LCD modules.

Please dispose in accordance to regulations for this module.

14-4) The country of origin of the TFT-LCD module

JAPAN

14-5) Other

About RUEKO DCC

RUEKO DCC (Display CORE CHIP) is a display controller whom ALPINE and SHARP developed.

(15) Reliability test contents

Table	ble 15-1 Temperature condition is based on operating temperature condition			
No.	Test items	Test condition		
1	High temperature storage test	Ta = +85 °C 240h		
2	High temperature storage test	Ta = +95 °C 120h		
3	Low temperature storage test	Ta =-40 °C 240h		
4	High temperature and high	Tp = +50 °C , 95%RH 240h		
	humidity operation test			
5	Hi temperature operating test	$Tp = +85 ^{\circ}C$ 240h		
6	Low temperature operating test	Ta = -40 °C 240h		
7	Electro static discharge test	$\pm 200V \cdot 200$ pF(0Ω) 1 time for each terminals		
		\pm 2KV \cdot 150pF(330Ω) 3 time for each terminals		
		±15KV \cdot 150pF(330Ω) 3 time for the display center		
8	Shock test	980m/s ² · 6ms, $\pm X$; $\pm Y$; $\pm Z$ 3 times for each direction		
		(JIS C0041, A-7 Condition C) [caution]		
9	Vibration test	Frequency : 8 \sim 33.3Hz , Stroke : 1.3mm		
		Frequency : 33.3Hz \sim 400Hz,Acceleration : 28.4m/s ²		
		Cycle : 15 minutes		
		X,Z 2 hours for each directions, 4 hours for Y direction (total		
		8 hours) 【caution】 (JIS D1601)		
10	Heat shock test(Storage)	Ta= -30° C \sim +85 $^{\circ}$ C / 200 cycles		
		(0.5h) (0.5h)		

Table 15-1 Temperature condition is based on operating temperature condition

[Note]

Ta = Ambient temperature, Tp = Panel temperature

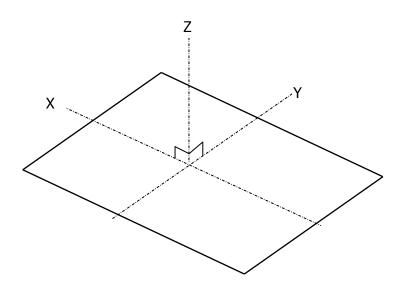
[Check items]

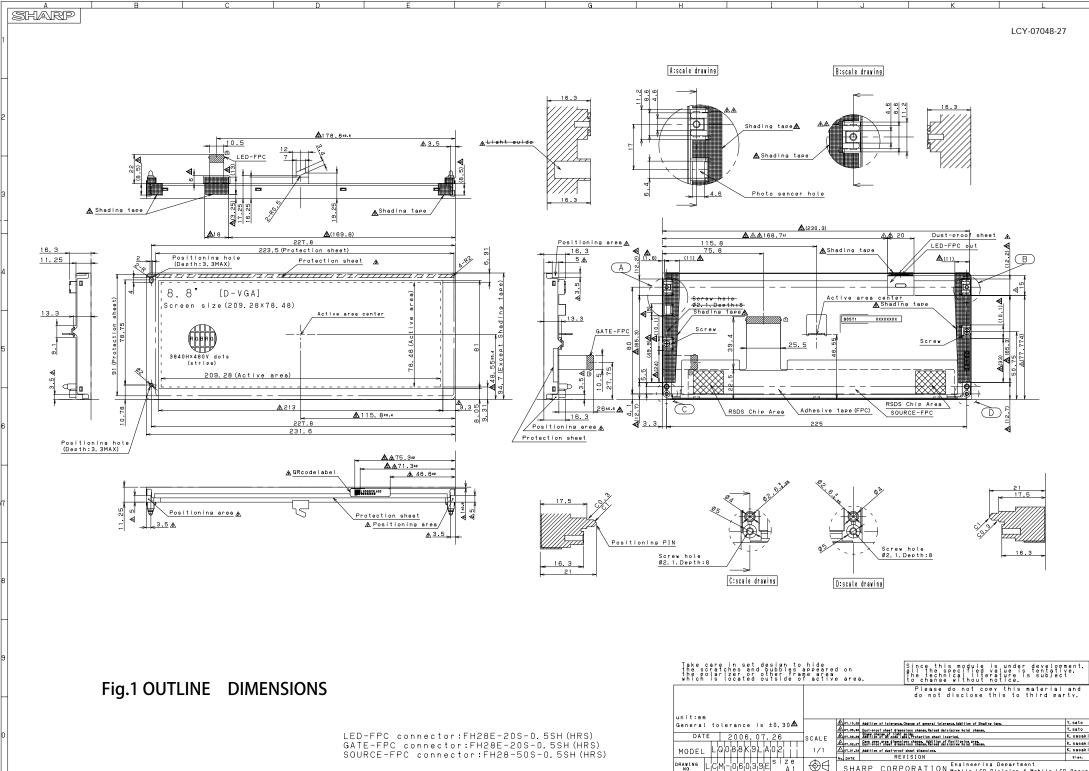
In the standard condition, there shall be no practical problems that may

affect the display function.

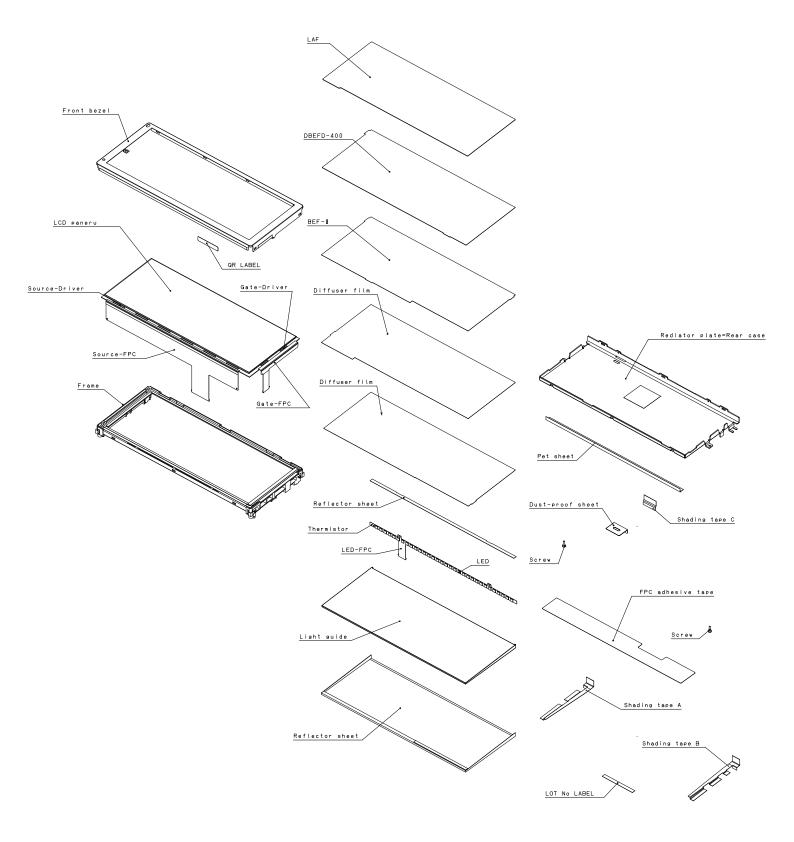
[caution]

Definition of X, Y, Z direction is shown as follows





SHARP CORPORATION Mobile LCD Division.4 Mobile LCD Group A 1





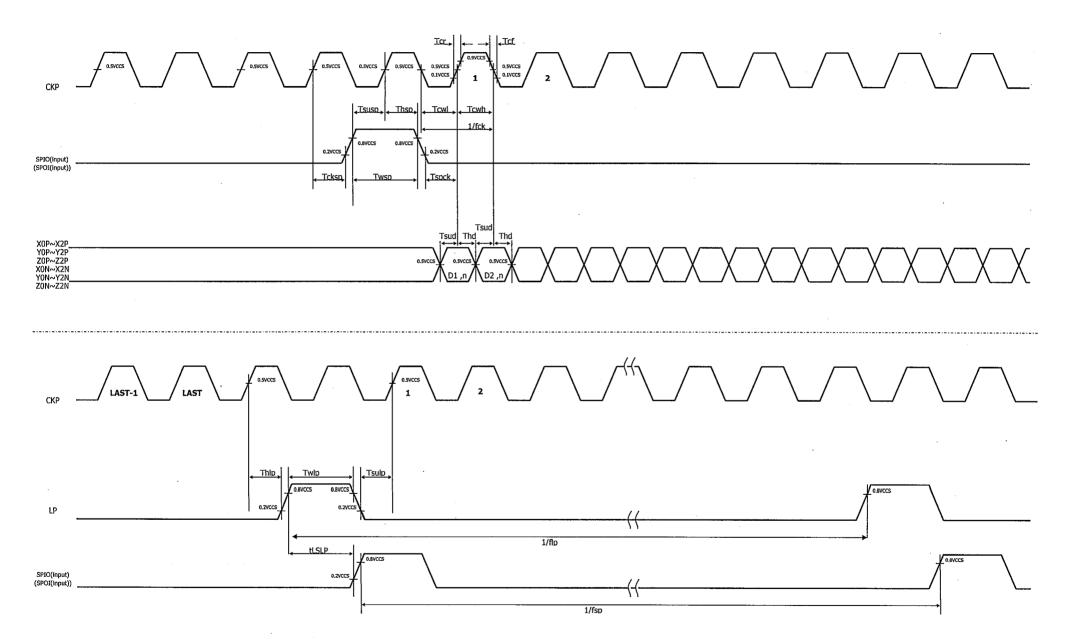


Fig.3-1 AC characteristics of input signals waveform



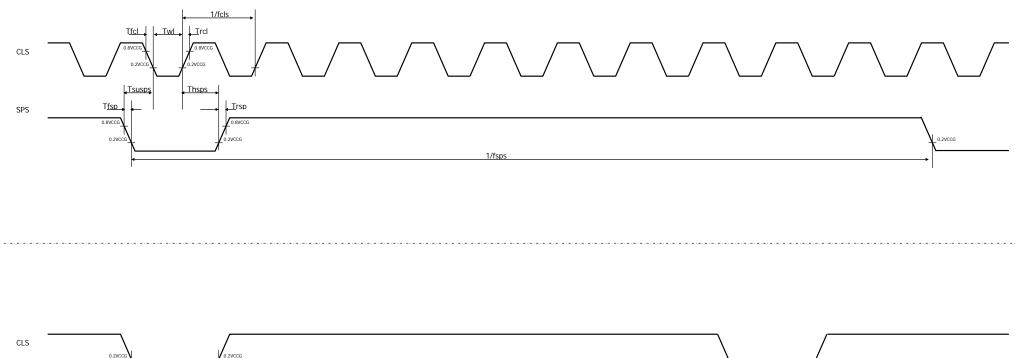




Fig.3-2 AC characteristics of input signals waveform

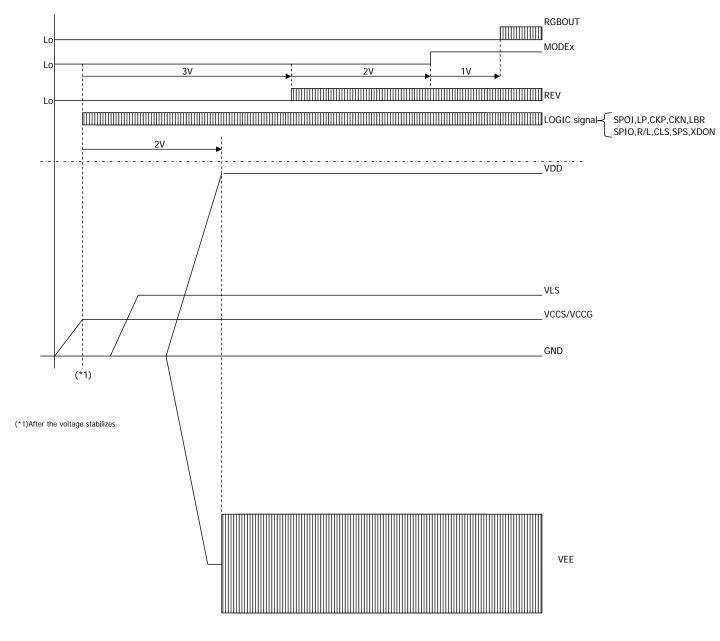
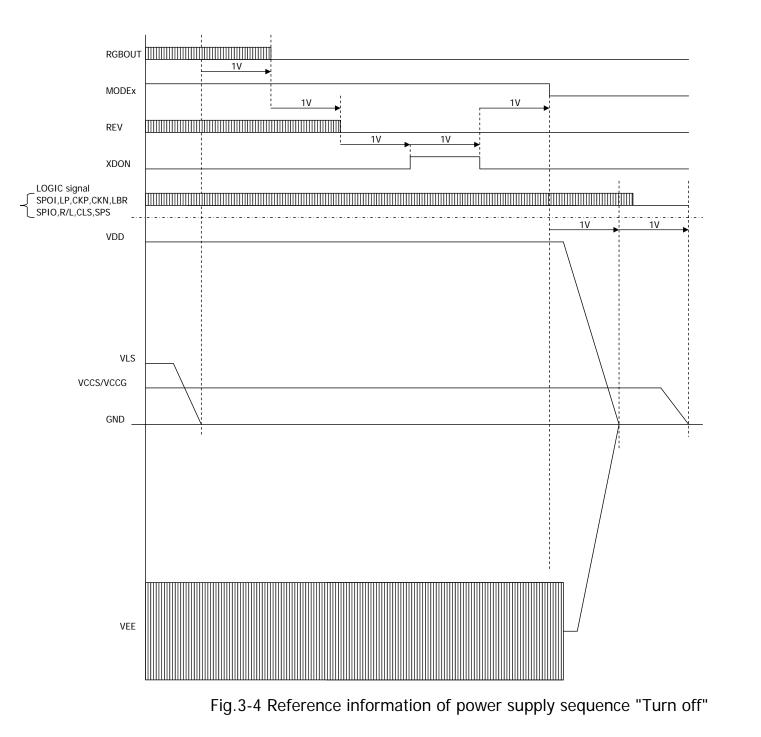
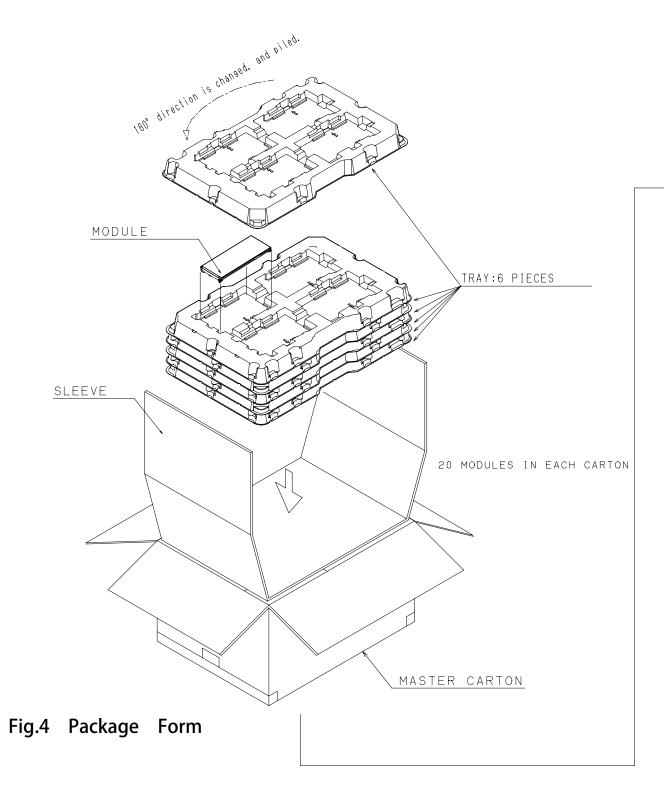
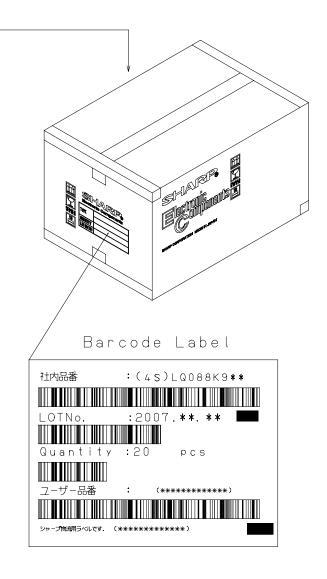


Fig.3-3 Reference information of power supply sequence "Turn on"



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(Appendix)

Adjusting method of optimum DC bias voltage of common electrode driving signal

Photoelectric devices are very effective to obtain optimum DC bias voltage of common electrode driving signal accurately, and the accuracy is with 0.1V. (In visual examination method, the accuracy is about 0.5V because of the difference among individuals.)

Adjusting method of DC bias voltage using the photoelectric devices is as follows

Measurement of flicker

Adjust the DC baias voltage so as to minimize flicker at NTSC : 60Hz(30Hz) / PAL : 50Hz(25Hz).

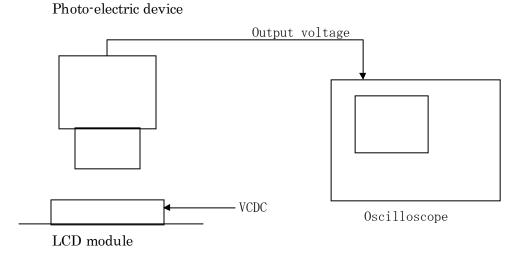


Fig. A Measurement system

Adjusting method of DC bias voltage

Measure the output voltage from Photoelectric device using the oscilloscope at the measurement system of Fig. A.

Then, change the DC bias voltage in small steps, and adjust it so as to minimize the flicker at NTSC 60Hz(30Hz) / PAL : 50Hz(25Hz). (Fig.B)

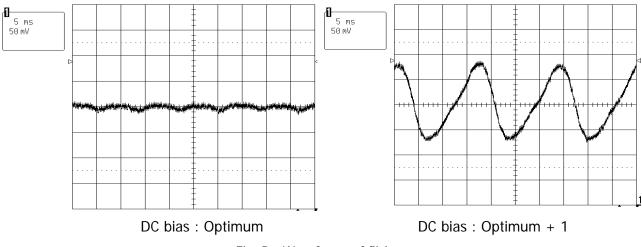


Fig. B Waveforms of flicker