

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4543 BCD to 7-segment latch/decoder/driver for LCDs

Product specification
File under Integrated Circuits, IC06

December 1990

BCD to 7-segment latch/decoder/driver for LCDs

74HC/HCT4543

FEATURES

- Latch storage of BCD inputs
- Blanking inputs
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4543 are high-speed Si-gate CMOS devices and are pin compatible with "4543" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4543 are BCD to 7-segment latch/decoder/drivers for liquid crystal displays. They have

four address inputs (D₀ to D₃), an active HIGH latch disable input (LD), an active HIGH blanking input (BI), an active HIGH phase input (PH) and seven buffered segment outputs (Q_a to Q_g).

The "4543" provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder driver. The "4543" can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the "4543" are directly connected to the segments of the liquid crystal.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay	C _L = 15 pF; V _{CC} = 5 V			
	D _n to Q _n		29	33	ns
	LD to Q _n		32	31	ns
	BI to Q _n		20	28	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	42	42	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:
 f_i = input frequency in MHz
 f_o = output frequency in MHz
 ∑ (C_L × V_{CC}² × f_o) = sum of outputs
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} -1.5 V

ORDERING INFORMATION

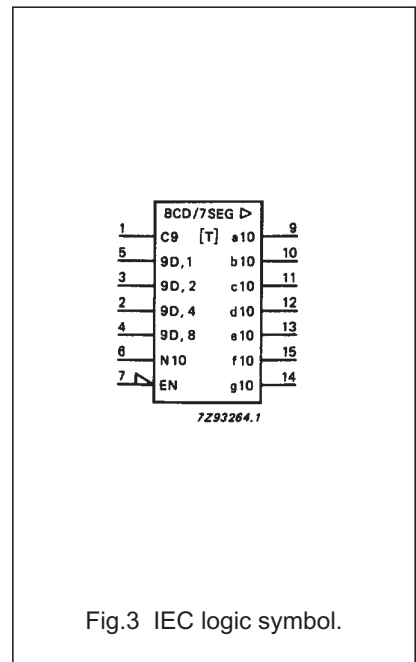
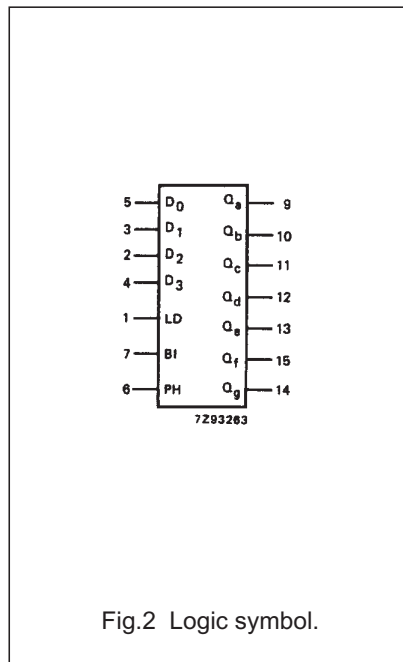
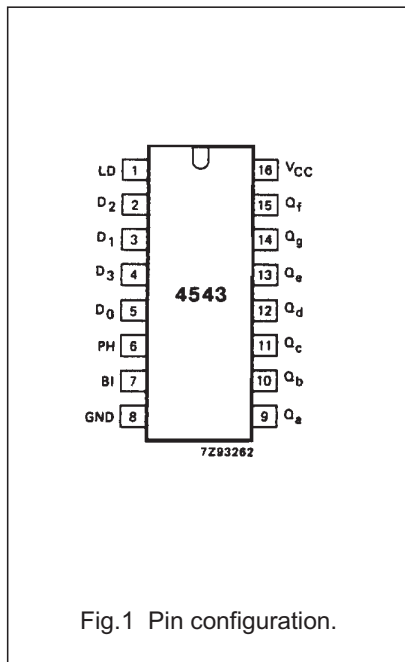
See "74HC/HCT/HCU/HCMOS Logic Package Information".

BCD to 7-segment latch/decoder/driver for
LCDs

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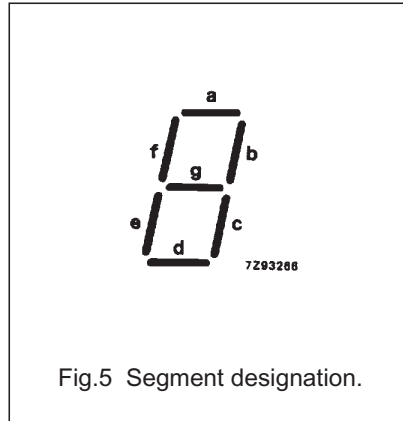
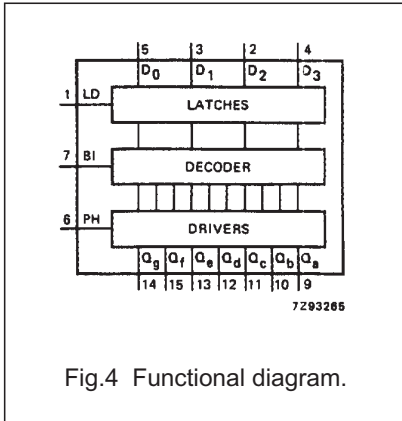
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	latch disable input (active HIGH)
5, 3, 2, 4	D ₀ to D ₃	address (data) inputs
6	PH	phase input (active HIGH)
7	BI	blanking input (active HIGH)
8	GND	ground (0 V)
9, 10, 11, 12, 13, 15, 14	Q _a to Q _g	segment outputs
16	V _{CC}	positive supply voltage



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APPLICATIONS

- Driving LCD displays
- Driving fluorescent displays
- Driving incandescent displays
- Driving gas discharge displays

FUNCTION TABLE

INPUTS							OUTPUTS							DISPLAY
LD	BI	PH ⁽¹⁾	D ₃	D ₂	D ₁	D ₀	Q _a	Q _b	Q _c	Q _d	Q _e	Q _f	Q _g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				(1)				(1)
as above		H	as above				inverse of above							as above

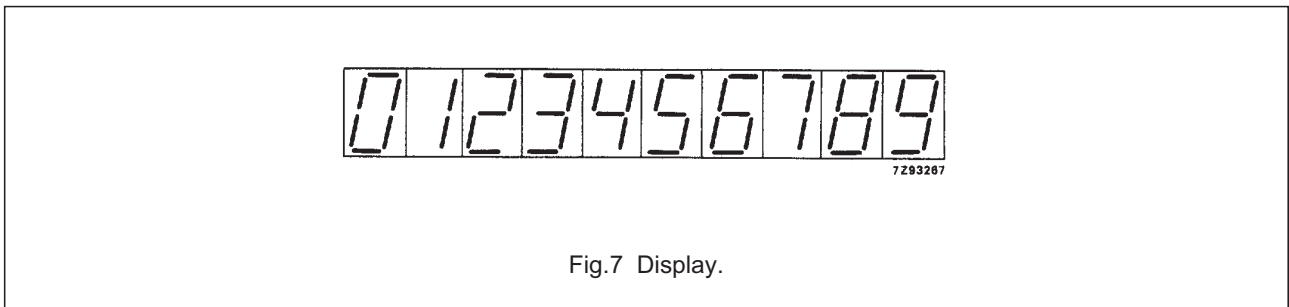
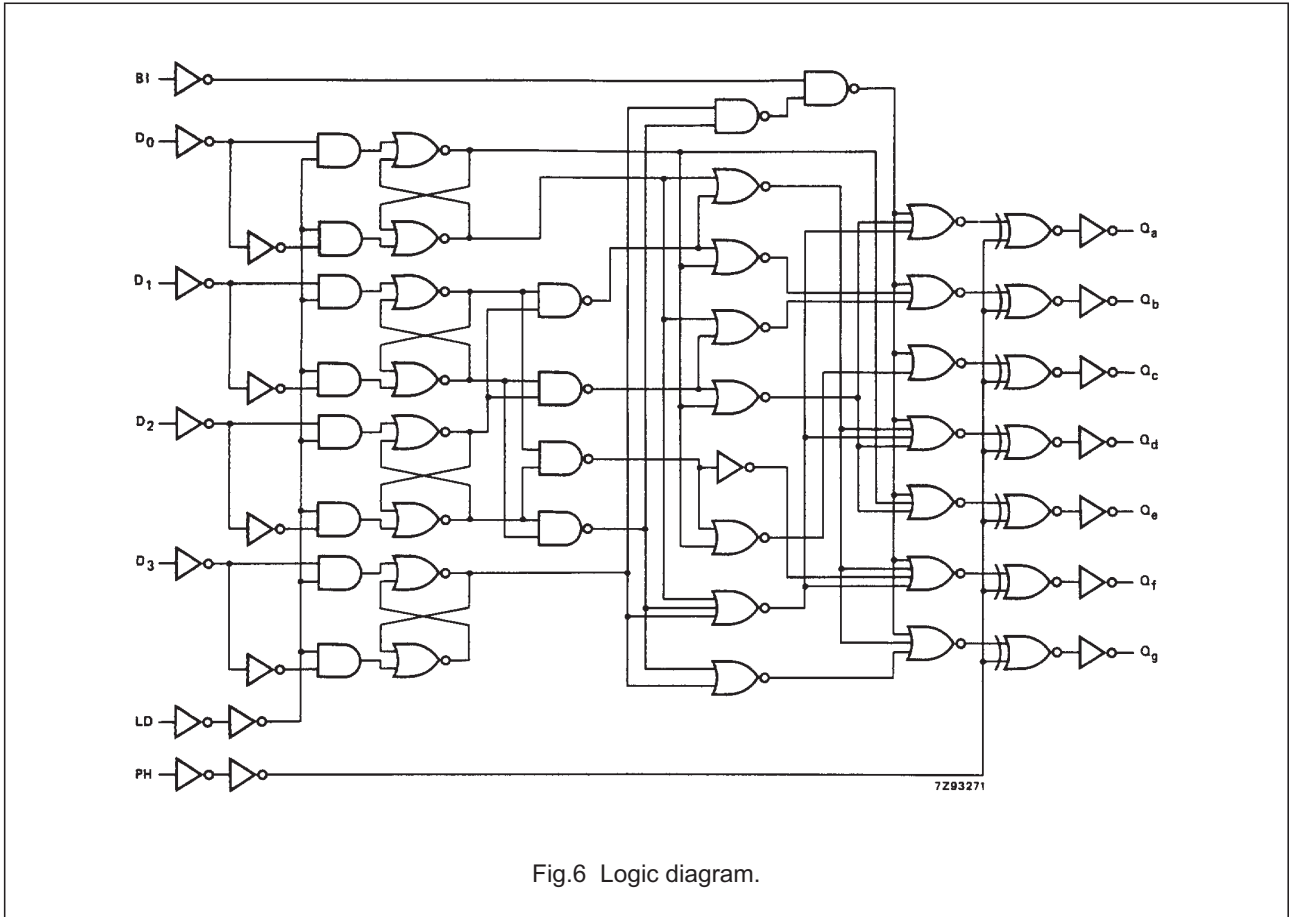
Notes

1. For liquid crystal displays, apply a square-wave to PH.
2. Depends upon the BCD-code previously applied when LD = HIGH.

H = HIGH voltage level
 L = LOW voltage level
 X = don't care

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).
 For RATINGS see *“74HC/HCT/HCU/HCMOS Logic Family Specifications”*, standard outputs.

BCD to 7-segment latch/decoder/driver for
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DC CHARACTERISTICS FOR 74HC

Output capability: non-standard

 I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)								UNIT	TEST CONDITIONS		
		74HC									V_{CC} (V)	V_I	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0			
V_{IL}	LOW level input voltage		0.7 1.8 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0			
V_{OH}	HIGH level output voltage	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20 \mu A$ $-I_O = 20 \mu A$ $-I_O = 20 \mu A$	
V_{OH}	HIGH level output voltage	3.98 5.48	0.15 0.16		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 1.0 mA$ $-I_O = 1.3 mA$	
V_{OL}	LOW level output voltage		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20 \mu A$ $I_O = 20 \mu A$ $I_O = 20 \mu A$	
V_{OL}	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 1.0 mA$ $I_O = 1.3 mA$	
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND		
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	6.0	V_{CC} or GND	$I_O = 0$	

BCD to 7-segment latch/decoder/driver for
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AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	OTHER
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D _n to Q _n		91 33 26	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig.12
t_{PHL}/t_{PLH}	propagation delay LD to Q _n		102 37 30	370 74 63		465 93 79		555 111 94	ns	2.0 4.5 6.0	Fig.13
t_{PHL}/t_{PLH}	propagation delay BI to Q _n		66 24 19	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig.14
t_{PHL}/t_{PLH}	propagation delay PH to Q _n		55 20 16	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	
t_{THL}/t_{TLH}	output transition time		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Figs 12, 13 and 14
t_W	LD pulse width HIGH or LOW	35 7 6	11 4 3		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig.13
t_{su}	set-up time D _n to LD	60 12 10	8 3 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.15
t_h	hold time D _n to LD	30 6 5	3 1 1		40 8 7		45 9 8		ns	2.0 4.5 6.0	Fig.15

BCD to 7-segment latch/decoder/driver for
LCDs

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DC CHARACTERISTICS FOR 74HCT

Output capability: non-standard

 I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_I	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20 \mu A$
V_{OH}	HIGH level output voltage	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 1.0 mA$
V_{OL}	LOW level output voltage		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20 \mu A$
V_{OL}	LOW level output voltage		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 1.0 mA$
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	$V_{CC} - 2.1V$	other inputs at V_{CC} or GND; $I_O = 0$

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Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D ₀ , D ₁ , D ₂	1.00
D ₃	0.50
BI	0.50
LD	1.50
PH	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} (V)	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay D _n to Q _n		38	80		100		120	ns	4.5	Fig.12
t _{PHL} / t _{PLH}	propagation delay LD to Q _n		36	68		85		102	ns	4.5	Fig.13
t _{PHL} / t _{PLH}	propagation delay BI to Q _n		32	66		83		99	ns	4.5	Fig.14
t _{PHL} / t _{PLH}	propagation delay PH to Q _n		24	66		83		99	ns	4.5	
t _{THL} / t _{TLH}	output transition time		23	50		63		75	ns	4.5	Figs 12, 13 and 14
t _w	LD pulse width HIGH or LOW	10	4		13		15		ns	4.5	Fig.13
t _{su}	set-up time D _n to LD	12	4		15		18		ns	4.5	Fig.15
t _h	hold time D _n to LD	8	2		10		12		ns	4.5	Fig.15

BCD to 7-segment latch/decoder/driver for LCDs

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APPLICATION DIAGRAMS

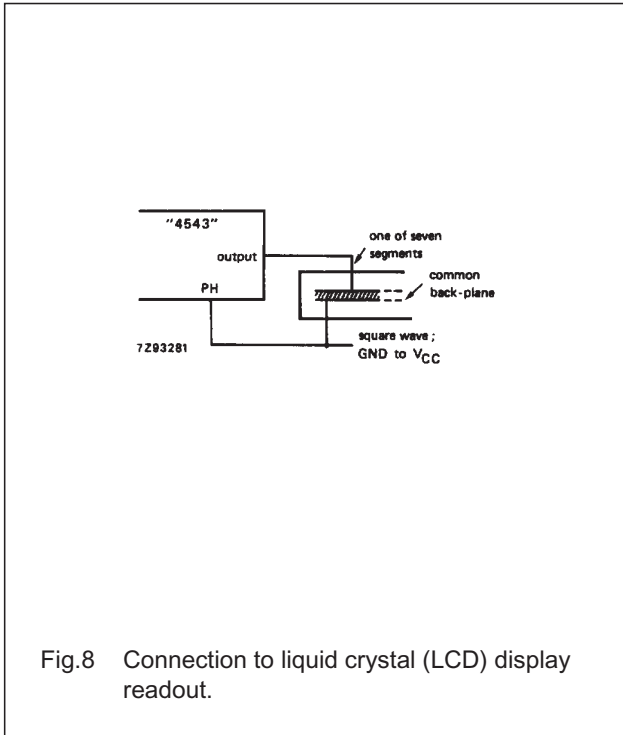


Fig.8 Connection to liquid crystal (LCD) display readout.

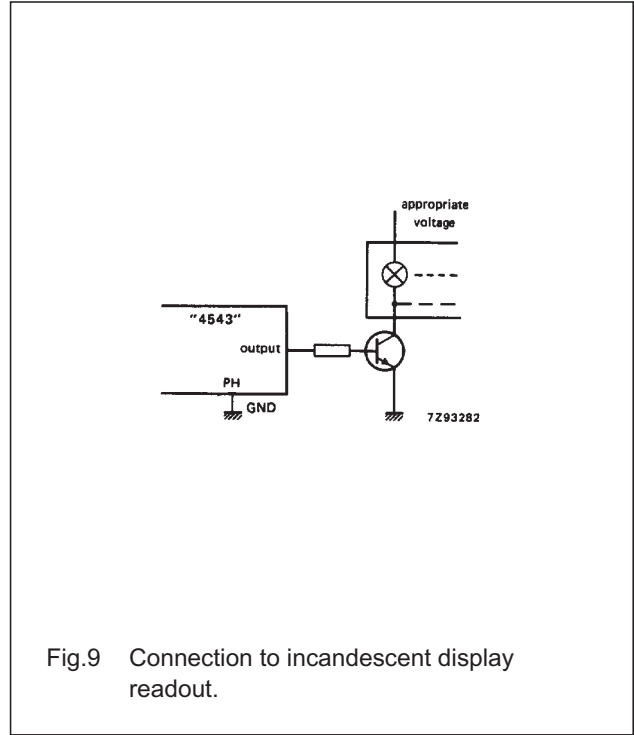


Fig.9 Connection to incandescent display readout.

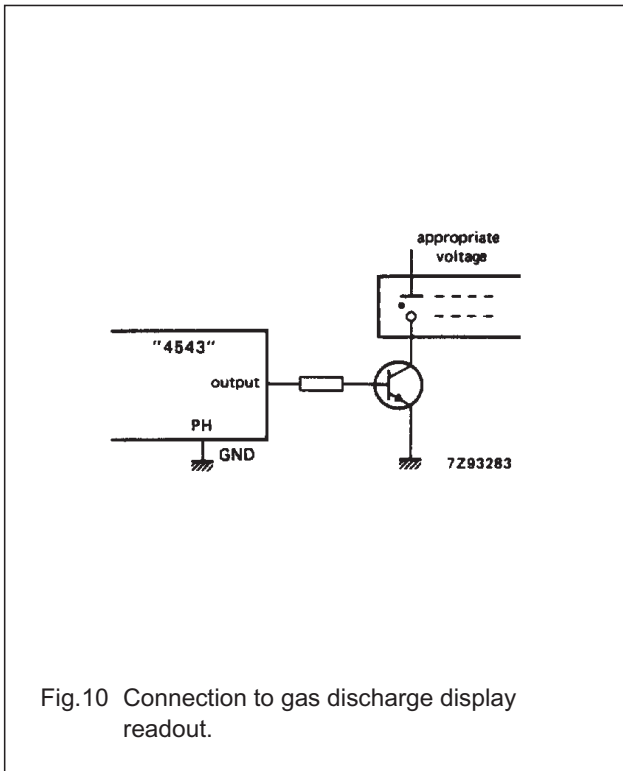


Fig.10 Connection to gas discharge display readout.

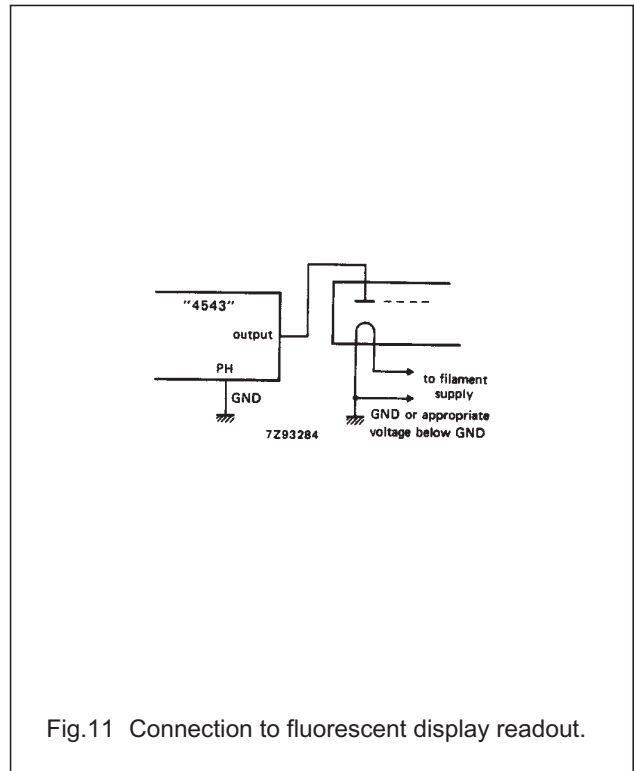
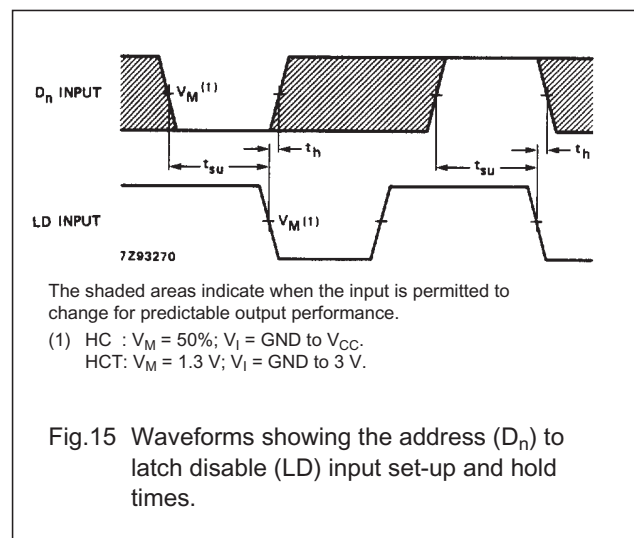
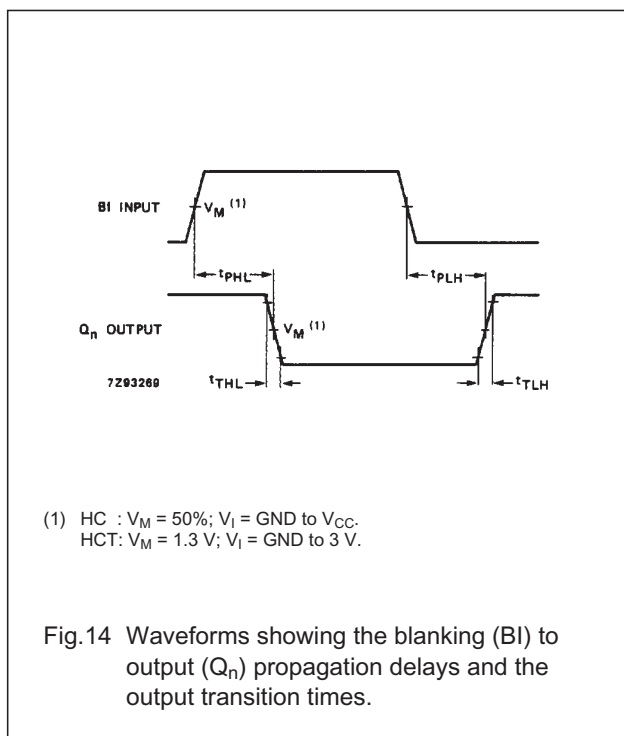
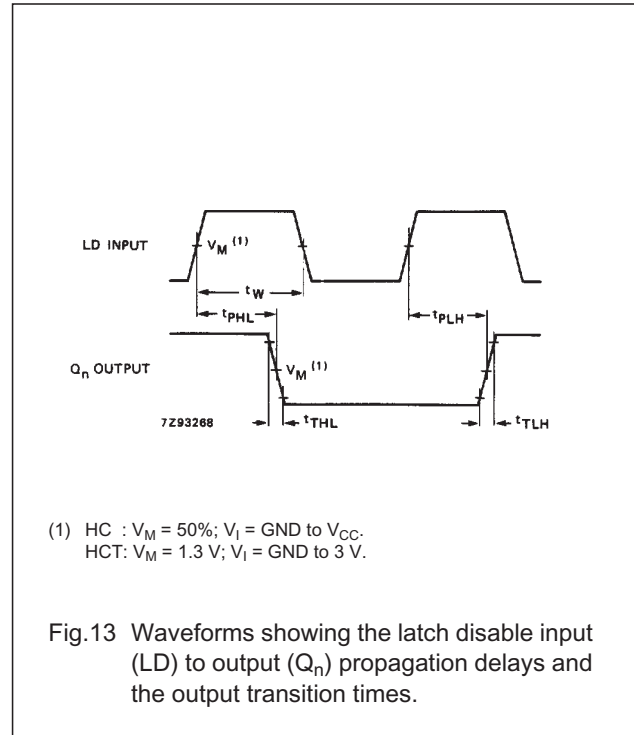
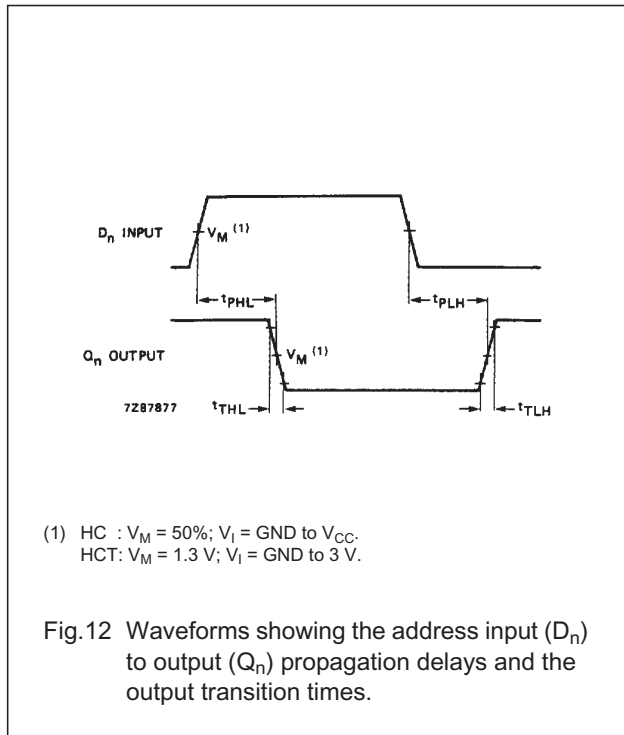


Fig.11 Connection to fluorescent display readout.

BCD to 7-segment latch/decoder/driver for LCDs

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".