Cortex-M1 FPGA Development Kit Cortex-M1 User Altera Edition version **Guide** 1.1

6.2.1. CPUID Base Register

Read the CPUID Base Register to determine:

- the ID number of the processor core
- the version number of the processor core
- the implementation details of the processor core.

The register address, access type, and reset value are:

Address

0xE000ED00

Access

Read-only

Reset value

0x410CC210

Figure 6.1 shows the bit assignments of the CPUID Base Register.

Figure 6.1. CPUID Base Register bit assignments

31	24 23	20	19 16	15	4	3 0
IMPLEMENTER	V	ARIANT	Constant	PARTNO		REVISION

Table 6.2 lists the bit assignments of the CPUID Base Register.

Table 6.2. CPUID Base Register bit assignments

Bits	Field	Function
[31:24]	IMPLEMENTER	Implementer code:
		0x41 = ARM
[23:20]	VARIANT	Implementation defined variant number:
		0x0 for r0p1
[19:16]	Constant	Reads as 0xc
[15:4]	PARTNO	Number of processor within family:
		0xC21
[3:0]	REVISION	Implementation defined revision number:
		0x1 = r0p1

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