Slides 1 – 12 will be covered in the webinar, including beginning and ending slides. This will take about 20 minutes.

Slides 13 – 16 contain extra information not covered within the webinar.

Introduction

I am Kumen Blake, a Technical Staff Applications Engineer specializing in linear signal processing products.

Subject Matter

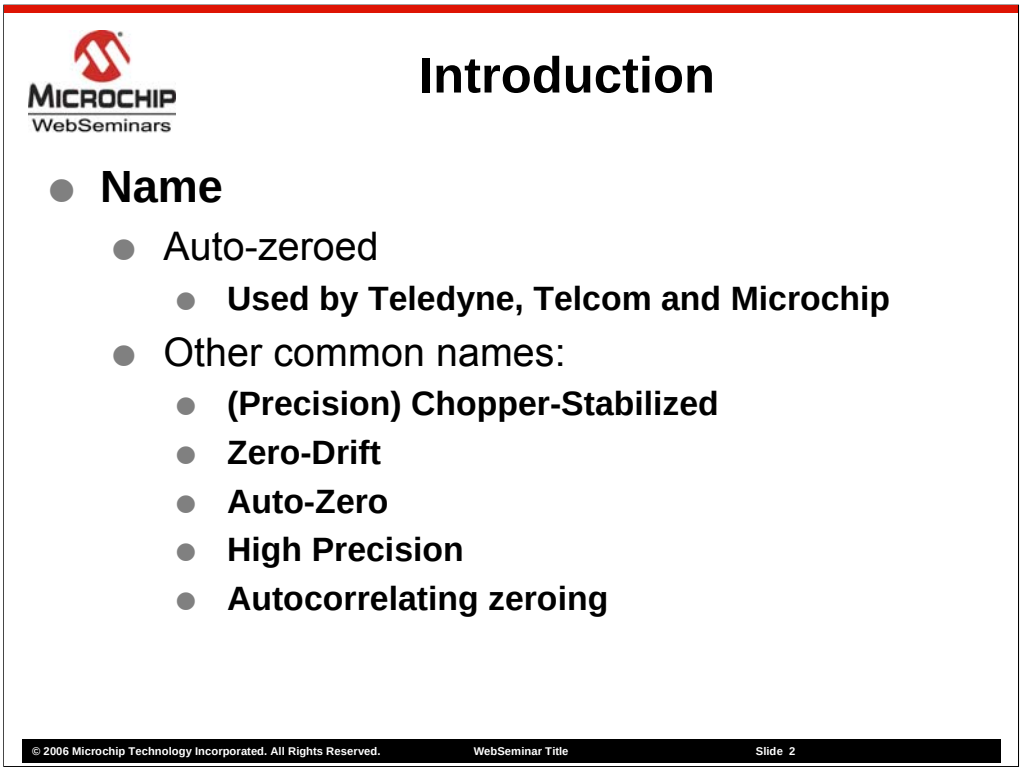
Today I would like to discuss the basic architecture of auto-zeroed op amps. This will help you, the designer, to understand the trade-offs involved in using this type of op amp in your design. Our new auto-zeroed op amps will be mentioned occasionally.

Estimated Presentation Time

This presentation will take about 20 minutes. The presentation slides contain references to additional material.

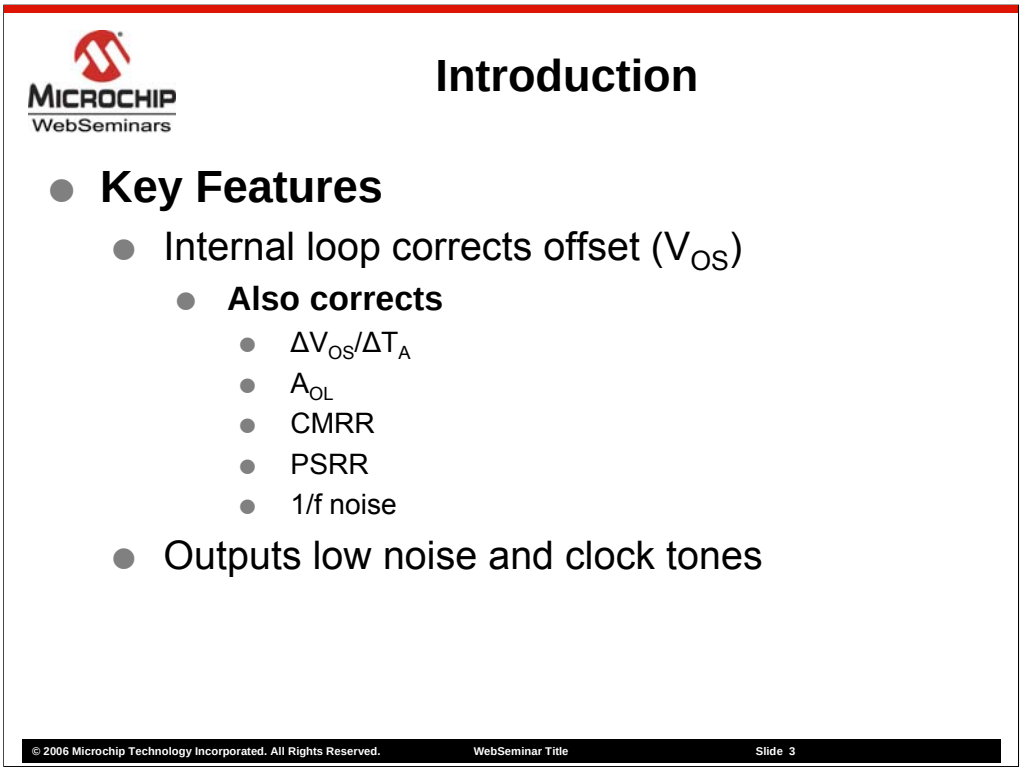
Topics

The topics we will cover include: other names used, key features, clock schemes, the two modes of operation, offset voltage related specifications, noise performance and clock tones.



We have a tradition of precision op amps at Microchip Technology Inc. We bought Telcom in 2001, which was preceded by Teledyne. They both were early innovators of chopper stabilized and auto-zeroed op amps.

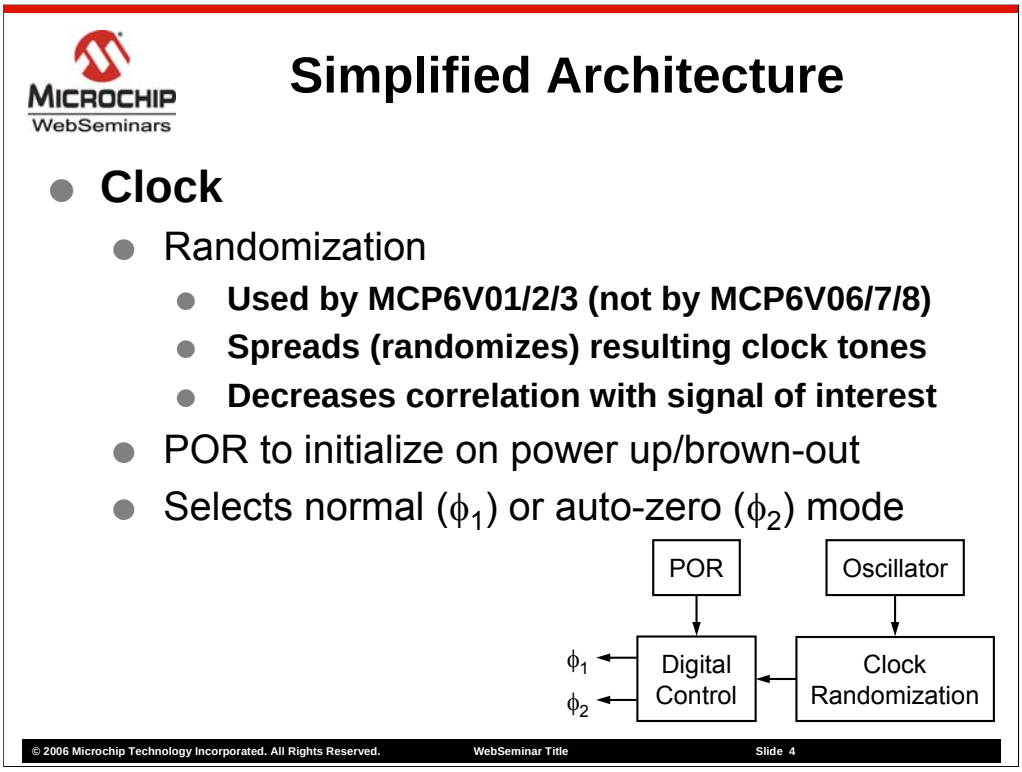
While many names have been used for this type of architecture, modern auto-zeroed op amps are reasonably similar. Technically speaking, chopper stabilized op amps have a different architecture from auto-zeroed op amps. Some writers have used these two terms interchangeably, however.



The key advantage to this architecture is that it corrects the input offset voltage using the advantages of CMOS. This means that the offset can be very low at a reasonable price.

The specifications listed in the slide are all based on input offset. The DC specifications can be thought of as changes in input offset as a result of changing another parameter (in order: temperature, output voltage, input common mode voltage, power supply voltage). 1/f noise is also corrected because it is an error at the input that changes very slowly.

Unlike the chopper amplifiers and chopper-stabilized amplifiers of 2 to 4 decades ago, the modern auto-zeroed op amps have low noise and clock tones at the output. The clock run at a higher rate, so they are easier to filter out.



Sometimes the clocks are randomized, which spreads the clocks tones and making them look more like noise. Done properly, this energy appears well below the op amp's noise floor. This makes the correlation between signal and tones to be negligible for all practical applications. This supports wider bandwidth applications. See the MCP6V01/2/3 data sheet.

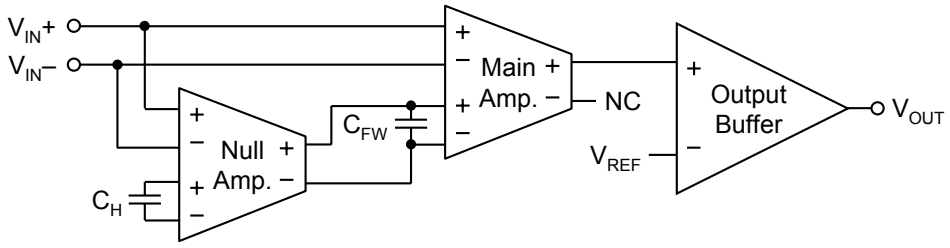
Non-randomized clocks have the advantage of lower noise a low frequencies. Their output has significant clock tones, which limits this variation to lower frequencies. See the MCP6V06/7/8 data sheet for an example.

The POR is very helpful in keeping the internal digital circuitry working properly; even during power brown out conditions.

The normal and auto-zero modes (ϕ_1 and ϕ_2) alternate approximately every 100 µs for the MCP6V01/2/3 family, and every 50 µs for the MCP6V06/7/8 family. This means that the input offset voltage is corrected at this rate.

Simplified Architecture

- **Normal Mode (ϕ_1)**
  - Signal path through Null Amp
  - C_H holds last correction for Null Amp.
  - C_{FW} stores current best value for Main Amp.



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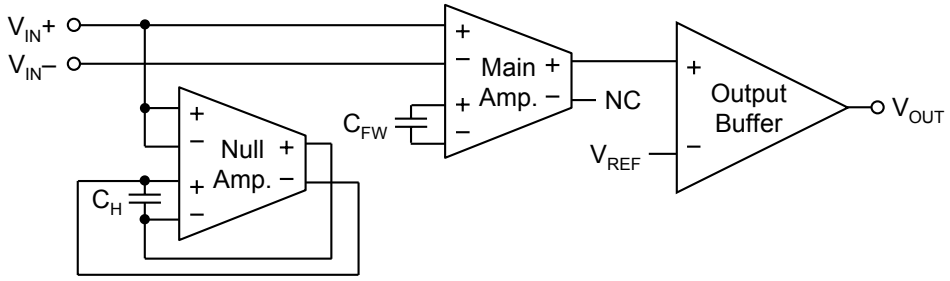
The gain through the Null Amp. is so high, for lower frequencies, that the Main Amp. has minimal influence on V_{OUT}. This means that the Null Amp.'s input offset strongly dominates the overall offset. The capacitor C_H holds a voltage that minimizes the Null Amp.'s offset, so the overall offset is also low.

When the signals at the input are slow, C_H does a great job of correcting the offset. When the input changes fast, however, Inter-modulation Distortion (IMD) appears at the output. This happens because the correction is no longer as accurate as when it was first set.

The Null Amp. forces the voltage on the capacitor C_{FW} to correct the Main Amp.'s input offset. This voltage is updated continuously in this mode.

Simplified Architecture

- **Auto-zero Mode (ϕ_2)**
  - Signal path through Main Amp
  - Null Amp.'s inputs track input common mode
  - C_H is corrected by Null Amp.'s high gain
  - C_{FW} holds last correction for for Main Amp.



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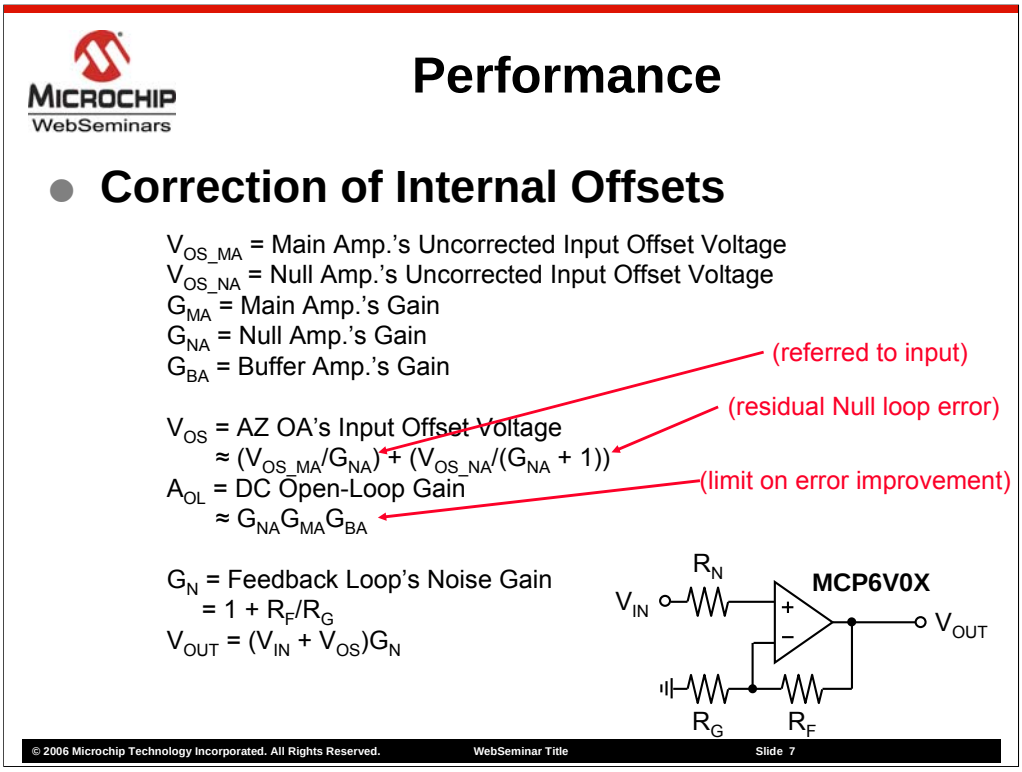
Now the signal goes through the Main Amp. only. Because the voltage across the capacitor C_{FW} is set during the Normal Mode, the input offset is very good at the beginning of this mode. It looses its corrective power, however, as time goes on when the input signals are large and fast.

Placing the Null Amp. in this unity gain configuration forces the best possible correction voltage across the capacitor C_H. Because the Null Amp. inputs are at the input common mode voltage (V_{CM}), and the supply voltage does not change quickly, the correction is at its best possible value the moment we switch back to Normal Mode.

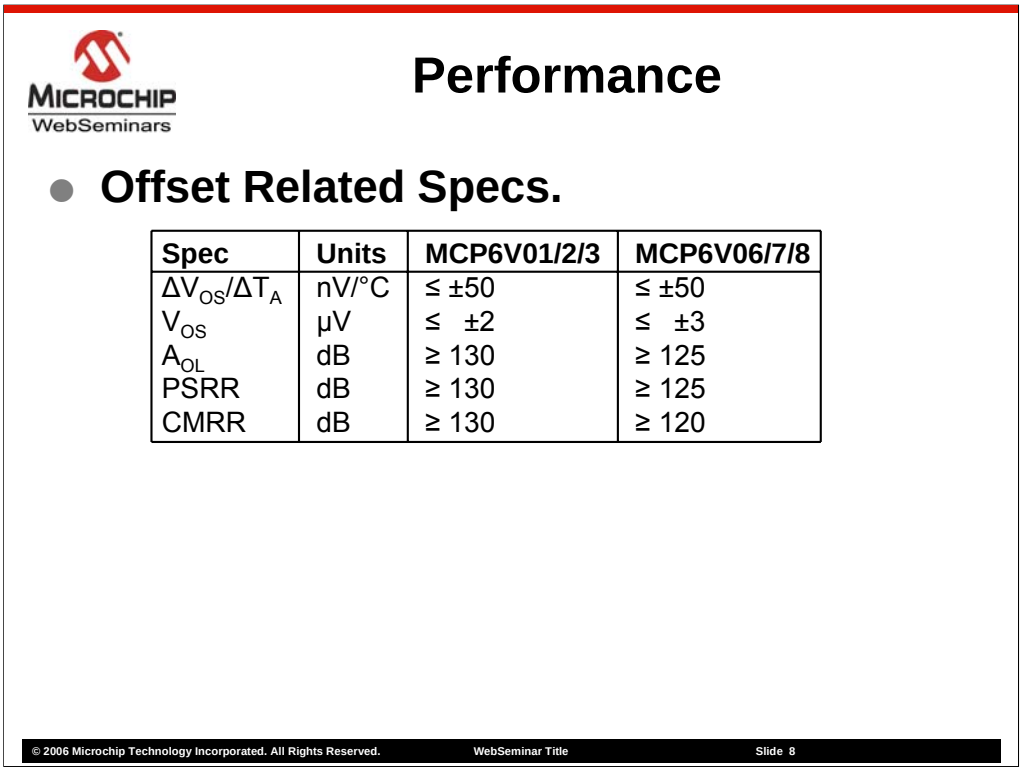


This slide has information that you can examine in greater detail after this presentation. You do not have to grasp all of it at this time.

The equations state that the best correction we can achieve is limited by the Main and Null Amps.' gains; this architecture trades off DC gain for accuracy.

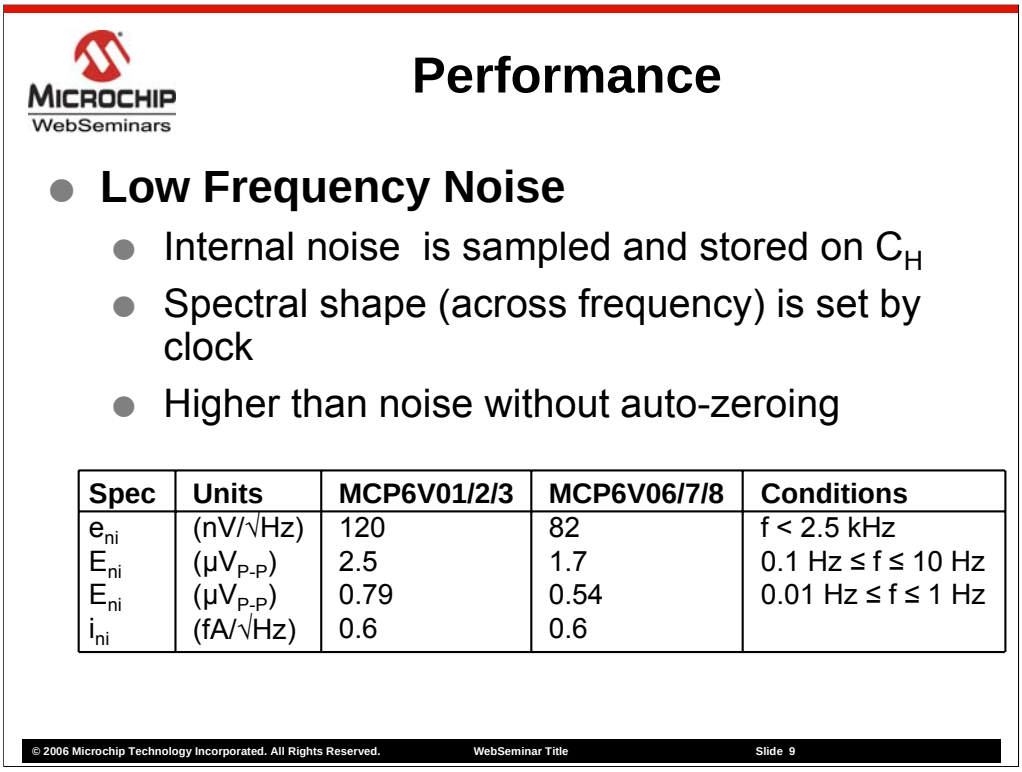
The input offset voltage has two components: the corrected Main Amp. input offset and the corrected Null Amp. input offset. As long as the Null Amp.'s gain is high enough, say 100 dB, the corrected offsets are good. Other error sources are also addressed in a good design.

The DC Open-Loop Gain is the cascaded gain of the Null Amp., Main Amp. and the Output Buffer. If this gain is high enough, then the offset terms can be good. If not, then it is difficult to correct for all of the error sources.



This table gives you an idea of what modern auto-zeroed op amps are capable of. These specification were measured on the bench with good printed circuit boards and good measurement techniques. To take advantage of these specifications, your design also needs to pay attention to these issues!

Notice that the specifications support very accurate applications, even though they represent performance at the parts' minimum supply voltage of 1.8V. They can be though of as supporting 20-plus bits worth of accuracy, depending on the design, when compared the full-scale output range.



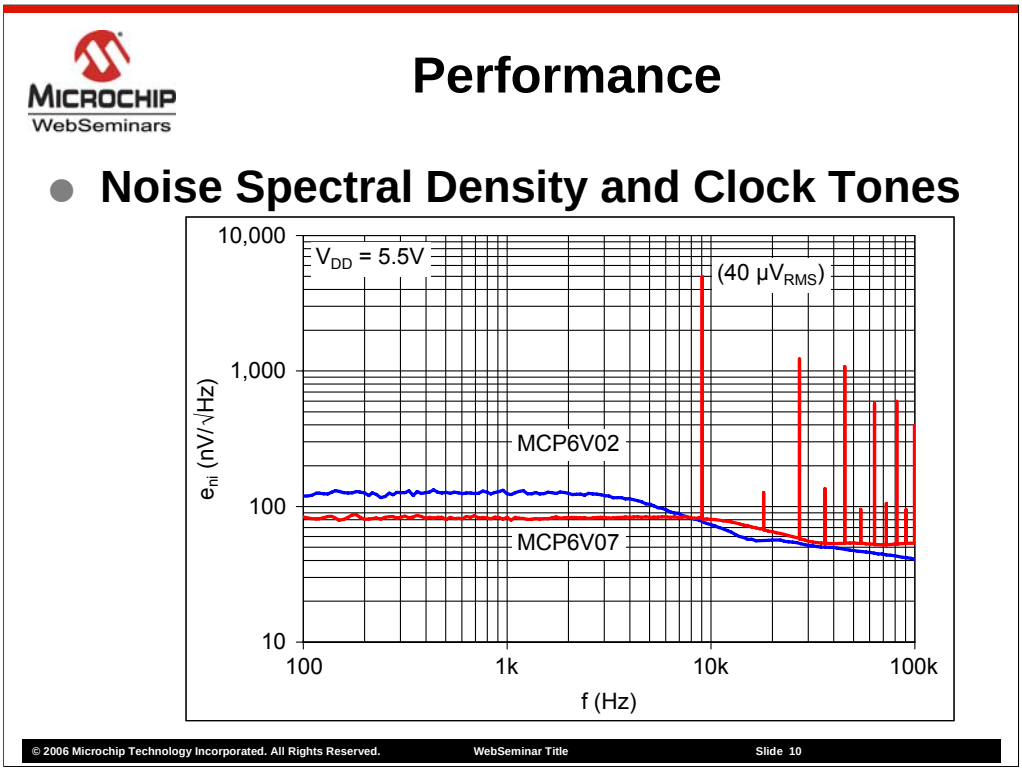
This type of part is accurate enough that your design's noise performance can easily cause greater errors in the output. Picking a part with low noise, using low valued resistors and using a filter with the lowest bandwidth possible, will help minimize this concern.

An auto-zeroed op amp's input noise, at low frequencies, is dominated by the noise that the capacitor C_H samples. Different designs trade-off noise against accuracy and other specifications.

The internal clock sets the noise spectrum's shape. Different clock schemes will give different tradeoffs in noise and clock tone performance.

Looking at the table entries, you can see the importance that selecting the best signal filter can have.

The integrated noise terms (E_{ni} in μV_{P-P}), when divided by 2 to convert to peak voltage (μV_{PK}), can be added directly to the input offset specification (V_{OS}) to obtain the expected range of input offsets that will be seen at any arbitrary sample of the output.

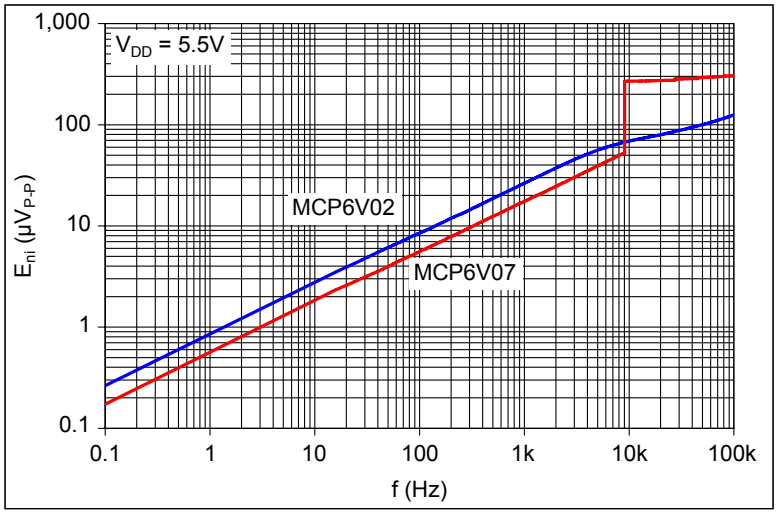


The noise spectral density is a measure of how the op amp's internal random noise interacts with the external circuit's frequency shaping (filtering). You will notice that the MCP6V07 does better at low frequencies, but the MCP6V02 does better at higher frequencies.

The clock tones produced by the MCP6V07 are best represented by power (μV_{RMS}), not power density ($\mu V_{RMS}/\sqrt{Hz}$). The FFT results used for this plot had a frequency spacing of 64 Hz; this was used to convert to the first tone's power (40 μV_{RMS}). The other tones can easily be scaled accordingly.

Performance

- **Integrated Noise (0 Hz to f)**



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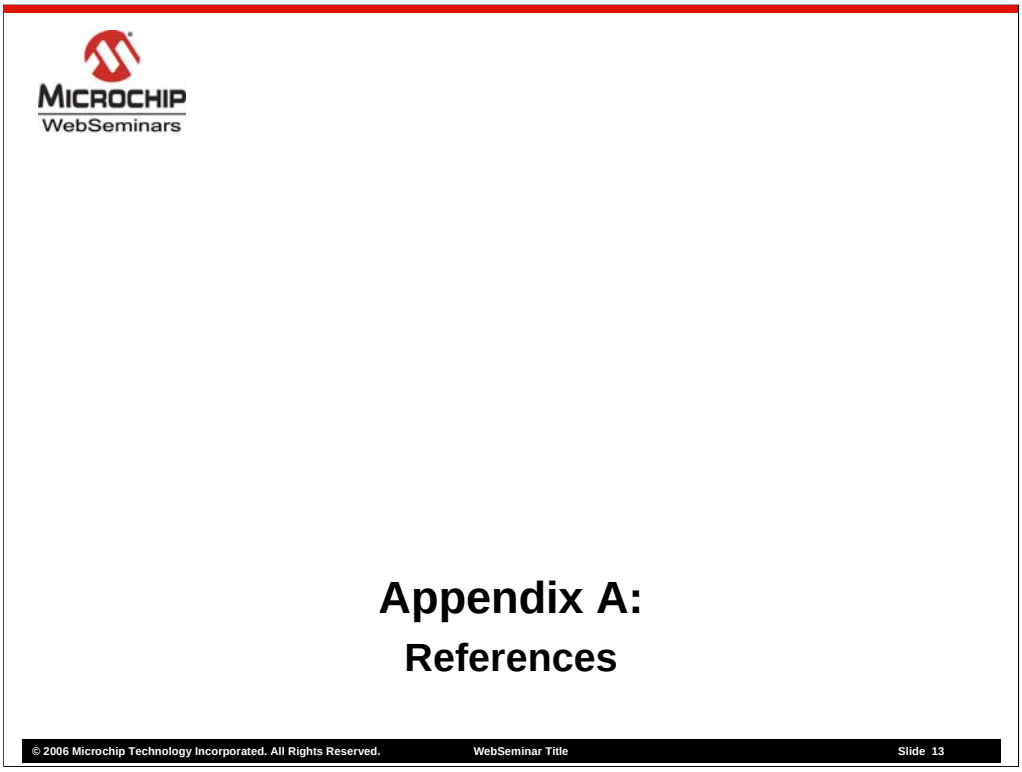
The integrated noise curves shown here are based on a brick wall filter at f (for simplicity) and noise down to 0 Hz (infinite time). The MCP6V07 has an obvious advantage in integrated noise up to the first clock tone (around 9 kHz), while the MCP6V02 gives better integrated noise at high frequencies.

Obviously, applications with a bandwidth much higher than 10 Hz will have greater random variation in V_{OS} than the data sheet spec (see slide 10). Lower bandwidth applications will be affected more by the V_{OS} spec.

End of the presentation.



MATERIAL FOR THE CUSTOMER'S CONVENIENCE *AFTER* THE WEBINAR.

Some of the documents are shown as "Not Released Yet;" they had that status as of the date June 19, 2008.

References

- **App Notes**
  - AN684 (Thermocouple)
    - **Rev. A (traditional amplifier solution)**
  - AN687 (RTD)
    - **Rev. A (absolute reference, complicated)**
    - **Rev. B (not released yet; filter fixes, …)**
  - AN884 (OA & CL)
    - **Rev. B (not released yet)**
  - AN1177 (OA DC Errors)
    - **Rev. A**

References

- **Demo Boards**
  - MCP6V01 Thermocouple Auto-Zeroed Reference Design Board
- **User's Guides**
  - MCP6V01 Thermocouple Auto-Zeroed Reference Design Board

References

- **Data Sheets**
  - MCP6V01/2/3 Data Sheet
    - **Rev. B, “300 µA, Auto-Zeroed Op Amps,” DS22058, Microchip, 2008**
  - MCP6V06/7/8 Data Sheet
    - **Rev. A, “300 µA, Auto-Zeroed Op Amps,” DS22093, Microchip, 2008**

