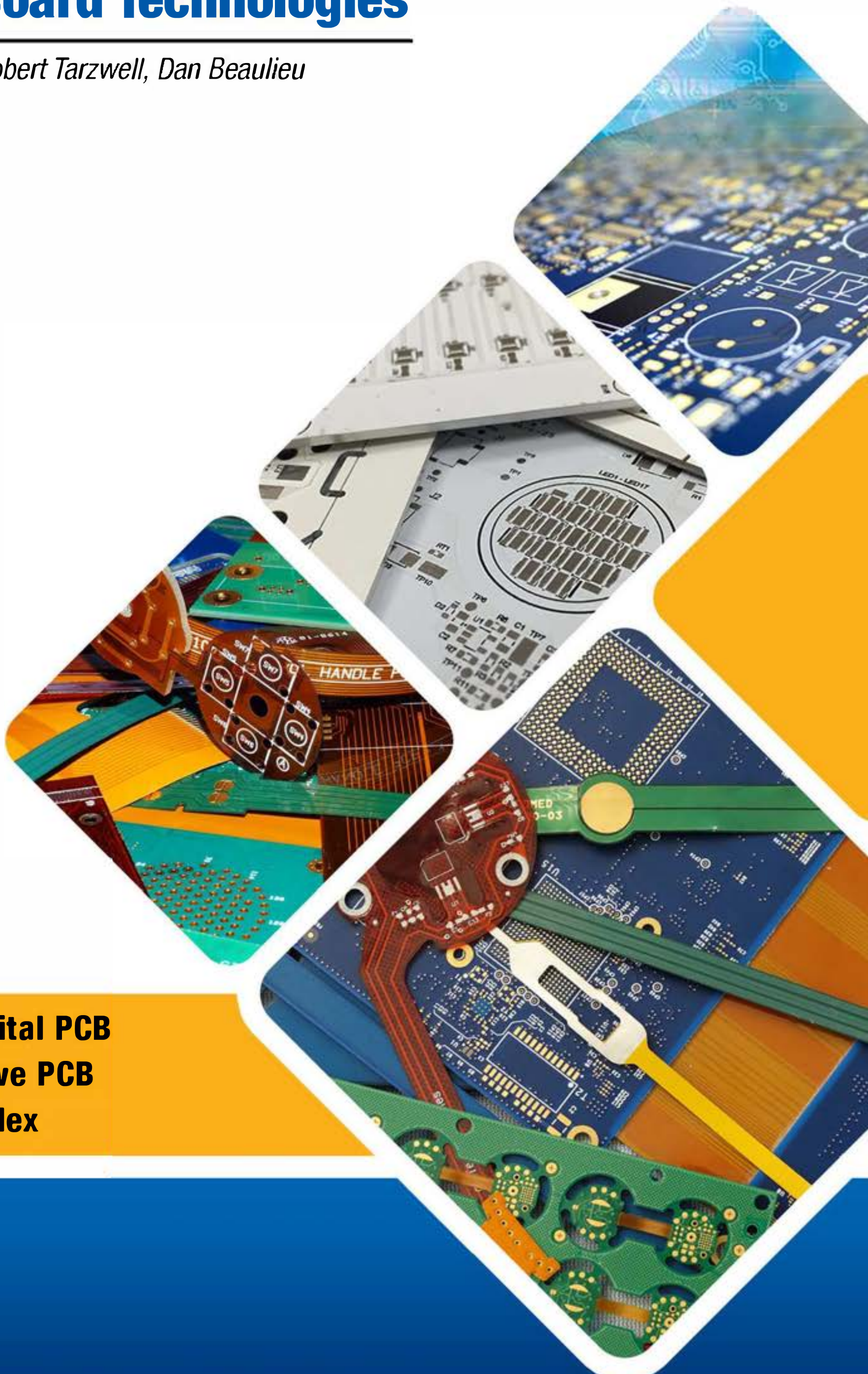
Fundamentals of Printed Circuit Board Technologies

Anaya Vardya, Robert Tarzwell, Dan Beaulieu



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Meet the Authors

Anaya Vardya has over 35 years in the electronics manufacturing business and is currently the President & CEO of American Standard Circuits, Inc. He was previously COO of Canadian based Coretec Inc. and Sr. VP Operations of Merix (both now part of TTM). He was also the Corporate Development Manager at Continental Circuits. Prior to that he had a variety of management and non-management positions at IBM Endicott and IBM Austin. He has a Masters in Chemical Engineering from the University of Cincinnati and a Bachelors of Technology from the Indian Institute of Technology.

Robert Tarzwell started in printed circuit boards in 1964. He started a printed circuit, quick turn, manufacturing company specialized in high technology research and development to manufacture many different types of high technology circuit boards, very fine lines below 40 um and very heavy copper up to 40 oz's. Since selling his company in 2000, Robert worked as a consultant and has written 42 books on printed circuits and hundreds of articles.

Dan Beaulieu, strategist, marketing guru, tactician, sales coach, trusted advisor, writer and networking expert has been in the business of strategic business consulting for over 20 years. During that time, he's worked with over 200 companies helping them increase their market presence, branding and most importantly sales. His column, *It's Only Common Sense*, has appeared on I Connect007.com for nearly 700 consecutive Mondays. He can be contacted at 207-649-0879 or danbbeaulieu@aol.com.

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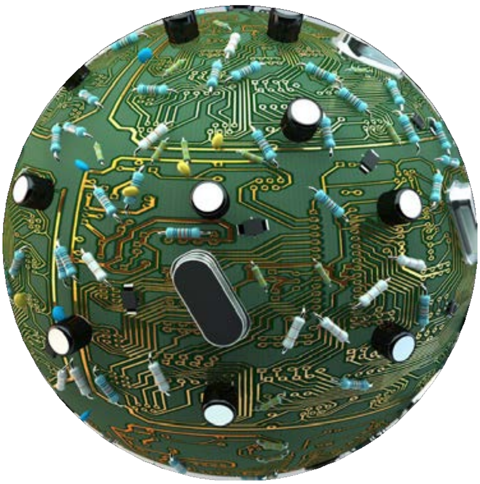
Introduction

Welcome to this special American Standard Circuits book on the **Fundamentals of Printed Circuit Board Technologies.**

American Standard Circuits business philosophy has always focused on the needs of our customers and theirs. To provide a complete understanding of PCB technology and process considerations used in the market, ASC thought it would be beneficial to partner with the authors of The PCB 101 Handbook, Robert Tarzwell and Dan Beaulieu, and together we have written a more comprehensive version of their original book.

Our vision was to provide our customers with an extensive understanding of design and printed circuit board fabrication techniques. The processes from single sided, double-sided construction, to the higher technologies such as flex, rigid-flex, and metal-backed printed circuit boards. Further, we wanted to provide a book that would demonstrate design considerations from standard product to advanced technology.



This book was designed to be a handy reference for someone needing a quick overview of the processes, or the definition of technical terms. We have comprehensive descriptions of various technologies, complete with illustrations; as well as a comprehensive glossary of common industry terms.

Finally, we wanted to contribute value add to the novice or industry expert. Our primary objective of this book is to educate, however, we would be pleased to support our customers or theirs on a more comprehensive level. This book is also meant to be helpful for young people just entering our profession, private equity firms looking to invest in our business, designers and engineers who need to have a thorough understanding of our technology and to our own employees, both present and future, who will find this book a valuable training tool.

I would like to thank Gordhan Patel, our Chairman and Founder, for inspiring us to write this book.

And one more thing: we want this book to be a living document, one to which you can contribute. Your feedback will be a valuable consideration for our future editions. In the months to come, we will be sending you an updated tech bulletin, based on this book, which will allow you to take part on a more personal basis in the development of future editions. Because after all, this book is for you.

Respectfully
Anaya Vardya
President and CEO
American Standard Circuits

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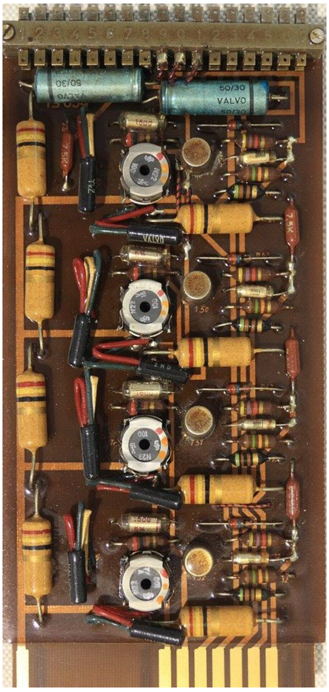
Chapter 1

History of the PCB

Although there are stories about earlier copper strips screwed to wood, it is known that printed circuits started in early 1915. As radio communications started to proliferate, the amateurs who built radios used cellulite and ivory to make resistors. They drilled holes in the material, inserted copper rivets and drew resistors with Indian carbon ink, which when cured made an excellent resistor.

Most historians give Paul Eisler of the United Kingdom, circa 1943, the first patented method of etching the conductive pattern, or circuits, on a layer of copper foil bonded to a glass-reinforced, non-conductive Bakelite base. Widespread use of Eisler's technique did not come until the 1950s, when the transistor was first introduced for commercial use. The portable, battery-operated radio and 45 record player were the most widely spread products made with the new PCB.

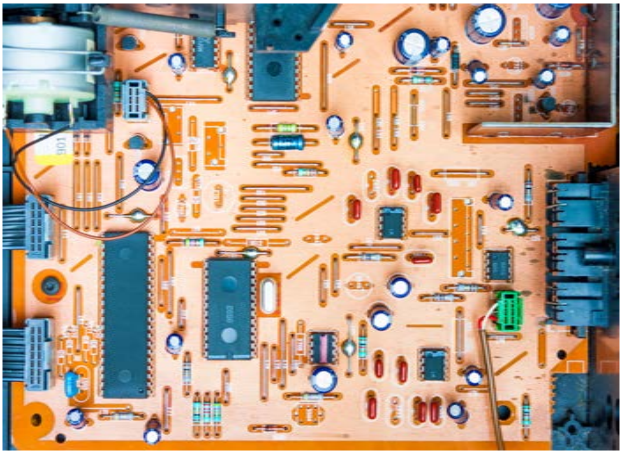


During the 1940s and wartime, Bakelite strips were fitted with eyelets and wires with components soldered on to make a rudimentary circuit board. By 1945, a real etched circuit was made for aircraft radios. Early in the 1950s, copper was laminated onto materials and etched to form a crude circuit, which was used in military radios. By 1964, commercial PCB production was in full force. The industry was producing double-sided through hole printed circuit boards on fiberglass laminate.

In the early 1960s, transistors, “one of the world’s top ten most important inventions” were now becoming integrated into all electronics. The older tube electronics were too hot and heavy for a PCB. The transistor allowed engineers to miniaturize the designs and take advantage of the properties of a PCB. Circa 1968, the first multilayers were manufactured. To supplement this important invention, the industry now had crude NC drills, new green solder mask and less polluting plating copper solutions. In the early 1980s, computers and small photo plotters allowed for electronic creation of the PCB design in Gerber. The Gerber file was used to generate photo plots to image the circuit traces. Before using computerized Gerber data, the industry first used red ruby litho film.

A rotary blade was used to trace and cut out the 1:1 hand-drawn negative PCB designs. The cut ruby litho film was applied to screen frame with silk mesh stretched tight forming the screen pattern which enabled the image of the copper pattern to be screened in etch resist ink on the copper surface. The next design invention was Bradley self-sticking tape in various widths which, along with dots for pads, were used to lay out 2:1 or 5:1 designs. The paper tape designs were converted by a large camera into films to make silk screen patterns.

Electronic multi-head drilling machines were introduced in the early 1970s. Although they ran on paper tape, punched with an 8-bit pattern, it was a big improvement over hand-drilled or stylus-drilled boards. Additionally, during the 1970s, new dry film lamination and exposure systems eliminated screen printing as the main imaging system. Also conveyorized processing was developed, eliminating cumbersome handling operations leading to higher quality, higher throughput.



During the 1980s and 1990s, inventions such as flying probe electrical testers, laser drilling, laser photo plotting, and multilayer alignment systems all improved PCB technology and allowed increased production. In the 2000s, the main invention was laser direct imaging. This removed the cost of photo plotting and manual exposure alignment of layers on the PCB.

Therefore, ASC continues their investment in new technology including direct imaging, drilling equipment that can achieve fine holes and automatic legend equipment. Innovators, equipment, software, and certifications are what define 21st century PCB fabricators.

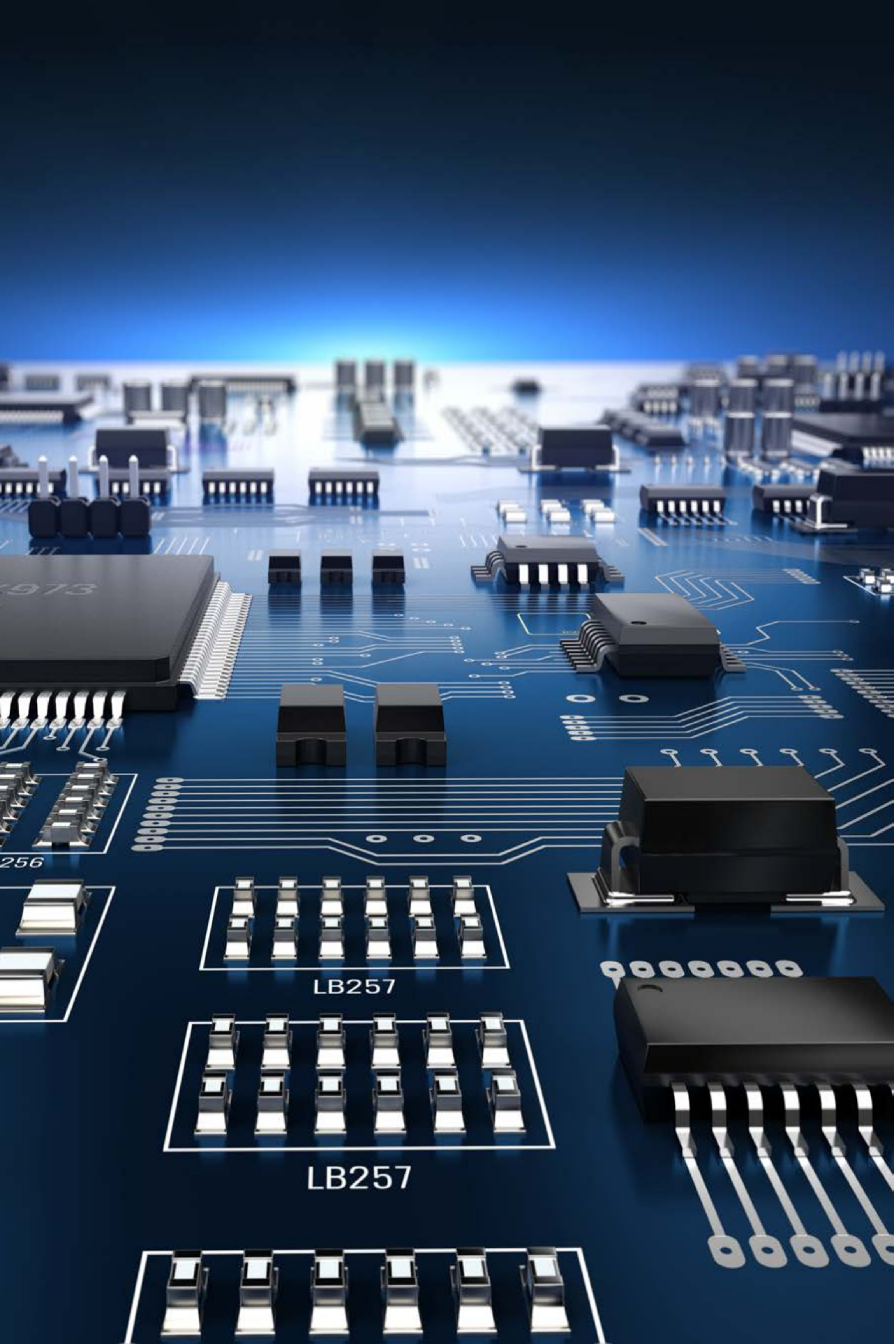
Chapter 2

PCB Industry Today

Today, worldwide annual PCB sales are over $70 billion, with most of that being built in Asia. China accounts for 50% of the global PCB production, Taiwan builds 15%, while less than 10% are built in North America and Europe. Today, there are approximately 2,700 board shops throughout the world, with about 400 of those being in North America and Europe. The rest are scattered throughout the world, with the bulk of the companies in China, which boasts about 1,000 circuit board fabricators.

Fortunately, North America still leads the way when it comes to new product development and innovation. Our electronics companies still use local PCB fabricators when developing their new products, a trend that is likely to continue into the foreseeable future. In fact, there are some strong indications that printed circuit board production is coming back to the United States. Certainly, the days of the mega-volume shops are over. We no longer have the infrastructure to handle large volumes, but with the recent trend to on-shoring, the rise of contract manufacturing in Mexico and Canada bodes well for our local industry. The growing movement in economic nationalism is also causing large electronic companies to start up fabrication facilities in North America.

So, it is with a certain degree of cautious optimism that we look toward the future of the PCB industry. The trend in North America is toward smaller, better-established and profitable companies focused more on the quick-turn prototype and technology markets. North American companies still lead the world in marketing and innovation. There is still a consistently growing demand for printed circuit boards as exemplified by the development of and the demand for new and innovative products, not only for commercial markets like medical electronics, but also domestic and retail markets like computers, smart phones, smart appliances and cars. Significant inroads into LED lighting create a need for more thermal management products. There is also a growing demand for more sophisticated military defense products as we continually change the way countries defend themselves, switching from manned aircraft to drones and robotics. ITAR is now specifying all military boards be built in the USA.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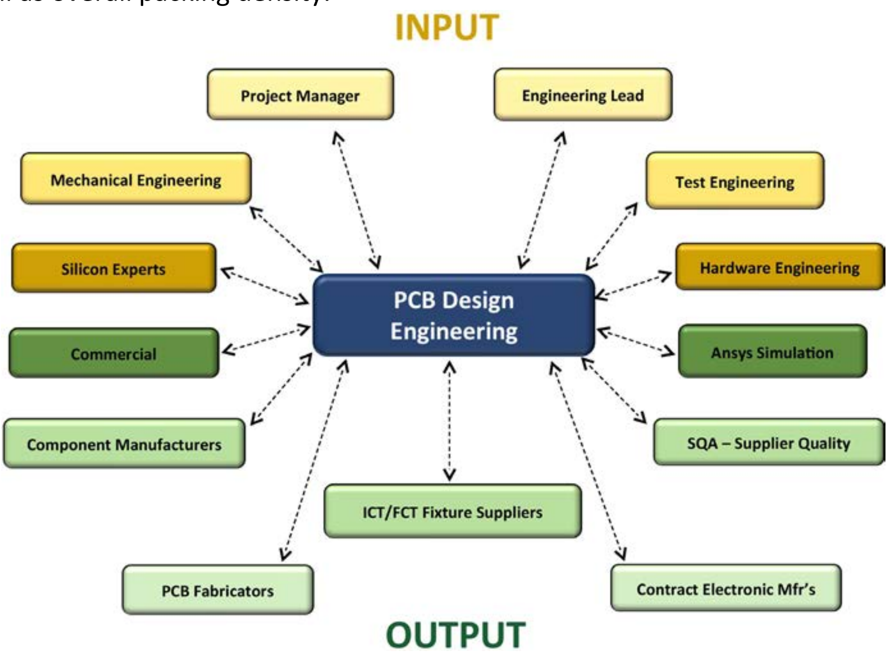
Chapter 3

Designing a PCB

The PCB design starts with the designer creating an electronic circuit, which is then tested on a fixture. After the circuit is debugged, the components are selected, and a circuit layout is generated on CAD software. The designer will work and modify the CAD data until all the components are properly placed. Today's advanced CAD design software will determine the best signal trace layouts and interactively route the traces and interconnecting vias. This feature avoids many hours that would have been spent in laying out 16 layers and ensures all the traces fit. The design will include overall size, power requirements and control component placement. The CAD designer will also take into consideration electrical and thermal outputs, mechanical constraints, and test point allocation, as well as overall packing density.



PCB Designer: Nucleus for all PCB and PCBA Activities

After the main design is routed, the net lists are generated for electrical testing, drill files for the CNC drilling units and solder mask and nomenclature files. The designer will order a proto-board which will be assembled and tested for function of the circuit and evaluation of its electrical and thermal performance. If the prototype circuit board is successful, he will then order production printed circuit boards. More advanced circuits may use HDI or high layer multilayer designs. The designer would need to consider advanced electrical properties such as controlled impedance and crosstalk.

It is important for the PCB designer to work closely with the PCB fabricator during the PCB design process on controlled PCBs. It is beneficial to select the fabricator first and then work with them on a stackup prior to completing the design. The calculated stackup may be different from one fabricator to another due to different materials and processes.

Any PCB circuit design, whether simple or complex, will provide the board fabricator with a great deal of manufacturing information needed to properly manufacture the desired circuit board. The data required are the board dimensions, hole sizes, hole locations, copper thickness, silk screening data, solder mask layout, each layer trace design and overall mechanical size. Additional data is required to satisfy all areas of the manufacturing facility. The data format used by most PCB designers is Gerber RS274x. The electronic data system describes the locations of holes and traces in blocks of X-Y coordinate points. This data (called CAD data) can be used to generate photographic images of the PCB and to produce other manufacturing tooling subsystems such as drilling, scoring and final routing. ODB++ is another widely used format that continues to gain popularity.

Some high frequency RF circuits and very high density, chip packaging designs use AutoCAD as the drawing format. This allows for more advanced features and compound hyperbolic curve drawings; Gerber is unable to handle due to its more rigid X-Y point to point data system.

The dimensions of the copper conductors of the printed circuit board are related to the amount of current the conductor must carry. Each trace consists of a flat, narrow part of the copper foil that remains after etching. Signal traces are usually narrower than power or ground traces because their current carrying requirements are usually much less. In a multilayer board, one entire layer may be mostly solid copper to act as a ground plane for shielding and power return. For printed circuit boards that contain microwave circuits, transmission lines can be laid out in the form of stripline and microstrip with carefully controlled dimensions to esure consistent impedance. For more information refer to Chapters 10 & 14. In radio frequency circuits, the inductance and capacitance of the printed circuit board power and ground layers can be used as an electronic passive part of the circuit design, reducing the need for additional discrete components.

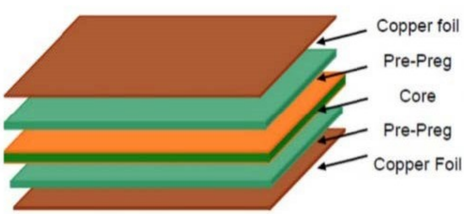
The history of the design of circuit board manufacturing has progressed from red lithograph, hand cut, 1:1 sized, silk screened, very crude circuits to today's laser-imaged, high layer count designs of very complicated art. We progressed through the 1:1 hand cut image stage to 3:1 times up hand-taped black features on clear films, which were photographically reduced on film. We progressed to CAD generated photo-plotted directly to the operational film and then to direct write with a laser.

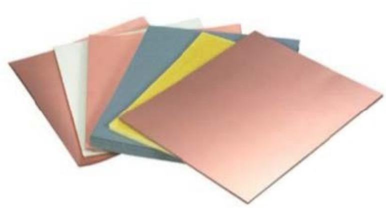
By 1990, capable, quality-oriented PCB shops were generating their own photo plots with the aid of CAM software. By 2005, many manufacturing facilities had begun to eliminate photo tools, transmitting CAD data via internal networks to laser direct imagers and ink jet identification marking printers. LDI (Laser Direct Imaging) creates a higher resolution image in reduced time with lower operational cost.

All PCB front-end operations today utilize advanced CAM software to computerize manufacturing details such as work orders, panelization, coupon generation, tracking and impedance control. As your design becomes more advanced from standard to leading edge technology, the price of your design will generally increase. To minimize these costs, properly engineered products, material selection and choice of suppliers is critical.

Materials
PCBs are constructed from three basic material types; copper foil, prepreg and cores.

- Copper foil: Sheets of copper foil are incorporated into the outer layer of the PCB placing it on the prepreg to create the outer layers.
- Prepreg: This is most commonly semi-cured (B-stage) glass-epoxy material. There is no copper attached to this material. This is an insulating layer.
- Core: This is most commonly fully cured (C-stage) glass-epoxy material with copper laminated to both sides. This is used for internal layers. A core is constructed from either of one sheet of prepreg (single-ply) or two or more sheets of prepreg and two layers of copper foil.

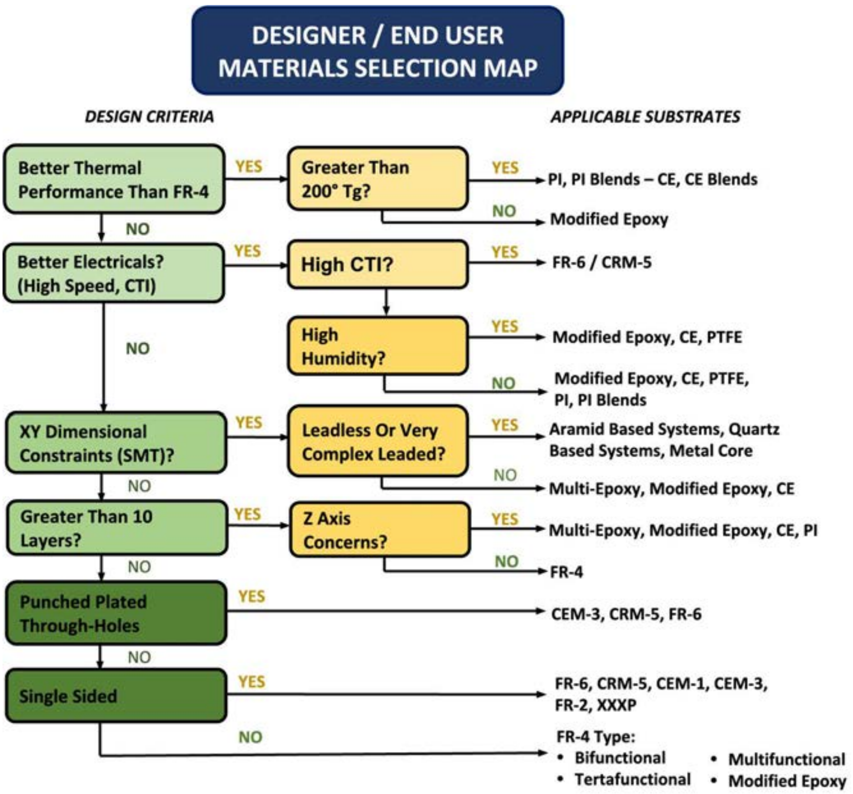




PCB layers are typically made of thin copper foil laminated to insulating layers. The dielectric spacing in multilayers is the epoxy resin prepreg used to glue the cores together. Quite a few different laminates can be chosen to provide different insulating values, depending on the requirements of the circuit.

While most PCBs are manufactured using FR-4 laminates, there are a large variety of laminate materials. Some of the more common laminate materials that one hears about are:

FR-2 (Phenolic cotton paper), FR-3 (Cotton paper and epoxy), FR-4 (Woven glass and epoxy), FR-5 (Woven glass and epoxy), FR-6 (Matte glass and polyester), G-10 (Woven glass and epoxy), CEM-1 (Cotton paper and epoxy), CEM-2 (Cotton paper and epoxy), CEM-3 (Woven glass and epoxy), CEM-4 (Woven glass and epoxy), CEM-5 (Woven glass and polyester), Teflon ® (High frequency laminate lower loss / higher Tg materials), High Tg epoxy as well as polyimide and a variety of low loss laminates. A material selection flowchart per IPC 2222A Sectional Design Standard for Rigid Organic Printed Boards follows:

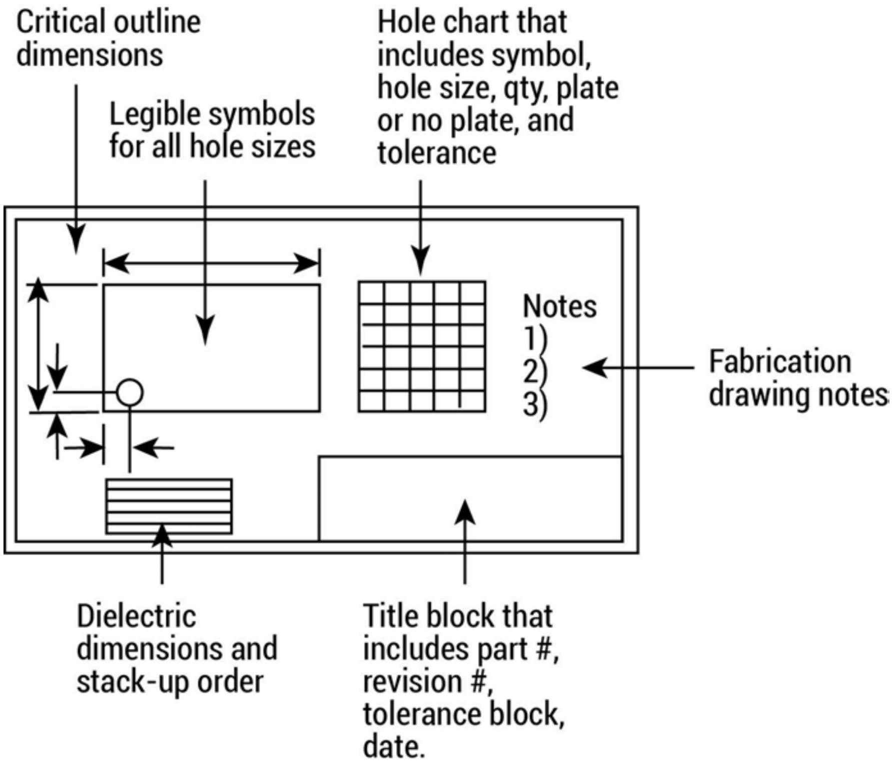


As mentioned before, the most prominent laminate is FR4. There is a large selection of higher functionality FR4. It is also available as epoxy, woven and unwoven, as well as high temperature and lead-free versions. Some FR4 is designed for higher frequencies and quick rise times.

Thermal expansion is an important consideration, especially with BGA and naked die technologies. Non-woven Kevlar fiber G85 offers the best dimensional stability but suffers from lack of availability, high cost and difficult processing parameters.

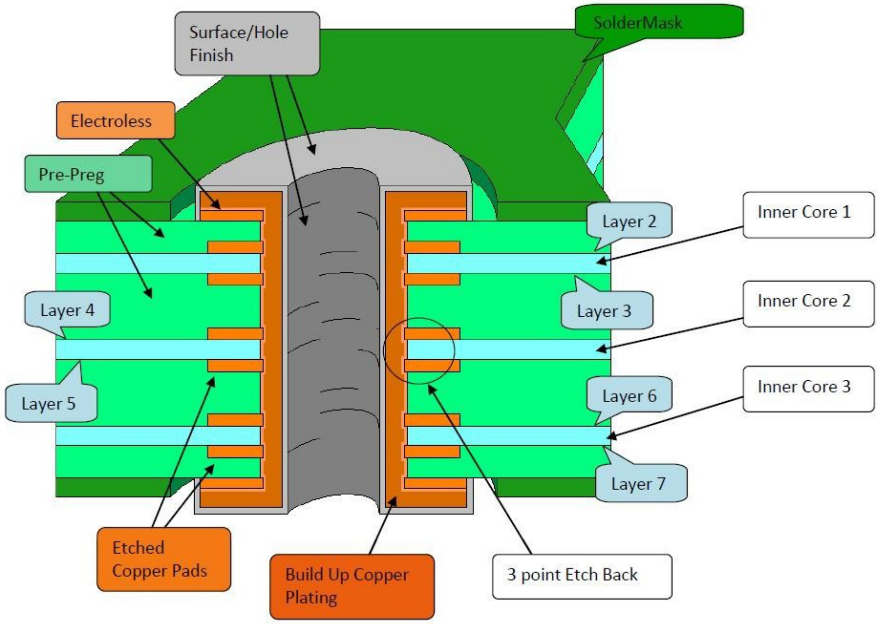
Manufacturing Information

Gerber designs files, one for each layer, solder mask layout, drill file, router file, nomenclature layout, cross-sectional build up data, i.e. layup drawing, material specifications including copper thicknesses, plating thickness, solder mask type and color any final fab information such as router slots, cut outs, bevels, scoring, final finish or any special feature and specification notes. The designer also needs to furnish any UL and other quality specification requirements. A list of sample industry specifications can be found in Chapter 18. Additional data such as electrical testing, reliability testing and any controlled impedance testing requirement should be well documented. Sample fabrication drawing below:



Power Planes

Not all PCB layers are used for signal wiring. Most PCBs utilize some layers for use as power planes. As their name implies, planes are nearly continuous sheets of copper. A plane is used to carry power to many or all components on the PCB with low inductance and resistance and reduce power induced noise.



Cross Section of a Typical 8-layer PCB

These electrical properties become critical in fast and sensitive circuitry. Planes are continuous except for via clearance holes. Clearance holes are necessary to prevent vias shorting their signals to the power planes. This would normally happen because vias are drilled through all PCB layers (or some layers with blind and buried vias). The solution etches away a circle of copper in each plane where each via hole is drilled. There is no electrical connection between the via and the plane. Most PCBs have several planes and assign each plane to carry a specific power rail.

Boards may have 5-volt v++ and 3.3 v+ volt power supplies plus ground and signal return. The PCB may have up to six different planes; most have two grounds. It is possible to split a plane into multiple areas for multiple power rails. Whether or not this split is possible depends upon the circuit's electrical designs. A split plane is constructed by etching copper open areas in a continuous plane of copper.

Chapter 4

Getting Accurate PCB Quotes

PCB suppliers get many RFQ's. Unfortunately, often they struggle to give you an accurate quote. A lot of times PCB suppliers are left guessing at what your exact requirements are.

The quality and completeness of information varies widely. Sometimes we are sent a complete data package, on other occasions we get partial drawings or even verbal descriptions. Since PCB fabrication is a build-to-print exercise, in-complete information usually leads to quotations taking a lot longer and a frustrating experience for both parties. Some people working on the quotes may make several assumptions and others will ask a lot of questions.

The person that makes a lot of assumptions is trying to get the quote off their desk as quickly as possible. Unfortunately, the customer may get a number of these quotes and different people might have made different assumptions, so the customer is left with quotations that are apples and oranges. They really cannot compare.

The person that ends up asking a lot of questions is often told, "I had a few other companies bid already. Not sure why you need to ask so many questions."

The necessary details just to get a PCB quote may appear very time-consuming, but the more information you can provide, the more accurate the quote. A little time spent initially preparing complete information will result in a less frustrating experience for all and enable you to receive quotes quickly from multiple fabricators with less variation caused by differing assumptions about missing requirements. We understand that sometimes in the design stage customers are looking for ballpark information. This can be provided if everyone understands that this is purely budgetary in nature.

It's not too difficult to provide suppliers with adequate information to ensure you receive prompt and accurate quotes.

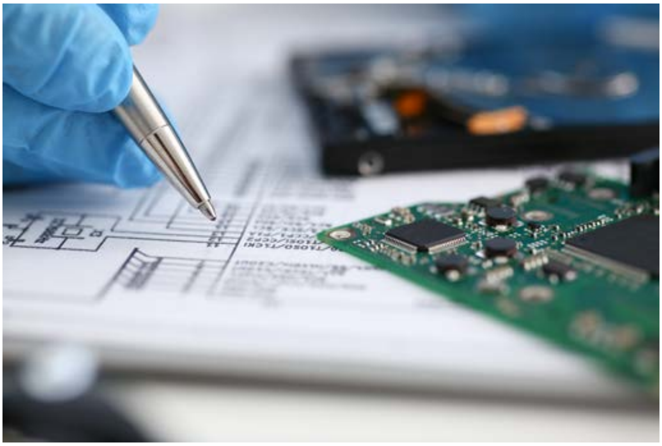
In Appendix A we have a detailed checklist of all the data needed to obtain an accurate quote. As a quick summary:

- Gerber files for ALL layers, including circuitry, solder mask, silkscreen legend, solder paste, and an accurate outline showing all mechanical features such as slots, etc. on a single layer.

- Fabrication drawing, including laminate information, hole sizes and locations, surface finish, plating requirements, solder mask color, silkscreen color, quality requirements.
- If the PCB needs to be supplied in an array or panel, a panel drawing or a description of how many PCBs on the array, width of array rails and depanelization method (routed, scored, or both).
- If required, impedance requirements, material stack-up, and any special testing or qualification requirements that are unusual. If one doesn't have a fabrication drawing, a README or similar document listing the requirements works as well.

Prototype Quotes

There is one other option for customers that design a lot of PCBs that are standard technology and time is of the essence. ASC works with the customer to understand their needs and then designs a pricing matrix that we share with our customer. Typically, this covers 1-5 manufacturing panels at various turn times for various layer counts. Usually they come with adders for some variations that drive extra cost. The advantage of this is the customer has price predictability and the confidence to send us the data and get the job started first, get ASC to give the quote to them (which is based on the agreed price matrix) and then cut the PO. The prototype job is not held up for the RFQ / PO process that can sometime eat up a few hours and can ultimately delay a shipment by a day.



Conclusion

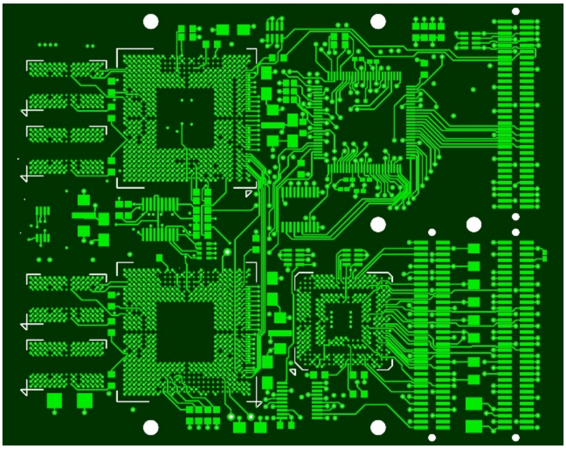
Appendix A has a checklist for both accurate quotes and setting up your part for manufacturing. Providing a complete data package will result in receiving accurate quotes. This will allow you to make apples to apple comparisons of competing quotes, thus making informed decisions about awarding your purchase order to the ideal supplier while not compromising your end customer.

Chapter 5

Front End Engineering

The PCB fabricator today will usually receive the electronic data via the internet. Once a PO is received, the customer service representative (CSR) will ensure that all the files are available, ensure that the appropriate material is available / ordered, enter the PO in the ERP system. The CSR will issue a sales order in the system and acknowledge the customer's PO. The Front-End Engineering department then takes over the process.

The first step in the tooling cycle is a DRC/DFM (Design for Manufacturability) check. The CAM Engineer will use the CAM Software to check the design for possible shorts and opens, tracks too close or drill/pad violations, impedance violations along with several other design features to make sure it is manufacturable. Check the drill sizes and overlay layers and ensure no drilled holes intersect lines or features. After all the manufacturing checks and edits have been completed including date codes, logos, UL or other specific markings, the single up version is panelized. The CAM software "steps and repeats" the PCB image and adds features to the panel such as copper thieving, and venting, any unique features used for in process quality checks and all the required coupons. Every file will have it's own separate layer besides the PCB layers. This includes solder mask, solder paste, drill and rout files, and legends.



The front-end engineer will decide several variables such as:

- The number of boards up in the panel or layout for array setup. They will typically interact with the customer to ensure that the array meets their requirements.
- Panel size: The most common are 18" x 24", 12" x 18", while larger orders or bigger boards may require other panel sizes. While shops in the US/Europe tend to have standard panel sizes, the practice in Asia is more custom panel sizes for parts based on maximizing material utilization

- The correct panel borders based on layers and operations, solid outer borders to allow the copper plating rack to connect to the panel or open dot pattern for inner layer prepreg flow.
- Material layup: Often, the customer selects the individual layer materials. However, if the electrical specifications are not critical, these decisions are left to the fabricator.
- Drilled hole sizes: Since subsequent plating operations deposit copper in the holes, the holes must be drilled larger than the finished size, typically 3 to 4 mils.
- Tooling holes or target locations: Most fabricators use the Multiline Technology tooling systems that define the locations of tooling features in the multilayer presses and drilling machines.
- Coupons: The appropriate coupons that are required on the panel for the required quality testing. Depending on the complexity of coupon requirements the number of PCBs that can be laid out on a manufacturing panel could be impacted.

The CAM engineer will look at the base copper thickness used on each layer. The data is modified based on the base copper weight to allow for etch compensation. Essentially the circuit features are grown to a predictable size that accommodates the loss of copper that will occur during the etching process. The heavier the copper weight the more the data must be enhanced to allow for etching.

All the information process flow and laminate information are included in a work order, either written or computerized, that follows the order through the shop.

Multilayer Lay-Ups

The front-end engineer will provide the shop with a traveler providing all the steps in the order required to manufacture the design. This would include a stack-up for multilayers showing the type and required sheets of prepreg or bonding materials to meet the drawing and electrical specifications.

Most traveler software has a feature that depicts the stack up graphically for clarity to assist the lamination department when processed.

There exists a large variety of copper thickness, laminate thickness and prepreg thickness as well different glass weave available.

The final combination must be carefully defined and engineered before starting fabrication. Multilayer boards are defined with more data as to the construction, specifying the buildup, the different layers, thickness, materials used in each core and the prepreg between each core. The information will specify the copper weights and copper type e.g. RA (rolled annealed) in flex/rigid applications as well as overall build up thickness and any impedance requirements.

Prepreg is available in a large variety of glass weaves and resin compositions. Varying these parameters has a direct effect on the lamination process and the final electrical properties as well as the final thickness, so proper selection of the material is critical.

The designer may specifically engineer and design the buildup to control electrical properties such as dielectric voltage strength and impedance. In many instances, the selection of the prepreg and the core is left up to the fabricator, if only the finished thickness is specified the front-end engineer will use a standard 1 core design for a 4-layer board or 2 cores for a 6-layer. If not specified as lead free, the PCB shop may use lower temperature laminate.

Please ensure that your design shows all features. You may know every detail of your multilayer design, but the shop does not. The only place they can get correct information is your data, prints and READ ME files. ASC is willing to consult with you or your customer should you have any concerns or issues with your customer design.

Drill and Route Data

There is a wide variety of different CNC drill and rout machines available and it is not unusual for a shop to have more than one type. Most CAM software have outputs for different types of machine manufacturers or customer scripts can be written for the output. There may be multiple different drill files if the order contains blind and buried vias, non-plated holes, internal cutouts or complicated final routing. Included in the data are the machine commands to change drill bits, spindle feed (RPM) and control the in feed and exit rate of the spindles. The drilling and routing machines transfer the electronic information to the drilling area via internal network.

Route data, generated in the same way, is the information that instructs the CNC router as to the finished board dimensions, speed of travel and router RPM as well as head up/down and foot clamping of the board before the end of a route line.

Slots

When designing with plated slots, the same theory applies as drilling. The pad must have a larger initial slot, which is then plated inward to the desired finial dimensions. There are minimum sizes of slots that can be produced; check with your shop for their specifications. Milling thick laminates with small bits is difficult, resulting in excessive broken milling bits, increasing costs. The suggested minimum width of a plated slot without a cost driver is .030 inch.

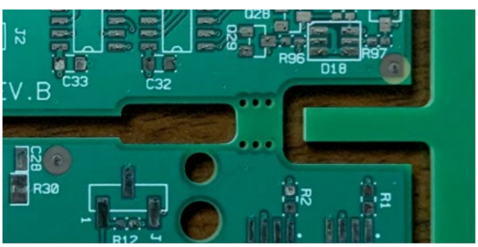
For internal gold fingers, the bevels can be beveled on a router machine. The angled cutter removes just a small amount at the tip of the gold fingers, the board is turned over and run through to finish the bevel. For gold fingers that are on the PCB edge these are usually beveled on a machine designed for this. Non-plated slots will be included in the final router file and machined into the finished panel. Then, the individual board will be routed out.

Scoring

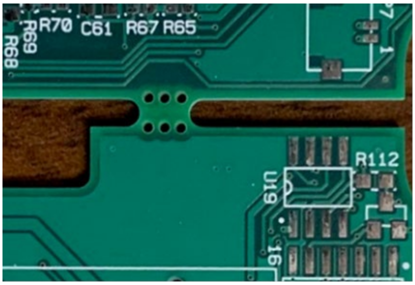
Scoring is a technique where a fine triangle cut is placed in both sides of the panel to a depth that will allow for assembly of the larger panel then break out of each individual circuit. The cut will be adjusted to leave about 1/3 of the material in the center of the panel Any thicker and it may be difficult to break. Any thinner and the panel will separate early during assembly handling. Scoring is done in straight lines in both X and Y axis to enable the cutters to run right across the surface. This is a restrictive way to panelize the board and is not desired in many situations. One example being in the case of overhanging components.

Route and Breakaway Tab

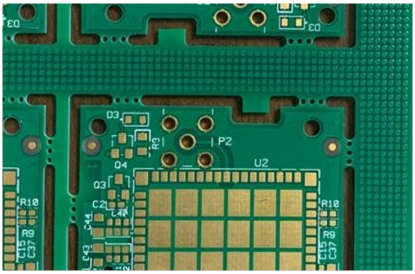
This is an alternative method to break out each individual circuit from a larger panel after component assembly. A combination of routing and drilling is used. There are a few different options illustrated.



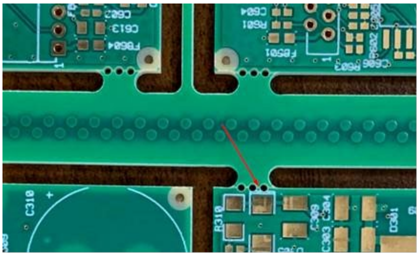
Double row of Mouse Bites designed to follow various width route lines



Double row of Mouse Bites designed for 0.093" route following route lines



Single row of mouse bites designed when finished edge tolerance is not an issue



Single row of mouse bites designed with flush edge on PCB and no mouse bites in scrap area

Solder Mask

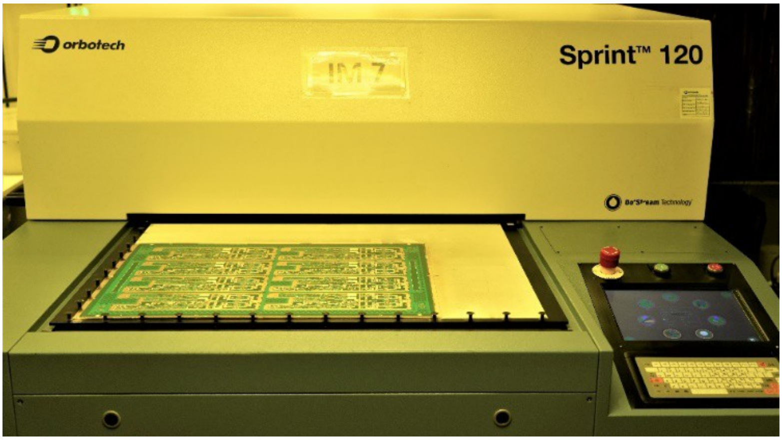
If solder mask clearance in the data is not provided, the CAM engineer will need to add clearance to allow for any misregistration. The minimum clearance would be .002". The board is coated with a solder mask that is typically green in color and is specified by the designer. Many other colors are normally available such as blues, reds, yellows, whites and black; the correct color is recorded on the shop traveler.

The newer ink jet solder mask units are of higher resolution and can image closer to the pads, using a thermal cure or UV cure ink. They, therefore, require only a final cure and can skip the exposure and develop cycle.

Spray solder mask machines use a series of spray nozzles and coat the board with an even coating of photo imageable ink. The ink is then oven tack cured and exposed with an image developed to remove any ink that is not wanted, and final oven cured.

Silk Screening

The minimum line thickness that a silkscreen can print is in the 6 to 9 mil area. If you go this thin, the small letters and numbers may be hard to read. You are advised to silk screen nomenclature on any single-sided board to ensure that they are made right side up. It is easy to make a single-sided board inside out. Correct reading letters on the board in copper and white marking prevent this. New ink jet marking machines can spray a very fine line--so fine, in fact, that it’s hard to read.



Inkjet white nomenclature machine

The CAM engineer will check the silk screen nomenclature to ensure there is no ink on pads. He will clip back any lettering or symbols to clear the open pads for soldering by 5 or more mil or the solder will not flow properly. He will also check that the letters are right reading and not mirrored. The CAM engineer will clip the artwork and send the file to the ink jet printer or the photo plotter to generate a film to make the screen. A lot of PCB fabricators today are using inkjet printers to apply the markings, or identification marking. It saves making photo tools and silkscreens, both are expensive and not environmentally friendly. This is also advantageous because one can serialize the PCB, if required, and ensure that coupons are serialized relative to the panels for unique identification.

Final Finishes

The shop floor traveler will include the type of surface finish required. Until the mid-1980s, the predominant conductor finish was electroplated and reflowed tin/lead (solder). The use of solder mask started in the ‘60s and provides the isolation needed to prevent solder used in the assembly process from shorting between traces. Solder resist is a tough photoimageable, epoxy-based, thermosetting resin applied by screening, spray/roller coating or in rare cases inkjet machines.

It covers and insulates all the traces and pads. Any pad opening desired is imaged and developed away to allow solder to contact the finished circuit and electrically connect the components. Solder mask over bare copper (SMOBC) is the most commonly used solder mask type. During the front-end engineering evaluation, the engineer would look at the final finish and the solder mask to ensure compatibility.

Inspection and Test Data

Before the 1990s, inspection of PCBs for shorts and opens was often performed visually, under magnification by QA personnel. Visual inspection was wrought with problems; operator fatigue, missed faults and low outputs. As the line width and the spaces decreased, it became necessary to use optics and computers to find breaks or shorts in the finer lines. This technology is automatic optical inspection (AOI).

AOI has been fully integrated by all board shops since the 1990s. Originally, the operators would program the AOI memory with a known good board (golden board) as the reference. The machine would compare the memory of the golden board to the image that it just scanned and look for any mismatch. The machine would identify the location to assist the operator in detecting defects. This provides the opportunity to fix repairable defects. Today’s AOI machines feature more computing power and better optics and use the original Gerber image data and compare the manufactured board to the original data with higher speed and improved fault-finding abilities. This method eliminates the need to rely on a golden board and significantly reduces the chances of producing costly, incorrect product.

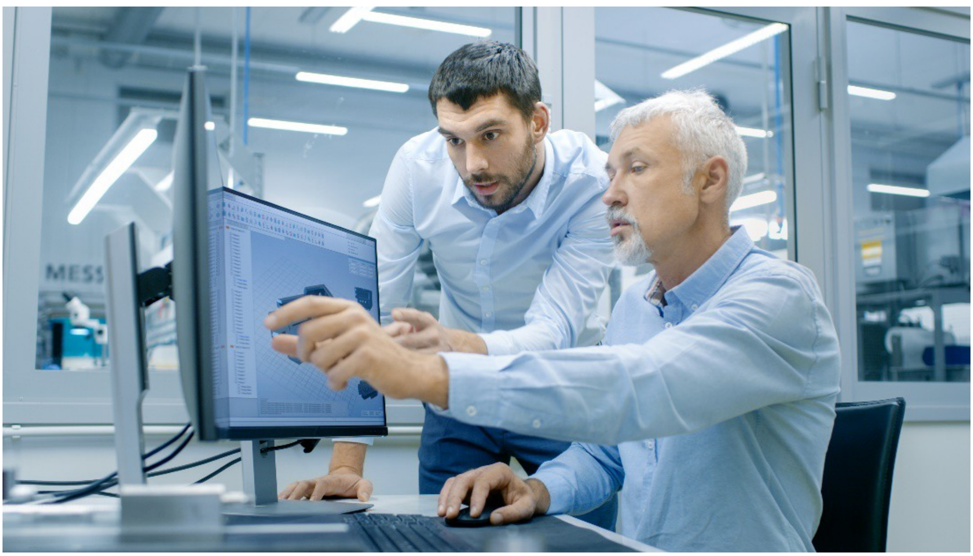
The CAM engineer will create an AOI data file and send it directly to the AOI machine. Some AOI and verifier systems today feature a built-in UV laser that will automatically fix shorts and copper spots left on a panel by laser ablating them.

Electrical test data is now automatically generated from the original CAD data. The generated test data includes drill X-Y data for test fixture (“bed of nails”) and net lists that identify each individual test string.

Flying probes electrical testing has gained popularity in the last decade, with increased speed and operational abilities from newer higher power computers and higher resolution optics. A flying probe tester uses from 4 to 16 separate computer controlled little automated spider like arms with electrical test points. The probes contact the two ends of the line and measure resistance while the others contact circuits close by the line to check for shorts. The engineer will decide which machine will test the boards, create a proper test file and send the data to that machine.

Engineering Questions (EQ) or Technical Questions (TQ) Process

Many times, the CAM engineer when working on the customer’s data will see questions or changes, they will need to make in the data to improve PCB manufacturability. Most fabricators will communicate this via an EQ form making suggestions and asking for the designer to approve changes. This form usually has screen shots of the suggested area of change. On complex designs this may happen a few times before the CAM engineer is able to finalize the data and release it to the manufacturing floor.



The more advanced your design, the more it will cost. As your design progresses up the chart from standard technology to bleeding edge, the price of your circuit board will increase.

Technology	Standard	Advanced	Leading Edge	Bleeding Edge
Min. component pitch (in)	0.016	0.015	0.012	0.010
Min. line width	0.005	0.003	0.002	0.001
Min. drill finished hole size (in)	0.008	0.006	0.004	0.003
Max. thickness (in)	0.150	0.200	0.250	0.300
Min. thickness (in)	0.005	0.003	0.002	0.001
Min. copper base thickness (in)	0.0012	0.0007	0.0004	0.0002
Max. copper thickness	4 oz.	6 oz.	10 oz.	20 oz.
Number of layers	10	14	20	>30
Tolerance plated holes (in)	+- 0.003	+- 0.002	+- 0.0015	+- 0.001
Tolerance routed edge	+- 0.005	+- 0.004	+- 0.0035	+- 0.003
Ratio thickness to drill	8:1	10:1	14:1	16:1
Trace to edge of board (in)	0.014	0.010	0.008	0.006
HDI technology	N/A	N/A	4-8 layers	10 + layers
Pad to drill allowance (in)	0.012	0.010	0.008	0.006
Min. solder mask web (in)	0.003	0.0025	0.002	0.002
Max. sized board (in)	16 X 22	19 x 22	22x22	22 x 28

Chapter 6

Manufacturing Single-Sided PCBs

There are hundreds of individual sequential operations in order to manufacture a PCB, with numerous methods and technologies involved. Although each fabricator may have a different process, they primarily perform the same end function. The individual differences in manufacturing processes are mainly due to different equipment, materials, and chemistries. This book looks at the typical manufacturing method but will include comments on some of the more popular variations.

Pre-Production Engineering

Before the manufacturing begins, the front-end engineer reviews all the information and data sent by the customer in electronic format. The mechanical drawings and specifications are included in the electronic data. The engineer will set up the manufacturing process and design the process to ensure proper flow while still producing the desired final board.

Manufacturing Methods

Most standard single-sided printed circuit boards are processed by starting with a kit up of precut FR4 copper clad single-sided laminate and drill back-up materials. The laminate is drilled, then deburred and cleaned to remove any small edge burrs and to remove dirt/dust in the hole left by the drill.

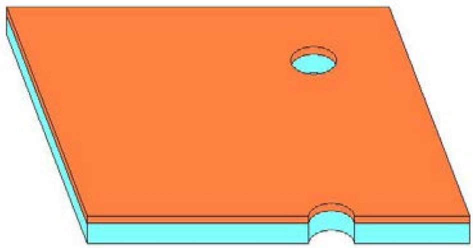
The cleaned panel is transported to imaging where a photoimageable dry film is applied and the desired image exposed, then developed, creating a negative image of the circuit. The panel is then etched using the dry film as an etch resist and dry film stripped. The panel will now have the desired copper circuit image. The drilled holes will be verified for the specified diameter and tolerance.

The circuit board will be inspected for opens and shorts on the AOI to ensure full compliance to the original design. If desired, the circuit board will be electrically tested. The single-sided board will be pumice scrubbed to create a clean outer copper surface for the solder mask and an LPI (Liquid Photoimageable) solder mask applied by silk screen or by inkjet printing.

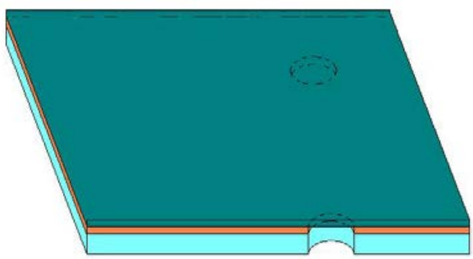
The solder mask is tack dried to prevent it from sticking to the photo tool and then exposed and developed. After developing, the solder mask is fully cured in an oven and sent to final finish; ENIG, immersion tin, silver or hot air solder application are the most popular. Before the final finish, the white identification marking is applied.

Process steps for manufacturing a single sided circuit board

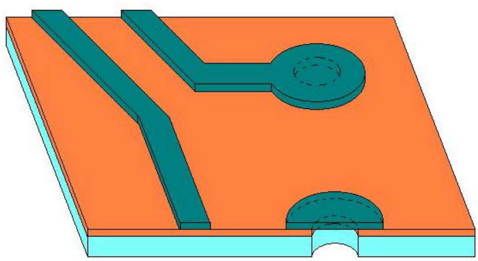
Copper clad laminate



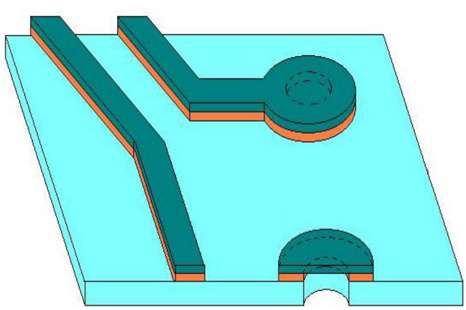
Holes drilled



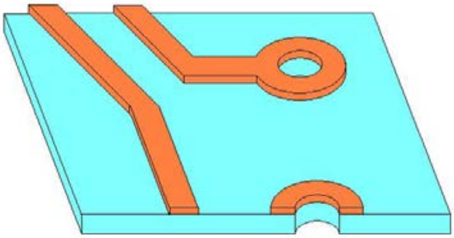
Dry film applied



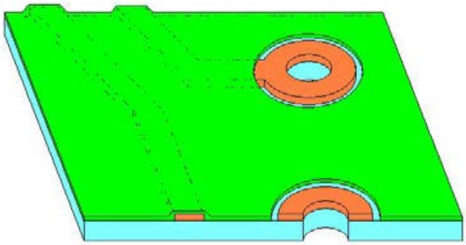
Dry film exposed and developed



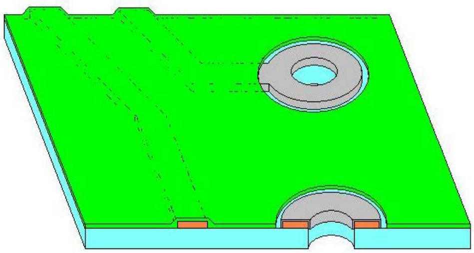
Copper etched off



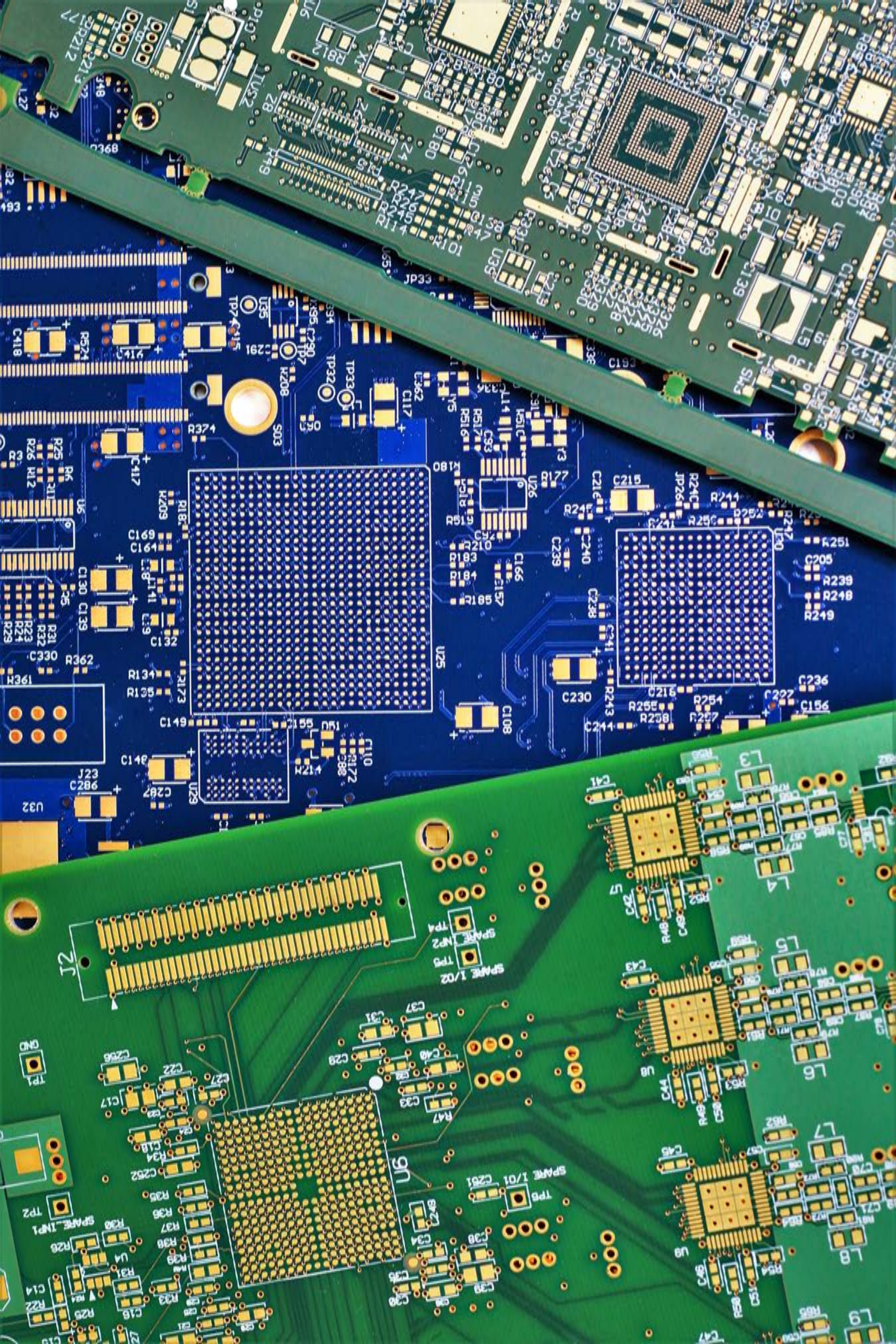
Dry film removed



Solder mask over bare copper (SMOBC)



Final finish applied



Chapter 7

Manufacturing Double-Sided PCBs

The following sequence describes the steps used to produce a double-sided circuit board with plated through-hole (PTH), solder mask over bare copper (SMOBC) with white component silkscreen. Although most North American printed circuits are multilayer boards, double-sided production technologies are the basis of all circuit board manufacturing technology.

Material Kit Up

Using the information on the traveler, the correct material is prepared with the number and size of the panels. In North America, most shops buy panels and entry and backer boards pre-cut to size to speed up the process. As a contrast, most shops in Asia purchase master sheets and their first operation is cutting the material from a master sheet. The traveler and the panels are then sent to drilling.

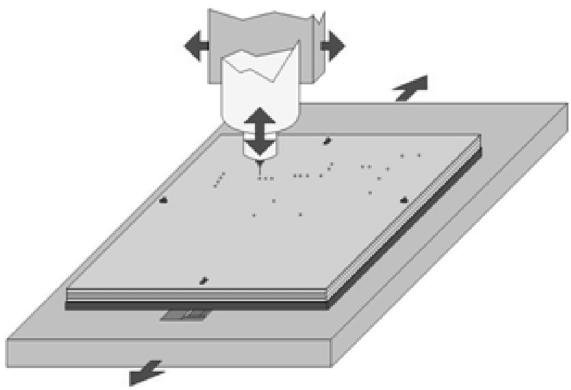
Drilling

The copper-clad panels are placed in a pinning machine, which automatically pins the panel by drilling two holes and injecting special tooling pins with entry material on top and a backup board on the bottom. The dowel pins protrude slightly from the bottom and are placed in tooling holes on the deck of the CNC drill. The panels are taped down at the edge to prevent movement and keep the top aluminum entry material in place. The height of the drill stack varies depending on a few parameters. Below a size 10 mil drill, the length of the drill flute is too short so the operator will reduce the number of panels stacked to one or two panels depending on material thickness. For normal drill size, if the material is .093″, the stack would be 2 panels; for .125″ or thicker, the number of panels would be reduced to one panel, increasing drilling cost. Normally, the operator would drill three .062″ panels stacked together.

The entry material serves several purposes. It gives the drill bit a soft material to enter before hitting the copper-clad panel. This improves accuracy and prevents burrs (little spurs of copper created where the drill enters the panel). The biggest reason for entry material is that it prevents nicks and dents in the copper of the top panel from broken drill bits or dirt which get imbedded in the drill pressure foot. As the drill is coming down to drill a hole, a pressure foot first contacts the stack of panels to hold it firm and take up any gap between the panels. This pressure foot can hit quite hard and push with 25 lb. force, so any sharp broken bit ends would embed in the soft foot material and the subsequent dent would be transferred to the panel each time it drills a hole. Entry material is made from

Phenolic, aluminum foil or paper and ranges in thickness from 0.005" to 0.012".

The backup board placed on the bottom of the drilled stack is composed of Phenolic, paper composite, or aluminum foil-clad fiber composite. Its purpose is to prevent exit burrs from forming on the bottom panel and to protect the drill table. Backup material is most often 0.093" thick to allow enough room for the drill to completely exit the bottom panel without hitting the bed of the CNC machine. Backup material is flipped over and used twice as the drills penetrate less than halfway. Some of the used backup material is reused a third time as backup on the router table during final route.



Drill head motion

Before the panel is drilled, the operator will select and inspect the drill sizes specified in the traveler. The drill point is checked under a 100x microscope to ensure the point and cutter edges are perfect. The drill bit selected is usually 4 mils (.004”) larger than the finished hole size to compensate for the copper that will be plated in the hole. The plated copper of 1.2 to 1.5 mils thick will close the hole diameter by two times the plating thickness. The operator will place the drill bits in special tooling pods from which the drill machine will automatically select the drill bits. The drill machine will check that the selected drill diameter is correct and that the drill is running true by inserting it into a special laser reader and running up the RPM.

The laser reader measures the drill diameter, which is compared to the electronic drill page to ensure the correct diameter hole is being drilled. The laser also measures drill run out which can widen the hole and cause rough drilling. The CNC drill machine then drills the holes, averaging one hole per 1/4 second or 240 holes per minute. With three panels high this reduces as hole diameter decreases or panel thickness increases. A good CNC drill machine can drill 3000 holes per minute with as many as 5 heads. An important aspect of the drilling operation is the user's ability to program the machine's Z-axis drill stroke with different drill diameters at different rates. These rates are typically engineered to achieve the best in output and hole quality while avoiding tool failure or breakage. Measured in inches per minute (ipm), feed rates depend on the tool diameter, machine capability and stability, laminate material type, copper layers, and stack height. The in-feed rate controls the chip loading. If a 1.5 mil chip load is required for premium drill wall quality, then the machine must move down 1.5 mils for every revolution. A drill bit moving at 120,000 RPM will only have 40 revolutions to travel through a .059″ material.

The operator will enter in the CNC drill machine memory, the in-feed rate and RPM speed for each drill diameter based on chip loading. Newer CNC drill machines receive the in feed and RPM information electronically with the drill data. Today's CNC drill machines have very high-pressure air bearing spindles running as high as 250,000 RPM. Drill machines vary from dedicated single spindle machines for high density, fine drill work to production 5 and 6 spindle machines. The minimum drill size used today with very high RPM air bearing spindles is in the 3 to 4 mil range (.004″). Air bearings require high pressure, compressed air that is dry and oil free. The computers that run today's drill machines are networked with front end computers allowing quick transfer of data. The machines weigh more than 15,000 pounds, requiring special floor construction to prevent vibrations from affecting adjacent machines.

Many modern drilling machines are equipped with automatic load and unload stations with automatic drill bit changers and broken bit detectors. The automatic load/unload and drill change features allow the machines to run continuously with minimum operator input, offering significant labor savings. The broken bit detectors provide assurance that panels with missing holes resulting from a broken bit do not proceed further in the process.

Spindle Speeds

Spindle speed settings control the rotation of the drill bit during the drilling cycle. Measured in revolutions per minute (RPM), speed also impacts the quality of the drilled hole as well as the drill cutting edge condition. High chip loads can result in excessive cutting-edge corner breakdown, or "rounding". This is an undesirable condition, resulting in the drill "punching" rather than shearing through the material stack creating a rough hole wall. Some laminates drill better than others with specific chip loads. Chip loads should remain constant throughout the drilling range except when limited by the spindle capability. Spindle speeds have risen during the history of PCB manufacturing. During the early days, with manual drill machines, RPM was limited to 15,000. When CNC machines became available, they featured high speed spindles of 60,000 RPM. In the '80s, air bearing spindles were invented, and the RPM was increased to 120,000 RPM. Today, we have micro hole machines above 250,000 RPM, drilling .003 inch diameter holes at 180 holes a minute.

Retract Rate

The z-axis return speed is programmable as well. This rate, known as retract rate, is measured in inches per minute (IPM). This is set to a speed that will minimize the duration of the drill bit inside the hole. The z-axis stability of the machine and drill bit diameter determine the optimum retract conditions.

Drill Bit, Hit Count

The number of holes, or hits, a drill bit can produce depends highly on the material it is drilling, the feeds and speeds, the amount of copper and the hole quality required to achieve proper electroless plating. Each drill stroke results in added wear, causing the cutting edge to become worn and less effective. Typically, drill bit hit count range is from 600 to 2,000 hits for "via" diameter range (0.006" - 0.0300") and 1,500 to 3,000 for “component" diameter range (0.032" - 0.080"). The drill bits are then sent out for re-pointing which can typically be done two to three times.

Z-axis Offsets

The floating position of the heads above the stack of boards to be drilled and a final bottom position are adjustable. The final penetration depth of the drills into the stack of panels is important for two reasons. The first being, the drill must pass through the laminate into the backer board deep enough to make a hole on the lower side without a taper due to the angle of the bit. Secondly, the drill must not pass through the backup material to enter the bed of the drill machine. Entering this value into the computer as a z-axis offset will elevate the base of the pressure foot just above the stack and the bottom limits will ensure the bit does not go too far down. The point clearance is directly related to the diameter of the drill bit and point angle; as the diameter increases, so does the distance needed to clear the point angle.

5 head CNC drill machine

Technologies of Drill Bits

Holes through a PCB are drilled with tiny drill bits made of solid tungsten carbide with a standard .125″ shank. Plastic collars are fitted on each drill bit to ensure the bit mounts in the chuck with precision. Most common laminate is epoxy filled fiberglass. Drill bit wear is in part because glass, being harder than steel on the Mohs scale, will dull even tungsten carbide. High drill RPM necessary for cost effective drilling of thousands of holes per board causes very high temperatures at the drill bit tip. High temperatures (400°C to 700°C) can cause epoxy smear on the side walls.

Picture of a micro drill bits with locating collars

When very small vias are required, drilling with mechanical bits is costly because of high rates of wear and breakage. In this case, the via hole may be drilled or evaporated by lasers. Laser-drilled vias typically have a tapered inferior surface finish inside the hole. It is also possible with controlled-depth drilling, laser drilling, or by pre-drilling the individual sheets of the PCB before lamination, to produce holes that connect only some of the copper layers, rather than passing through the entire board. These holes are called *blind vias* when they connect an internal copper layer to an outer layer, or *buried vias* when they connect two or more internal copper layers and no outer layers.

De-burr

Today's high-speed CNC drills produce relatively burr-free holes. Operators remove the panels from drilling and process drilled panels through a de-burring machine which has rotating abrasive brushes that mechanically remove any copper burrs at the rims of the holes and remove the protective zincate coating, which would prevent proper copper plating. Due to the superb quality of today's new CNC drilling machines, separate automatic hole checking is not usually performed. The de-burr cleaner units have high pressure clean water spray nozzles which blast out any drilling dust or debris which would affect electroless plating.

Hole Preparation

When processing double-sided boards using FR4 based materials, there is typically no requirement for any process to prepare the hole for the electroless copper plating process. There are, however, many other materials e.g. Teflon-based materials that need to either be processed through plasma or sodium etch. For some materials sodium etch is the only option.

Electroless Copper Plating

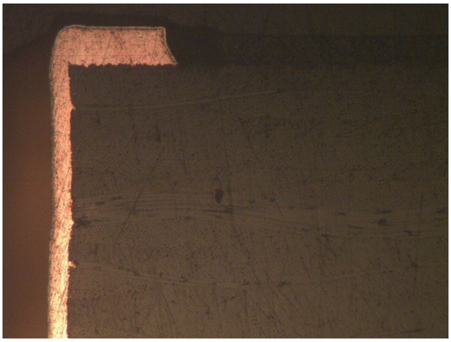
After de-burring, the panels are placed in racks and processed through a series of chemical baths to enable electroless copper to adhere in the holes. The first four tanks clean the panel and remove a small amount of the copper to create a clean surface for adhesion of the electroless.

The next tanks sensitize the epoxy and glass on the walls of the drilled holes with a palladium colloidal solution so it can receive a thin coating of copper in the electroless copper bath. This thin copper coating alone is not sufficiently thick enough to carry the electrical load, but it provides a metalized base upon which additional copper can be electrolytically deposited.

Automated electroless plating line

Electroless copper deposits range from about 20 micro-inches to 90 micro-inches thick. The thicker deposits are called "heavy deposit electroless."

Inside of multilayer shows glass fibers and copper plating



Although electroless copper plating provides the most cost-effective method for metalizing the through holes of a PCB, the process waste is costly to treat. Several alternative green processes such as carbon coating, direct metallization and conductive polymers have been introduced and are becoming main-stream. Based on data and use electroless copper has been generally accepted as the most reliable process for high technology printed circuit board designs.

Carbon or graphite metallization machines coat the board with a series of chemicals which allows a carbon bath to stick to the inside of the holes. An etch bath removes the carbon from the copper surface and leaves it in the holes. Carbon/graphite-based systems have advantages in flex and high-density boards because they do not produce long internal wicking, like electroless copper baths do.

Imaging

After electroless, many fabricators chemically clean the panel's electroless copper surface to promote adhesion of the dry film. The panels are dry film laminated on a vacuum automatic laminator or a hot roll pressure assisted laminator. The dry film, typically 1.2 to 2 mils thick, is photo sensitive and applied in a clean yellow lit room. The lights in the area are yellow or UV blocked to inhibit the UV sensitive dry film exposure. In addition, the room is kept very clean to limit dust and particles from imaging onto the panel. The laminator will remove one of the two protective films from the dry film during lamination. The temperature setting depends on the type of dry film used. Typically, it is around 100°C to 125°C. The temperature is set to ensure the dry film just melts to the surface providing maximum adhesion to the PCB. If the temperature setting is too high, blistering may occur. The lamination speed is around 3 to 5 feet per minute.

To image the panel, a silver halide film with the desired 1:1 image is optically aligned to the drilled holes in the panel and usually exposed with a powerful 5 kw 365 nm UV light unit. The silver halide film is placed emulsion side in contact with the PCB panel. The exposure machine has two vacuum trays. While one panel is in the machine being exposed, the operator is aligning the next panel. When ready, they switch position. There are two styles of vacuum trays. In the first type, the top frame has a clear mylar film and the bottom is glass. In the second type, both top and bottom have glass frames. Both styles of frames have a vacuum which is used to hold the film as tight as possible to prevent any light from leaking around the image on the film. Advanced shops like ASC use laser direct imaging (LDI) systems, which directly images the panel's dry film by rastering a laser over the panel. This eliminates the photo plotting process of silver films. The LDI allows for automatic scaling to compensate for panel movement due to temperature change and will center the pad more accurately on the hole and eliminates any defects that can be associated with plotting films or damaged film.

The exposure operator will use a 21 Stouffer step film to check for proper dry film exposure. As the exposure light intensity increases, more steps are cleared. There is a correlation between exposure levels and dry film performance. Most dry films and solder masks aim for 8 to 10 clear Stouffer steps.

LDI imaging unit in yellow room lighting

After exposure, the top protective plastic film is removed from the dry film and the panels are passed through an automatic horizontal spray developer. The developer using a relatively environmentally friendly, .8 percent sodium carbonate solution vigorously sprayed through oscillating nozzles. The solution dissolves any unexposed dry film. When the dry film is exposed to UV light, it hardens by cross polymerization. Where the image on the silver photo film blocked the light, the dry film will remain soft. The developer solution removes the soft unpolymerized film, exposing the base copper in the areas where we want copper plating to build up the thickness. The developed dry film panel is then AOI checked or inspected by humans for shorts and nicks and passed to copper plating. If the dry film image is damaged or rejected, it can be stripped and re-imaged, saving the panel.

The PCB panel is now patterned with an image of dry film resist and bare copper where the traces, holes and pads will be copper plated and built up to form the circuit. Liquid resist can be applied by roller machines, by spray or by silk screening.

Copper Pattern Plating

The panels are clamped in plating racks that electrically contact the plating open area that front-end engineering placed on the edge of the panel. The panels are then immersed in a series of chemical baths.

The first tank cleans and removes any dry film resist residue followed typically by two rinses. The next tank is a microetch solution that removes a small amount of copper to reduce the surface tension and create wetting of the surface. Then a quick dip in a 10% sulfuric acid solution creates an acidic surface. Next, the panels are immersed in the copper plating solution. The panels are electrolytically charged with a negative polarity and the solution is positively charged, which causes copper ions that have been dissolved off the copper anodes to attract and adhere to the exposed copper areas on the panel. Copper is plated to the specified thickness on the traveler and verified by an electronic copper thickness gauge. Typically, the operator plates to a thickness of 0.0012" on the surface and in the holes. Heavy copper boards can be plated upwards of 12 oz. of copper for high current applications. The entire copper plating process takes about 90 minutes per one oz. plated. The panels are moved from bath to bath, either by hand or by machine. Automatic plating equipment is computer controlled and the hoist moves the racked panels through the plating sequence without human intervention and with precise timing.

The panel with the dry film negative circuitry pattern is plated with copper where the dry film was removed by the developer. The panels are further electroplated with tin, like the copper plating process.

The tin is plated only a few microns thick in 10 minutes. The tin provides a metallic etch barrier for the alkaline etch process. In the past, tin/lead was used as an etch resist, but due to RoHS environmental laws, lead is now a controlled substance. For that reason, all fabricators have switched to pure tin etch resist.

Large automated copper plating line

To have an even greener etch system, a very thin base copper 3 or 5 micron thick copper can be used which is plated by .0014 mils of copper; no tin etch resist is used and a quick pass through the etcher removes the exposed thin base copper without hurting the traces and hole copper. This is called differential etching and is preferred due to it’s ability to produce finer lines with less pollution.

Strip Etch Strip

The panels are now stripped of the dry film (resist stripping) by a tank in batches or processed through conveyorized spray equipment containing 5% sodium hydroxide solution to remove the dry film.

After the resist is stripped from the panel, the panel is placed in a conveyorized spray etcher. A chemical ammonia etchant removes the unprotected copper but does not attack the tin coating on the tracks and in the holes. The tin coating resists the actions of the ammonia etchant and protects the copper underneath. The etcher is carefully controlled to minimize over or under etching. Over etching reduces the line width and creates a large overhang and under etching leaves copper on the surface and between tracks. A measuring microscope is used to ensure the correct etch rate and the correct line width once the panel is etched.

The tin etch resist is then chemically stripped from the copper with nitric acid by an automatic conveyorized spray stripper, revealing the copper circuitry pattern. The tin is easily recycled from the nitric acid providing a close looped system, reducing pollution.

Automated Optical Inspection (AOI)

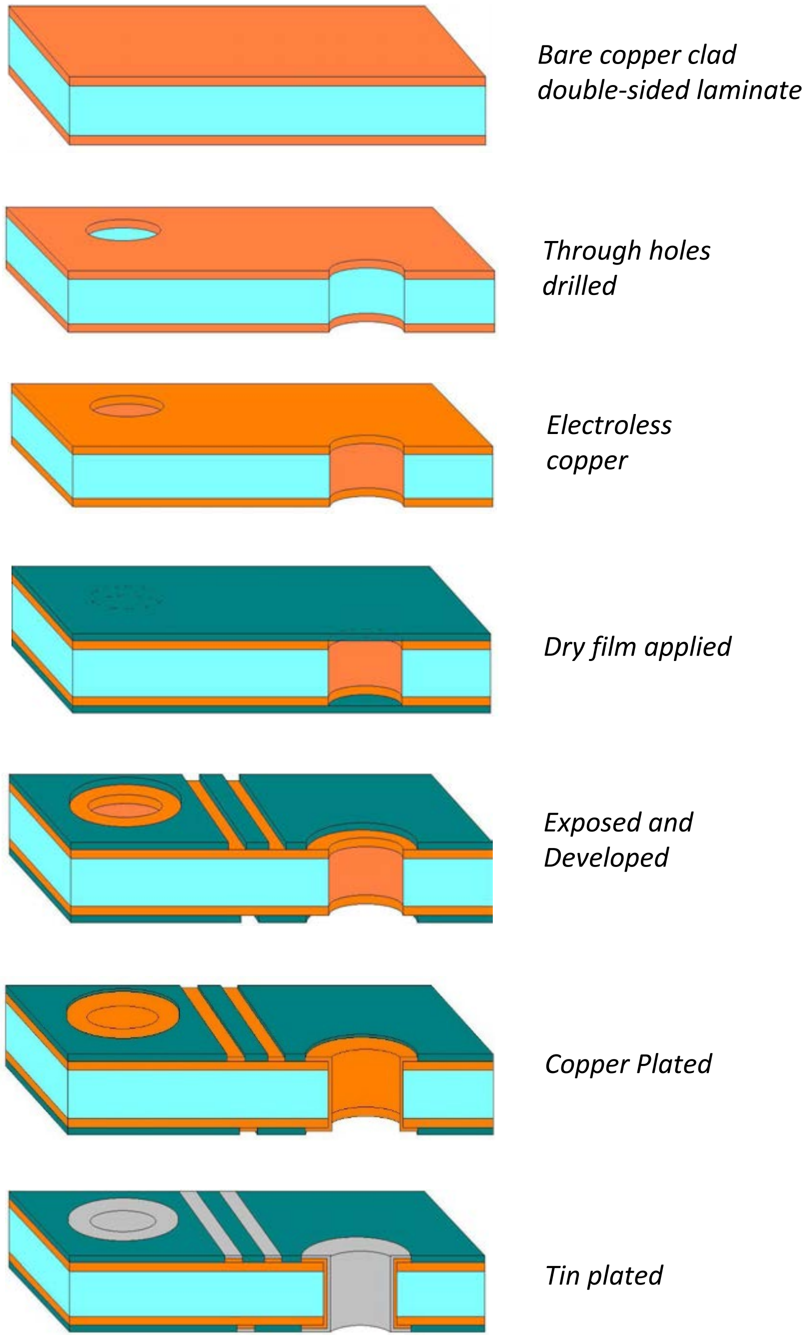
The etched panels are inspected before the solder mask application, as faults can be found and easily fixed, without the problem of trying to see and work through the solder mask. The AOI computerized optical inspection only takes a few seconds. It scans the panel and then compares the image with the original Gerber files. Any error is listed and the operator then keys through each one. The AOI shows the operator a picture of the fault. The operator must decide if it is a repairable fault, in which case, it is either laser removed with the internal UV laser in the AOI machine or marked for manual repair such as welding an open or marked as a rejected panel. Most PCB fabricators have stopped the welding of opens due to long-term reliability issues.

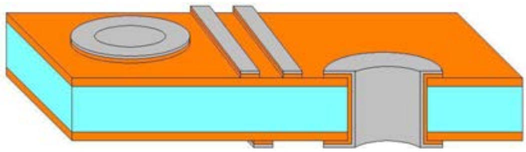
The AOI is also capable of finding near shorts on significant line reductions that are a defect; these cannot be caught by electrical test since testing only catches opens or shorts. The AOI is so sensitive it can find many false faults, so a knowledgeable operator and correct set up are required.

Solder Mask

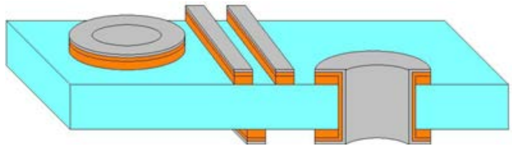
A solder mask, or “solder resist,” is a nonconductive photoimageable epoxy coating that is applied to the surface of a PCB, then imaged and developed to create an image of the through hole pads and SMT pads to allow soldering at a later stage.

Process steps for double sided circuit board

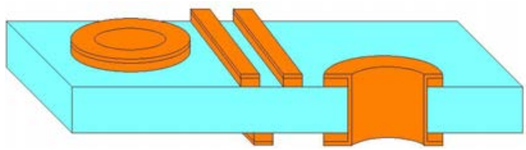




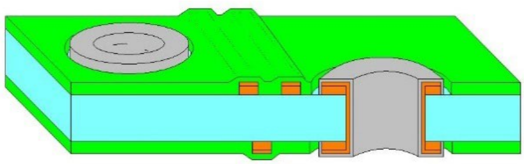
Dry film resist stripped



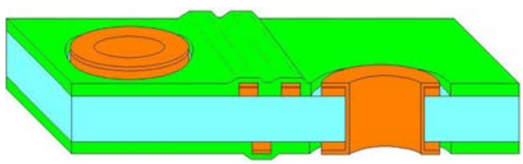
Etched copper



Tin resist stripped



Solder mask applied exposed & developed



Final Finish

In the past, the main method of solder mask application was thermally cured, silkscreened solder mask. The screen was coated with a photoimageable film and exposed with a negative of the solder mask pattern and washed out. The ink was pushed through with a squeegee onto the panel and the ink cured. The problem with this method is the line definition and the width of a solder dam was not enough for new finer printed circuit technology. The mesh of the screen is very elastic and is subject to variances in repeatability. For a short time, dry film solder mask was used, but due to environmental and operational problems, it was soon replaced by liquid, photo imageable solder masks, LPI.

The LPI solder mask is first applied with an open mesh silk screen set up, roller coater, curtain coater or a spray coater. The applied ink is tack dried to ensure that the photo tool does not stick to the mask. A photo tool is aligned and exposed.

The solder mask is then developed in a conveyorized solder mask developer with a mild sodium carbonate solution to clear the unwanted mask. The solder mask is then thermally cured for one hour in a special high air flow oven. Newer LDI (Laser Direct Imaging) solder masks are more common as the advantages of the technology become more utilized. The higher sensitivity of the new inks allow the lower power laser imaging units to expose the solder mask. The advantages are reduced cost of not having to produce photo tools, better alignment accuracy and automatic image scaling to better fit the image onto the PCB panel, which expands and contracts during the process, making proper solder mask alignment a problem when using fixed photo tools.

In the 1980s, solder mask over bare copper (SMOBC) became the dominant fabrication method. The older style PCB was made with electroplated tin lead “solder,” covering all traces, then solder masked over the tin lead. The solder mask wrinkled and peeled over the tin lead surface when the board was assembled. SMOBC became the preferred method for this reason. Did you ever wonder why PCBs tend to be green? It was the result of a study by a big company to find ways to relieve eyestrain of the assembly people.

A green PCB with white component marking was the easiest color on their eyes. Today, green is simply the default color for solder mask that most PCB fabricators use. Solder mask is applied over the entire surface of a PCB, except for land patterns and other copper areas that must make electrical connections. The solder mask prevents solder from adhering to areas other than the pad to be soldered. Solder mask helps prevent dendrite growth between circuits. Solder mask is available in a wide range of colors including blue, red, white, black and clear. Many companies specify red boards for design prototypes and use green for only pro- duction boards. A lot of LED boards specify bright white solder mask for reflectivity.

Some companies are currently working on developing an inkjet application of the solder mask. The advantage of this is that it significantly reduces the number of process steps.

White Component Legend

Also called “nomenclature,” “white marking,” silk screening or “ident.” The component legend comprises the identification symbols screen printed on the board to aid the assembly operation, field service personnel and to identify the fabricator and date. The screen-printed text indicates component designators, switch setting requirements, test points, and other features useful in assembling, testing, and servicing the circuit board. Modern assembly machines do not require the silkscreen to place a component. They do, however, need fiducial or alignment tooling holes to zero X-Y of the component placement heads to the board.

Component legend is screen printed on the panel with a thermal or UV cured epoxy ink, which comes in a variety of colors; white is most often specified.

Occasionally a liquid photoimageable (LPI) white ink is flood screened on the solder mask, then tack dried and exposed for very fine image, then developed and baked.

New inkjet digital printing machines are replacing the traditional screen-printing process. This technology allows printing of finer line component marking on the PCB, including incremental serialization and barcode information for managing traceability. It uses a thermal or UV cured ink and eliminates the tack bake, exposure, develop, as well as using less ink, so it is more environmen-tally friendly.

Final Finish

The final finish is normally applied at this stage. Due to the variety of possibilities, we have dedicated Chapter 9 this topic.

Final Fabrication

Final fabrication refers to the mechanical operations such as routing, beveling and scoring, slots and notching that are performed on a PCB board to meet the specifications on the work traveler. Routing the final shape is performed on a dedicated router with lower RPM spindles, with more power. CNC routers also feature a locked foot that clamps down on the last section of the route path to hold the board in place to ensure that the last route cut does not allow the board to wiggle loose and damage the edge by hitting the cutter.

The front-end engineer will design the route path, set the direction so the router is cutting into the path, and pick the entry and exit points. The router path may include cut outs for impedance coupons and cross-sectional coupons, needed by QA to ascertain that the board is correct. Scoring is a process where ‘V’ grooves are machined on opposite sides of the panel to the specified depth to allow the user to break apart boards from the panel after assembly. A sub-panel is routed out of the main panel with extra area on the sides and special tooling holes for clamping in the assembly machines. Typically, a .062″ or .093” carbide router bit is used. Copper is a very soft metal and difficult to machine smoothly without a rough edge. Therefore, your design needs to keep the copper traces back from a routed edge, normally .014″ (.34 mm) is enough.

The same theory applies to solder mask; routed solder mask can chip. For best results, solder mask should be kept .010″ (.25 mm) away from a routed edge. For thicker copper boards, allow more space for the solder mask to cover the edge of the copper.

Electrical Test

As one of the final quality checks, the boards are electrically tested (also called *bare-board test)* where each circuit connection (as defined in a *net list*) is verified as correct on the finished board. For high-volume production, a bed of nails tester and a specifically designed and manufactured fixture is used to contact copper lands or holes on one or both sides of the board to facilitate testing. A computer will *instruct* the electrical test unit to apply a small voltage to each contact point on the bed-of-nails as required and verify that such voltage appears at other appropriate contact points. A "short" on a board would be a connection where there should not be one; an "open" is between two points that should be connected but are not.

For fixed pin testing from the CAD-generated test data, a test fixture is made. A test fixture is usually constructed by drilling a piece of non-conductive material such as Lexan ® or Plexiglas ® with the same pattern as the drilled holes and SMT pads in the PCB to be tested. Spring-loaded, gold tipped metal pins are inserted in the drilled holes of the test fixture to contact the corresponding points on the PCB to be tested. The opposite ends of the metal pins are connected to the test equipment by a standard bed of nails.

This type of test fixture is unique to the specific PCB and cannot be used for any other board. Some bed of nails test fixtures contact one side of the PCB. However, most testers today feature a hinged “clam-shell” that has two beds of nails; one on the top and one on the bottom.

The electrical tester will send a signal out to two or more points, which are in the beginning or end of the electrical net. This will indicate if the trace is open. The machine will send out signals to all the pins located around the trace to measure if it is shorted to any other trace. The machine can measure very high resistance to pick up such faults as 10 meg ohm wicking or low resistance signals to check if the track has a large nick in it which would increase its resistance.

The tester machine will record any problems and provide a printout for the operator to check on a verifying computer.

The verifying computer shows a picture of the trace and any other trace that it is shorted to or if it is open. The operator will buzz out the shorted or open tracks with an ohm testing unit that changes sound pitch as the resistance gets lower.

Flying probe electrical tester

This way an operator can zero in on the short as the machine changes tone when the probes get close to the short. Shorts are usually removed with a careful cut under a microscope or using the AOI UV laser but opens in the outer layer cannot be fixed.

The other way to electrically test a panel is with flying probe testers. The advantage is lower cost as no fixture is needed. The main problem is that flying probes are slower than pin testing when testing large orders. The flying probe has up to 16 little computer-controlled arms that whip around the panel, testing each net for opens and shorts. Flying probes are used for quick turn, low volume work.

Final Inspection

The final step in the manufacturing process is a visual and mechanical inspection of the finished PCB. The PCBs are checked for correct mechanical dimensions. Hole sizes are checked with pin gauges. The solder mask and identification marking are visually examined for overall appearance and other cosmetic parameters. The solder mask is checked to see if there is any encroachment on the pads and the quality and coverage of the final finish is examined. If the board specification is class three, a cross-section coupon is taken and checked for cracking in the holes after a stress test in molten solder and for correct plating thickness. Cross-sectioning is described in more detail in Chapter 17. SMT components became widely used by the mid 1990’s. Components were mechanically redesigned to have small metal tabs or end caps that could be soldered directly onto the PCB surface. Components have become much smaller and component placement on both sides of the board with SMT is more common than the older through-hole mounting components.

For high volume inspection applications Automated Visual Inspection (AVI) tools are now available and can be seen in some of the higher volume PCB facilities.

Chapter 8

Manufacturing Multilayer PCBs

Approximately 60% of the North American PCB manufacturing output is multilayers, with 4, 6 and 8 layers being the most common, and an upper limit of about 60 layers. The multilayer design of layer-layer interconnect allows for much higher wiring density with separate ground and power planes, various signal layers and two component layers. We will concentrate on the inner layer and lamination cycle as after pressing, the panel is treated almost the same as a double-sided and we will note the differences. To fabricate an eight-layer board, we need to manufacture the 3 cores, which will be laminated together with prepreg and copper foil layers added to top and bottom to form the final panel.

Material

The cores are usually high Tg FR4 material or alternate materials based on customer requirements. They are typically ½ oz. or 1 oz. copper. The copper weight and specification are put into the manufacturing kit by the stock room following the work order traveler.

Inner Layer Circuit Formation

This process is like the outer layer process described in the previous chapter on Manufacturing Double Sided PCBs. The one major difference is while the outer layer process is considered additive due to plating the circuitry, the formation of inner layer circuitry is a subtractive process.

The cores are chemically cleaned. This also removes the zincate anti-oxide coating. The cores are sent to the clean room to be laminated with dry film. After a short waiting time to let the dry film stabilize, the inner layers are exposed in a special frame, which aligns the top and bottom photo tool film in tight registration with each other. Today like ASC, most top PCB fabricators in North America have laser direct imaging (LDI) machines that use a series of drilled holes to know where the inner layers need to be located to account for shrinkage in the lamination process, called scaling. The panels are then developed in an automatic spray developer after exposure and sent to QA for inspection. If every item is correct, the panels are etched. The normal etchant for inner layers is cupric chloride. It provides a finer etch quality with the ability of easily removing the copper allowing for recycling of the copper. Cupric chloride cannot be used with tin or tin etch resist, so it is mainly used for inner layers. After etching, the photoresist on the core is stripped in a sodium hydroxide solution.

Cupric chloride inner layer etcher

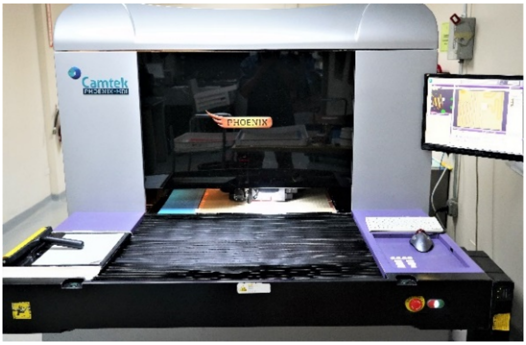
Post Etch Punch (PEP)

After the core is stripped, it is punched with tooling holes on a post etch punch. The computer controlled optical aligned punch finds the alignment marks that the front-end engineer placed on the photo tool, it appears in the core and finds the center of each side. The post-etch punch unit punches four holes, which are used to align the cores on the lamination press plates. One hole is usually offset to align all the layers in the same orientation. This method prevents panels from being placed upside down or rotated within the multi-layer structure.

Inner layer post etch punch

AOI

After the etching/stripping process, the cores are inspected with an AOI machine to find any opens or shorts. Shorts can be laser-removed in the AOI or cut out in some situations. If allowed, opens can be fixed by arc welding a small gold wire across the open. However, today most customers will not allow welding of inner layer opens. Some of the more complicated inner layers will be electrically tested on a special inner layer flying probe tester, which stretches the thin core tight allowing the probes to find the pads.



AOI scanning optical inspection

Alternate Oxide

The cores are sent to an alternate oxide treatment to be cleaned, micro-etched to increase the surface area and a coating is applied which promotes the adhesion of the prepreg to the copper. This can either be a vertical dip process or a horizontal conveyorized process. In the past a brown or black oxide was used to create adhesion to the prepreg. This treatment consists of a type of chemistry designed to increase surface area or to promote adhesion between the specific resin system in the bonding adhesive and the surface copper of the layers to be lamiated. Treated inner layer cores are transported into the lamination set up room.

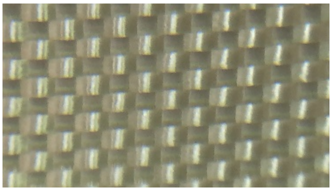
Lamination

The lamination process starts with layup, which involves assembly of the copper foil, inner layer cores and prepreg, to prepare the panel.

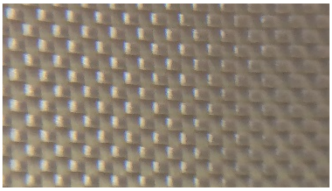
The layup starts with heavy special steel lamination caul plates, 1/2-inch-thick, which have 4 tooling bushings that fit the round holes punched in the cores. All the steel separator and prepreg are pre-punched with the same slotted round configuration. This serves to aid in the layup process Thermal lagging materials are added to the multilayer construction in order to slow the rate of heat rise in the package and to evenly distribute the pressure across the surface of the panel.

This is necessary due to the height differences of the various copper traces on the multiple layers that form the multilayer package which creates the finished panel. We want to control the temperature rise, to create the proper flow and fill characteristics for a given prepreg or bonding sheet resin system. This allows the resin and any filler materials to flow and fill even small gaps or blind vias in subassemblies within the multilayer package. A sheet of stainless steel is then placed on top of the thermal lag sheets to provide a flat surface for the outer side of the panel. A sheet of thin aluminum is used to provide a dent-free surface, along a sheet of high temperature Tedlar® provides a non-stick surface so that the prepreg flow out will not ruin the stainless-steel separation sheets or glue the whole stack together.

Prepreg is a B stage material that has been partially cured to enable the operators to handle the sheets; with pressure and temperature the prepreg sets up and fully cures. There are different kind of prepregs used depending on thickness, electrical and other requirements. The press cycle used is dependent on the type and properties of the prepreg being used. Glass cloth photos courtesy of Isola.



7628 Glass Cloth

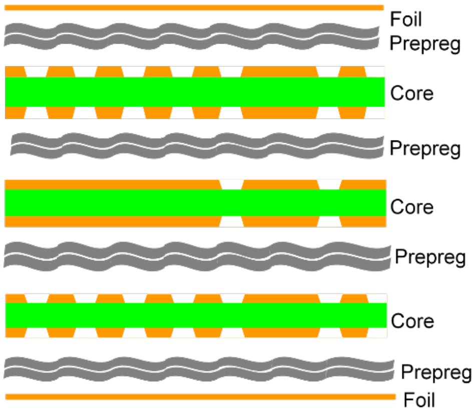


2116 Glass Cloth

Style	Thickness	Resin %
106	1.8 - 2.5	69-77
1067	2 - 2.7	68-76
1080	2.5 - 3.6	64-72
1086	3 - 3.5	61-68
2113	3.5 - 4.2	55-60
2116	4 - 5.4	53-59
7628	6.4 - 7.5	40-50

Chart of Common FR-4 Prepreg

The first copper foil is laid on and followed by 2 or 3 sheets of prepreg to provide the glue which sticks the multilayer together. The first core layer 6-7 is laid in, 2 or 3 prepregs are placed on the stack, then core 4-5, followed by 2 or 3 prepregs, then core layer 2-3, 2 or 3 more prepreg laid in and the final copper foil sheet. We now reverse the process; a sheet of Tedlar®, a sheet of thin aluminum, a stainless-steel separator.



8-Layer Stackup

This can be repeated quite a few times with 5 to 10 multilayer panels to build up the thickness of the overall package. A thermocouple will be placed in the stack up to measure the temperature rise in degrees F per minute to allow the prepreg the proper time and viscosity to flow into all the spaces and openings. The rate of temperature rise or flow window will be controlled to within the specified parameters for a given resin system.

As an alternate layup process, many shops buy a pre-made sandwich of Copper / Aluminum / Copper, Copper / Aluminum, Aluminum / Copper. The advantage of this solution is that it reduces the possibility of nicks and contamination of the copper and makes for a less labor-intensive lay-up process. Sheets of Tedlar® are then not used between panels.

The buildup package is loaded into the multilayer press where either a pre-vacuum is applied, or the pressure starts immediately beginning the lamination cycle.

During this time, the package has started to heat up. The lamination pressure may then be applied in either a ramped configuration or directly to full pressure. Force is expressed in force per unit area or in this case, pounds per square inch (PSI).

Different structures and resin systems require different pressures, some as low as 25-50 PSI in and others 500 PSI or more. An 18″ x 24″ panel at even a moderate pressure of 300 PSI is a staggering 130,000 pounds of total force. After 60 to 180 minutes at full pressure and heat, the prepreg has flowed and cured by molecular cross-linking which bonds all layers together.

After the full pressure cycle, the multi-layer stack up is cooled slowly, removed and the pins are removed with a small hydraulic press. Many facilities bake the panels after lamination to relieve any stress locked in during lamination. Warp and fill are the direction that the fibers run in the laminate material. All cores and prepreg in the stack up should be in the same orientation. This helps reduce or eliminate warping.

Many presses use a vacuum to eliminate volatiles. This helps with reducing edge voids, and reduces the pressure required in the lamination cycle com-pared to a press without vacuum.

High pressure vacuum multilayer lamination press

Most fabricators, like ASC, utilize vacuum assisted hydraulic presses. Some fabricators utilize hydraulic presses without vacuum. Two other options that are rarely utilized are the autoclave and direct current or continuous foil method.

De-flash

After the laminated stack has been de-pinned and taken apart, the prepreg has flowed out and cured and the copper foil creates a sharp edge “the flash.” A dedicated router is usually set up and the panels are de-flashed, then cleaned.

Drill

An x-ray unit is used to determine the best overall center of all the pads to pin the panels on the drill. As the layers move around when pressed and shrink during the lamination process, the exact center of all the pad locations through the eight layers is difficult to find. To ensure the various layers align as best as possible after the pressing cycle, the front-end engineer will scale the size of each layer so they all align after lamination.

Ground planes do not shrink as much as signal layers because the remaining copper lowers the shrinkage rate of the epoxy as it cures. The scaling of each panel is constantly tracked from each build up and followed to continually improve the scaling numbers.

Newer x-ray pinner drill units look at special alignment targets placed on each layer through the panel with x-rays, average the error between the inner pads and drill the tooling holes for the drill. These units also interface with the front-end engineer’s computer and track the scaling for each job, keeping a running log of similar jobs and predicting the scaling involved.

The panels are pinned on the drill and a few test holes drilled into special test pads in the corners. The panel is removed from the drill and checked with a manual x-ray unit. If the holes are not centered in the inner pads, the operator can move the zero X-Y position of the drill table to compensate. If one end aligns properly but the other end is too long, the operator can scale the drill file and shrink or stretch the data file. Multilayer panels are different than double-sided panels as the drills cut through more copper and glass, so they need to be changed more frequently. Multilayers must have smooth, smear-free holes. As the drill bit passes through layers of copper and epoxy glass, it generates heat, which can cause the epoxy to melt and smear along the sides of the hole and the copper interconnections. The subsequent copper plating must form a reliable bond with the internal copper circuitry, so the holes must be free of drilling dust, debris, and smear. Higher density multilayer designs often have smaller holes than double sided designs. To maintain quality, smaller stack heights of two high or even a single panel, are placed on the drill.

De-burr

The same method that is used to remove drill burrs from double-sided boards is used for multilayer panels, but additional care is needed because of the smaller hole sizes. The smaller holes are more prone to retaining drilling debris. If the holes are clogged, plating solution cannot flow through them and deposit copper. Partial or no copper deposit in the hole means little or no electrical connection to the circuitry on the inner layers and the reliability will suffer. Special high-pressure washing units blow the debris out of the small holes.

Smear Removal

A multilayer panel requires several additional chemical process steps to complete the electroless deposit of copper. These extra steps remove the epoxy smear that may have been created in the drilling process. The smear prevents the electroless copper from bonding to the copper and glass fibers on the inner layers, thus creating an open circuit or an unreliable plated through hole.

The epoxy smear is removed before electroless plating by immersing the panel in a cleaning chemical tank to remove any dust or debris in the holes. It is followed by immersion in potassium permanganate or concentrated sulfuric acid, then into a glass etch solution to etch back the epoxy and glass fibers in the hole.

As an alternate process, smear removal and some etch back can also be created by using a high frequency, high powered electronic plasma generated by exiting molecules in an oxygen and fluorocarbon rich gas mixture. After smear and etch back removal, the panels are processed through electroless same way as double sided. Some materials require a plasma treatment and others may require sodium etch. PCB fabricators usually work with the raw material supplier to ensure they understand the specific requirements of the resin systems and the desmear/hole preparation requirements prior to electroless.

Electroless Copper

This process is the same as a double-sided PCB. As hole sizes reduce the electroless process can be more challenging and many times the electroless baskets may need to be vibrated and ultra-sonics may be required in some of the tanks to ensure uniform electroless coverage inside the via holes.

Imaging

The processing is almost the same as double-sided boards. The multilayer panels can require a higher level of dimensional control because of smaller surface mount pads and higher layer counts and larger dimensional changes due to CTE (coefficient of thermal expansion) movement of the cores. The higher densities make clean rooms, static control, temperature and humidity control critical in the imaging area. The scaling of the package must be considered, as each layer and the whole package will all move around at different numbers, a typical 18” x 24” panel may shrink .018” which if unaccounted for would result in drills completely missing smaller inner pads and will lead to misregistration defects.

Plating Differences

As layer counts increase and hole sizes decrease, the aspect ratio (the ratio of the panel thickness to the hole diameter) increases dramatically. This higher ratio demands special techniques and chemistries to achieve uniform plating and adequate thickness in the hole. Specially designed agitation systems and solution movement methods such as impingement and ultrasonic vibration increase the solution flow through the holes, thus improving the plating uniformity. More advanced chemistries have been developed to enhance the uniformity and quality of the deposit in smaller holes with pulse plating technologies. The rest of the multilayer process is almost the same as double-sided except for increased quality control checks.

Post Plating Processes

The post plating processes are similar to double-sided PCBs and are covered in Chapter 7.

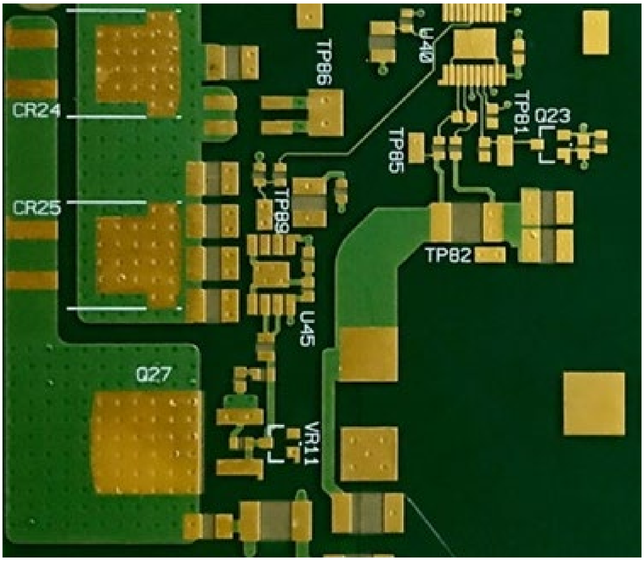
Multilayer Variation

The processes detailed in this chapter represent the methods used to produce the bulk of PCBs in North America today. Each step can be performed in a large variety of ways with additional changes created by the different equipment and technologies used. One significant processing sequence change comes from a technology called blind and buried via holes.

Blind via is a plated hole that does not extend through the entire thickness of the board but stops at a given layer and is usually drilled with a laser, controlled depth drilling, or uses cap technology. Buried via plated holes are between inner layers only and do not extend to either external surface.

Manufacturing multilayers that call for buried vias is not difficult. You drill a core or series of cores, laminated together and process it like a double-sided PCB. Blind vias, however, require the ability to drill to a given depth of the panel and no deeper (controlled depth drilling). Special drilling equipment such as laser drills or machines capable of controlled depth drilling is required and the operation itself is more expensive than regular drilling since the panels cannot be stacked.

With increased density of semiconductor packaging demanding more inter-connections, the number of designs using blind and buried vias is increasing. As the width of the conductors decrease and the hole sizes shrink, it allows us to fit more circuitry in the same size package.



Blind and buried vias are also discussed in Chapter 11.

There are two little used "subtractive" methods (methods that remove copper) to produce printed circuit boards. Silk screen printing uses etch-resistant inks to protect the copper foil from the etchant, which removes the unwanted copper. Alternatively, the ink may be conductive which is printed on a blank (non-conductive) board. The latter technique is also used in the manufacture of hybrid circuits.

PCB milling for printed circuit boards uses a three-axis mechanical milling/drilling system to mill away the copper foil from the substrate and drill the holes. A PCB milling machine operates in a similar way to a plotter, receiving commands from the host software that control the position of the milling head in the X, Y, and Z axis. Data to drive the PCB milling unit is extracted from files generated in PCB design software.

Chapter 9

Final Finishes

Final finishes provide a surface for the component assembler to either solder, wire bond or conductively attach a component pad or lead to a pad, hole or area of a PCB. The other use for a final finish is to provide a known contact resistance and life cycle for connectors, keys or switches. The primary purpose of a final finish is to create electrical and thermal continuity with a surface of the PCB.

The following considerations should be taken when choosing a final finish:

- Lead tolerant or Lead Free (LF) process
- Shelf life
- Flatness
- Lead or Ball Pitch
- Wire bondability
- Lead insertion
- Solder joint integrity
- Corrosion resistance
- Potential assembly problems
- Cost

Before we look at pros and cons of each finish, it's important to understand the types of final finish that are available and what they have to offer. Normal printed circuit boards have copper as their main conductor. If the copper finish is left unprotected, the copper will oxidize and be difficult to solder. Some circuits utilize nickel/gold, copper/palladium or solid gold, as the main conductors and may not need a surface finish. The ideal surface finish would have good solderability, flat coplanar surface, relatively low cost, unlimited number of heat cycles and minor to none, health and safety concerns.

There are various final finishes available. The most prevalent are: Lead Free Hot Air Level (LF-HASL), Hot Air Solder Leveling (HASL), Reflowed Tin-Lead, Organic Solder Preservative (OSP), Electroless-Nickel Immersion Gold (ENIG), Immersion Silver and Immersion Tin, Plated Nickel/Plated Hard Gold, Plated Nickel/Plated Soft Wire Bondable Gold, as well as special finishes which are plasma applied. Each finish has good points and bad points. Different types of finish are best suited for different applications. For example: LF-HASL tends to be the most commonly used surface finish for standard printed circuit work but it is not flat enough for higher pin count BGA pads.

HASL was the predominant surface finish. With the ROHS directive in place, most PCBs manufactured now have lead-free capabilities.

LF HASL (Lead Free Hot Air Solder Level)
This is the predominant 'unleaded' surface finish presently used in the industry. To understand the causes for uneven surfaces from LF HASL, it helps to understand the process.

The board is dipped into the solder and held there for a dwell time. The excess solder is then removed by 'air knives,' which blow hot air across the surface of the board removing any excess solder. This process is very violent and hot, there are a lot of variables that must be controlled such as air pressure, dwell time in the solder pot, angle of the air knives, speed of entry and retraction. Each one of these items, and many more, will influence the leveling result.

A fine line circuit is very thin and easily damaged. The hot air leveling process is not well suited to thin traces or thin laminate. In applications where a flatter solder is required, eliminate the problem by using a finish alternative such as (ENIG, silver, OSP etc) or specify a horizontal leveler which has less variation of solder thickness and shape. The horizontal leveler does have different thickness, top to bottom. There are several things that cannot be easily controlled; the physical orientation of the pads or size of the pads, for example. If you have a board with a BGA pad set on it, you will generally see that the solder is higher in one direction than the other. The pads going vertical will have thicker solder than the pads going horizontal, for this reason some machines use a 45-degree angle on the panel.

For the assembly process, LF HASL has many advantages. It is one of the cheapest PCB finishes available and the surface finish remains solderable through multiple reflow, wash and storage cycles. For electrical testing, LF HASL also provides automatic covering of the test pads and vias with solder. However, the flatness, or co-planarity, of the surface is poor when compared to other alternatives. LF HASL has been serving the printed circuit industry well for many years but with the advent of fine line circuits requiring a very flat surface; its usage maybe reduced. In addition to the lead-free issues such as reduced sol-der pot life, the increased complexity of boards and the finer pitches have exposed many limitations of the LF HASL finish.

HASL (Hot Air Solder Level)
This is not lead free compatible. This is a 63% Tin / 37% Lead alloy. The process and equipment are very similar to LF HASL except the molten solder is at a slightly lower temperature. A lot of the process concerns are like the LF HASL mentioned above.

Reflowed Tin-Lead

Before the widespread use of solder mask, the most commonly used method was to electroplate a coating of tin-lead on the copper. This was followed by re-flowing the tin-lead in hot oil. This final finish is used on many military boards. ASC has this surface finish in-house.

OSP (Organic Surface Protection)

OSP is designed to produce a thin, uniform, protective layer on the copper surface of the PCBs. This coating protects the circuitry from oxidization during storage and assembly operations. For assembly, it has superior capabilities over traditional LF HASL with respect to co-planarity but requires significant process changes with the type of flux and number of heat cycles.

Careful handling is needed as acidic fingerprints degrade the OSP and leave the copper susceptible to oxidization. Assemblers prefer to work with metal finishes that are more flexible and endure more heat cycles. With OSP finish, the test points can mark the surface of the pad significantly deep enough to reject the circuit.

The OSP does limit the number of rework cycles as the coating degrades with each heat cycle. Some assemblers do not like the dermatitis effect OSP has on their skin. OSP is seen by some to offer immediate cost savings and to be the first choice for LF HASL replacement.

ENIG (Electroless Nickel Immersion Gold)

ENIG coatings are used with great success, despite the higher per unit cost. It has a flat surface and excellent solderability. An effect known in the industry as 'black pad' or 'mudflat cracking' presents some problems. The black smut pad can also be caused by improper plating bath chemistry and application. This has led to a poor, not justified, reputation for ENIG. Pros: excellent solderability, coplanar flat surface, excellent shelf life, withstands multiple reflows. It is a good surface finish for fine line boards. Cons: higher cost (approx. 5x HASL), 'black pad' issue, which is mostly solved now, however manufacturing process can use potentially dangerous chemicals like cyanide and must be addressed with robust safety and handling procedures.

Immersion Silver

Immersion Silver is a relatively recent addition to the PCB finish. During the final soldering process, the silver layer gets dissolved into the solder joint leaving a tin, copper, silver alloy on the copper which provides very reliable solder joints for BGA packages. The contrasting color makes it easy to inspect. Immersion Silver is a very promising finish as it remains solderable throughout manufacturing process and has no negative effect on probe contact at testing. For fine lead pitches (< 0.64mm), it has some issues with solder bridging and thickness. Advantages are comparable per unit cost to LF HASL, excellent co-planarity, lead free process, improved solderability and minimum changes needed to the assembly process. It is a very good fine line finish. Additions to the process have eliminated the dendritic growth concerns.

Immersion Tin

This is also called white tin. Many fabricators are actively testing this new finish and it may well emerge as the best lead-free fine line circuit finish. Tin is a newer alternative surface finish with many similar characteristics to its silver counterpart. However, there are some health and safety issues to consider, due to the precautions needed with the Thiourea (a suspected carcinogen) used in tin solution during the PCB manufacture.

There are also some concerns over Tin Migration ('Tin Whisker' effect), although the new solutions with anti-migration agents have had very good success in limiting the whisker problem. Proper testing of CAF (Conductive Anode Filament) growth should result in minimal resistance change. The CAF test is 500 hours with bias voltage of 100 volts @ 65˚C and 85% relative humidity, with less than 25 percent drop out of resistance. Immersion Tin is a good fine line surface finish.

Hard and Soft Gold

This is usually plated over electro plated nickel and is a well-tested reliable lead-free finish. There are some problems with gold embrittlement in solder. However, the new lead-free solder has gold in the mix, so it is questionable if the new SCA (Silver Copper Antimony) solder will suffer from gold embrittlement. Hard gold can suffer from slivers in some fine line situations. Soft gold over nickel tracks will solder well and wire bond with gold wire resulting in excellent pull strengths. Most fine line circuits with COB (chip on board) will utilize soft gold over nickel, but gold is expensive.

Palladium

Palladium traces allow for fine line plating as well as excellent solderability. Although palladium is extremely expensive, the overall cost is low because there is very little metal on a typical fine line circuit board. This is very rarely used.

ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold)

ENEPIG is a relatively new surface finish. This surface finish is much more expensive than ENIG but is the only finish that is solderable without creating a brittle solder joint and wire bondable. This is usually used in applications requiring both these features due to its costs. Due to its infrequent usage, most shops in North America subcontract this operation.

EPAG (Electroless Palladium Autocatalytic Gold/ EPIG Electroless Palladium Immersion Gold)

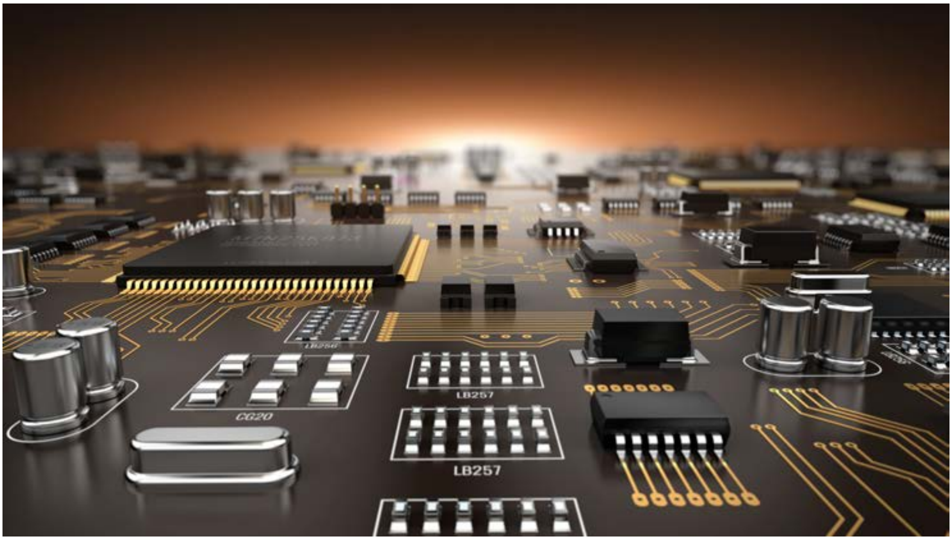
These are newer surface finishes that have been introduced into the market to be a potential replacement for ENEPIG. The process deposits palladium directly on the copper, eliminating the Nickel layer which often creates issues in high frequency applications. The added benefit is that these finishes are intended to be both wire bondable and solderable.

Multiple Surface Finishes

Multiple surface finishes are required on some designs. The manufacturing costs increase significantly when more than two surface finish types are used. Some combinations should not be used together and its best to discuss these situations with your PCB fabricator.

Conclusion

In summary, there is no 'holy grail' of printed circuit board final finish. Each has its own set of issues that will need serious consideration. Some issues are worse than others. All these finishes require adaptation during the process steps to prevent fixture contact reliability issues at electrical test. As a designer if you wonder what surface finish is best for your application, you should work the application engineering team of your PCB fabricator.



Chapter 10

Controlled Impedance

Controlled impedance PCBs are typically used in high frequency applications. In these applications, PCB traces behave differently than just electrical connections. At these higher frequencies, and we need to ensure that signals are not degraded as they route through the PCB. Impedance control should be considered in PCBs used for fast digital applications, telecommunications, computing 100MHz and above, high quality analog video, signal processing and RF communication.

Impedance is measured in Ohms (Ω) but it is not to be confused with resistance, also measured in Ohms (Ω). Resistance is a DC characteristic, while impedance is an AC characteristic which becomes important as the signal frequency increases.

PCBs that contain controlled impedance lines require specific constructions and tighter manufacturing process controls. PCB fabricators tailor the construction, for PCBs requiring impedance, to precisely match the required nominal impedance values. The fabrication drawing should specify the required nominal impedance and tolerance. Data for these designs should separate impedance lines apart from other lines of the same size, as well as lines on other impedance sets with different requirements. This is done commonly by changing the line width of the impedance lines of the same sets by a value of .0001”. This allows PCB fabricators to easily identify impedance lines from others. PCB fabricators will model your requirements and create a construction to meet your impedance re--quirements and should send it to you for your approval.

The primary impedance factors are trace width, copper thickness, dielectric spacing, overall PCB thickness and material requirements. Most fabricators use proprietary impedance modeling software, to determine the specific PCB construction required to produce the specified impedance. The PCB drawing should only specify the nominal impedance, tolerance and nominal line width. This will allow the fabricator to create the most cost-effective PCB material stackup.

Some PCBs require multiple impedance values on the same signal layers. The fabricator needs to have the ability to create impedance coupons to reflect the appropriate model for each impedance requirement. However, testing multiple impedance values on a given signal layer will cause the coupon to be wider than normal. These wider coupons take up additional valuable panel real state, and because of this, designate one target impedance value to be tested per layer whenever possible.

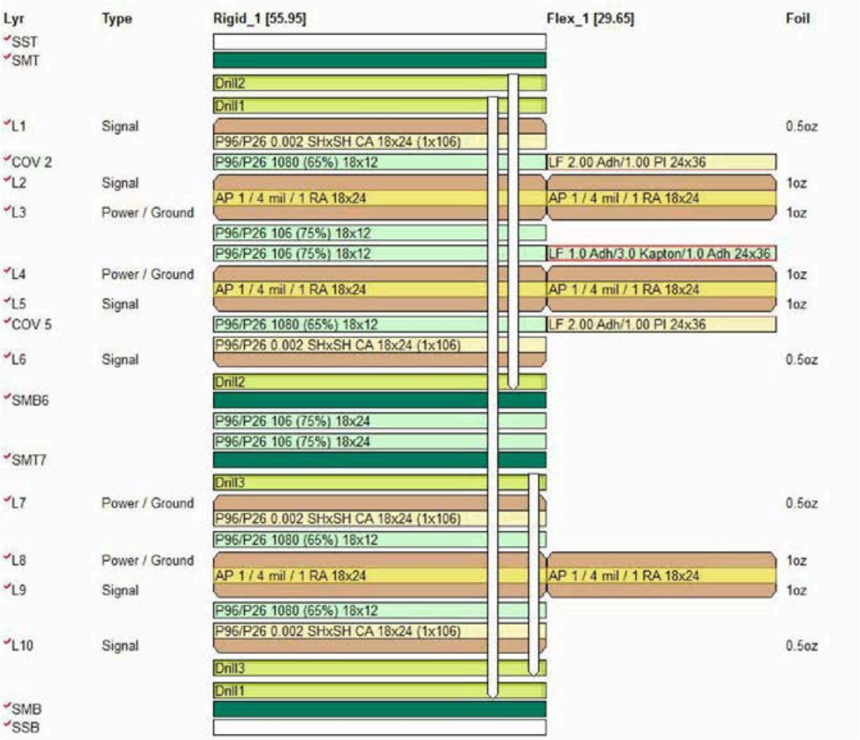
American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

STACKUP & IMPEDANCE REPORT

DFM Engineer:
Parul Patiel

Job Name: **Q7509**
Custiomer: *

Custiomer Required Finished Thickness **47.00 (± 4.70) mils**
Estimatied Finished Thickness **55.95 (Over mask on plated copper)**
Estimatied Over Lam Thickness **40.15**



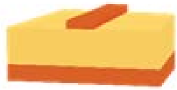
Impedance Table													
Layer	Zone	Req'd Imp (Ohms)	Tolerance (Ohms)	Calc'd Imp (Ohms)	Impedance Type	Upper Ref	Lower Ref	Design L/W (Mil)	Design Space (Mil)	Finished L/W (Mil)	Finished Space (Mil)	CoPlanar Spacing (Mil)	Artwork L/W (Mil)
L9	Flex_1	50.0	±5.0	50.64	se_uncoatied_microstirip	L8	None	8.00	---	8.25	---	---	8.75
L9	Rigid_1	50.0	±5.0	52.73	se_uncoatied_embedded_2b	None	--	7.00	---	8.00	---	---	8.50

Sample of controlled impedance report

The two types of impedance classifications that are generally specified are Single-ended and Differential.

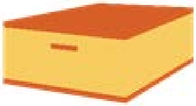
Single-ended Impedance
Single-ended impedance is established by the interaction of a single trace and its reference layer(s). Commonly these reference layers are planes layers. Some examples of single-ended controlled impedance structures:

- Microstrip: a trace on an outer layer with a single reference plane below it.

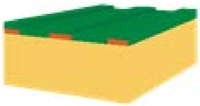


- Embedded Microstrip: a microstrip line that has a di- electric over the top of it; solder mask will change a microstrip into an embedded microstrip line.

- Dual Stripline or Offset Stripline: a stripline, which is sandwiched between two reference planes. It generally is used when two adjacent signal layers are routed orthogonal and have reference planes out- side of them.



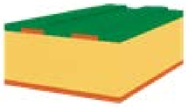
- Coated Coplanar Strip: a single controlled impedance trace with two ground traces of a specified width on either side. All traces are coated with solder-mask.



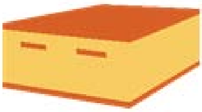
Differential Impedance
Differential impedance is established by the interaction of two traces and their reference layer(s). These reference layers are usually plane layers. The three common basic differential impedance classifications are:

- Edge Coupled Microstrip: comprised of two adjacent traces on an outer layer with a single reference plane below it.

- Edge Coupled Embedded Microstrip: an edge coupled microstrip line that has a dielectric over the top of it; soldermask will change a microstrip into an embedded microstrip line.

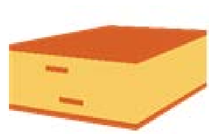


- Edge Coupled Stripline: a configuration with two



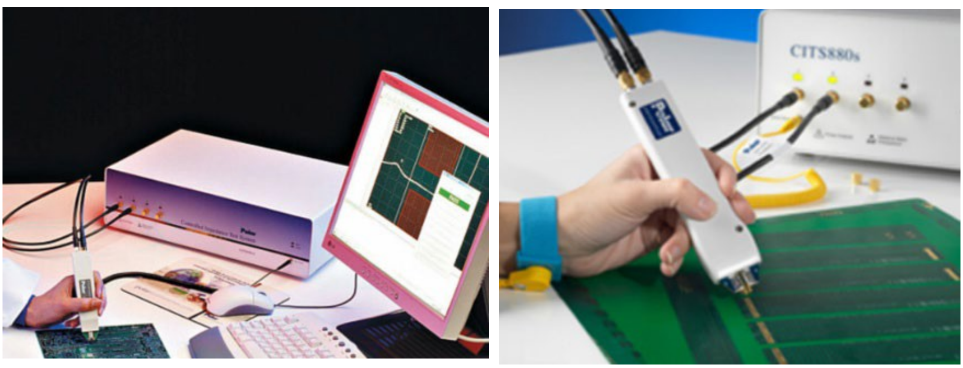
adjacent traces on an internal layer, which is centered between a reference plane above and below it.

- Broadside Coupled Stripline: a configuration with the two differential lines on adjacent layers directly one above the other; these are offset striplines centered between their two reference planes.



Conformance Tests

Most fabricators will test all impedance coupons. Before the impedance has been tested, the coupon and PCB have a serial number marked on them for traceability between the coupon and the board.



Polar Instruments CITS 880s Controlled Impedance Test System

Chapter 11

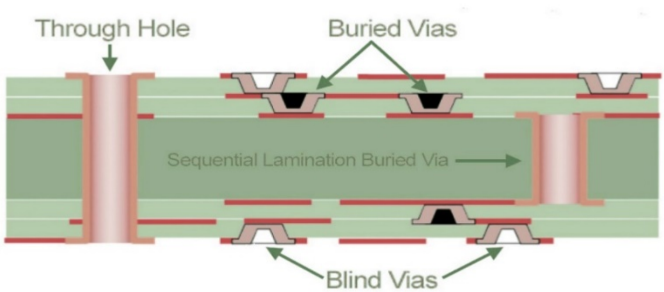
Manufacturing HDI

One of the fastest growing printed circuit technologies over the past decade is high density interconnect (HDI). With the continuum of miniaturization, trace routings and component footprints continue to challenge the available real estate as never before. While there are many contributing factors, microvias are the primary enabling technology to support HDI PCBs.

HDI technology has been around for quite a long time but has now become mainstream as designs become tighter and tighter. HDI is not relegated only to printed circuit boards; HDI advances have also driven changes in electronic components to improve performance and decrease power consumption. Escalating demand for more features in a smaller footprint is driving an exploding need for smaller feature sizes, component geometries and printed circuit boards (PCBs). HDI designs allow for higher circuitry density than traditional technology due to a more concentrated arrangement of smaller components, all in a smaller space. Today's average automobile or smart phone are the electronic poster child for HDI in both PCBs and components.

Microvias

One of the most important technological advancement that made HDI viable was development of the microvia; a very small hole (typically 0.006" or smaller) that only connects certain layers either as "blind" or "buried" via holes. This represents a totally new way of making electrical connections between layers on a PCB. Traditional PCB technology has utilized "through holes", which are drilled through the entire PCB connecting the two outside layers with the internal layers. The ability to strategically connect only certain pads on certain layers greatly reduces the real estate needed for a PCB design and allows a much greater density in a smaller footprint. The figure below shows through holes and buried and blind vias.



Microvias vs. Through Hole Vias

Types of Vias

- Blind Via: Used to connect one surface layer with at least one internal layer.
- Buried Via: Used to create connections of internal layers with no contact to the surface layers.

Mircovia Formation

Microvias can be formed through several methods, primarily mechanical drilling, laser drilling and sequential lamination.

- Mechanical Drilling: Uses traditional drilling equipment to mechanical form holes, but typically limited to 0.006” diameter and dependent on the depth needed.
- Laser Drilling: Special drilling equipment that utilizes a laser to form the hole and can go down to 0.001” in diameter.

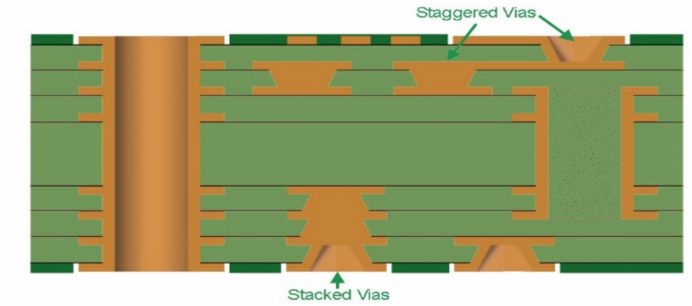
Laser Drilling and CO_2

The UV Yag laser is used to cut through copper and laminate. The first series of pulses removes the top copper. A series of modified lower power pulses or CO_2 pulses ablates the dielectric material with the lower power but does not damage the lower copper landing pad. To utilize a CO_2 laser only, the copper sheet is pre-etched with the vias. The CO_2 laser will not attack copper, only laminate. Any opening in the copper will be laser ablated downward to the copper landing pad below. Most laser ablated holes will have a noticeable taper to the wall.

Sequential Lamination: A process where the microvias are drilled all the way through a sub-panel of the layers that need to be connected by the via, which could require multiple lamination, plating, filling and planarization operations.

Stacked vs. Staggered Microvias

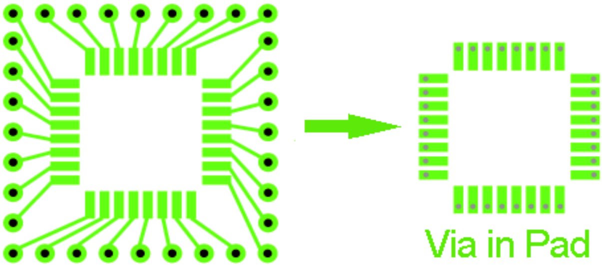
- Stacked: Microvias that are electrically connected and literally stacked vertically on top of each other through various layers of the PCB.
- Staggered: Microvias that are electronically connected and offset to one another through various layers of the PCB.



Staggered & Stacked Microvias

Via-in-Pad Structures

The via-in-pad production process allows you to place vias in the surface of the flat lands on your PCB by plating the via, filling it with one of the various fill types, capping it and, finally, plating over it. Via-in-pad is typically a 10- to 12-step process that requires specialized equipment and skilled technicians. Via-in-pad is often an optimum choice for HDI PCBs because it can simplify thermal management, reduce space requirements and provide one of the shortest ways to bypass capacitors for high-frequency designs.



Transformation of QFP configuration to Via-in-Pad

Via Fill Types

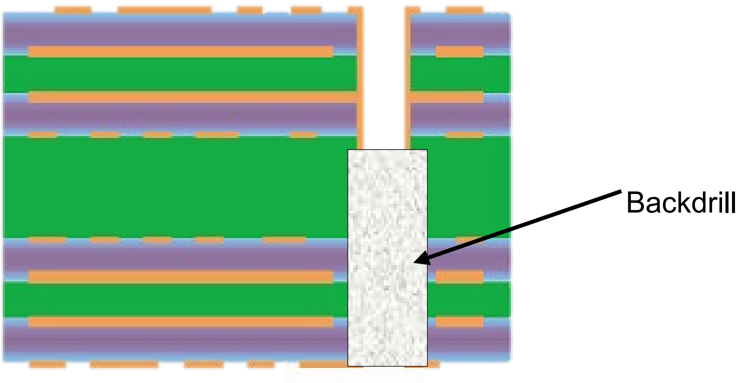
Via fill types should always match your specific application and PCB require-ments. Via fill materials we work with on a regular basis include electrochemi-cal plating, silver-filled, copper-filled, conductive epoxy and nonconductive epoxy. The most common via fill type is nonconductive epoxy. You want to choose a via fill that's flush with the flat land and will solder entirely, just like tra-ditional lands. Fills must allow microvias and standard vias to be blind, buried or drilled, then plated to hide it beneath SMT lands. We often use multiple drill cycles at precisely controlled depths to ensure the drilling process is done right each time. This level of control requires specialized equipment and longer development time.

Back Drilling

Back-drilling is a process to remove the stub, an electrically unnecessary portion of a plated thru hole (PTH) via. It is a post-fabrication drilling process where the back-drilled hole is of larger diameter than the original PTH.

- Reduces a particularly problematic form of signal distortion called deterministic jitter
- Since bit error rate is strongly dependent on deterministic jitter, any reduction in deterministic jitter significantly reduces the overall bit error rate of the interconnect

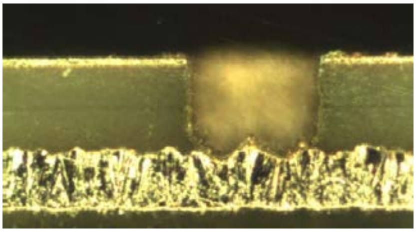
- Less signal attenuation with improved impedance matching
- Minimal design and layout impact
- Reduces EMI/EMC radiation from the stub end
- Lower cost than sequential lamination for limited number of holes

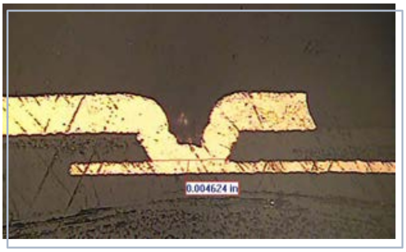


Conclusion

As recently as 10 years ago, HDI was found only in the most expensive designs due to manufacturing complexity, a limited supply base and prohibitive costs. Thanks to advancements in technology, equipment and processing, HDI is readily available to designers today with an ever-expanding base of highly qualified PCB fabricators. HDI applications touch many market segments today, and with the continued miniaturization of the electronics industry there seems to be no end in sight.

Micro laser drilled via





Plated micro via ¼ oz. base copper with 1 mil of copper

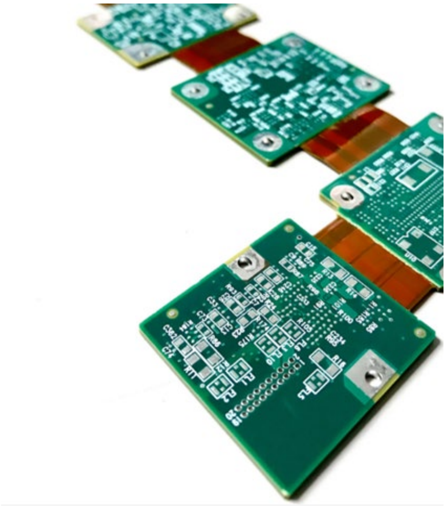
Chapter 12

Flexible / Rigid-Flex PCBs

Flex circuits are printed circuit boards manufactured from material that can bend, fold and twist. Rigid-flex circuits have both a rigid and a flexible component. Rigid-Flex circuits have proven to be among the most versatile and useful electronic interconnection technologies; however, they are also among the most complex.

Why Flex / Rigid-Flex Circuits?

Since their introduction, flexible and rigid-flex circuits have been steadily moving from the fringe of electronic interconnection toward its center. Today flex and rigid-flex circuits are found in countless products from the very simple to the highly complex. The reasons for this shift to the center are numerous and most of them are related to the advantages they offer. An examination of some of the benefits and advantages will make this clear.



They are a remedy to natural product packaging problems. Flexible circuits are often chosen because they help to solve problems related to getting electronics inside the product they serve. They are a true three-dimensional solution that allows electronic components and functional/operation elements (i.e., switches, displays, connectors and the like) to be placed in optimal locations within the product assuring ease of use by the consumer. They can be folded and formed around edges to fit the space allowed without breaking the assembly into discrete pieces.

They help reduce assembly costs. Prior to the broad use of flexible circuits, assemblies were commonly a collection of different circuits and connections. This situation resulted in the purchasing, kitting and assembly of many different parts. By using a flex circuit design, the number of part numbers required for making circuit related interconnections is reduced to one.

They eliminate potential for human error. Because they are designed as an integrated circuit assembly with all interconnections controlled by the design artwork, the potential for human error in making interconnections is eliminated. This is especially true in the cases where discrete wires are used for interconnection.

They can reduce both weight and volume requirements for a product. Flexible circuits are appreciably lighter than their rigid circuit counterparts. Depending on the components used and the exact structure of the assembly and final products, they can save perhaps as much as 60% of the weight and space for the end-product compared to a rigid circuit solution. Additionally, their lower profile can help a designer create a lower profile product than is possible with a nominal 1.5mm thick rigid board.

They facilitate dynamic flexing. Nearly all flexible circuits are designed to be flexed or folded. In some unusual cases, even very thin rigid circuits have been able to serve to a limited degree. However, in the case where dynamic flexing of a circuit is required to meet the objectives of the design, flexible circuits have proven best.

They improve thermal management and are well suited to high temp applications. Not only can they handle the heat, their thinness allows them to dissipate heat better than other thicker and less thermally conductive dielectrics.

They help improve product aesthetics. While aesthetics may seem a low order advantage, people are commonly influenced by visual impressions and frequently make judgements based on those impressions.

They are intrinsically more reliable. Flexible circuits help to reduce the complexity of the assembly and can reduce the number of interconnections that might be otherwise required using solder. Reductions in complexity is a key objective of a reliable design. With respect to the minimization of the number of solder interconnections, reliability engineers know all too well that most failures in electronic systems occur at solder interconnections. It follows naturally that a reduction in the number of opportunities for failure should result in a corresponding increase in product reliability.

In summary, flex and rigid-flex circuits have significant advantages. There are many additional advantages which go beyond the short list provided here. What is important to remember is that most of the advantages stem from the versatility and unique integrative abilities these important members of the electronic inter-connection family can offer. If you have any concerns about your flex / rigid-flex ASC can consult with you or your customer on design related issues.

Materials

Flex and rigid-flex circuits are manufactured using numerous types of materials to meet a wide array of cost targets and performance requirements, both physical and electrical. Because of this variety, relative to the prospective concerns re-lated to each choice, it is vitally important that the designer provide detailed information about the dielectric materials to be used. It is recommended that designers educate themselves about the choices available in terms of cost and performance. The Internet is packed with easily tapped information about flexible circuit materials and how they might be used. The PCB fabricator can also help with this topic. The basic flex material types are:

- Adhesiveless materials, which have no acrylic bonding the copper to the polyimide dielectric.
- Adhesive materials, which have acrylic bonding the copper to the polyimide dielectric.
- Flame retardant and non-flame-retardant laminates, coverlayers, and bond plies.

Adhesiveless Flex Core

Flex Core with Adhesive

Adhesiveless vs Adhesive Flex Cores

The type of copper used most often for flexible circuits is rolled and annealed copper (RA copper), which has the best properties for dynamic flex (repeated bending) applications in the flexible section.

Coverlayers are a polyimide film with B-staged adhesive used to cover and protect the copper traces of the flex circuit. This is a flexible coating of sorts that protect the delicate surface traces from physical damage and potential wicking of solder along circuit traces. The coverlayer offers protection while leaving open access to design features where interconnections are to be made to components by soldering. Coverlayers are available in various thicknesses of polyimide and various thicknesses of adhesive. For example, one can have a 1 mil polyimide coverlayer with a 1 mil adhesive or 2 mils of adhesive. It is important to determine the thickness of the polyimide and adhesive on the coverlayer as a balance needs to be made between allowing for maximum flexibility while also ensuring there is enough adhesive on it to accommodate the copper weight (the more adhesive, the less flexible).

Some one or two-layer flex circuits that will not be subject to multiple flex cycles or extreme radius bends can be coated with an epoxy-based solder mask that is designed to flex without cracking. However, this is not recommended when the design requires any dynamic or extreme flexing. The other option is a laminated flex coverlayer. These are typically materials that have a makeup that is identical to the flex core material and are best suited for dynamic flexible circuit applicaions.

Front-End Engineering

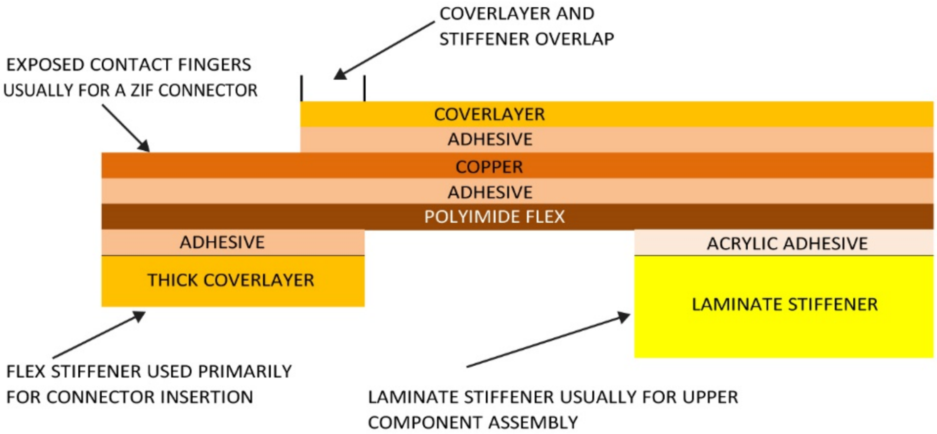
It is important to understand that it takes a lot longer to engineer flex and rigid-flex boards than it does rigid boards of similar layer count. While there are many process similarities, there are many other unique design and processing attributes that contribute to added engineering time.

Single-Sided Flex

Single-sided flex circuits are manufactured by starting with a pre-pressed and glued sheet of a thin polyimide or polyester with a copper outer layer. The circuit formation is like the single-sided rigid PCBs. The panel is cleaned, dry film resist laminated and then exposed with a negative image of the circuit pattern. Then it is developed to remove unwanted dry film and etched to remove the copper between the tracks. The remaining dry film protecting the tracks is stripped. If required, a coverlayer is pre-drilled and then laminated over the copper side. The coverlayer performs the same function as solder mask does in rigid PCBs. As an alternative, a flexible solder mask may be used but it does have certain limitations. The panel is silk screened with a flexible white marking ink, die cut or laser routed, inspected and shipped.

Options for all types of flex circuits include silver ink, which is screened onto the flex circuit to act as an electrical shield and/or the addition of FR4, polyimide or metal stiffeners, which are added after the panel is die cut, using 3M double sided tape or epoxy glue. Stiffeners may also be attached using prepreg under temper-ature and pressure. Some fabricators of high volume, single-sided, flex circuits have set up all the production machinery in one long line and make thousands of single-sided flex circuits per hour, using flex material in long rolls.

Process Flow for Single Sided Flex



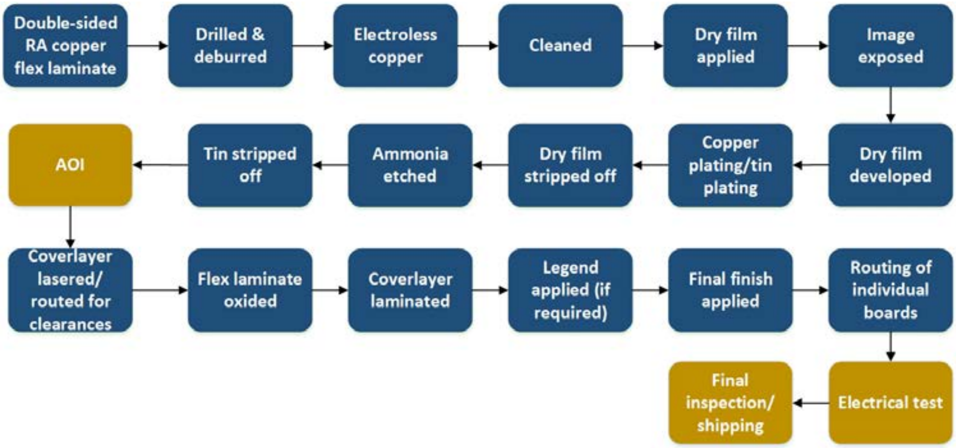
A Single-Sided Board with Different Kinds of Stiffeners

Double-Sided Flex

A double-sided flex circuit would consist of flexible polyimide cores usually from 1-5 mils thick and copper weights per the customer specification.

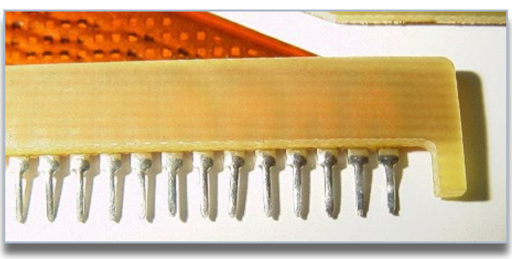
The process of forming the circuits is like a double-sided rigid PCB. The bare polyimide, copper-coated sheet is drilled, and any slots or mechanical features are machined into its surface. The surface and holes are made conductive by conventional through hole plating with an electroless copper bath. A layer of photosensitive dry film is laminated onto both the copper surfaces. The image of the top and bottom layers is applied to the dry film using either laser direct imaging or a UV light source. The exposed circuitry design will cross-link and become quite solid in nature. By developing in a mild alkaline solution, sprayed under pressure, the soft unexposed areas will be washed away. The now defined circuit image is plated with copper to the desired thickness. Some plating options are to button plate the via only leaving the special flexible RA (rolled and annealed) copper for the flex portion of the circuit unplated. A thin layer of tin is added to protect the plated copper circuits from the etchant. The dry film is now stripped. Then the panel is cleaned and washed. The non-plated base copper is etched away with ammonia etchant. The traces are pro-tected from the etchant by the tin plating. The protective plated tin surface is removed with a nitric acid-based solution and the board is washed and dried. A copper pattern closely following the desired shape is now prominent on the surface.

A pre-drilled (either CNC drilled or laser depending on the size of the openings) coverlayer is laminated to each side with a hydraulic press or a flexible liquid photoimageable solder mask is applied, exposed, developed and cured. A legend ink is screened onto the panel and cured. A surface finish like rigid PCB is then applied to the flex circuit to protect the copper before soldering and assembly. The circuit is die cut, laser cut, or routed to size, with any large unplated holes also drilled/cut at this time. The circuit is then electrically tested, inspected and shipped.



Process Flow for Double Sided Flex

Some flex circuit boards may require stiffeners. Stiffeners are typically either FR4, polyimide or in some cases aluminum. The materials are pre-routed on CNC machines. The stiffener can be any desired thickness, either just to strengthen a part or to really secure the circuit to something. The 3M double-sided pressure sensitive adhesive (PSA) used to secure the stiffener, is quite strong and permanent. Also, some stiffeners are bonded to the flex circuit via a press utilizing higher temperature and pressure.



Routed FR4 stiffener

Polyimide stiffener

Multilayer Flex

To manufacture multilayer flex boards, the inner layers are made first using standard Polyimide with copper on both sides. Forming the circuit on the inner layers is again like rigid inner layer process. The biggest difference is that these layers is again like rigid inner layer process. The biggest difference is that these cores are more difficult to handle since they are typically flimsy compared to rigid cores. So, handling and processing through equipment becomes far more challenging and the manufacturing process needs to be set up to handle this.

The panel is cleaned and laminated with etch resist dry film. The dry filmed panels are then exposed using either laser direct imaging or photo tools and developed. The negative dry film image acts as an etch resist, which results in the etch removing the unwanted copper. The dry film is then stripped. The inner layers then go to AOI prior to further processing.

The boards are then baked to remove any moisture. The amount of adhesive used to bond the flex layers together is dependent on the inner layer copper weight.

The layers are then aligned with tooling holes and put on pins that are in the lamination plates and pressed together in a vacuum hydraulic press. The temperature, time, and pressure are determined based on the panel size and the material suppliers' specifications. The press package typically has special padding that conforms to the flex panels to assist with adhesive conformation and air removal. After the board is pressed and the flash trimmed, the panel is processed as a normal, double-sided board.

The bare copper laminated board is drilled, and any slots or mechanical features are machined into its surface. A cleaning etch plasma cycle is performed to promote copper adhesion to the hole wall. The panel is then cleaned to remove any ash created by the plasma before electroless plating. The holes are made conductive by conventional through hole plating with an electroless copper bath or carbon process. A layer of photosensitive dry film is laminated onto both the outer copper surfaces. The outer layer images are exposed using either laser direct imaging (LDI) or photo tools. By developing in a mild alkaline solution and spraying under pressure, the soft unexposed areas will be washed away. The now defined negative circuit image is plated with copper until the total thickness is 1 oz. or as specified in the drawings. A thin layer of tin is added to protect the plated copper circuits from the etchant. The dry film is removed by a strong alkaline solution and then the panel is cleaned and washed. The non-plated base copper is now etched with ammonia etchant. The circuit trace is protected by the tin plating. The protective plated tin surface is removed with a nitric acid-based solution and the board is washed and dried. A copper pattern exactly following the desired shape is now prominent on the surfaces. The outer layer circuitry is now automated optical inspected (AOI).

A pre-drilled polyimide coverlayer is laminated onto each side of the etched panel to protect and seal the circuitry. Alternatively, a flexible liquid photoimageable solder mask is applied, imaged, developed and cured. If required, a flexible legend ink is screened onto the panel and cured. The desired final finish is then applied to the panel.

The circuit is die cut, mechanically routed or laser routed to size with any large unplated holes also drilled or cut at this time. The circuit is then electrically tested, inspected and shipped. Some flex circuits use silver ink to provide electrical shielding or assist in controlling bend areas. It can be applied to the panel on top of the coverlayer. A FR4 or polyimide stiffener can be applied to improve tear resistance and assist assembly.

Rigid-Flex Manufacturing

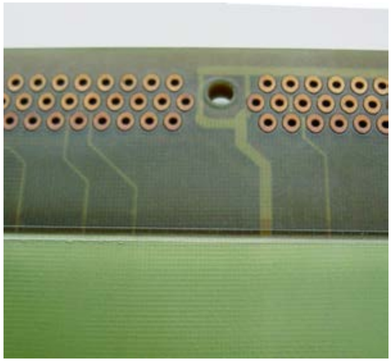
When manufacturing rigid/flex boards, special engineering consideration must be spent on how to section and release the non-circuit areas between the rigid and flex sections. The design calls for a rigid section comprised of FR4 or other rigid material and a section of flex that will extend from the main circuit. How the different areas separate is important. Many methods, such as Teflon blocks or polyolefin release sheets, allow areas of rigid and flex to be separate within the press package. Using a simple example of a 4-layer rigid flex with a double-side flex core. The flex arms that extend off the rigid board cannot adhere the FR4 sheets on top of the flex arms. The low flow prepreg is pre-routed to only cover over the FR4 board and not the flex extension arms. To facilitate final routing, the FR4 is pre-routed with a slot at the join line of the flex and rigid parts. When the board is routed, the slot facilitates the router not passing over or through the join area. To assist in removing the top FR4 layer, it can alternately be scored on the underside before pressing.

Panels can have cut outs in the inner layer filled with a Teflon plug, allowing even pressure from the laminating press but will not stick to either the FR4 or flex adhesive material. Polyimide core bonds to FR4 with prepreg or adhesive sheets providing a superior high strength joint. Expansion difference between flex and rigid sections is a problem for registration. CAD package manipulation is needed to scale and align the layers after processing and pressing.

Design time for rigid/flex is considerably more because of the engineering required to ensure the parts will separate and correctly align to the fingers of flex which extend from the main board to the sub boards.

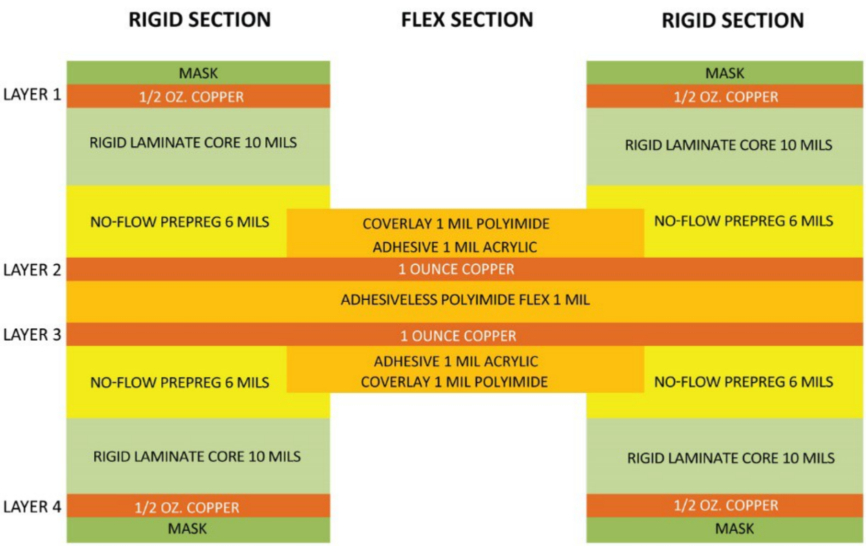
The drilling, electroless plating process all works with the materials normally used in rigid flex. A plasma etch cycle is done prior to electroless copper to prepare the hole.

Problems exist with trying to obtain a smooth transition from rigid to flex. Some fabricators seal this joint with a strain relief material, to add strength and cosmetically hide the joint. During the design phase, talk with your PCB fabricator to determine the best way to produce the board.



Rigid flex joint

Typically, the flex circuits are the inner two of the four layers, but it is possible to build flex as the outer layers. In the design of the layup and release sheet management you must solve how to mill out the FR4 inner section that's not used.

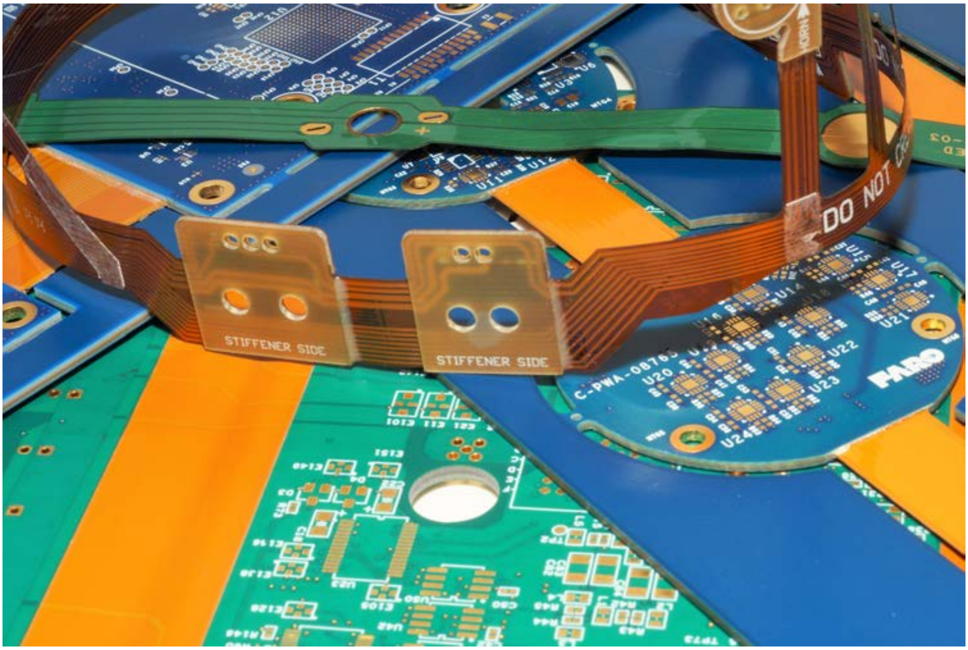


Sample 4 Layer Rigid-Flex Construction

When designs utilize un-bonded multiple flex layers in parallel, pre-routed cover layers are required to keep the polyimide layers from adhering to one another.

Process flow for a 4-layer rigid flex

It is possible to make individual multiple flex layers increasingly longer. This creates the proper radius and eliminates the stress. When a 4-6-layer flex arm area bends, it compresses the inner arms and expands the outer arms. By making each flex layer in the lamination package successively longer and pressing the package with expansion areas, the arms will be longer toward the outside of the bend. This is typically called a book binder flex and is much more expensive than a rigid-flex where all the flex layers are the same length.



Scan Here to download our book "The Printed Circuit Designers Guide to™ … Flex and Rigid-Flex Fundamentals" free or go to www.i007ebooks.com/flex

Chapter 13

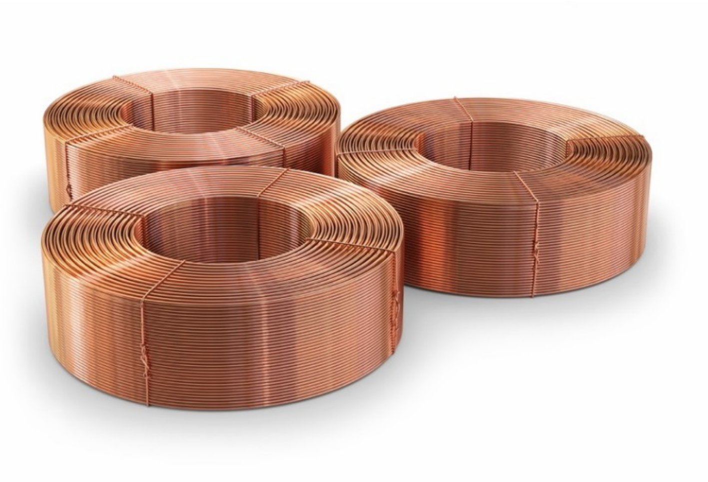
Heavy Copper PCBs

Increase In Demand

A growing trend in the printed circuit industry is creating an escalating demand for heavy copper printed circuit boards, powered (pun intended) by new technology in the automotive, computer, industrial control and MilAero market sectors. The driver behind this demand is the continuing increase in power requirements and the elimination of complex wired buss configurations. This increased demand is creating a supply issue as more than 80% of the existing printed circuit board manufacturing companies are not capable of producing reliable heavy copper printed circuit boards in volume.

How Heavy is Heavy Copper?

Most commercially available printed circuit boards are manufactured for low voltage/low power applications, using copper traces & planes made up of copper weights ranging from 1/4 oz/ft2 to 3 oz/ft2 on both inner layers and the outer layer finished surface. Heavy copper is then generally defined as any-thing greater than 3 oz, with some power designs routinely calling for 15 – 20 oz of solid copper. Copper weights above 20 oz/ft2 and up to 200 oz/ft2 are also possible and are often referred to as Extreme Copper. Thermal management is more important than ever in today’s new designs as electronics are used in demanding environments and operate at higher currents. Heavy copper PCBs can help conduct heat away from components, so failure is great-ly reduced. These heavy copper PCBs conduct electricity better and are more capable of withstanding the increased thermal stress while under power.



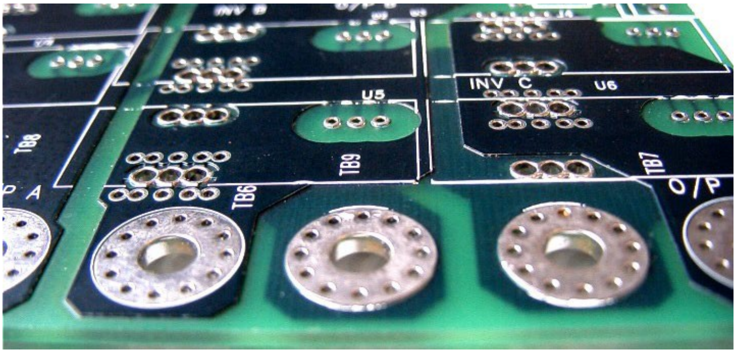
Top 10 Applications of Heavy Copper PCBs

1. Solar power converters
2. Electric vehicle charging (commercial and industrial)
3. Safety and signal systems
4. Power line monitors & UPS systems
5. Weapons & radar control systems
6. Traction converters for rail applications
7. Power grid switching systems & backup
8. Renewable energies and storage pumping plants
9. Overload & protection relays
10. HVAC systems

The Cons

Heavy Copper Requires Unique Processes

The key to successful heavy copper printed designs is choosing the right PCB manufacturer. Fabricating heavy copper printed circuit boards requires a major change in processing for most manufacturers, and in some cases, also requires specialized equipment. The obvious challenges are plating and etching as the process guidelines for traditional copper weights can be thrown out the window. Manufacturing with normal etching methods do not work for heavy copper, as they tend to produce uneven edge lines and over-etched trace margins. Fabricators have evolved advanced plating and etching techniques to obtain straight edges and optimally etched margins with processes like high-speed/step plating and differential etching.



12 oz. heavy copper board, with extra holes to increase thermal transfer

Fabrication Challenges:

- The etching process is difficult & slow
- Reduced yields and increased throughput time

- Increased opportunity for delamination & misregistration
- Huge amounts of copper need to be removed & disposed of during the etching process
- Lamination process requires the use of prepregs with very high resin content to incapsulate the heavy copper traces
- Heavy copper traces on the outer layers makes the surface uneven and it is difficult to print solder mask and legend on the uneven surfaces (may require multiple applications)
- Coexisting heavy copper traces and standard copper finer lines for digital control is difficult to control

Cost

Copper is expensive, and when you are talking heavy copper the cost increase becomes a significant portion of the overall price of the PCB. In the case of extreme copper designs, the cost of copper can be 200x the cost of a traditional PCB. The substrate material of the PCB is another factor that must be considered as a laminate with a very high glass transition temperatures (Tg) may be required to support the power and thermal requirements of the design. Along with Tg, the coefficient of thermal expansion (CTE) between copper and the substrate material must also be considered, as thermal stresses generated by high currents through traces may lead to cracks, layer separation and ultimately PCB failure.

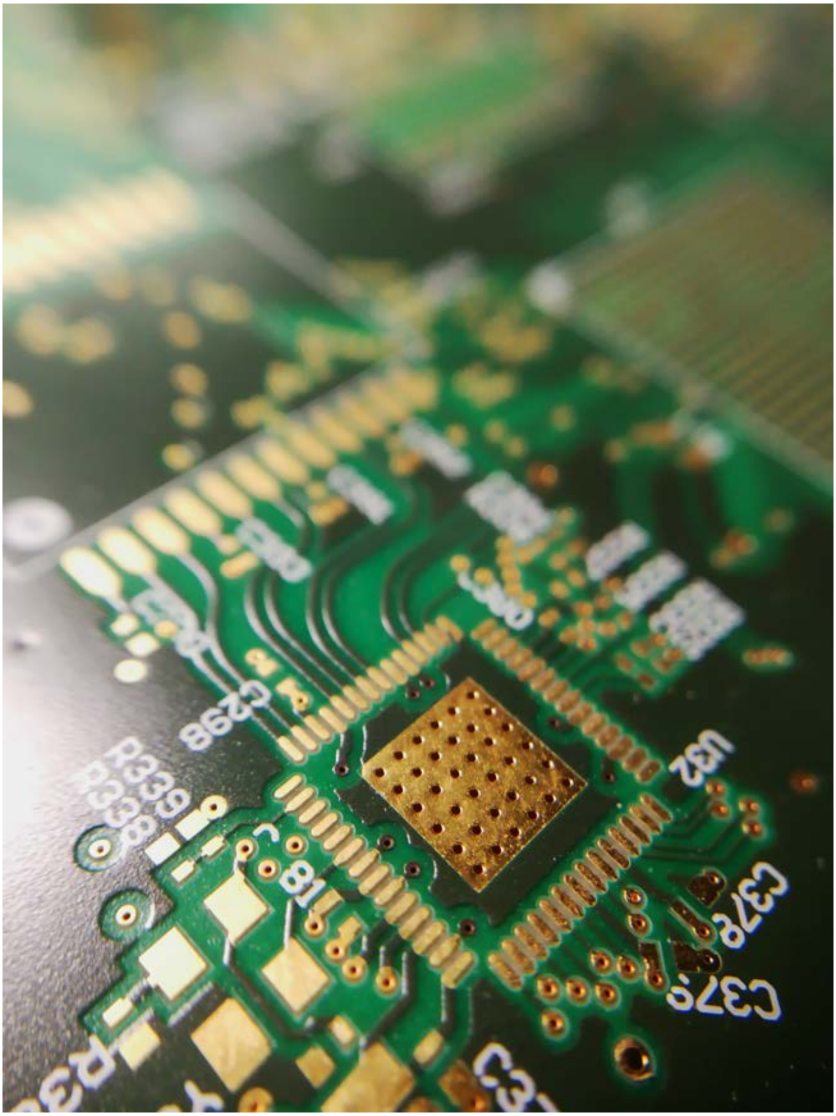
Pros

The primary benefits of using heavy copper PCBs revolve around thermal management and current carrying capability. The list below is not all-inclusive but provides a snapshot of the variety of benefits that using a heavy copper PCB can provide.

- Increased endurance to thermal stress & cycling
- Ability to perform in high temperature operating environments
- Increased current carrying capacity
- Increased mechanical strength at connector sites and in PTH holes
- Utilization of high temperature materials to their full potential without circuit failure
- Reduced product size by incorporating multiple copper weights on the same layer of circuitry
- Heavy copper plated vias carry higher current through the board and help to transfer heat to an external heatsink
- On-board heatsinks directly plated onto the board surface using up to oz copper planes
- On-board high-power-density planar transformers

Conclusion

With the ever increasing thermal and power requirements showing no sign of slowing down, the demand for heavy, and extreme, copper printed circuit boards will certainly follow this trend. Selecting a printed circuit fabricator that routinely produces this technology and has invested in the required processes and equipment is critical to success.



Chapter 14

RF/Microwave Circuits

RF technology is rapidly growing business. Demand for RF and microwave modules have been on a meteoric rise for a while now, resulting in a multibillion-dollar market. In today's 24/7/365 connected world, RF powers our wireless networks, cell phones, smart TVs, and tablets. We can even check what's in our refrigerator from the grocery store and adjust the lights and temperature in our homes while on vacation courtesy of RF technology! RF is how the world works today, and printed circuit boards are the backbone of this technology. This is especially true with the advent of new 5G technologies.

Material Selection

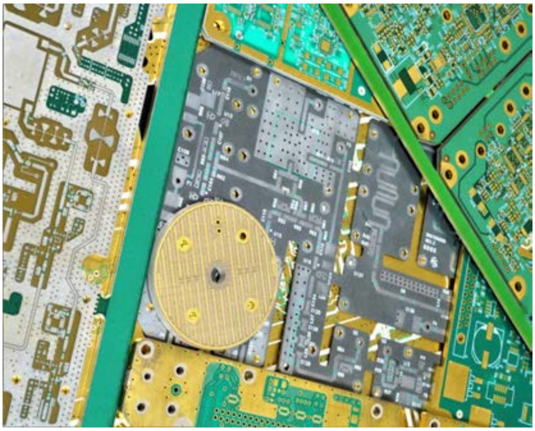
Choosing the right material for RF/Microwave applications is perhaps the most critical decision that will determine the success of the project. When discussing the right choice for materials to use in designs, today's engineers are much more knowledgeable than they were during the early years of RF PCB technology. At that time, there were only a couple options of low-loss Teflon materials, and most of them contained the word Duroid. Today, there are literally dozens of controlled-Dk and low-loss materials available on the market, many of which contain proprietary resin systems that allow the PCB fabricator to manufacture them using similar processes to standard FR-4 materials.

Key RF Parameteres

RF/Microwave circuits usually process precision and/or low-level signal transmissions, which means that these circuits require much tighter control of parameters relating to signal loss. The two greatest concerns are losses caused by signal reflections due to impedance mismatch (loss tangent) and signal energy loss into the dielectric of the material (Dielectric Constant). The material choice (laminate and copper) can have a major impact on all these sources of energy loss. As a result, materials geared to the RF arena tightly control these two key parameters.

Loss Tangent: As loss tangent results from impedance mismatch, it is important to fully understand how much loss a design can tolerate, or in other words, how much power in versus how much power out.

With an infinite supply of power, loss is unimportant. Adjustments can always be made to compensate for the loss of the materials or conductors. The exception to this is in the heat generated by conductor and return losses, but fortunately this is seldom a reality.



Dielectric Constant: The critical consideration here is understanding the required dielectric material thickness and conductor width needed to achieve a given impedance value. This turns into a copper loss and power handling issue. The secondary issue is the ability to dissipate the heat that occurs both at the power devices and in the conductors. This heat needs to be transmitted somewhere (the PCB itself) and the materials need to be of a low enough dielectric constant or have thick enough conductor widths to carry whatever power the circuitry requires. A careful con- sideration of these two parameters will provide guidance to the proper material type and thickness required for the PCB being designed.

Dimensional Stability: Another aspect that needs to be carefully considered when making selections for an RF/Microwave PCB is an understanding of how various materials react under operating conditions (dimensional stability). There are three types of materials related to dimensional stability that need to be considered:

- Homogeneous: Material of uniform composition throughout that cannot be mechanically separated into different materials such as plastic, glass, and/or resin.
- Isotropic: Material with properties that are equal in all directions (X, Y, and Z), such as glass microfiber RT/duroid®.
- Anisotropic: Material with properties that might vary depending on direction, such as woven glass fabric in traditional FR-4 and certain glass fabric-reinforced PTFE materials.

There is no right or wrong material type; the key is matching the proper material type for the RF/Microwave application.

Copper Surface Roughness

In high-frequency signals, the current in the PCB copper circuit is concentrated within a small depth near its surface, which is referred to as the “skin depth”. Skin depth is a measure of how (and where) electrical conduction takes place in a conductor and is strictly a function of frequency. One common misconception about skin depth is about which surface of a conductor is carrying the RF current. In most cases all four outer sides carry the current, the bottom the most, the top less and the sides even less.

Circuit conduction occurs at the surface nearest the dielectric from which the electromagnetic wave propagates; in other words, the bottom copper surface that is against the laminate in a microstrip design.

There are 4 primary methods for producing copper for laminate, with each having copper roughness pros and cons that need to be matched to the applica-tion. These methods are ED (electrodeposited), Reverse Treated, VLP (very low-profile) and RA (rolled annealed). All of these have specific tradeoffs between adhesion and conductor loss.

***Electrodeposited*:** Formed by electrolytic deposition onto a slowly rotating polished drum from a copper-sulfate solution. The side against the drum provides the smoother finish.
***Reverse Treat*:** Electrodeposited foils that have had subsequent treatment of the smooth side of the copper are referred to as reverse treated foil (RTF). These treatments are very thin, rough coatings that improve adhesion.
***Very Low-Profile*:** Extremely smooth copper foil is called very low-profile (VLP), which has a greatly reduced surface roughness. Again, care should be taken when evaluating the adhesion of this method for the specific application.
***Rolled Annealed*:** Rolled annealed (RA) copper foils are created by successively passing an ingot of solid copper through a rolling mill, and then applying high temperature to anneal, or strengthen, the copper.

RF Layer Stakeup (Pure Build Verus Hybrid Build)
The term, “Pure build” refers to a multilayer PCB material construction that is composed of the same type of material throughout the stackup, such as a construction entirely of FR-4, PTFE, or another high-frequency material. A “hybrid build” multilayer PCB uses materials with significantly different critical properties than those associated with a traditional pure multilayer PCB. A hybrid could use a mix of FR-4 materials with high-frequency materials, or a mix of high-frequency materials with different dielectric constants, etc. Cost is the key differentiator, and the more RF material used in the stackup, the higher the cost.

Regardless of the material used, maintaining a balanced construction (layup, stackup, etc.) in relation to the z-axis median of the board will ensure minimum bow and twist. This balance includes the following: dielectric thickness of layers, copper thickness of layers, distribution and location of circuits, and plane layers.

Whenever possible, planes should be balanced around the z-axis median line of the layup and ideally located internal to the board.

Stripline and Microstrip Structures: The two most common RF/microwave transmission-line formats are microstrip and stripline. The decision on which transmission line technology should be used is based on several factors, including expected performance and ease of implementation. RF PCB designers need to recognize the differences between the two technologies to be able to select the right approach.

A stripline is a high-frequency transmission-line technology that is essentially a conductor on an internal layer that has a ground plane above and below it. Due to being surrounded by insulator (dielectric) material, stripline transmission lines do not radiate and are described as being non-dispersive. Because of this, stripline circuits can be closely spaced and densely packed, thus lending themselves to miniaturization at microwave frequencies.

A microstrip high-frequency transmission-line technology is a simpler structure with a single ground plane, conductor and dielectric layer separating the signal conductor and ground plane. Since a microstrip is not insulated with dielectric, it tends to radiate more with increased spacing between the transmission lines and the ground plane. As a result, microstrip is often a favored transmission-line format for radiating structures, such as miniature microstrip patch antennas.

Conclusion

Today's RF/microwave designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing RF/microwave PCBs. In addition to the traditional military/aerospace, medical, and telecom applications, the explosion of wireless technologies in all aspects of our lives and businesses will ensure the need for high-frequency PBCs will continue to grow exponentially.

Chapter 15

Thermal Management and RF/Microwave Technology

Rapid advances in the use of RF/Microwave frequency bands have forced increased density of RF/microwave devices to achieve escalating frequencies to support the "smaller, faster, cheaper" design evolution. These constraints require efficient thermal management. Thermal management plays a very important role in the design of RF/microwave electronic devices. A large quantity of heat is generated when signals are processed in high-frequency applications, particularly in the amplification of high frequency signals. Reliable performance of an RF/microwave device depends on maintaining a constant value of the dielectric constant of the PCBs dielectric layer.

The dielectric constant varies as a function of temperature and it will have a direct impact on the high-frequency performance of the circuit since changes in the dielectric constant will result in changes in the RF/microwave circuit impedance. Variation in dielectric constant occurs because any rise in temperature results in an increase of thermal conductivity and, consequently, a decrease in the dielectric constant (since the dielectric constant is inversely proportional to the thermal conductivity. Tightly controlling the thermal coefficient of dielectric constant and coefficient of thermal expansion (CTE) characteristics of the PCB material is required to ensure signal and power level performance.

Thermal management of an RF/microwave component, circuit, or system is simply a matter of removing heat from sensitive areas of a design that can suffer damage or performance degradation from the heat. This article primarily focuses on the different methods of using metal to enable improvements in thermal management. It is also important to understand that apart from the thermal management function, the metal also acts as a grounding (plane) layer. The heat sinks and PCBs are typically connected thermally and electrically, utilizing the metal heat sink to control thermal dissipation and grounding of circuits.

At a high level, there are two ways to achieve thermal management of RF PCBs utilizing metal. The first is pre-bonded and the second is post-bonded. Pre-bonded laminate has a cost premium and is typically single-sided, although **ASC has a proprietary capability** to pre-bond within a multilayer. Contact ASC for additional information. In a pre-bonded circuit board, the PCB supplier buys the laminate material pre-bonded to the metal. The post-bonded process is the most common in multilayer applications. Most of the available RF/microwave laminate materials can also be bought in a pre-bonded configuration. The two laminate suppliers that have most of this market are Rogers and Taconic. The PCB fabricator is then tasked with processing this material, making circuits and machining the metal. In a post-bonded circuit, the PCB supplier manufactures the PCB and the metal concurrently and separately, and then bonds the two together using a variety of methods.

Bonding Options

There are several pros and cons of the various methods. Pre-bonded PCBs are typically used in high reliability, military, aviation, and telecom applications since they offer precise dielectric constant control, no risk of delamination and high reliability. The two disadvantages of this methodology are that it is restricted to a single layer of circuitry, and in general costs tend to be significantly higher with pre-bonded vs. post-bonded largely because of the premium price and increased risk of processing low loss materials in conjunction with a thick metal layer. Simply put, the costs are higher because the laminate materials are significantly more expensive, processing is more challenging, and any yield issues result in very expensive scrap. There are cases where pre-bonded PCBs can be converted to post-bonded PCBs for a cost reduction. Any multilayer applications that require metal for thermal management will need to utilize post-bonding.

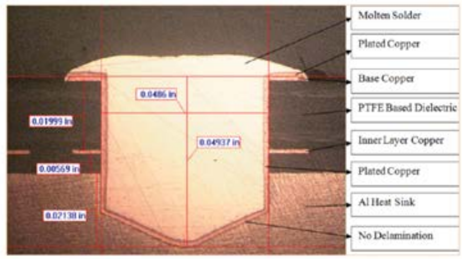
Pre-Bonded Laminates

There are several design parameters that need to be considered, starting with the laminate selection. The first step is to determine dielectric material, dielectric thickness and the copper foil weight appropriate for the design application. The next step is to determine the thickness and type of metal to be used. The typical metals used are Aluminum 6061-T6 and Copper C110, but depending on the ap- plication, Brass may be used. Again, a cost-benefit balance must be considered as Aluminum is lighter and cheaper than copper, but more difficult for the PCB fabricator to process in pre-bonded applications.

Pre-Bonded Laminate

Heat Dissipation

Post-bonding dissipates heat through the mechanical connection between the bottom side PCB ground plane and the heat sink. This is more challenging as dissipation is dependent on the integrity of the bonding material. The pre-bonding method uses a blind via process, which requires some special equipment and processes, but results in a more robust thermal management solution.



Cross-section of Solder Stressed Blind Hole

Post-Bonding

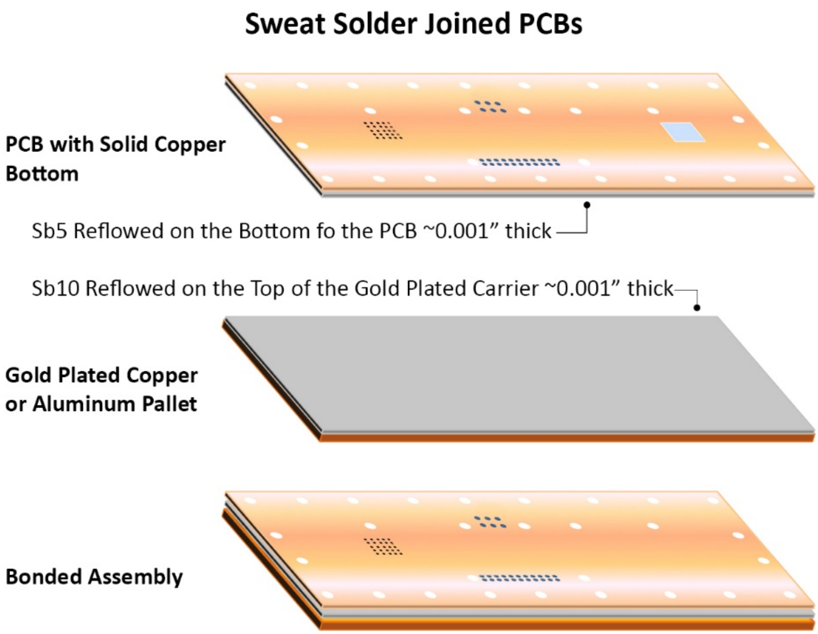
In a post-bonded application, a double-sided PCB or a multilayer PCB is manufactured first. Typically, the bottom layer is mainly a ground layer or occasionally contains a few circuits. While the PCB is being manufactured, the metal can be simultaneously machined on a CNC machining center. There is more flexibility in terms of the shape and features in a post-bonded application and allows for the metal to be plated independently of the PCB. The form factor of the metal can be quite different than the PCB. Once the PCB and metal are completely manufactured, they can be bonded together. This is typically done in piece form (i.e. a single-up PCB bonded to the metal). However, there are some special applications where multiple PCBs may be bonded to the same piece of metal. Since the bonding is done post PCB processing, these different PCBs do not need to be the same material set or thickness.

PCBs are typically post-bonded using one of two methods; sweat solder or sheet film adhesive. A custom bonding fixture will be required to ensure registration between the PCB and the metal carrier, and to control the pressure being applied in the bonding process.

	BONDING MEDIUM	FIXTURE TYPE	REGISTRATION	Preferred Hole size
Electrically & Thermally Conductive	Electrasil-1 & -2	High Temp FR4, Polyimide, or Metal Al 6061	2 diagonal holes preferably 3 holes at outermost edge of the part	.125" or larger
	CF3350/Ablefilm	High Temp FR4, Polyimide, or Metal Al 6061	2 diagonal holes preferably 3 holes at outermost edge of the part	.125" or larger
	Sweat Solder	Metal-AL 6061	Scattered holes throughout the part as equally distributed as possible for even pressure distribution.	2-56 or 4-40 tapped

Typically, the “bottom” layer is primarily a ground layer and has no or very little solder mask. The bonding techniques are as follows:

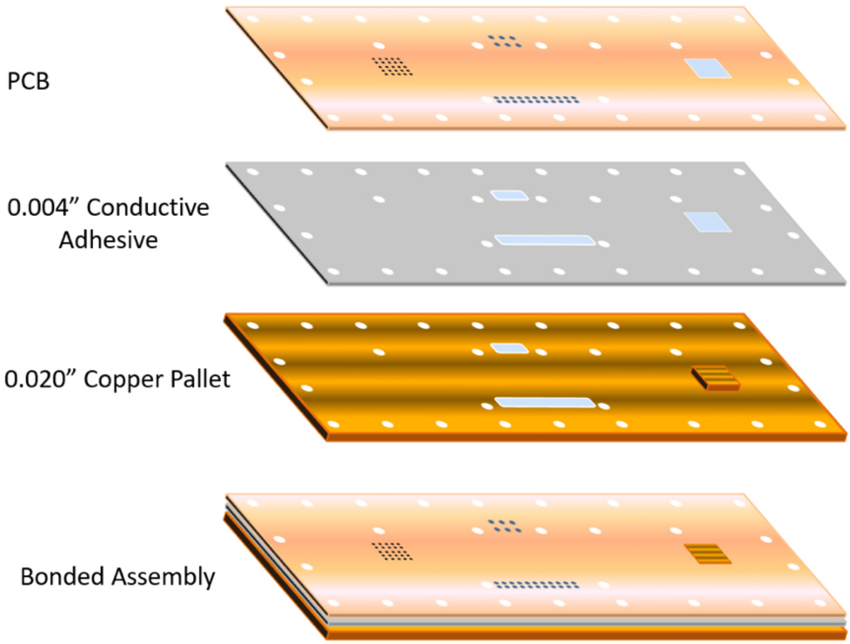
- Sweat Solder: High temperature solder is used to bond the PCB to the metal. The solder used is such that there is no risk of de-bonding in subsequent assembly soldering operations. One of the biggest discussions associated with this technique is void volume. Since the solder paste is a mixture of flux plus solder, as the flux volatizes it creates air gaps. Below shows conceptually how a sweat solder board is put together.



- Sheet Film Adhesive: Silver filled conductive epoxy films are commercially available, some examples are CF3350 and Ablefilm 5025E™. The PCB and metal are bonded using temperature and pressure with a sheet film adhesive.

- Silver filled conductive silicone films: These are patented ASC materials (US patents 7527873 and 7867353) and have some differences from the commercially available materials. The PCB and metal are bonded using temperature and pressure with a sheet film adhesive.

Below shows how a sheet film bonded assembly is put together.



Conclusion

Today’s RF/microwave designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing RF/microwave PCBs.

In addition to the traditional mil/aero, medical and telecom applications, the explosion of wireless technologies in all aspects of our lives and businesses will assure the need for high frequency PCBs will continue to grow exponentially.

Chapter 16

Thermal PCBs

There are several different options that a designer may choose to help them dissipate the heat generated by the various components on the PCBs. This chapter primarily focuses on options in the non-RF / Microwave area that utilize metal attached directly to the PCB during the PCB manufacturing process to help with the heat dissipation process.

When metal is attached to the PCB, the bonding material is thermally conductive and electrically isolative (Insulated Metal PCBs or Metal Core PCBs).

Some applications of IMPCBs are:

Power Conversion: Thermal clad laminate offers a variety of thermal performances, is compatible with mechanical fasteners and is highly reliable.
LEDs: Using thermal clad PCBs assures the lowest possible operating temperatures and maximum brightness, color and life.
Motor Drives: Thermal clad dielectric choices provide the electrical isolation needed to meet operating parameters and safety agency test requirements.
Solid State Relays: Thermal clad laminate offers a thermally efficient and mechanically robust substrate.
Automotive: The automotive industry uses thermal clad boards as they offer long-term reliability under high operating temperatures coupled with their requirement of effective space utilization.

Single-Sided IMPCBs

In its simplest form an IMPCB is copper foil that is bonded to a thermally conductive dielectric and a metal substrate. Typically, a PCB supplier can buy the copper foil laminated to the base metal from several different laminate fabricators.

Single Sided IMPCB Laminate

The copper foil thickness most commonly used are 1 and 2 oz. The thicker the copper the more expensive the cost of the PCB. ASC has seen some designs with up to 6oz of copper.

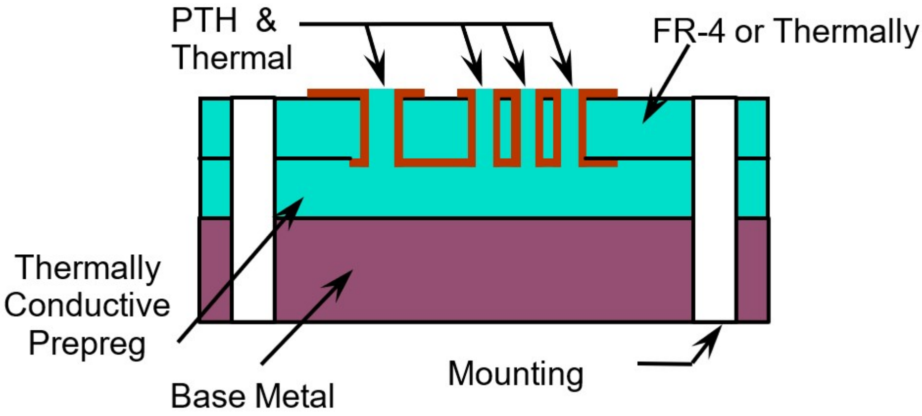
The thermally conductive prepreg is one of the most important elements of this construction and what typically differentiates the various suppliers. This is the substance that both electrically isolates the copper circuitry from the main metal and helps with rapid transfer of heat between the two. It ensures that heat generated by the components is dispersed to the base metal heat sink as quickly as possible. The prepreg is typically an organic resin with ceramic fill-ers to increase thermal conductivity. The performance of the various prepregs is measured by the thermal conductivity (Watts per meter Kelvin or W/mK) and thermal impedance (Kelvin, meter squared per Watt or Km2/W). The higher the thermal conductivity the better the heat transfer, the lower the thermal impedance the better the heat transfer. It is important to understand that the better the heat transfer associated with the prepreg, the greater the cost. It is therefore critical not to overdesign. To put this in perspective, the thermal conductivity of FR-4 is approximately 0.4 w/mK whereas the thermal-ly conductive prepregs that are available on the market today range from 1 W/mK to 8W/mK. Apart from thermal conductivity, the thickness of the die-lectric is directly related to the materials over all thermal conductivity. Typically, the thickness of the dielectric ranges between 2 to 6 mils.

Aluminum is the most common base metal used. The two most common types are 5052H32 and 6061T6. The thickness of the aluminum typically ranges between 40 and 120 mils. 40 mils and 60 mils are the most common thicknesses available. Copper is also used as a base metal. This is a significantly more costly solution.

There are many single-sided IMPCB designs that are used for LED lights. Many of these applications require a consistent white solder mask for better reflectivity. All white solder masks are not made equal. The issue is that they look different when you put them side by side. Some solder masks have a “bluish” hue and others have a “yellowish” hue. There can be an interaction between the surface finish, the solder mask and subsequent heat processing steps in the assembly process. Boards with lead free HASL tend to become “yellower.” Boards with ENIG after the solder mask process may get “pink” with subsequent reflow.

Double-Sided/Multilayer IMPCB

The PCB supplier manufactures a double-sided or multilayer IMPCB and then bonds it utilizing a thermally conductive prepreg to metal. The bonding process is done in the same multilayer press that is used to manufacture a multilayer PCB.



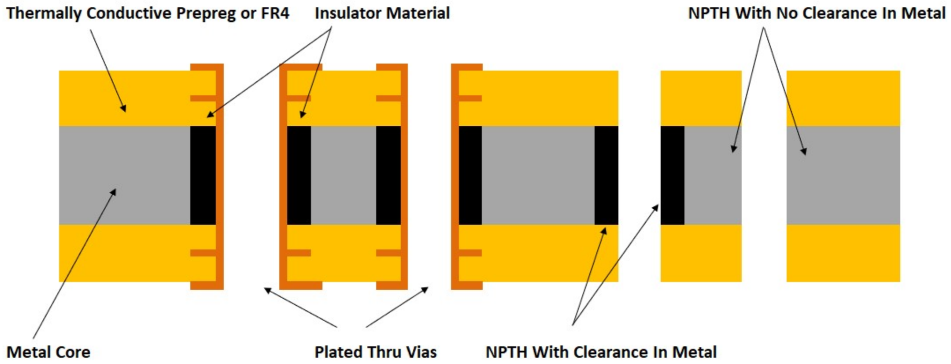
Metal Core Boards

Conceptually a metal core board is exactly like it sounds: the metal is in the middle of the PCB. The metal core is sandwiched between layers on both sides. Metal core PCBs usually have blind via layers located on both sides of the metal core substrate. There are also plated thru holes (PTH) going through the entire package. From a PCB perspective, it is important to isolate the metal from the thru hole; otherwise the board would short out completely. In order to accomplish this, one must start out by drilling the metal core approximately 40-50 mils larger than the plated thru holes, slots, or cutouts. It then needs to be filled with a non- conductive epoxy filler and then pressed. After pressing the metal core, it needs to have the filler compound removed from the surface and then prepared for lamination with the inner layer cores. After lamination, you drill the PTH and process the PCB through normal manufacturing processes.

While thermal management is a factor in these PCBs, one of the other reasons that metal core boards are used is to help with vibration reduction ensuring that assembly joints don’t crack or fail in high-vibration applications.

Multilayer Metal Core Board

The metal core can be copper C110 or aluminum 6061T6 or molybdenum.



The metal core boards are drilled oversized. The insulator filler material acts to insulate the PTH from the metal core, so the layers do not short out. The powdered filler is applied to the surface and holes and put in a multilayer lamination press. This is a critical process because you want to make sure there are no voids in the filler or the PTH chemistry can leach back to the metal core and cause a short. The core is then sanded to remove the excess filler on the surface. The filler material is a ceramic-epoxy combination.

Stack up: It is preferred to be symmetrical in terms of number of layers on top of the metal core and number of layers below the metal core. Also, copper weight symmetry is preferred between all the layers. Lack of symmetry could lead to excessive warpage issues.

Chapter 17

PCB Reliability

Electrochemical Migration (ECM)

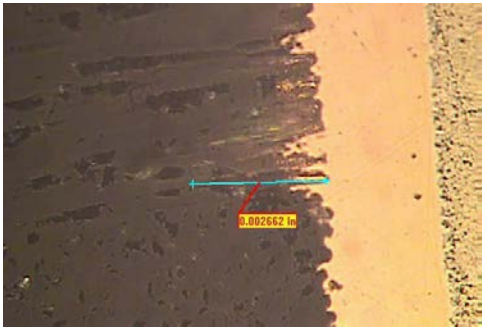
This is the growth of conductive metal filaments on, or in, a printed circuit board under the influence of a DC voltage bias. Silver, zinc, and aluminum are known to grow dendrites (whiskers) under the influence of an electric field or pressure. Pure silver also grows conducting surface paths in the presence of halide and other ions, making it a poor choice for electronics use. Newer immersion silver has modifiers added to eliminate the dendritic growth.

Tin and silver will grow "whiskers" due to tension in the plated surface. Tin/lead or solder plating also grow whiskers, only reduced by the percentage tin replaced. Reflow to melt solder or tin plate to relieve surface stress lowers whisker incidence.

Conductive Anode Filament Growth

A different, but related, type of potential circuit short is metal ion migration. This potentially dangerous printed circuit defect is generated by applying a DC potential across two copper conductors close together and adding moisture. The copper ions will migrate from the positive to the negative potential through conductive salts being moistened with humidity that the laminate absorbs. The preferred path is along the glass fibers where the moisture tends to collect. The laminate's ability to absorb moisture is a big problem in CAF (conductive anode filament) growth, as most, if not all, circuits use some form of DC potential. All boards can be subject to CAF growth. It is possible to grow .150-inch-long dendrites in a few minutes with the right conditions.

There are many different types of laminate and they all absorb moisture at different rates. Polyimide absorbs moisture at twice the rate of FR4, and the new higher Tg lead-free laminates absorb the least. CAF does not easily pass from one layer to another layer due to the lack of porosity between layers. The conductors need to be relatively close to create the correct conditions necessary for filament growth. The most likely place for CAF in a printed circuit board is between two close holes or from a hole to a close copper trace where the laminate is the thinnest. Drilling causes the most damage to the laminate as a horizontal crack is a potential site to start CAF due to wicking in of the electroless copper. Conductive growth is also created from dendrites growing on the surface of the PCB. These are caused by flux residue left from “no clean type” flux applications during assembly and grow from the cathode to the anode.



Wicking of electroless

The proper cleaning and flux use are important to prevent dendrite growth. With the new lead-free solder requiring more active flux, this is an area where caution and testing is required to ensure long-term reliability. The most reliable thermal life cycle testing is thermal cycling using resistance monitoring through multiple cycles. The samples are first heated six times to temperatures representing component soldering. The thermal cycling is like tests requested first by the avionic industry and now by the automotive industry: -25°C/-40°C to +145°C for 1000 times, with real time evaluation of the resistance variation by means of a via string daisy-chain. Some companies request multiple thermal stresses in Sn/Pb, after conditioning at high and controlled temperatures.

Laminate Material Integrity:
A series of tests can be performed with sophisticated instruments, such as DSC (Differential Scanning Calorimetry), TMA (Thermo Mechanical Analysis) and TGA (Thermo Gravimetric Analysis). These tests will determine the percentage cure rate in the laminate as well as its ability to resist X axis expansion.

- Tg Value: It represents the temperature where the resin changes from the solid to the plastic state and this transformation relates to the movement of the polymeric chains. This test can be carried out both with DSC and TMA, leading to different values. Usually, it is carried out with DSC, which supplies data that can be compared more easily. The value itself of these analyses is not indicative for the thermal reliability of the laminate. Typical values of the traditional FR4 are in the range of 130°C to 140°C, 165°C to 180°C for high performance FR4 and 175°C to 190°C for phenolic-based FR4.
- Z–CTE (X-Y): A sample is submitted to heating for a certain time (from 50° C to 250°C) in order to verify its expansion in z-axis. It can be carried out also on the plane area, i.e. in the axis x and y. The problem

of thermal degradation in the expansion in z-axis is more critical, whereas the expansion in x-y involves more the capability of component mounting such as ceramic BGA.

- Extended CTE: Using a heating ramp of 10°C/minute until 300°C, the test measures at which temperature the delamination/expansion takes place.
- TGA: A sample is submitted to a ramp of temperatures until a loss of weight of 5% (the value varies at the different test versions). A substantial loss of weight is clearly a symptom of the material degradation.
- T260 Test: Generally, the TMA test uses a heating ramp of 10°C/minute and then isotherm at 260°C. This test serves to observe how many minutes the specimen can survive at 260°C before delaminating dramatically and, consequently, before showing a strong expansion on the Z-axis. This test is not relevant in lead-free applications because the test temperature is not high enough.
- T300 Test: Same as the TMA test but with a 300°C maximum temperature.
- Peel Strength: Copper adhesion to dielectric expressed in lbs. per sq. in. (5 to 7 is normal).
- Electrical Tests: Dielectric constant (Dk) are usually measured at different frequencies. For FR-4 it is typically, 4.3 to 4.5. Dissipation Factor (DF) or Tangent Loss is also measured at different frequencies. For FR-4 it is typically, .009 to .013.

Tests on PCBs

There are also several tests that can be performed on finished PCBs.

- Cross Sections: This is detailed in the section below.
- Ionic Contamination Testing: This test is performed to determine the level of ionic material left on the board. Ionic contamination if left on the board can cause latent failures due to corrosion and current leakage or shorting.
- HPCT (High Pressure Cooker Test): This is a test to evaluate the integrity of a laminate and solder mask after exposure to steam at a certain pressure for a certain time and following stress in the Sn/Pb bath at 288°C. It is also used to measure moisture absorption.
- Thermal Cycling: This is a resistance monitoring of copper barrel cracking and inner layer interconnects on IST or HATS testing machines. Typical testing involves 3 to 6 pre-cycling cycles, with up to

2000 cycles testing at 200°C delta temperature swing to find where the via cracks.

- Float Resistance at 288°C: This is a time-extended version of the older MIL test. It is sometimes difficult to see any results without extensive cross-sections
- Flammability Test: This test is performed by UL or similar lab to determine the flammability rating. Typically, we look for a rating of UL 94V0

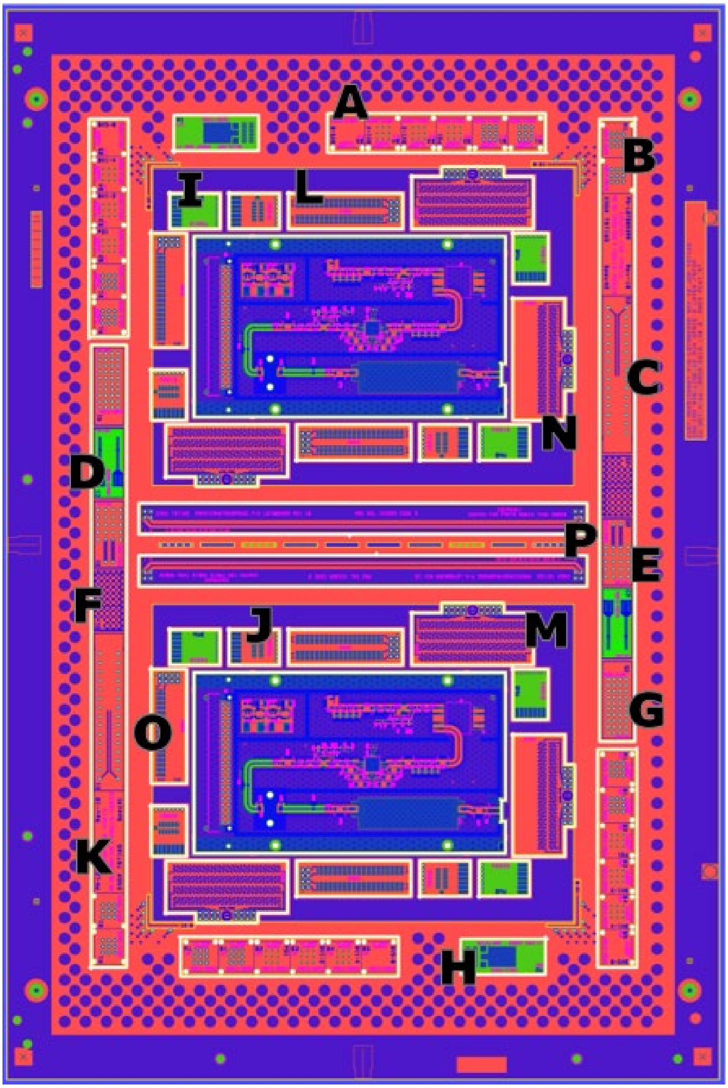
Cross sections:

In many cases one of the final quality inspection steps before a job can ship to the customer is evaluation of the printed circuit board by cross sections. Typically, the PCB production panel has special coupons at the edge of the panel that is used for this evaluation. There will be a coupon for every via structure and every via fill structure. On complex PCBs all these sections will be evaluated. Occasionally, customers request sections be taken in the functional part of the PCB. This is the only way one can really look at the inside of the plated through hole.

The quality of the cross-section is extremely important, and this can require a precise cut in the middle of the holes and correct polishing of the sample. The polishing operation will be repeated many times using higher grit sand paper, fol- lowed by a special fine polish with diamond polishing paste on a special cloth. An application of ammonia will etch into the copper and bring out any cracks.

The evaluator needs to look for good quality of the plating deposit, barrel cracking, corner cracks, hole wall pull-away, resin recession, delamination of the resin fibreglass system, as well as poor hole wall quality due to poor drilling. The cross-section is examined for symptoms of pad lifting showing a low expansion in z-axis and post separation for a good connection of inner layer and plated copper. Measurements are also taken of the plating thickness, the dielectric layers, finished copper thickness on all layers and soldermask thickness.

Inspection and test criteria are based on IPC-A-600 and IPC-6012, Class 2 unless otherwise specified, on customer drawings or specifications.



Sample Panel with several different quality/ reliability coupons

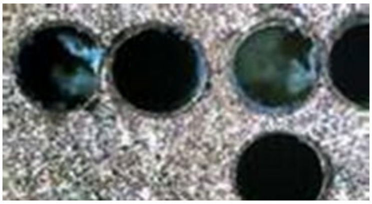
Legend for the Various PCB Coupons:

A. Plated Hole Evaluation
B. PTH Evaluation
C. Moisture Insulation Resistance
D. Plating Adhesion
E. Thermal Shock
F. SM Adhesion
G. TH Solderability
H. SMT Solderability

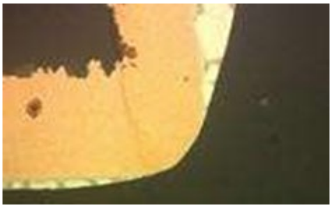
I. Plating / SMT Solderability
J. SMT Solderability
K. PTH Evaluation
L. Interconnect Resistance – IST
M. HATS Coupon / Thermal Reliability
N. HATS Coupon
O. Interconnect Resistance – IST
P. Controlled Impedance Coupon

Height of solder mask

Etching undercut

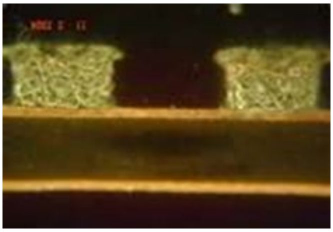


Top down cross-section showing debris in holes, drill running into other holes

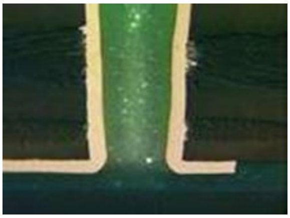


Glass fibers in the holes, a crack in the corner

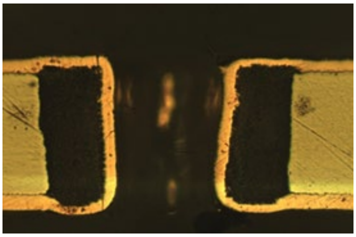
Cross-section of filled via and via fill material



Line overhang from over plating

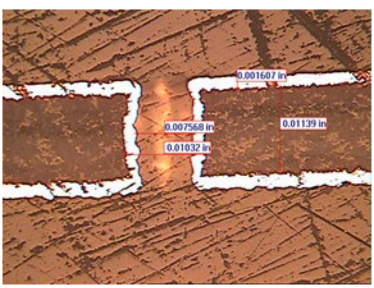


Good hole wall

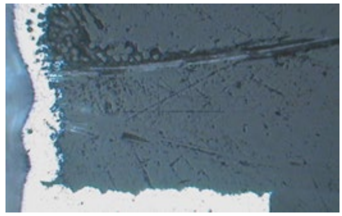


*Very poor drilling wicking,
poor fill and plate in hole
through Copper Invar Copper*

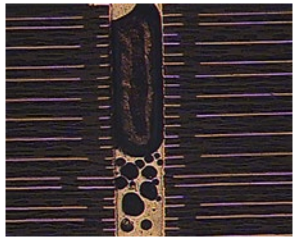
*Plated micro via of
very good quality*



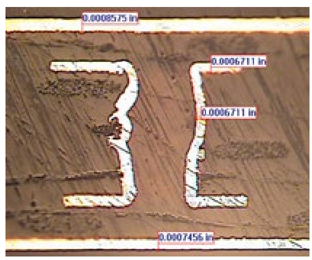
Good board with no cracks



Wicking and crack



*Rejected 28 layer
multilayer via,
one core is shifted,
thin copper plating*



*Poor Drilling with bulge
in the center*

Chapter 18

Industry Specifications

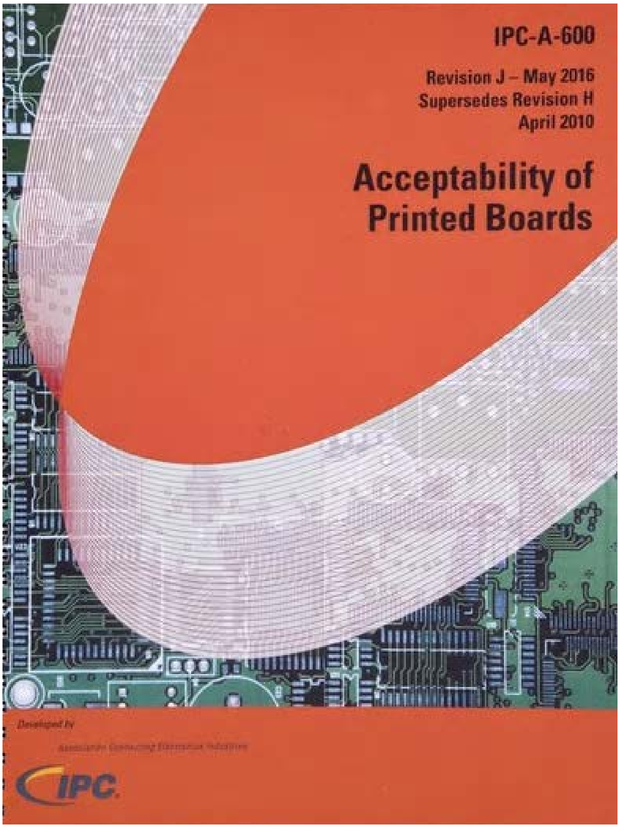
There are two types of specs commonly used in the PCB industry - IPC and the MIL Specs. Below is a list of some of the specifications.

IPC-SPECS

- IPC-A-600 Acceptability of Printed Boards
- IPC-A-610 Acceptability of Printed Wiring Assemblies
- IPC-T-50 – Terms and Definition
- IPC-MF-150 – Metal Foil for Printed Wiring Applications
- IPC-FC-231 – Flexible Bare Dielectrics for Use in Flexible Printed Wiring
- IPC-FC-232 – Specification for Adhesive Coated Dielectric Films For Use as Cover Sheets for Flexible Printed Wiring
- IPC-FC-241 – Flexible Metal Clad Dielectrics for use in Fabrication of Flexible Printed Wiring
- IPC-SM-840 – Qualification and Performance of Permanent Solder Mask
- IPC-2221 – Generic Standard on Printed Board Design
- IPC-2223 – Sectional Design Standard for Flexible Printed Boards
- IPC-4101 – Laminate/Prepreg Materials Standard for Printed Boards
- IPC-6011 – Generic Performance Specification for Printed Boards
- IPC-6012 – Qualification and Performance Specification for Rigid Printed Boards
- IPC-6013 – Qualification and Performance Specification for Flexible Printed Boards
- IPC-6018 – Qualification and Performance Specification for High-Frequency (Microwave) Printed Boards
- J-STD-001 – Requirements for Soldered Electrical and Electronics Assemblies
- J-STD- 002 – Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires
- J-STD-003 – Solderability Tests for Printed Boards
- J-STD -004 – Requirements for Soldering Fluxes
- J-STD- 005 – General Requirements and Test Methods for Electronic Grade Solder Paste
- J-STD-006 – General Requirements and Test Methods for Soft Solder Alloys and Fluxed and Non-Fluxed Solid Solder for Electronic Soldering Applications

MIL-SPECS

- MIL-P-50884 – Flex Manufacturing and Performance
- MIL-STD-2118 – Flex Design Standard
- MIL-STD-105 – Sampling Procedures and Inspection Tables
- MIL-STD-129 – Marking for Shipment and Storage
- MIL-STD-130 – Identification for Marking
- MIL-STD-202 – Test Methods for Electronic Equipment
- MIL-STD-2000 – Soldering and Assembly
- MIL-STD-45662 – Calibration System Requirements
- DOD-D-1000 – Engineering Drawings
- DOD-STD-100 – Engineering Drawing Practices
- ANSI-Y-145 – Dimensioning and Tolerancing
- MIL-S-13949 – Plastic Sheet, Laminate, Metal Clad (for PWB's)
- MIL-C-14550 – Copper Plating (Electrodeposited)

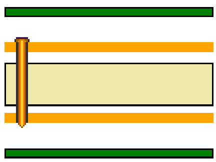


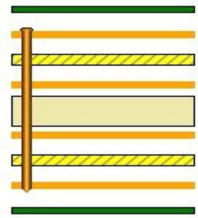
Chapter 19

Printed Circuit Board Cost Drivers

In general, as technology increases it drives higher costs. There are several ways that cost can be mitigated in the design phase. If you are wondering about cost tradeoff's it is always good to discuss with your PCB fabricator.

Layer Count:
The first, and most obvious cost driver is layer count. More dielectric material implies more imaging, more etching, more plating, all of which increase the cost.





Base Laminates:
Base laminates required for RF/MW or any high-performance boards can range wildly depending on the needs of the performance you require. Also use high frequency materials only between the layers where it is required. Do not change all layers to the high-performance materials unless it's required.

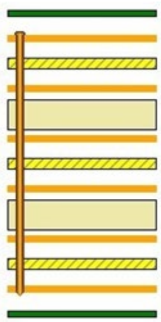
Copper Weight:
Whenever the finished copper weight exceeds 1 ounce, cost will rise exponentially as the copper weight rises. In addition, the etch factor becomes much more critical and challenging to control. This results in greater minimum space required and higher cost.

Drilling:
Hole density per board or per panel drive up costs. The more holes and variety of hole sizes, the longer the drills must be active and drill bits must be monitored and changed accordingly. Drill bit life is monitored carefully by the drill programs. After so many hits the drill will stop, and the bit must be changed to ensure clean hole-drilling which allows for plating chemistries to flow.

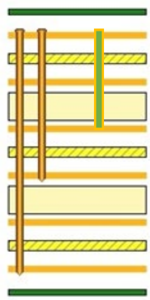
Very small features and tolerances requires extra oversight and careful process control. Upgraded entry and back-up drill material to ensure against things like "drill-wander" and over or under-etching.

Laser drilling may be necessary which also adds cost, especially if the fabricator does not have laser drills in house.

HDI:
Every time you add buried and blind vias you increase the number of lamination cycles, drill operations, de-smear and plating operations, all of which increase costs

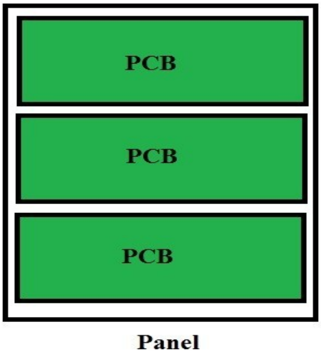


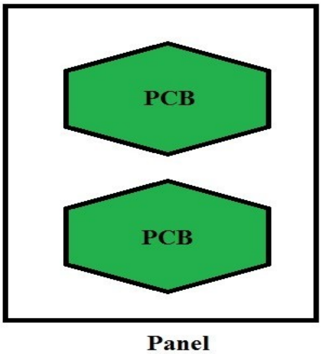
Normal multilayer



Sequential lamination

Board Size:
For obvious reasons, the larger the board or array, the greater the cost. Also investigate how boards will fit into a production panel to ensure maximum material utilization occurs.





X-Outs:
No X-outs specified, when building and shipping PCBs (multiple up) in panel form, some customers require that every board in the panel be a good board, with no X-outs allowed for defective boards. This forces the board supplier to run more

panels in order to get the required yield to fulfill the customer's order. This cost gets passed on.

Controlled Impedance

Controlled impedance should only be requested if required. Costs increase due to potential reduction in usable panel area in coupons, serialization of the panels and controlled impedance testing. If controlled impedance is required, following guidelines will help to minimize impedance costs:

- Specify impedance only on layers that really require this
- Route all controlled impedance traces onto the same layer
- Specify a +/– 10% tolerance when possible.
- Designate one target impedance value to be tested per layer
- Couple power/ground on adjacent layers when possible
- Allows for modifying the construction to meet overall tolerance

Via filling

When filling vias, not only do the via holes need to be filled, but they must be cured properly and then planarized. In addition, typically the via holes that need to be filled will be drilled and plated first, vias filled and then the holes that don't need via fill are drilled and plated. Obviously, adding all these extra operations adds cost.

Vias can be filled with either non-conductive material or conductive material. Conductive via-filling is much more costly than non-conductive via filling. There are tiny particles of conductive material present which adds costs. Conductive materials offer minimal performance enhancement and there are alternative methods to get similar enhancements. If you must fill holes non-conductive fill-ing is the preferred method.

Edge Plating

Plating edges requires extra processing steps which adds to the cost.

Chapter 20

American Standard Manufacturing Process Capabilities

Rigid PCB's

Specification	Standard Production	Advanced or Proto-type
General		
Panel Sizes (inches)	9"x12", 12"x18", 18"x24", 21"x24" 32" x 32" (SS / DS), 24" x 48" (SS / DS)	20" x 32" Call for any other sizes
Number of Copper Layers	1-20	>20
Workmanship Specification	Per IPC 6012 (Rigid Products) / 6018 (Microwave Prod-ucts), Class 3, Class 3 DS, Class 3 DA MIL-PRF-31032 /1, /2, /3, /4 and MIL-PRF-55110, Appendix B	
Materials		
Materials Rigid / Thermoset/Flex	Standard FR4 Epoxy, High-Temp FR-4 Epoxy, High Td FR-4 Epoxy, RoHS Compliant FR-4 Epoxy Polyimide, BT, Isola FR408, Itera, Astra, Megtron 4, 6 &7, Rogers 4000 Series, Hitachi Theta, Dupont, Panasonic	
Materials – Microwave & High Frequency Materials	Nelco, Rogers, Taconic – See Laminate Selector Guide FEP, Rogers 3001, Rogers 2929, Itera, Astra, Megtron 4, 6,7, Taconic FastRise, Pre-bonded RF Materials (Rogers, Taconic) Custom Order Pre-bonded	
IMS Materials	Bergquist, Aismalibar, C-Sem, Laird, Ventec, Totking	
Buried Passives	Capacitance: Farad Flex, C-Ply Resistors: Ticer, Ohmega Ply	
Foil Weight: (inner layer)	¼ oz - 6 oz 8 µm- 212 µm	>6 oz >212 µm
Foil Weight: (outer layer)	¼ oz-6 oz 8 µm-212 µm	>6 oz >212 µm

Specification	Standard Production	Advanced or Proto-type

Dielectric & PWB thickness		
Overall board thickness:		
Double sided	.001”-.350” 0.0254 mm-8.89 mm	>.350” >8.89mm
Multi-layer	.008”-.350” 0.2032 mm-8.89 mm	>.350” >8.89mm
Thickness Tolerance	+/- 10%	Call for Specifics
Warp and Twist	0.7% std - dependent on material and stack-up	<0.7%

Line Width and Space		
¼ oz. Min. line width/spacing 8 µm Min. line width/spacing	0.003”/0.003” 75/75 µm	0.002”/0.002” 50/50 µm
½ oz. Min. line width/spacing 17 µm Min. line width/spacing	0.003”/0.003” 75/75 µm	0.002”/0.002” 50/50 µm
1 oz. Min. line width/spacing 35 µm Min. line width/spacing	0.004”/0.004” 100/100 µm	0.003”/0.003” 75/75 µm
Etch Tolerance (Inner Layers) ¼ oz. copper 8 µm copper	+/-.0003” (Design Specified) +/- 7 µm (Design Specified)	
½ oz. copper 17 µm copper	+/-.0005” (Design Specified) +/- 12 µm (Design Specified)	
1 oz. copper 35 µm copper	+/-.0005” (Design Specified) +/- 12 µm (Design Specified)	
2 oz. copper 71 µm copper	+/-.001” (Design Specified) +/- 25 µm (Design Specified)	
Etch Tolerance (Base Copper Outer Layers) ¼ oz. copper 8 µm copper	+/-.0003” (Design Specified) +/- 7 µm (Design Specified)	
½ oz. copper 17 µm copper	+/-.0005” (Design Specified) +/- 12 µm (Design Specified)	
1 oz. copper 35 µm copper	+/-.001” (Design Specified) +/- 25 µm (Design Specified)	
2 oz. copper 71 µm copper	+/-.002” (Design Specified) +/- 50µm (Design Specified)	

Specification	Standard Production	Advanced or Proto-type

Drilling		
Min. drilled hole diameter	0.008” 203 µm	0.006” 150 µm
Max. drilled hole diameter	0.250” 6.35 mm	
Max. Aspect Ratio	10:1	15:1
PTH diameter tolerance	+/- 0.002” +/- 50 µm	+/- 0.002” +/- 50 µm
NPTH diameter tolerance	+/- 0.002” +/- 50 µm	+/- 0.001” + /- 25 µm
Hole location tolerance	+/- 0.003” Hole to Edge +/-75 µm Hole to Edge	

Routing		
Edge-to-edge tolerance	+/- 0.005” +/- 127 µm	+/-0.003” +/- 75 µm
Edge-to-datum hole tolerance	+/- 0.005” +/- 127 µm	+/- 0.002” +/- 75 µm
Min. internal radius	0.015” 381 µm	0.010” 254 µm
Scoring		
Jump score capability	Yes	
Available scoring angles	20º ,30º, 45º	
Edge beveling		
Available angles	30º, 45º, +/- 5º	Call for specifics

Multilayer lamination		
Technique	Hi-Temp Vacuum Assisted Hydraulic Pressing Capabilities	
Core to Core Registration	+/- 0.005” +/- 127 µm	Call for Specifics
Front to Back Registration	+/- 0.001” +/- 25 µm	+/- 0.005” +/- 12 µm

Specification	Standard Production	Advanced or Proto-type

Soldermask		
Type	LPI, LDI LPI	
Colors	Green, Blue, Red, White, Black, Grey, Orange, Amber, Yellow	Custom
Min. soldermask clear-ance	0.002” (per side) 50 µm (per side)	0.0015” (per side) 37 µm (per side)
Min. soldemask web thickness	0.0033” Color Specific 83 µm	
Legend		
Type	Ink Jet Printer, UV Thermal	
Colors	Ink Jet: White, Black UV Thermal: White, Black, Yellow	
Smallest line width:	Ink Jet Printer: .003”, 75 µm Thermal: .010”, 254 µm	

Hole Plugging	
Conductive via plugging	Tatsuta AE3030 (Preferred), DuPont CB100 Min. Hole Size .010”, Max. Hole size 0.030”, A.R.=8:1max 1:1 min Min. Hole Size 254 µm, Max. Hole size 762 µm, A.R.=8:1max 1:1 min
Non-conductive via plugging	Taiyo THP 100DX1, SanEi IR10F, Peters PP2795 Min. Hole Size .010”, Max. Hole size 0.030”, A.R.=8:1max 1:1 min Min. Hole Size 254 µm, Max. Hole size 762 µm, A.R.=8:1max 1:1 min
Surface Finishes	
Type	Hot Air Solder Level, ROHS Compliant Hot Air Level (SN100CL), OSP Entek Plus 106A, Electroless Nickel / Immersion Gold (ENIG), Electroless Nickel / Electroless Palladium/ Immersion Gold (ENEPIG), Electrolytic Nickel, Electrolytic Hard Gold, Electrolytic Soft Gold, Immersion Silver, Immersion Tin, Electrolytic Matte Tin, Plated Tin Lead, Hot Oil Reflow

Specification	Standard Production	Advanced or Proto-type

Electrical Test		
Pitch	0.0197” 500 µm	0.012” 304 µm
Fixture types	2 Sided	
Test voltages available	Per Requirement up to 250V DC	
Resistivity testing:		
Open resistance	10 Ω	50 Ω max.
Short resistance	10 MΩ min.	100 MΩ max.
Netlist capability	Yes 100%	
Flying Probe	Yes	
Test voltages available	100 volts	30 -1000 volts
Controlled Impedance	+/- 10%	+/- 5%
Passives Testing	Buried Resistors / Capacitors	
Resistivity testing:		
Open resistance	50 Ω	5 – 80 Ω
Short resistance	17 MΩ min.	500 MΩ max
Hipot Test	0-2500VDC	0-6000VDC

Flex & Rigid-Flex PCB's

Specification	Standard Production	Advanced or Proto-type
General		
Panel Sizes	12" x 18" 304 mm x 457 mm	20" x 32" 508 mm x 813 mm
Number of Copper Layers	16	17+
Bookbinder Number of layers	8	10+
Workmanship Specification	Per IPC 6013A Class II & III MIL-PRF-31032 & MIL-PRF-50884F	
Materials		
Polyimide Film	DuPont Panasonic Shin-Etsu	
Foil Weight: (inner layer)	½ oz-3 oz 17 µm-106 µm	>3 oz >106 µm
Foil Weight: (outer layer)	½ oz-3 oz 17 µm-106 µm	>3 oz >106 µm
Material Thickness		
Base Material	1/2 mil-5 mil 12.7 µm-127 µm	Call for Specifics
Cover Film	1/2 mil-5 mil 12.7 µm-127 µm	Call for Specifics
Adhesive	1/2 mil-5 mil 12.7 µm-127 µm	Call for Specifics
Copper RA	1/2 mil-5 mil 12.7 µm-127 µm	Call for Specifics
PSA	1/2 mil-5 mil 12.7 µm-127 µm	Call for Specifics

Specification	Standard Production	Advanced or Proto-type

Line Width and Space		
1 oz. Min. line width/spacing 35 µm Min. line width/spacing	0.004”/0.004” 100/100 µm	
½ oz. Min. line width/spacing 17 µm Min. line width/spacing	0.003”/0.003” 75/75 µm	0.0025”/0.0025” 62/62 µm
Etch Tolerance 1/2 oz. copper (Base Copper) 17 µm copper	+/- .0005” (Design Specified) +/- 12 µm (Design Specified)	
1 oz. copper 35 µm copper	+/- .001” (Design Specified) +/- 24 µm (Design Specified)	
2 oz. copper 71 µm copper	+/- .002” (Design Specified) +/- 50 µm (Design Specified)	

Tolerances		
Edge to Edge	0.003” 75 µm	0.002” 50 µm
Edge to Hole	0.005” 127 µm	
Edge to Feature	0.005” 127 µm	0.004” 100 µm
PTH diameter tolerance	+/- 0.003” 75 µm	+/- 0.002” (after OSP/NiAu/Tin/Silver) +/- 50 µm (after OSP/NiAu/Tin/Silver)
NPTH diameter tolerance	+/- 0.002” +/- 50 µm	+/- 0.001” + /- 24 µm
Hole location tolerance	+/- 0.003” +/- 75 µm	
Miscellaneous		
Stiffeners	FR4, Polyimide, Aluminum	Call for Specifics
Shielding	Silver Paste, Silver Film	Call for Specifics
Strain Relief	Eccobond (Any Type)	Call for Specifics

RF Thermal Management PCB'S

Specification	**Standard Production**	**Advanced or Proto-type**
Heat Sink Bonding		
Bonding processes	Thermally & Electrically Conductive Silicone Adhesive (Electrasil 2), Sweat Solder All available prepregs Emerson & Cumming CF3350, Ablestick 5025E & 0563ECF. Rogers Cool Span, 3M7373	
Sweat Solder Pastes	63% Tin 37% Lead 95% Tin 5% Antimony SAC 305	Call for Other
Board to Carrier Registration	+/- 0.005" +/- 127 µm	+/- 0.003" +/- 75 µm
Machining Capabilities		
Profile / Feature Tolerance	+/- 0.005" +/- 127 µm	+/- 0.002" +/- 50 µm
Internal Radii (Min)	+/- 0.031" +/- 787 µm	+/- 0.012" +/- 304 µm
Machined Feature to Circuit Image	+/- 0.005" +/- 127 µm	+/- 0.003" +/- 75 µm
Depth Control (Pockets, Counterbore, Countersink)	+/- 0.002" +/- 127 µm	+/- 0.001" +/- 25 µm
Surface Finish	64√	32√

Specification	Standard Production	Advanced or Proto-type

Metal Carrier Finishes over Aluminum		
Electroless Ni (per MIL-C-26074E, Class 1, Grade A) Electrolytic Silver (per QQ-S-365D, Type I, Grade B)	100-300 µ in. Nickel 2.54-7.62 µm Nickel 200 µ in. min. Silver 5.08 µm min. Silver	Nickel – Range Specified Silver – Range Specified
Electroless Ni (per MIL-C-26074E, Class 1, Grade A) Electrolytic Matt Tin	100-300 µ in. Nickel 2.54-7.62 µm Nickel 200 µ in. min. Tin 5.08 µm min. Tin	Nickel – Range Specified Tin – Range Specified
Electroless Ni (per MIL-C-26074E, Class 1, Grade A) Electrolytic Ni (per MIL-S-QQN-290A, Class I, SD) Electrolytic Soft Au (per MIL-G-45204C, Type III, Grade A)	50-100 µ in. Nickel 1.27-2.54 µm Nickel 100-300 µ in. Nickel 2.54-7.62 µm Nickel 3 µ in. min. Gold 0.0762 µm min. Gold	Nickel – Range Specified Gold – Range Specified
Electroless Ni (per MIL-C-26074E, Class 1, Grade A) Electrolytic Ni (per MIL-S-QQN-290A, Class I, SD) Electrolytic Hard Au (per MIL-G-45204C, Type II, Grade C)	50-100 µ in. Nickel 1.27-2.54 µm Nickel 100-300 µ in. Nickel 2.54-7.62 µm Nickel 3 µ in. min. Gold 0.0762 µm min. Gold	Nickel – Range Specified Gold – Range Specified
Chromate conversion coating (per MIL-C-5541E, Class 3)	Coverage	

Specification	Standard Production	Advanced or Proto-type
Metal Carrier Finishes over Copper		
Electrolytic Silver (per QQ-S-365D, Type I, Grade B)	75-150 µ in. Silver 1.905-2.667 µm Silver	
Electrolytic Matt Tin	75-150 µ in. Tin 1.905-2.667 µm Tin	
Electrolytic Ni (per MIL-S-QQN-290A, Class I, SD) Electrolytic Soft Au (per MIL-G-45204C, Type III, Grade A)	100-300 µ in. Nickel 2.54-7.62 µm Nickel 3 µ in. min. Gold 6.6762 µm min. Gold	Nickel – Range Specified Gold – Range Specified
Electrolytic Ni (per MIL-S-QQN-290A, Class I, SD) Electrolytic Hard Au (per MIL-G-45204C, Type II, Grade C)	100-300 µ in. Nickel 2.54-7.62 µm Nickel 3 µ in. min. Gold 0.0762 µm min. Gold	Nickel – Range Specified Gold – Range Specified
Electroless Ni (per MIL-C-26074E, Class 1, Grade A)	100-300 µ in. Nickel 2.54-7.62 µm Nickel	Nickel – Range Specified
Immersion Au (per MIL-G-45204)	3-8 µ in. Gold 0.0762-0.2032 µm Gold	

References & Acknowledgements

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Printed Circuit Designers Guide to…™ Fundamentals of RF and Microwave Circuits, John Bushie & Anaya Vardya

Flexible Circuit Technology, Joseph Fjelstad

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APPENDIX A

PCB Data Checklist for Accurate Quotes and Manufacturing

Complete PCB Gerber File Set:

- One file for each circuitry layer (from 1 to n)
- One file for each soldermask layer or coverlayer
- One file for each silkscreen legend layer
- One file for each solder paste layer
- An accurate outline layer representing the PCB contours, plus all features such as slots and cutouts
- A fabrication drawing in Gerber format whenever possible. 1:1
- If PCB is to be panelized, supply a separate drawing or describe configuration.
- All files should be RS274X (Gerber Extended) format. Output resolution preferred 2:5 Imperial or 3:3 Metric.

Stack Up Information:

- Laminate type and thickness.
- Copper weight for each layer
- Desired finished copper thickness in mils or inches for each outer or plated sub layer
- Cross sectional view showing layer thicknesses (for multilayer) if critical
- Impedance information (trace width, spacing, value in Ohms) if control and testing are required

NC Drill and Associated Report Files:

- Plated through drill file including tool codes in (readable text) formatNon
- Plated through drill file including tools codes in ASCII (readable text) format
- Blind Via drill file(s) including tool codes in (readable text) format
- Backdrill file(s) including tool codes in (readable text) format
- Buried Via drill file, including tool codes, in ASCII (readable text) format.
- Slot File if required (slots may be shown on Gerber Outline layer instead). 1:1

Fabrication Drawing Information:

- Basic outline dimensions
- Dimensions for any features where location is critical

- Pattern of drilled holes with drill table showing size, tolerance, and plating status symbol

Soldermask / Silkscreen Information:

- Define soldermask color, layers, and sheen (Green by default)
- Define silkscreen color and layers (white by default)
- Define fabricator marking locations (UL logo, flammability rating, date code, and any others)

Final Finish Requirement:

- Type of final finish (examples: Lead Free HAL, ENIG etc)
- Any quality requirements specific to the finish e.g. thickness

Quality Requirements:

- Tolerance information for all features (linear and hole diameter tolerances typically separate.)
- Separate fabrication and inspection classes per IPC (IPC 6012 Class 2 for fabrication and IPCA 600 inspection Class 2 standard)
- List any special requirements (ITAR, medical, military, automotive, aerospace)
- If you or your end customer have a general specification, include it if applicable

Glossary

A

Activating: A chemical treatment that allows non-conductive laminate to accept electroless. Also called, catalyzing, seeding and sensitizing.
Additive Process: A process in printed circuit board manufacturing where the circuit pattern is produced by the addition of metal rather than etching metal away.
Air Gap: A routed space between two traces to control creepage.
Alkaline: A chemical that has a PH above 7.
American Wire Gage (AWG): A method of specifying wire diameter. The higher the number, the smaller the diameter.
Analytical Services Lab: Performs various tests such as plating thickness, inner layer connections to hole walls, photos or x-rays of circuit boards when required.
Annular Ring: Copper material around a hole which creates a pad.
Anode: The positive element used in the plating tank. The power supply is connected to the positive potential. The anodes are used to supply and accelerate the metal ion towards the panel being plated.
Aperture: An indexed shape with a specified X and Y dimension, or line-type with a specified width, used as a basic element or object by a photo plotter in plotting geometric patterns on film. The index of the aperture is its D code. A line of textual data in an aperture list describing the D code and position, the shape, flash or draw and the X and Y dimensions of an aperture. See Gerber.
Aperture List: An ASCII text data file, which describes the size and shape of the D codes. See Gerber.
Array: A group of circuits arranged in a pattern.
Artwork: A photo plotted film 1:1 pattern, which is used to produce the Diazo production master.
ASCII: American Standard Code for Information Interchange. It is the character sets used in almost all present-day computers. US-ASCII uses only the lower seven bits (character points 0 to 127) to convey some control codes, space, numbers, most basic punctuation, and unaccented letters a-z and A-Z.
Aspect Ratio: The ratio of the circuit board thickness to the smallest drilled hole diameter.
Assembly Drawing: A drawing showing the locations of components, with their reference designators, on a printed circuit. Also called component locator drawing.
AutoCAD: A drawing software standard which is used by RF and silicon chip packaging designers, saved in a DFX format to convert to Gerber for PCB manufacturing.
Automatic Optical Inspection (AOI): computerized inspection of circuit boards to

find shorts and opens.

Automated Test Equipment (ATE): Equipment that automatically tests and analyzes electrical parameters to evaluate quality of the PCB.

Auto-router: Automatic router, a computer program that designs or routes the traces in a design automatically.

Axial Leads: Leads coming out of the ends and along the axis of a resistor, capacitor, or other axial part, rather than out the side.

B

B-Stage Material: Sheet material (fiberglass cloth) impregnated with a resin cured to an intermediate stage (B-stage resin). Pre-preg is the preferred term.

Back Planes: Interconnection panels onto which printed circuits, other panels, or integrated circuit packages can be plugged or mounted. Typical thickness is 0.125"- 0.300".

Backup Material: A .093 mil thick layer of Phenolic, paper or wood by products, to protect the drill plate and prevent exit burrs.

Ball Grid Array (BGA): A leadless chip package in which the external terminals form a grid-style array with solder balls which carry the electrical connection to the outside of the package. The PCB design will have round landing pads to which the solder balls are soldered when the PCB is heated in a reflow oven.

Bare Board: An unpopulated PCB with no components assembled on it yet.

Barrel: The wall formed by plating a drilled hole.

Base Copper: Copper foil provided in sheet form to clad one or both sides of a piece of laminate used as either internal or external layers.

Base Laminate: The dielectric material upon which the conductive pattern may be formed. The base material may be rigid or flexible.

Base Material: See Base Laminate.

Bed-of-Nails: A method of testing printed circuit boards that employs a test figure mounting an array of contact pins configured to engage plated thru-holes on the board.

Bevel: An angled edge of a printed circuit board for gold fingers.

Bill of Materials (BOM): A list of components of the assembly such as a printed circuit board. For a PCB, the BOM must include reference designators for the components used and descriptions which uniquely identify each component. A BOM is used for ordering parts, along with an assembly drawing.

Bleeding: A situation where a plated hole emits electroless solution from crevices or voids. Or the edge of a silkscreen ink line blotting or bleeding outward past the desired edge.

Blind Via Hole: A plated-through hole connecting an outer layer to one or more internal conductor layers of a multilayer printed board but not extending fully through all the layers of base material.

Blister: An area of swelling and separation or delamination between any of the

layers of a laminated base material or between base material and copper foil.
Blow Hole: A solder joint void caused by out-gassing of process solutions during thermal cycling.
Board House, Vendor: A fabricator of printed circuit boards.
Bond Strength: The force in pounds per square inches required to delaminate two adjacent layers of a board when attempting to separate the layers. See Peel Strength.
Bow: The measurement of flatness of a circuit board between corners and the center.
Break-away: A PCB panel format with board units connected to a panel by number of tabs around the units. Units break-away from panel after assembly. Panel profiling of this format may be routed or punched.
Breakdown Voltage: The voltage at which an insulator or dielectric ruptures or at which ionization and conduction take place and creates an arc.
Breakout: Poor registration between the drilled hole and the pad on a printed circuit board to the extent that the outer edge of the hole is not within the area of the pad.
Bridging, Electrical: The formation of a conductive path between two insulated conductors such as adjacent traces on a circuit board.
BT/Epoxy: The blending of bismaleimide/triazine and epoxy resin provides enhanced thermal, mechanical and electrical performance over standard epoxy systems.
Buildability: Team meeting to review customer designs against manufacturing process capabilities. Used to identify possible failure modes prior to fabrication.
Buried vias: Vias which start and end in the middle of the board.
Burr: A ridge left on the surface copper after drilling.
Buss: A heavy trace or conductive metal strip on the printed circuit board used to distribute voltage and grounds.
Bypass Capacitor: A capacitor used for providing a low impedance A/C path around a circuit element.

C

C-Stage: The condition of a resin polymer when it is in the fully cured, cross- linked solid state, with high molecular weight.
Chamfer: A rounded or shaped corner to eliminate a sharp edge.
Capacitance: The property of a series of parallel conductors between a dielectric to store electrical signals when a potential difference exists between them.
Card: An older name for a printed circuit board.
Card-edge Connector: A gold plated connector which is fabricated on the edge of a printed circuit board.
CEM-1: An older NEMA grade of printed circuit laminate having a substrate of woven glass surfaces over a cellulose paper core and a resin binder of epoxy. It

has good electrical and mechanical properties. It is inexpensive and can be punched.

Center-to-Center Spacing: The nominal distance between the centers of adjacent features or traces on any layer of a printed circuit board. Also known as "pitch."

CBGA Ceramic Ball Grid Array: A ball grid array package with a ceramic substrate.

Chamfer: A corner that has been rounded to eliminate an otherwise sharp edge.

Characteristic Impedance: A compound measurement of the resistance, inductance, conductance and capacitance of a transmission line expressed in ohms. In printed circuits, its value depends on the width and thickness of the conductor, the distance from the conductor to ground plane(s), and the dielectric constant of the insulating media.

Chase: The aluminum frame used in silk screening inks onto the board.

Check Plots: Photo plots that are suitable for checking only. Pads are represented as circles and thick traces as rectangular outlines instead of filled-in artwork. This technique is used to enhance transparency of multiple layers or may be a plot of holes only for missing drill hole checking.

Chip: An integrated circuit manufactured on a semiconductor substrate and then cut or etched away from the silicon wafer.

Chip-on-board (COB): Integrated circuits or bare die are glued and wire-bonded directly to printed circuit boards instead of first being packaged and then glob topped. It can be identified by the black glob of plastic covering the chip on the board.

Chip Scale Package: A chip package in which the total package size is no more than 20% greater than the size of the die within, e.g. micro BGA.

Circuitry Layer: The layer of a PCB containing copper conductors, including signal, ground and voltage planes.

Clad or Cladding: A thin layer or sheet of copper foil, which is bonded to a composite laminate core to create the base material for printed circuits. See Base Copper.

Clean Room: A room with very low specified limits of concentration of air born particles. It is controlled to lessen the effect of dust on imaging.

Clearance Hole: A hole in the conductive pattern larger than, but concentric with, a hole in the printed board base material.

CMOS: Complementary metal-oxide semiconductor.

CNC Drill File: Programs in Exelon format which a CNC drill machine uses to drill the holes in the panel.

Coefficient of Thermal Expansion (CTE): Thermal fractional change in dimension of a material for a unit change in temperature, expressed as ppm or percentage.

Component Hole: A through hole for the attachment and electrical connection (soldering) of component terminations, including terminals and wires, to the printed circuit board.

Component Side: That side of the printed circuit board on which most of the components will be mounted.

Computer Aided Design (CAD): A software program that calculates impedance modeling and provides graphical creation of a printed circuit boards conductor layout and signal routes.

CAD CAM: Simply a combination of the two terms CAD and CAM. A term used to name the work done to the PCB data.

Computer Aided Manufacturing: (CAM) The use of computers to crate tooling data and transfer the electronic design (CAD) to the manufacturing machines.

CAM Files: The data files used directly in the manufacture of printed circuits. One type of CAM files is a Gerber file, which controls a photo plotter, drill or LDI exposure unit.

Computer Assisted Engineering (CAE): In electronics work, CAE refers to schematic software packages.

Conductive Anodic Filament (CAF): An electrical short which occurs inside or outside the PCB when a conductive filament forms between two adjacent conductors under a DC electrical bias and humidity.

Conductive Pattern: The configuration or design of the conductive material on the base laminate through which electrical energy passes. Includes conductors, lands, and through connections.

Conductor: A copper area on a PCB surface or internal layer usually composed of lands (to which component leads are connected) and paths (traces).

Conductor Base Width: The conductor width at the plane of the surface of the base material. See Conductor Width.

Conductor Thickness: The total thickness of the trace or land including all metallic coatings.

Conductor-to-Hole Spacing: The distance between the edge of a conductor and the edge of hole.

Conductor Width: The observable width of the pertinent conductor on the printed circuit board.

Conformal Coating: An insulated protective coating that conforms to the components and is applied on the completed board assembly.

Contaminant: An impurity or foreign substance whose presence on printed wiring assemblies which could electrically, chemically, or galvanically corrode the system.

Continuity: An uninterrupted flow of electrical current in a circuit.

Controlled Impedance: The matching of substrate material Dk with trace dimensions and locations to create specified electric impedance as required by the designers.

Contract Manufacturing: The manufacturing of products or subcomponents of products to be sold under a different company's name.

Cool down: The period in the reflow process after peak temperature when the temperature drops to the point where the solder joints fuse or solidify.

Coordinate Tolerance: A method of qualifying hole locations in which the variance is applied directly to linear and angular dimensions, usually forming a rectangular area of allowable variation.
Copper Foil: See Base Copper and Clad or Cladding.
Copper Pouring or Copper Hatch: CAD/CAM terms. Refers to filling of an enclosed area (generally defined by polygon lines) with a solid or hatch pattern to create a copper plane or a section of copper plane.
Copper Thickness and Copper Plating: Copper thickness usually specified in terms of number of oz/sq. ft 1/2 oz: 17.5um or 0.0007"/sq. ft; 1 oz: 35 um or 0.0014"/sq. ft . The thickness of copper specified will be the final thickness of base material plus copper plating thickness. Generally base material comes with 1/4, 1/2, 1, and 2 oz, but finish copper thickness ranges from 1/2 to 6 oz.
Core: The copper foil laminated fiberglass panel that printed circuit boards are built upon. Also known as substrate panel or interlayer.
Corona: (also known as partial discharge) A type of localized emission resulting from transient gaseous ionization in an insulation system when the voltage stress, i.e., voltage gradient, exceeds a critical value.
Corrosive Flux: A flux that contains corrosive chemicals such as halides, amines, inorganic or organic acids that can cause oxidation of copper or tin conductors.
Cosmetic Defect: A defect such as a slight change in its usual color that doesn't affect a board's functionality.
Coupon: See test coupon.
Cover Layer or Cover Coat: Outer layer(s) of insulating material applied over the conductive pattern on the surface of a printed circuit board.
CPU: Central Processor Unit.
Crazing: A condition existing in the base material of connected white spots or "crosses" on or below the surface of the base material, reflecting the separation of fibers in the glass cloth and resin material.
Curing: The irreversible process of polymerizing a thermo-setting epoxy in a temperature-time profile.
Current Carrying Capacity: The maximum current which can be carried continuously, under specified conditions, by a conductor without causing degradation of electrical or mechanical properties of the printed circuit board.
Cut Outs: Removal of an internal area of the board.

D

D code: A datum in a Gerber file which acts as a command to a photo plotter. D code in a Gerber file takes the form of a number prefixed by the letter. "D20".
Data Exchange Format (DXF): Commonly used in mechanical CAD systems.
Datum Reference: A defined point, line, or plane used to locate the pattern or layer for manufacturing inspection.
Deburring: Process of removing burrs of base copper material that remain around

holes after board drilling.

Defect: Any deviation from the normally accepted characteristics of a product or component. Also see Major Defect and Minor Defect.

Definition: The accuracy of pattern edges in a printed circuit relative to the master pattern.

Delamination: A separation between any of the layers of a base material or between the laminate and the conductive foil, or both.

Design Rule Check: The use of a computer program to perform continuity and spacing verification of all conductor routing on all layers in accordance with appropriate design rules.

De-smear: Removal of epoxy smear (melted resin) and drilling debris from a drilled hole wall.

Destructive Testing: Sectioning a portion of printed circuit panel and examining the sections with a microscope. This is performed on coupons, not the functional part of the PCB.

Develop: An imaging operation in which unpolymerized (unexposed) photoresist is dissolved or washed away to produce a copper board with a photo-resist pattern for etching or plating.

Dewetting: A condition that occurs when molten solder has failed to properly coat a metal surface and then recedes, leaving irregularly shaped globules of solder separated by areas covered with a thin solder film; base metal is not usually exposed.

DICY: Dicyandiamide, common cross-linking agent used in FR-4 construction.

Die: Integrated circuit chip as diced or cut from a finished wafer.

Die bonder: Placement machine bonding IC chips onto a chip-on-board substrate.

Dielectric: An insulating medium, which occupies the region between two or more conductors and prevents electrical shorts.

Dielectric Constant (Dk): The ratio of permittivity of the material to that of a vacuum (referred to as relative permittivity).

Dielectric Strength: A measurement of the voltage required to create an arc inside the dielectric.

Differential Signal: A method of high-speed signal transmission through two wires, which always has opposite states. The signal data is the polarity difference between the wires.

Digitizing: A computerized method of converting feature locations on a flat plane to digital X-Y coordinates.

Dimensional Stability: A measure of dimensional change caused by factors such as temperature, humidity, chemical treatment, age or stress.

Dimensioned Hole: A hole in a printed circuit board where the means of determining location is X-Y coordinate values, not necessarily coinciding with the stated grid.

DIP: Dual in line package of silicon chip.

Discrete Component: A component that has been fabricated prior to its installation of resistors, capacitors, diodes and transistors.
Dock-To-Stock A supplier quality management practice that allows a component or product to enter.
Double-Sided Board: A circuit board with conductive copper patterns on both sides with through connected vias.
DRC: Design Rule Check.
Drills: Circuit board solid carbide cutting tools with four facet points and two helical flutes designed specifically for the fast removal of chips in extremely abrasive materials.
Drill File: A computerized file containing tool and coordinate information for drilling. Common format accepted are EIA or Excellon in either binary or ASCII text file.
Dry Film: A photo imagable material, which is laminated onto a bare copper panel. It is exposed with 365 nm UV light through a negative photo tool. The exposed dry film is hardened by the UV light.
DTF: Double-treated foil.

E
ED: Electro deposited
Edge Bevel: A bevel operation performed on edge connectors to improve their wear and ease of installation.
Edge-Board Connector: A connector designed specifically for making removable and reliable interconnection between the edge board contacts on the edge of a printed board and external wiring.
Edge Clearance: The smallest distance from any conductors or components to the edge of the PCB.
Edge Connector: A connector on the circuit-board edge of gold-plated traces used to connect to other circuit boards or electronic device.
Edge Dip Solderability: A solderability test performed by taking a prepared specimen, fluxing it and then immersing it into a pot of molten solder for 10 seconds dwell time, and then withdrawing it.
Electroless Plating / Electroless Deposition: The deposition of metal from an auto-catalytic plating solution without application of electrical current. Short for "electroless." This process is required to plate the nonconductive hole walls in order that they may be subsequently electroplated. Also called "PTH."
Electroplating: The electro deposition of a metal coating on a PCB. The board is placed in an electrolyte and connected to one terminal of a DC voltage source. The metal to be deposited is immersed and connected to the other terminal. Ions of the metal provide transfer to metal as they make up the current flow between the electrodes.
Embedded: Resisters, capacitors and small chip die are placed inside the PCB to

increase density.
ENIG: Electroless nickel, immersion gold final finish.
Entrapment: The damaging addition and trapping of air, flux, and/or fumes within solder mask or laminate. It is caused by contamination or improper plating.
Entry Material: A thin layer of composite material or aluminum foil or paper products that is placed on top of the boards to be drilled to improve drill accuracy and prevent burrs and dents.
Epoxy Smear: Epoxy resin that has been deposited onto the surface or edges of the conductive inner layer pattern during drilling. Also called Resin Smear.
ESD: Electrostatic discharge
Etch: Chemical removal of copper to achieve a circuit pattern.
Etch Back: The controlled removal of the glass fibers and epoxy of the base material by a strong chemical process on the sidewall of holes to expose additional internal conductor copper.
Etch Factor: The ratio of the depth of etch (conductor thickness) to the amount of lateral etch (undercut).

F

Fab: Short for fabrication.
Fabrication Drawing: A drawing used to guide construction of a printed board. It shows all the different sizes of holes to be drilled, tolerances, dimensions of the board edges and notes on the materials to be used. Called "fab drawing" for short.
Feed thru via: A plated through hole in a printed circuit board that is used to provide electrical connection between a trace on one side of the printed circuit board to a trace on the other side.
Fiducial: Etched features or drilled hole used for optical alignment during assembly operations.
Fill: Fill yarns lie across the warp direction.
Film Artwork: A positive or negative piece of film containing a circuit, solder mask, or nomenclature pattern.
Fine Line Design: Printed circuit design permitting two to three traces between adjacent chip pins. Typically, 2 mil line, 2 mil space is considered fine line.
Fine Pitch: Refers to chip packages with lead pitches below 0.050". The largest pitch in this class of parts is 0.8 mm, or about 0.031". Lead pitches as small as 0.2 mm (0.008") are used.
Finger: A gold-plated terminal of a card-edge connector.
First Article: A sample part or test board manufactured prior to the start of production to assure that the vendor can produce a circuit that will meet specified requirements.
Fixture: A device that enables interfacing a printed circuit board with a spring-contact probe test pattern.

Flat: A standard size sheet of laminate material, which is processed into one or more circuit boards. Also called panel.
Flex Circuit: Flexible circuit, a printed circuit made of thin, flexible material.
Flip-Chip: A mounting approach in which the chip is inverted and connected directly to the substrate rather than using the more common wire bonding technique.
Flux: A substance used to promote or facilitate fusion such as a material used to remove oxides from surfaces to be joined by soldering.
Flying Probe Tester: An electrical testing machine that uses multiple moving arms to contact two spots on the copper circuitry and send an electrical signal between them. A procedure that determines if a short or open exists.
FR1: A low-grade version of FR2. Tg 130°C.
FR2: A grade of flame-retardant industrial laminate having a substrate of paper and a resin binder of Phenolic. It is used for PCB laminate and cheaper than the woven glass fabrics. Tg 105°C.
FR4: A grade of flame-retardant industrial laminate having a substrate of woven-glass fabric and resin binder of epoxy. FR4 is the most common dielectric material used in the construction of PCBs. Its dielectric constant is from 4.4 to 5.2 at below-microwave frequencies. As frequency climbs over 1 GHz, the dielectric constant of FR4 gradually drops. Tg 150°C to 175°C.
FR6: Fire retardant glass and polyester substrate material for electronic circuits. Inexpensive and popular for automobile electronics.
Fused Coating: A metallic coating (usually tin or solder alloy) that has been melted and solidified, forming a metallurgical bond to the base material.

G

G10: General-purpose epoxy/fiberglass woven fabric PCB material. This has been replaced by a high-grade material such as FR4.
Gerber File: Data file used to control a photo plotter, named after Gerber Scientific Co., who manufactured the original vector photo plotter.
GIL Grade MC3D: A composite laminate comprised of woven glass sheets on both sides of a glass paper core. MC3D exhibits excellent electrical properties with a low and stable Dk and Df.
Glass Transition Temperature (Tg): The temperature at which a polymer changes from a hard and relatively brittle condition to a viscous or rubbery condition. When this transition occurs, many physical properties undergo significant changes. Some of those properties are hardness, brittleness, coefficient of thermal expansion, and specific heat.
Gold/Nickel plating: Used for contact fingers. Common specifications for this plating are: 0.000020" gold over 0.000250" nickel.
Grid: An orthogonal network of two sets of parallel, equidistant lines used for locating points on a printed circuit board.

Ground Plane: A copper conductor layer used as a common reference point for circuit returns, shielding or heat sinking.

H

Haloing: Mechanically induced fracturing delimitation on or below the surface of the base material. It is usually exhibited by a light area around holes or other machines areas, or both.
Heavy Copper PCB: Circuit boards with more than 4 oz. of copper and up to 20 oz of copper for power circuits.
Hermetic sealing: Airtight sealing of an object.
High Density Interconnect (HDI): Very fine lines and thin dielectrics, made with sequential lamination.
Hole Breakout: A hole which is not surrounded by the land.
Hole Density: The quantity of holes in a PCB per unit area.
Hole Void: A void in the metallic deposit of a plated-through hole exposing the base material.
Hole Wall: The vertical surface of a drilled hole of a printed circuit board.
Hot Air Solder Leveling (HASL): A method of coating exposed copper with solder by inserting a panel at 45 degrees into a bath of molten solder, then passing the panel rapidly past a series of hot air jets to remove excess solder.
HPGL Format: HPGL is a Hewlett Packard pen-plot format file generated from almost all CAD systems.

I

Image: That portion on artwork masters, working tools, silk screens, or photo masks that would be considered the photographic image. Also would include images created with photo-resists or silk-screening techniques. Generally, "one image" refers to a single circuit board image; thus there may be several images per flat.
Impedance: A capacitive opposition to the flow of AC electrical current. This term is used to describe how high frequency circuit boards will react.
Ink: Common term for screen resist.
Inner Layer: Any layer that will be laminated into the inside of a multilayer board.
Inspection Overlay: A positive or negative transparency made from the production master and used as an inspection aid.
Insulation Resistance: The electrical resistance of the insulating material as measured between any pair of contacts or conductors.
IPC: The Institute for Interconnecting and Packaging Electronic Circuits.
IPC-A-600: A PCB wide industry quality standard for acceptance of PCBs.
IPC-D-356: A CAD/CAM data exchange format developed by IPC. for use of photo plotting, electrical testing and other CAM functions.
IR: Infrared radiation

ISO: International Standards Organization; i.e. ISO9000.

J

Jumper Wire: An electrical connection formed by wire between two points on a printed board, added after the circuit is etched.

Just-in-Time: A system for producing the right items, at the right time, in the right amounts, for customers.

K

Kerf: A widening of the route path which allows extra space for hardware to be attached to the board.

Keying Slot: A slot in a printed circuit board that polarizes it, thereby permitting it to be plugged into its mating receptacle with pins properly aligned but preventing it from being reversed or plugged into any other receptacle.

L

Laminate: A product made by bonding together two or more composite layers of material.

Laminate Thickness: Thickness of the base material, not including metal-clad, prior to any processing. Applies to single or double-sided material.

Laminate Void: Lack of laminate material or epoxy in an area that normally should contain laminate material.

Laminating Presses: Multilayer equipment that applies both pressure and heat to laminate and prepreg to make multilayer boards.

Lamination: The process of pressing a laminate in a hot high-pressure hydraulic press.

Land: A portion of a copper conductive usually, but not exclusively, used for the connection and/or attachment of components. Also called pad.

Landless Hole: A plated-through hole without land(s). Also referred to as padless plated holes.

Laser Photo Plotter: A photo plotter which uses a laser on a X-Y computerized table to expose film to create the image.

Layer-to-Layer Spacing: The thickness of dielectric material between adjacent layers or conductive circuitry in a multilayer printed circuit board.

Lay-Up: (1) The technique of registering and stacking layers of materials (laminate and pre-preg) for a multilayer board in preparation for the laminating cycle. (2) The laying out of repeat images on film to create multiple groups of circuit boards.

Lead: A terminal on a component used to solder to the board.

Lead Time: The time a customer must wait to receive a product after placing an order.

Leakage Current: A small amount of current that flows across a dielectric area between two adjacent conductors.

Legend: Silkscreen printed letters or symbols on the PCB, such as part numbers and product, typically in white.
LDI: Laser Direct Imaging of dry film.
LPI: Liquid Photo Imageable refers to a liquid photo imageable solder mask or dielectric.

M
Major Defect: A defect that could result in a failure or significantly reduces the usability of the circuit for its designed purpose.
Manufacturability: A term defining the ability of a board design to meet manufacturing requirements.
Manufacturing and Technology Roadmap: A strategic outline of what manufacturing and technology methods, machines and process will be used.
Mask: A material applied to create selective etching, plating, or the application of solder or solder mask to a printed circuit board.
MCM: Multi-Chip Module.
Measling: Condition existing in the base laminate in the form of discrete white spots or "crosses" below the surface of the base laminate, indicating a separation of fibers in the glass cloth at the weave intersection.
Metal Foil: The thin sheets or rolls of conductive material of a printed circuit board from which circuits are formed. Metal foil is generally copper.
Metallurgical Laboratory (Met Lab): The process of inspecting internal board quality characteristics using micro sections.
Micro BGA: Micro Ball Grid Array
Micro Circuits: Very fine lines, 2 mil and less, and small micro vias 3 mil and less.
Microetch: The chemical process of removing a thin layer of copper from the copper surface of an interlayer or outer layer panel, leaving a rough surface topography.
Microinches: A unit a measurement in millionths of an inch. A common unit of measurement in the printed circuit board industry.
Micro Sectioning: The creation of a specimen for the microscopic examination of the material to be examined, usually by cutting out a cross section, followed by encapsulation, polishing, ammonia etching, and staining.
Micro Via: A via used to make connection between two adjacent layers, typically less than 6 mils in diameter. May be formed by laser ablation, plasma etching, or photo processing.
Mil: One-thousandth of an inch 0.001" (0.0254 mm); abbreviation of millionth of an inch.
MIL-P-55110C: A military grade quality standard for acceptance of PCBs.
MIL-STD-275E: A military grade quality standard for design layout of PCBs
Minimum Annular Ring: The minimum metal width, at the narrowest point on a pad between the edge of the drilled hole and the edge of the pad.

Minimum Conductor Width: The smallest width of any conductors, such as traces, on a PCB.
Minimum Electrical Spacing: The minimum allowable distance between adjacent conductors that is enough to prevent dielectric breakdown, corona, or both, between the conductors at any given voltage environmental condition and altitude.
Minor Defect: A defect that is not likely to reduce the usability of the circuit for its intended design. It may be a departure from established standards having no significant bearing to the operation of the circuit.
Mis-registration: The lack of dimensional conformity between successively produced features or patterns.
Mother Board: Also called Back Plane. A large printed circuit board on which modules, subassemblies or other printed circuit boards are mounted and inter-connections made by means of connectors on the board.
Multilayer Circuit Board: A processed printed circuit configuration consisting of alternate layers of conductive patterns and insulating materials bonded together in more than two layers.

N
Nail Heading: The flared condition of copper on the inner conductor layers of a multilayer board caused by hole drilling.
Negative: An artwork master or production master in which the intended conductive pattern is transparent to light and the areas to be free from conductive material are opaque.
Net: A collection of circuit points all of which are, or must be, connected to each other electrically.
Net List: List of names of symbols or parts and their connection points, which are logically connected in each net of a circuit. A net list can be "captured" (extracted electronically on a computer) from a properly prepared CAE schematic.
Node: A pin or lead to which at least two components are connected through conductors.
Nomenclature: Identification symbols applied to the board by screen printing or ink jetting.
Nonfunctional Land: A land on internal or external layers not connected to the copper conductive pattern on its layer.
Non plated hole: A hole in the PCB that is drilled after plating so it is not plated.
Normality: The measure of free acid in a solution. A pH of 7 would be considered normal.

O
Open: An unwanted break in the continuity of an electrical circuit which prevents current from flowing.

OSP: Organic Solderability Preservative.
Outer Layer: The top and bottom sides of a circuit board.
Outgassing: De-aeration or other gaseous emission from a printed circuit board when exposed to the soldering operation or to vacuum.
Overhang: Increase in printed circuit conductor width caused by plating build-up or by undercutting during etching.
Oxide: A chemical treatment to inner layers prior to lamination, for the purpose of increasing the roughness of clad copper to improve laminate bond strength.

P

Pad: The portion of the conductive pattern on printed circuits designated for the mounting or attachment of components. Also called a land.
Pad Stack: In CAD layout EDA systems, pad stack is a collection of pad shape and size information tables.
Panel: The square or rectangular base material containing one or more circuit patterns that passes successively through the production sequence and from which printed circuit boards are extracted, typically, 12″ by 18″ or 18″ by 24″. See back planes.
Panel Plating: The electrolytic plating of the entire surface of a panel (including holes).
Panelize: To lay up more than one (usually identical) printed circuit on a panel. Individual printed circuits on a panel need a margin between them. Lay-up multiple printed circuits called modules, into a sub-panel so that the sub-panel can be assembled as a unit. The modules are then separated after assembly into individual PCB.
Passive Component: A device which does not add energy to the signal it passes, e.g., resistors, capacitors, and inductors.
Pattern: The series of conductive copper and dielectric materials on a panel or printed circuit board. Also, the circuit design on related tools, drawings, and masters.
Pattern Plating: Selective electrolytic plating of a copper pattern.
PBGA: Plastic Ball Grid Array.
PC Board: Printed circuit board also called PCB or Printed Wiring Board (PWB).
PCB Design: The creation of artwork for the manufacture of bare PCBs on a computer database used to generate such artwork as data files (CAM files). Also called PCB layout.
PCB Design Service Bureau: A business engaged in PCB design as a service for others, especially electrical engineers. Also called PCB design shop.
Peel Strength: The force required to peel the conductor or foil from the base material.
Permittivity Measure: The ability of a material to store electrical energy when exposed to an electrical field.

Pick and Place: A manufacturing assembly process in which components are selected and placed onto specific locations according to the assembly file of the design.

Photo Mask: A silver halide or Diazo image on a transparent substrate that is used to either block or pass light.

Photo Plotter: A high-accuracy (>0.001 inch) flatbed or rotary plotter with a programmable, photo image projector assembly. It is most often used to produce actual size master patterns for printed circuit artwork directly on dimensionally stable, high-contrast photographic film.

Photo-Resist: A light-sensitive material that is used to establish an image by exposure to light and chemical development.

Pilot Order: First production order going through process.

Pinhole: A minute hole through a layer or pattern.

Pink Ring: A colored area around via and through holes caused by oxide application.

Pitch: The nominal distance between the centers of adjacent features or traces on any layer of a printed circuit board. Also known as "center-to-center spacing".

Plasma: A highly ionized gas containing an approximately equal number of positive ions and negative electrons. It is electrically neutral, though conductive and affected by magnetic fields. Used to clean contaminants off a PCB.

Plastic Leaded Chip Carrier (PLCC): An SMT chip package that is rectangular or square-shaped with leads on all four sides.

Plated Through Hole (PTH): A hole in a circuit board that has been plated with metal (usually copper) on its sides to provide electrical connections between conductive pattern layers.

Platen: A flat plate of thick metal within the lamination press, in between which stacks of pre stacked circuits are placed to be pressed.

Plating: Chemical or electromechanical deposition of metal on a pattern.

Plating Resists: Material that, when deposited on conductive areas, prevents the plating of the covered areas. Resists are available both as screened-on materials and as dry-film photopolymer resists.

Plating Void: The absence of a plating metal from a specified plating area.

Plotting: The mechanical converting of X-Y Gerber positional information into a visual pattern, such as artwork.

Polyimide Resins: High temperature thermoplastics used with glass to produce printed circuit laminates for multilayer and other circuit applications requiring high temperature performance.

Polymerize: To unite chemically two or more monomers or polymers to form a molecule with a higher molecular weight.

Positional Limitation Tolerancing: Defines a zone within which the axis or center plane of a feature which is permitted to vary from true (theoretically exact) position.

Pre-clean: Pre-cleaning steps taken prior to an operation to ensure success of the operation.
Pre-Preg: Sheet material consisting of the base material impregnated with a synthetic resin, such as epoxy or Polyimide, partially cured to
the B-stage (an intermediate stage). Short for pre-impregnated. See also B- stage.
Press-Fit Contact: An electrical contact that can be pressed into a hole in an insulator, printed board (with or without plated-through holes) or a metal plate.
Printed Circuit: A conductive pattern of printed components and circuits attached to a common base.
Printed Circuit Board (PCB): The general term for a printed or etched circuit board. It includes single, double, or multiple layer boards, both rigid and flexible.
Printed Wiring Board: Another name for a Printed Circuit Board.
Production Master: A 1:1 scale pattern that is used to produce one or more printed boards (rigid or flexible) within the accuracy specified on the master drawing.
Prototype: Manufacturing small initial quantities, in short production runs, of an electronic product for testing.
PTFE: Woven Teflon glass materials, with exceptionally well controlled electrical and mechanical properties. The dielectric constant range is 2.45 to 2.65 used for RF applications.
Pulse Plating: A method of plating that uses electrical pulses instead of a direct current.

Q

Quality Control (QC): A precise system of measurements to ensure the PCB meets the desired specifications. Also called Quality Assurance (QA).
Quick-Turn: Ability to produce a small lot of a product in a relatively short time; i.e. fabricating a printed circuit board in 24 hours from receipt of the design data.

R

Radial Lead: A lead extending out the side of a component, rather than from the end.
RCC: Resin coated copper.
Reflow: A process to form a solder joint by providing heat to the solder paste.
Reflowing: The melting of an electro deposit tin lead. The surface has the appearance and physical characteristics of being hot-dipped.
Registration: The amount of conformity of the true position of a pattern with its intended position to that of any other point.
Residue: An undesirable substance remaining on a substrate after a process step.
Resin Smear: Melted epoxy resin transferred from the base material onto the surface or edge of the conductive pattern normally caused by drilling. Sometimes called epoxy smear.

Resin-Starved Area: A region in a printed circuit board that has an insufficient amount of resin to wet out the reinforcement completely evidenced by low gloss, dry spots, or exposed fibers.
Resist: Coating material used to mask or to protect selected areas of a pattern from the action of an etchant, solder, or plating. Also see Dry Film, Plating Resists and Solder Resists.
Resistivity: The ability of a material to resist the passage of electrical current through it.
Reverse Image: The resist pattern on a printed circuit board enabling the exposure of conductive areas for subsequent plating.
Rework: Reprocessing that makes articles conform to specifications.
RF: Radio Frequency.
Rigid/flex: A PCB construction combining flexible circuits and rigid multi- layers, to provide a direct connection or to make a three-dimensional form that may include components.
Robber/Thieves: An exposed area generally attached to a rack used in electroplating, usually to provide a more uniform current density on plated parts. Robbers are intended to absorb the unevenly distributed current on parts, thereby assuring that the parts will receive a uniform electroplated coating.
RoHS: Part of the European Union Directive 2002/95/EC1. This Directive on the "Restriction on the use of certain Hazardous Substances in electrical and electronic equipment". This directive bans or severely curtail the use of lead, chromium, mercury, polybriminated biphenyls, cadmium and polybrominated diphenyl ethers in all products from automobiles to consumer electronics.
Router: A CNC machine that removes portions of the panel to release the individual board with the desired shape and size required from the production panel.

S

Schematic Diagram: A drawing that shows, by means of graphic symbols, the electrical connections, components, and functions of an electronic circuit.
Scoring: A machine in which grooves are cut on opposite sides of a panel to a depth that permits individual boards to be separated from the panel after the component assembly.
Screen: A cloth material (usually polyester or stainless steel for circuit boards) coated with a pattern that determines the flow and location of coatings forced through its openings.
Screen Printing: A process for transferring an image to a surface by squeezing suitable ink through a stencil screen with a squeegee. Also called Silk Screening.
Selective Plate: A process for plating unique features with a different metal than the remaining features will have. Created by imaging, exposing, and plating selected area and then repeating the process for the remainder of the board.

Shadowing: A condition occurring during etch back in which the dielectric material, in contact with the foil, is incompletely removed although acceptable etch back may have been achieved elsewhere.
Short Circuit: An abnormal connection of relatively low resistance between two points of a circuit. The result is excess (often damaging) current between these points.
Single Sided Board: Circuit board with copper conductors on only one side and no plated-through holes.
Solder Leveling: The process of dipping printed circuit boards into hot solder and leveling with hot air.
Solder Mask: An ink coating applied to a circuit board to prevent solder from flowing onto any areas where it is not desired or from bridging across closely spaced conductors.
Solder Mask Over Bare Copper (SMOBC): A method of fabricating a printed circuit board with the final copper metallization under the solder mask with no protective metal. The non-coated areas are coated by solder resist, exposing only the component terminal areas. This eliminates tin lead under the components which will reflow causing a blemish.
Solder Masking Coating: A term for a liquid resist.
Solder Paste: A paste form of solder to be screen or ink jet printed on SMT pads during assembly prior to soldering.
Solder Resists: Coatings that mask and insulate portions of a circuit pattern where solder is not desired.
Solder Wick: A woven band of wire removes molten solder away from a solder joint or a solder bridge or just for desoldering.
Solderability Testing: The evaluation of a metal to determine its ability to be wetted by solder.
Squeegee: The tool used in silk screening that forces the resist or ink through the mesh.
Stacked Vias: Micro vias in HDI stacked one upon each other.
Starvation Resin: A deficiency of resin in base material that is apparent after lamination by the presence of weave texture, low gloss, or dry spots.
Stencil: Stencil is a copper or nickel foil screen with SMD pads etched openings used for solder paste screen printing in assembly.
Step and Repeat: A computerized method by which successive copies of a single image are laid up to produce a multiple-up filling of the panel.
Strip: The chemical removal of developed photo resist or plated metal.
Substrate: See Base Material.
Subtractive Process: A process in printed circuit manufacturing
where the product is built by the subtraction of an already existing metallic coating. The opposite of additive processing.
Surface Mount Technology (SMT): Defines the entire body of the process and

components that create printed circuit board assembly with leadless components.

T

Td: Temperature of decomposition, where the circuit loses 5% of its volume due to outgassing.

Tg: Glass transition temperature, in degree C, the point at which the material starts to become soft and plastic like. Also, the point where the Z axis starts to expand non-linearly.

Teardrop: A widening of the trace near the pad for strengthening the connections between pads and tracks. Typically used when the annular ring is 0.005" or less but not needed.

Temperature Coefficient (TC): The ratio of a quantity change of an electrical parameter, such as resistance or capacitance, of an electronic component to the original value when temperature changes, expressed in %/ºC or ppm/ºC.

Tented Via: A via with dry film solder mask completely covering both its pad and its plated-thru hole. This completely insulates the via from foreign objects, thus protecting against accidental shorts.

Test Coupon: A sample or test pattern normally made outside the actual board pattern that is used for testing to verify certain quality parameters without destroying the actual board.

Thermal Relief or Heat Relief: A thermal relief or heat relief is a type of pad used at a location where there is a connection to a copper plane. The purpose of using a thermal relief pad is to provide a connection while dissipating heat through the big copper plane.

Through Hole: A plated hole on a circuit board used for component pins leads. The holes are plated creating a circuit between multilayers.

Thieve: Adding copper to balance out the electroplating processes.

Tooling Holes: Two specified holes on a printed circuit board used to position the board in order to mount components accurately.

Top Side: The component side.

Trace: A common term for the copper conductors.

Traveler: A "recipe" for the manufacture of a board. It "travels" with each order from start to finish. The traveler identifies each order and gives instructions for each step in the process.

Two-Sided Board: See Double Sided Board.

U

Underwriters Laboratory (UL): Certifying agency for consumer electronics. See also Underwriters Symbol.

Underwriters Symbol: A logotype denoting that the product has been recognized by Underwriters Laboratory Inc. (UL).

UV Cure: Polymerizing hardening or cross inking a material by exposing to ultra-violet light.

V

V-Scoring (Scoring): A board profiling process that involves cutting straight tapered lines from both sides of board, suitable for medium to large volume production with panels requiring only straight-line cuts. With this process, minimum space is needed between units and the panel can be assembled as a larger board.
Via: A plated thru hole that is used as an inner layer connection but doesn't have a component lead in it.
Void: The absence of substances in a localized area (e.g., air bubbles).

W

Warp: Warp yarns are the ones that lie in the length (machine direction) of the fabric. The warp direction is also commonly called the grain direction. This is usually marked on the material to ensure the materials for the different layers are oriented the same way. The opposite direction is called fill.
Warping: Warping generally refers to finished board warp and twist. All boards may have a certain degree of warp as a result of manufacturing. Customers will specify the warping tolerance.
Wave Soldering: A process wherein assembled printed boards are brought in contact with a continuously flowing and circulating mass of solder.
Wicking: Migration of conductive copper chemicals into the glass fibers of the insulating material around a drilled hole.
WIP: Work In Progress.
Wire Bonding: A method used to attach very fine wire to semiconductor components (dice) to interconnect these components with each other or with package leads. The gold or aluminum wires 1 to 2 mils in diameter.

X Y Z

Young's Modules: A measurement as to the amount of force an object applies as it contracts or expands due to temperature change, expressed in Mpsi or Gpa.
Zero Defects Sampling: A statistical based attribute sampling plan where a given sample of parts is inspected and any defects found are cause for rejection of the entire lot.

Engineering Data

One oz. of copper is 1.39 mils thick; one mil is 25.4 microns

Voltage E=I * R

Notation and Formula

C	capacitance	Farads	F
E	voltage source	Volts	V
e	Instantaneous E	Volts	V
G	conductance	Siemens	S
I	current	Amps	A
i	instantaneous I	Amps	A
k	coefficient	Number	#
L	inductance	Henrys	H
M	mutual inductance	Henrys	H
N	number of turns	number	#
P	power	Watts	W
Q	charge	Coulombs	C
q	instantaneous Q	Coulombs	C
R	resistance	Ohms	Ω
T	time constant	Seconds	S
t	instantaneous time	Seconds	S
V	voltage	Volts	V
v	instantaneous	Volts	V
W	energy	joules	J

Conversion Factors

10^{12}	tera	T
10^{9}	giga	G
10^{6}	mega	M
10^{3}	kilo	K
10^{-1}	deci	d
10^{-2}	centi	c
10^{-3}	milli	m
10^{-6}	micro	µ
10^{-9}	nano	n
10^{-12}	pico	p

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