```
1   ----------------------------------------------------------------------------------
2   -- Company:
3   -- Engineer:
4   --
5   -- Create Date:    09:08:42 02/02/2009
6   -- Design Name:
7   -- Module Name:    Taktteiler - Behavioral
8   -- Project Name:   FPGA-VHDL-Training
9   -- Target Devices: Spartan 3A DSP 1800 Board
10  -- Tool versions:
11  -- Description:    Hello World mit dem FPGA
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  --use IEEE.STD_LOGIC_ARITH.ALL;
23  --use IEEE.STD_LOGIC_UNSIGNED.ALL;
24  use IEEE.NUMERIC_STD.all;
25
26  ---- Uncomment the following library declaration if instantiating
27  ---- any Xilinx primitives in this code.
28  --library UNISIM;
29  --use UNISIM.VComponents.all;
30
31  entity Taktteiler is
32      Port (  CLK_tt               :  in    STD_LOGIC;
33              Takt_in_tt           :  in    integer range 0 to (125000000/2-1);
34
35              x_tt                 :  inout integer range 0 to (125000000);
36              y_tt                 :  inout integer range 0 to (125000000);
37              A_tt                 :  inout integer range 0 to (125000000);
38              B_tt                 :  in    integer range 0 to (125000000);
39
40              frequenz_zaehler_tt  :  out   integer range 0 to (125000000/2-1);
41
42              sub_fertig_tt        :  inout STD_LOGIC);
43
44  end Taktteiler;
45
46  architecture Behavioral of Taktteiler is
47
48  begin
49
50  process(CLK_tt,sub_fertig_tt)
51  begin
52     if rising_edge(CLK_tt) then
53           if x_tt >= B_tt then
54              y_tt <= y_tt + 1;
55              x_tt <= A_tt - B_tt;
56              A_tt <= x_tt;
57           else
58              sub_fertig_tt <= '1';
59              frequenz_zaehler_tt <= y_tt - 1;
60           end if;
61        end if;
```

```
62            end if;
63        end process;
64
65        end Behavioral;
66
67
```