----------------------------------------------------------
LIBRARY ieee;
USE ieee.std\_logic\_1164.ALL;
USE ieee.std\_logic\_arith.ALL;
USE IEEE.std\_logic\_unsigned.ALL;
----------------------------------------------------------
ENTITY frequenzteiler IS
    PORT(
        clk                : in    std\_logic;
        reset\_n            : in    std\_logic;
        clk\_out         : out   std\_logic

        );
END frequenzteiler ;
----------------------------------------------------------
architecture beh of frequenzteiler  is

signal    test\_sig\_1         :   std\_logic;
signal   clk\_temp        :   std\_logic;
signal   count           :   std\_logic\_vector( 24 downto 0 );--(25000000/4 -1)24

begin

fret:process(clk,clk\_temp,reset\_n)
    begin
        if clk'event and clk = '1' then
------------------------------------------------
         if (reset\_n = '0') then
         clk\_temp <='0';
         count <= (others =>'0') ;-- setze alle bit auf null
          else
          count <= count + 1;
          if count = "10111110101111000001111" then
          clk\_temp <= not clk\_temp;
          count <= (others=>'0');
          end if;
         end if;  --  x"17D7840"
------------------------------------------------
        end if;
    end process fret;
    clk\_out <= clk\_temp;

  end beh;
----------------------------------------------------------