Capacitive divider
For the capacitive voltage divider consisting of C_1 and C_2, the values in the same range as the $C_{\max}$ have been chosen, so $C_1 = C_2 = 22\,\mathrm{pF}$. This should allow for a loop gain of $G_{\mathrm{LG}} \geq 3\,\mathrm{dB}$.

The circuit with the element values is shown in Fig. 11.5. The values of C_k and R_k are empirically determined by means of a SPICE simulation, whereas R_E was initially chosen to $1\,\mathrm{k\Omega}$.

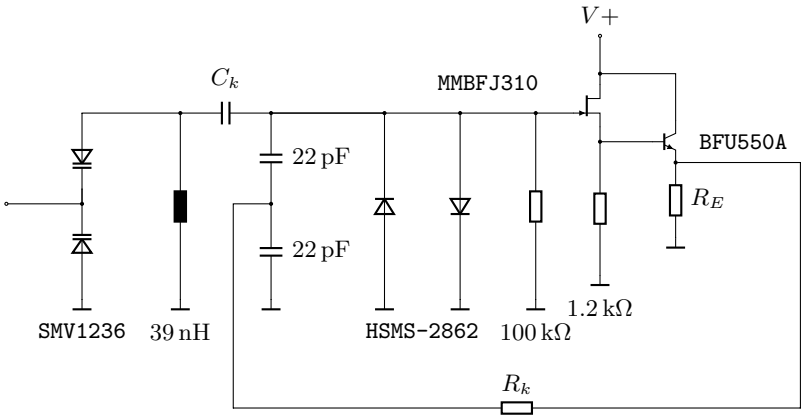

Fig. 11.5. The designed Goral VCO

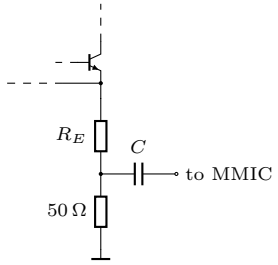

Fig. 11.6. Output network to couple a MMIC to the VCO

Output coupling
The output of the oscillator should not be directly connected to a load. This is because the load dissipates power and thus may lower the loop gain. To overcome such problems, an MMIC amplifier is used as output buffer. This has the advantage that the MMIC will provide a $50\,\Omega$ output. To couple the MMIC to the oscillator, the emitter network of the output transistor is slightly modified, as shown in Fig. 11.6. Such a network presents a $50\,\Omega$ source impedance to the MMIC, while isolating the tank from the influence of C. The output amplitude may be adjusted by changing R_E.

11.2.1 Loop Gain Analysis

A loop gain analysis is performed with $V_{\mathrm{tune}} = 0\,\mathrm{V}$ and $V_{\mathrm{tune}} = 12\,\mathrm{V}$. For this first simulation, the values $R_k = 10\,\Omega$ and $C_k = 22\,\mathrm{pF}$ were used. The loop is cut open between R_E and R_k. An AC source is then connected to the open end of R_k, while the voltage across R_E is measured. The resulting frequency response is shown in Fig. 11.7.

Following observations can be made:

- The loop gain stays almost constant, which is the desired behaviour.
- The frequency range is wrong: from $\approx 170\,\mathrm{MHz}$ to $\approx 240\,\mathrm{MHz}$.

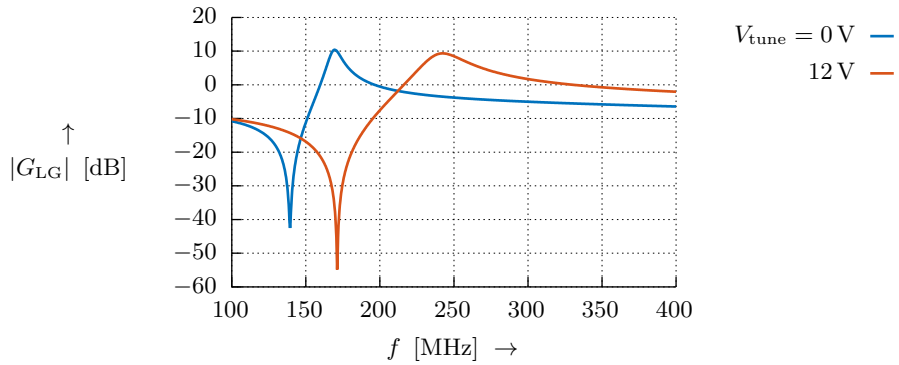

Fig. 11.7. Loop gain of the initial VCO design

Due to these observations, the design must be optimised. First, the frequency shall be corrected. For this, the influence of C_k on f_m is analysed at $V_{\mathrm{tune}} = 0\,\mathrm{V}$. The resulting frequency response is shown in Fig. 11.8.

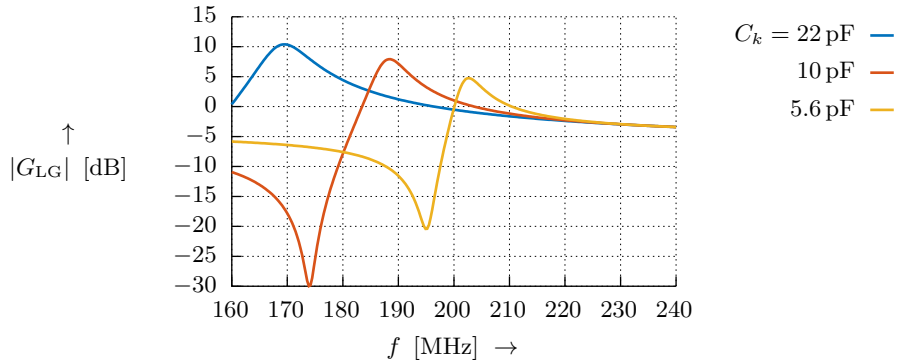

Fig. 11.8. Loop gain of the VCO as the coupling capacitor is varied

With $C_k = 5.6\,\mathrm{pF}$, the loop gain is $\approx 5\,\mathrm{dB}$, which is sufficient, but f_m is too high ($> 200\,\mathrm{MHz}$). Therefore, $C_k = 10\,\mathrm{pF}$ is selected. Since the loop gain is high, about 8 dB, the feedback resistor R_k is optimised next. It makes sense that the loop gain becomes smaller if R_k is increased. The resulting frequency response for varying R_k is shown in Fig. 11.9. With a value of $33\,\Omega$, a G_{LG} of about 4 dB can be obtained which is sufficient.

Since C_k is also a frequency-determining component and it has been optimised previously, the frequency range of the VCO must be checked. To do this, G_{LG} is plotted for different tuning voltages V_{tune}. The resulting frequency response is shown in Fig. 11.10.

It can be observed that the lowest f_m is about 190 MHz and the highest f_m is about 320 MHz. This is sufficient for the VCO's tuning range. To be sure that the oscillator will be stable, the loop phase must also be checked. It should be 0° at the resonant peak. The corresponding Bode diagram is shown in Fig. 11.11.

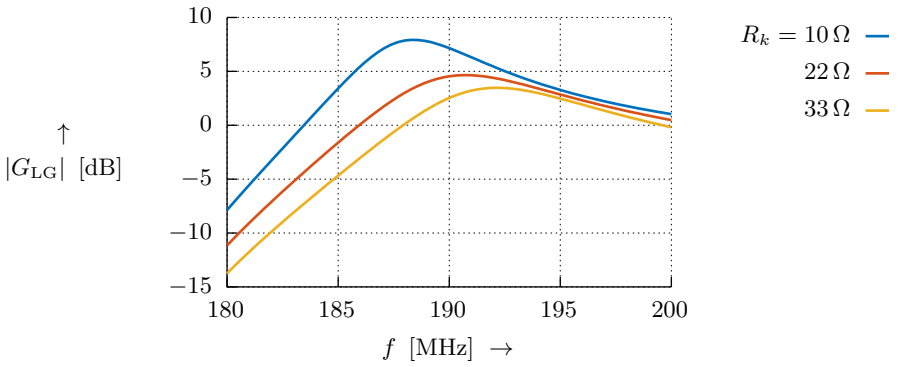

Fig. 11.9. Loop gain of the VCO as the feedback resistor is varied

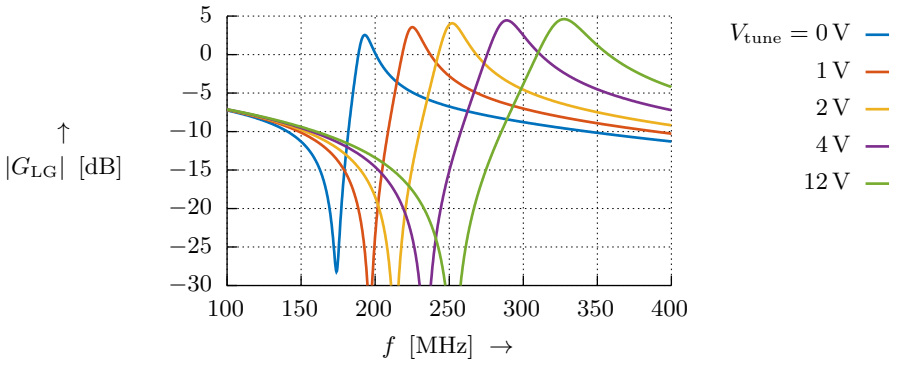

Fig. 11.10. Loop gain of the VCO for different tuning voltages

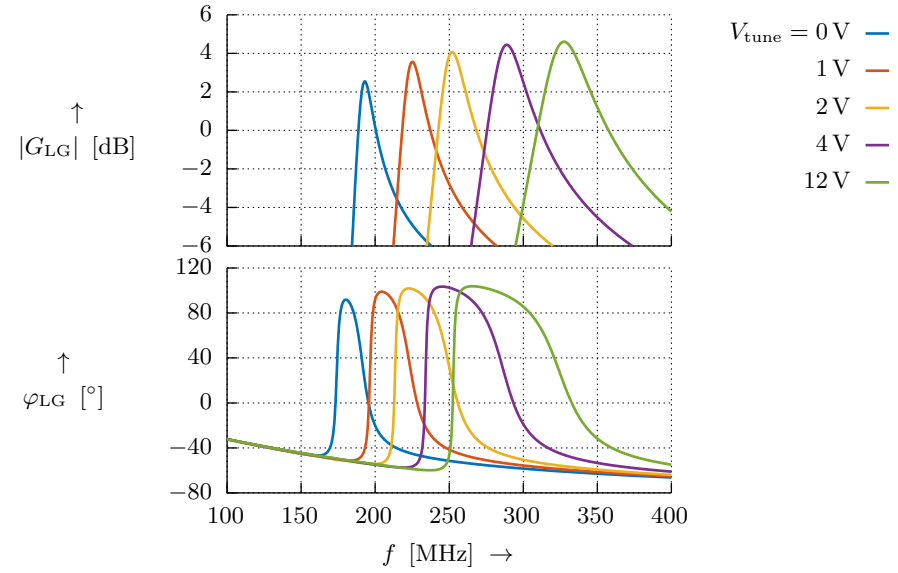

Fig. 11.11. Bode diagram showing loop gain and loop phase