MEDIATEK

MT6252 Design Notice

V0.1

2010/12/10

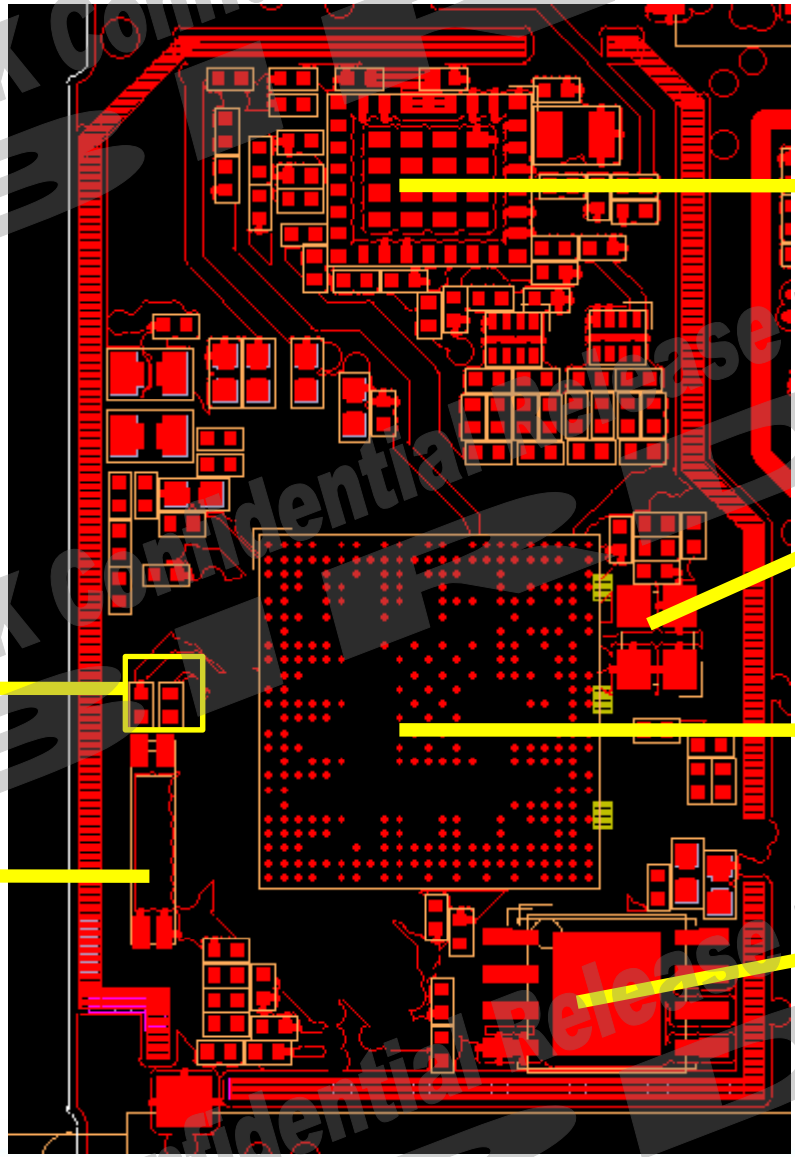
Confidential B

Baseband design notice

MT6252 Design notice Quick View

Function	MT6253	MT6252	Importance Quick view
BB	2 HW trapping pins	3 HW trapping pins	1.Pin HW notice 2.SRCLKENAI notice
Memory	ADMUX NOR+PSRAM	Serial Flash	1.Pin connection
PMU	BackLight with booster	BackLight with VBAT	1.Low bat LCM flicker
Charger	Linear charger	Pulse charger	1.Pulse charger 2.Important SW setting 3.Nokia Charger support
Audio	Class-D / AB Amp	Class-AB Amp	1. 2 in 1 application 2. Important part placement
Speech	SW algorithm	Same with 53	1. Important part placement
Camera	2M	VGA	1.Reference design
LCM	2.8V IO LCM	1.8V IO LCM	1. 1.8V IO LCM
MSDC	4 bit IO	1 bit IO	1.IOT 2.DAT3 as Card detect
RF	Quad band SOC	Same with 53	1.Schematic notice 2.Layout notice 3.BPI modification

Placement notice



TXM(PRF88144B)
+Rx SAWs

26MHz crystal ,
must close to BB

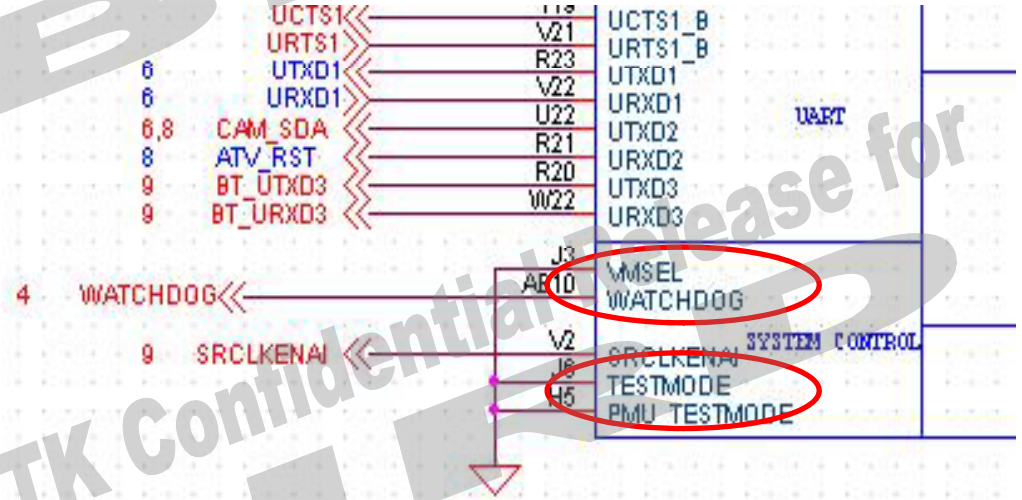
C-load,
Must close 32.768KHz

MT6252 SOC

32.768KHz crystal ,
must close to BB

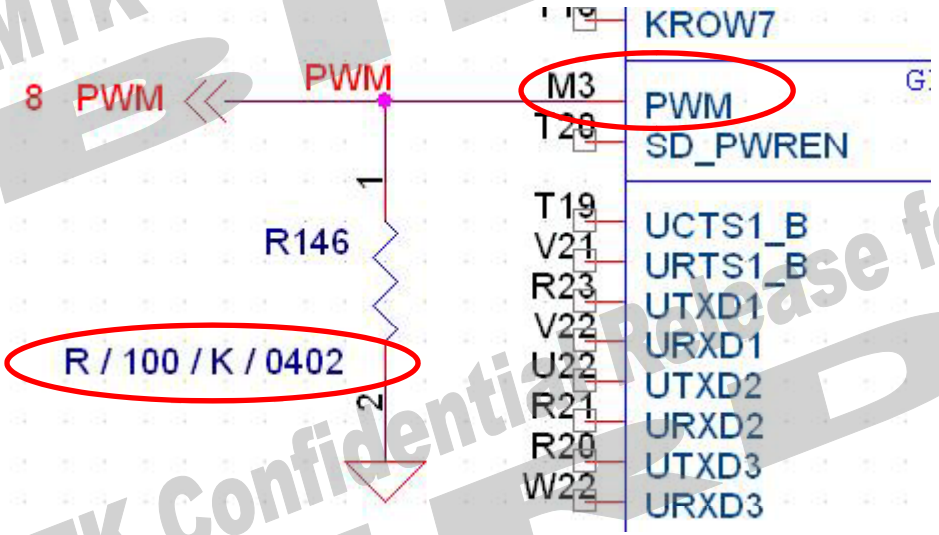
Serial Flash ,
must close to BB

MT6252 Chip configuration design notice (BB)

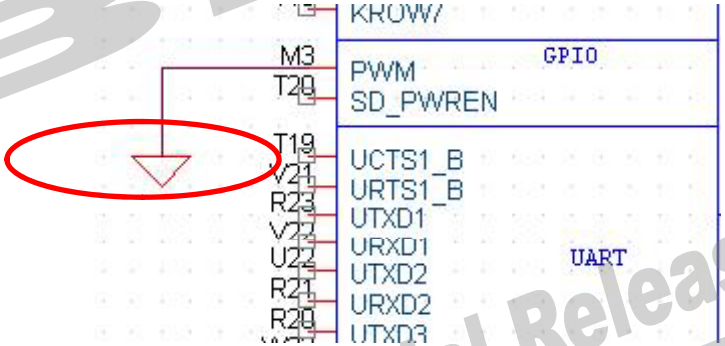


1.TESTMODE(Pin J6) should be connected to ground.
2.PMU_TESTMODE(Pin H5) should be connected to ground.
3.VMSEL(Pin J3) should be connected to ground.

MT6252 Chip configuration design notice (BB)

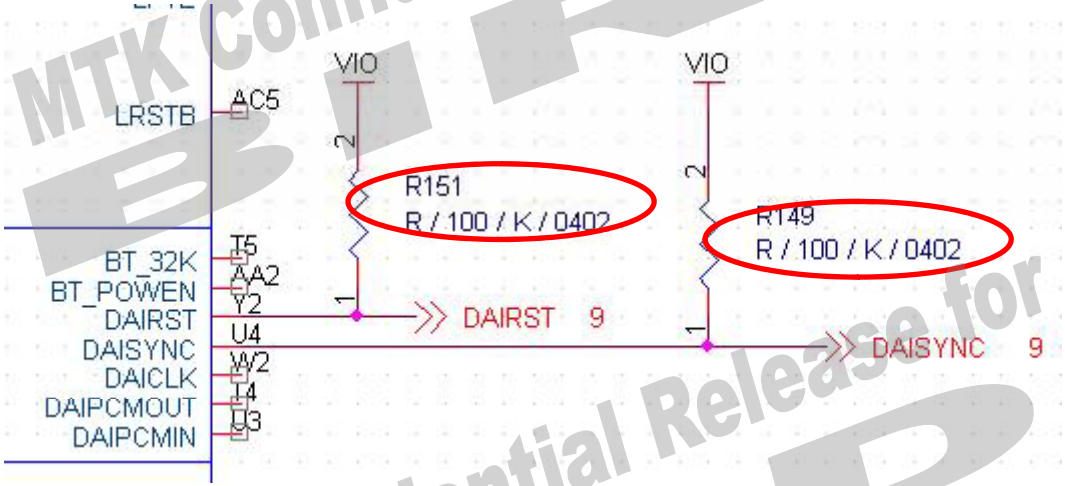


1.There should be a 100K ohm resistor connected to ground on PWM if PWM is used.

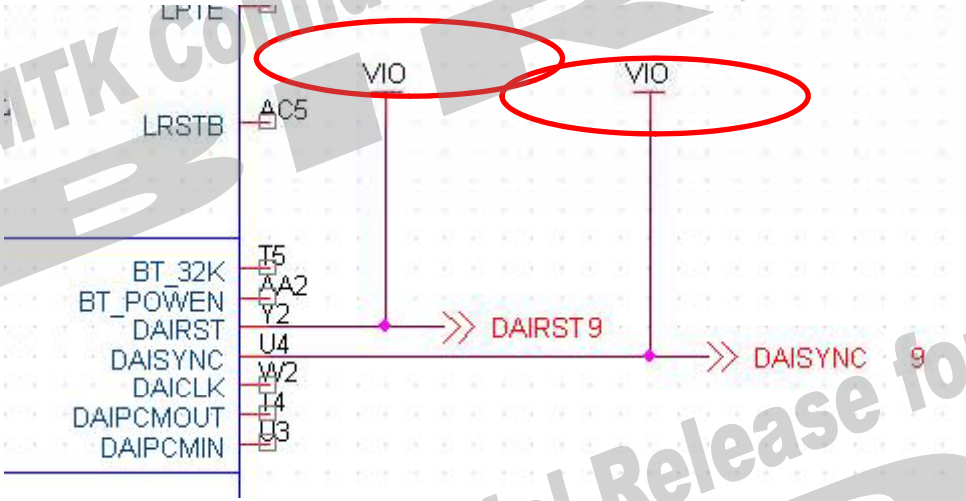


2.You can connect PWM to ground directly if PWM is not used. But please must configure this as GPIO input mode and pull up should not be enabled.

MT6252 Chip configuration design notice (BB)

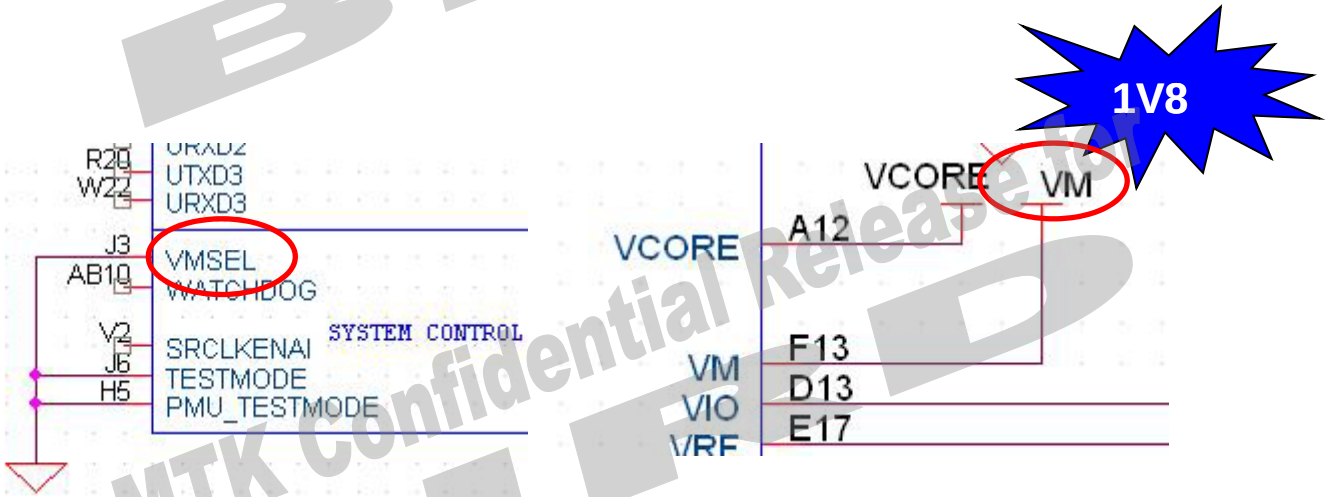


1.There should be a 100K ohm resistor connected to VIO on DAIRST and DAISYNC.



2.You can connect DAIRST and DAISYNC to VIO directly if these 2 pin are not used for any other function. But please must configure this as GPIO input mode and pull down should not be enabled.

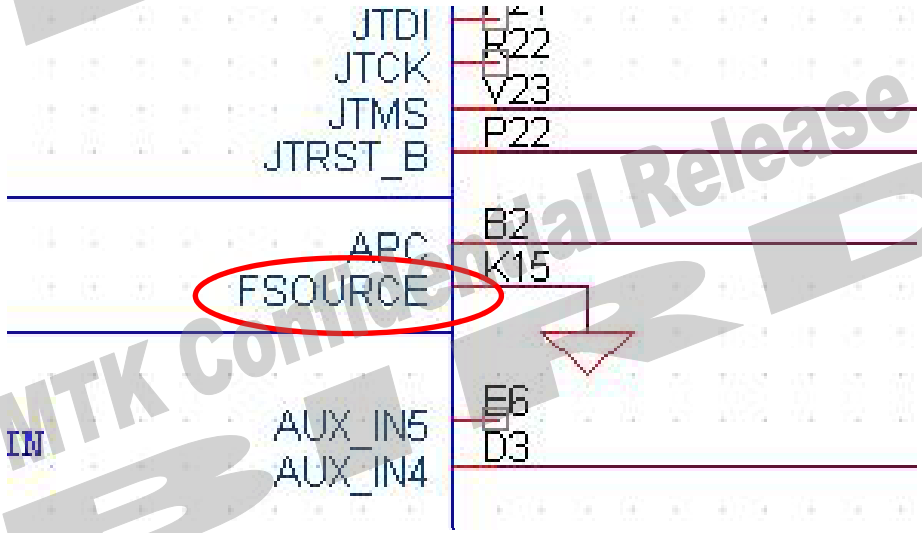
MT6252 Chip configuration design notice (BB)



1.VM_SEL connected to ground ➔ VM = 1.8V.

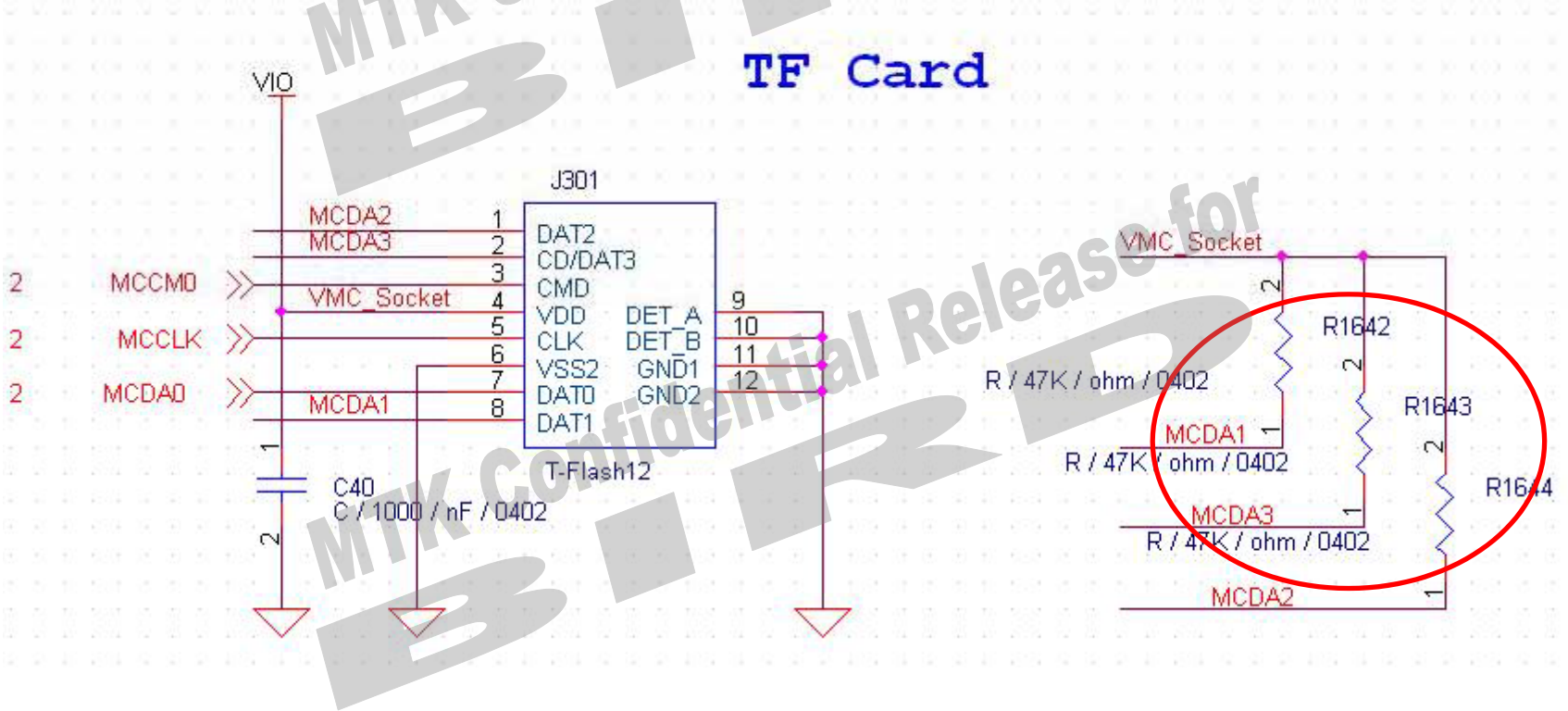
MT6252 only support 1.8V memory. VMSEL should always be low.

MT6252 Chip configuration design notice (BB)



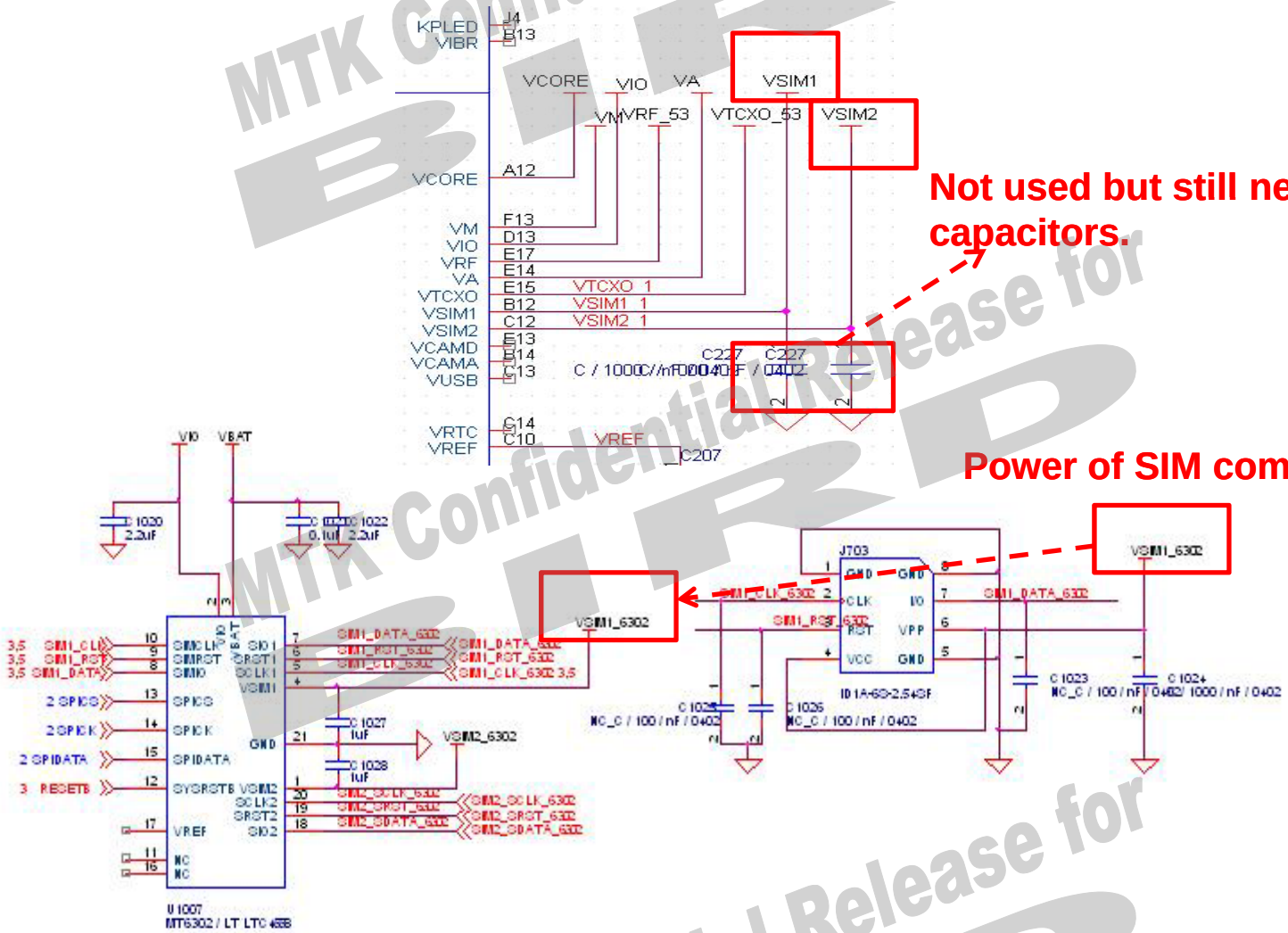
1.FSOURCE should be connected to ground.

MT6252 Chip configuration design notice (MSDC)



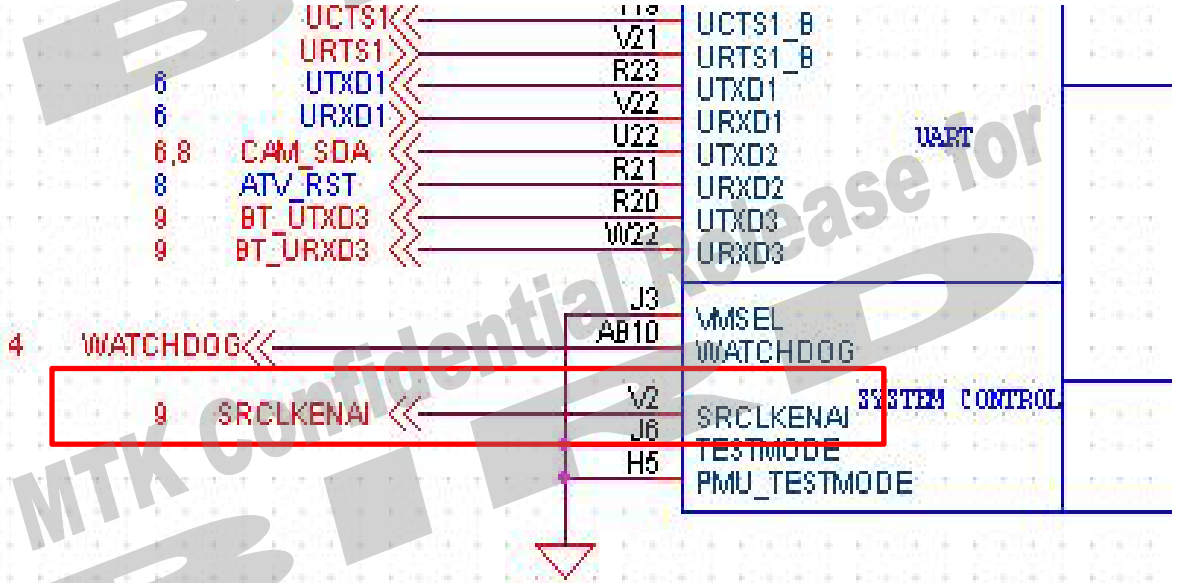
1. MT6252 only support 1 bit MSDC. If DAT3 is not used as card detection , DAT1~3 on memory card socket side should be pulled to VIO by 47Kohm.
2. You also can enable internal pull up but reserving SMT space for external pull up resistors is recommended.

MT6252 Chip configuration design notice(4 SIM)



1. Please remember to add bypass capacitors on VSIM1 and VSIM2 even these 2 LDOs are not used in 4 SIM application.

MT6252 Chip configuration design notice (SRCLKENAI)



1. Please remember to enable internal Pull down when this pin is used as 26MHz clock request from 6252. (In general , this is used by BT)

Confidential B

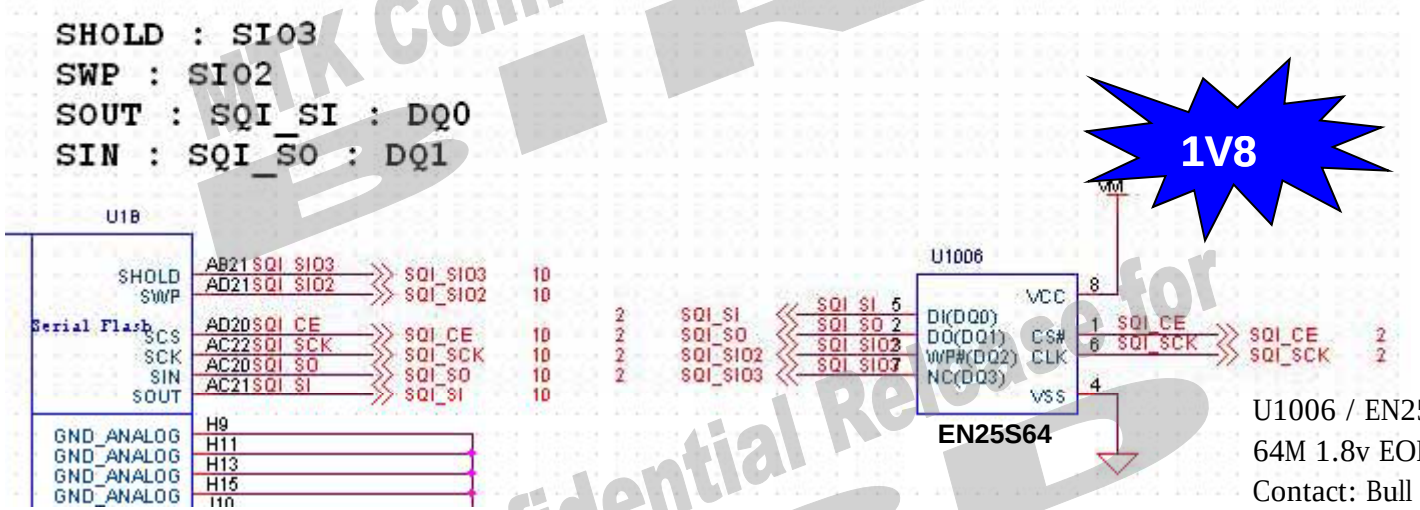
Memory design notice

EMI and Nand interface difference between MT6253/53D and MT6252

	MT6253	MT6253D	MT6252
Interface	NOR+PSRAM	NOR+PSRAM	Serial Flash with stacked PSRAM
Mode	1.Async 2.Sync Burst	1.Async 2.Sync Burst	Sync QPI
Clock Rate	104MHz	52MHz	Serial Flash : 78MHz / 104MHz PSRAM : 104MHz
EMI voltage	1.8V	1.8V	1.8V

1.MT6252 support 78MHz and 104MHz QPI mode Serial Flash.
2.The power domain of Serial flash is same as internal stacked PSRAM.So , please use 1.8V serial flash instead of 3V.

MT6252 Chip memory configuration design notice



6252

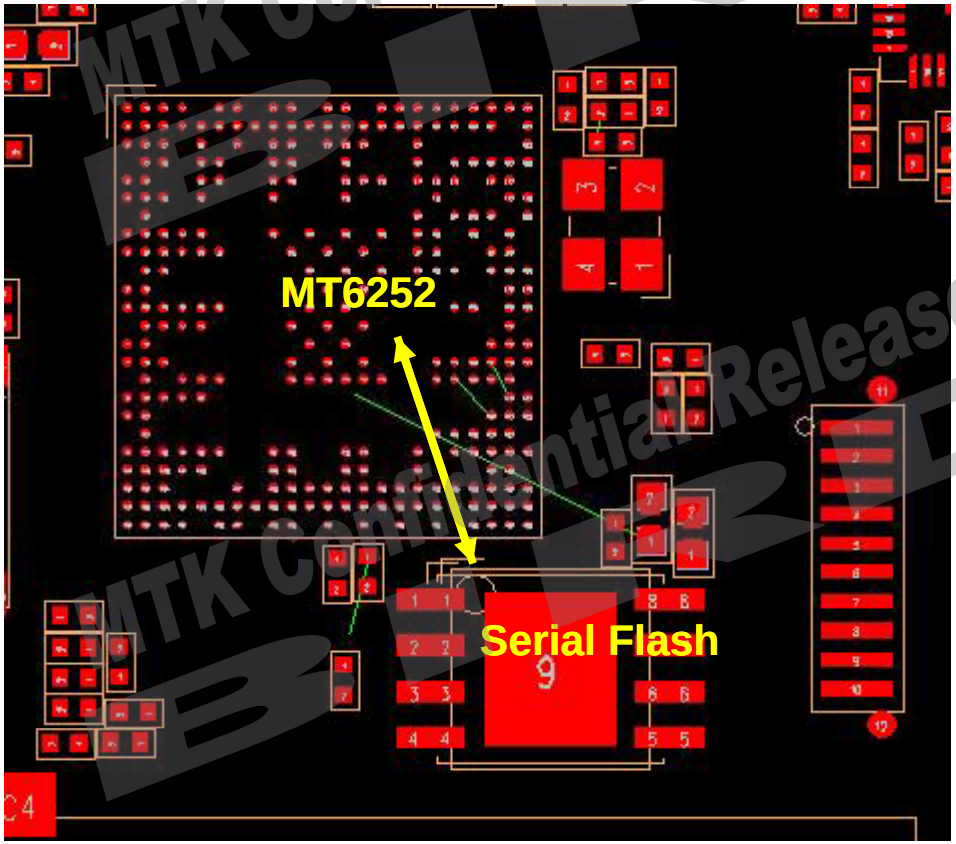
Serial Flash
(must be 1.8V)

U1006 / EN25S64
64M 1.8v EON
Contact: Bull Tang
bull1975@gmail.com 13502888931

Please connect the pins according to following table.

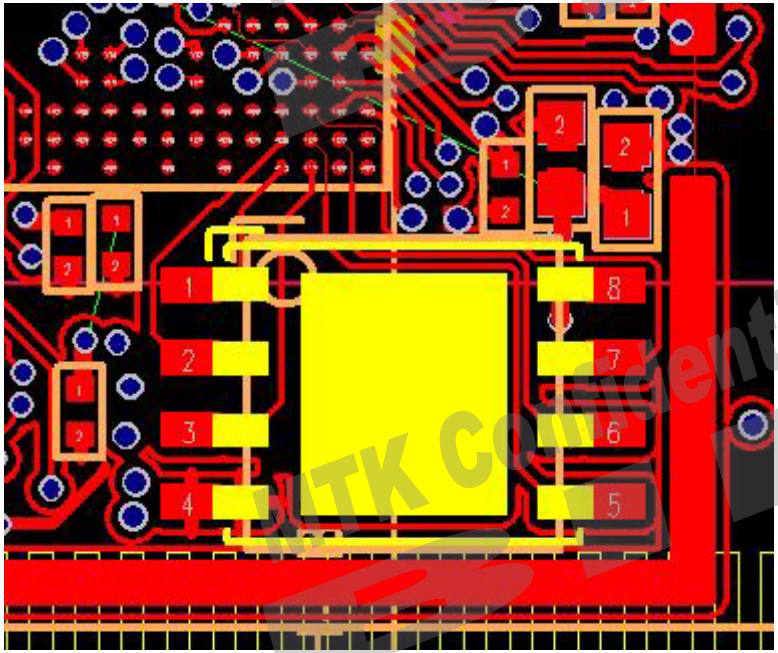
	6252	Serial flash
Interface	SHOLD	DQ3
	SSWP	DQ2
	SIN	DQ1
	SOUT	DQ0
	SCS	Chip enable
	SCK	CLK

MT6252 Memory Layout design notice

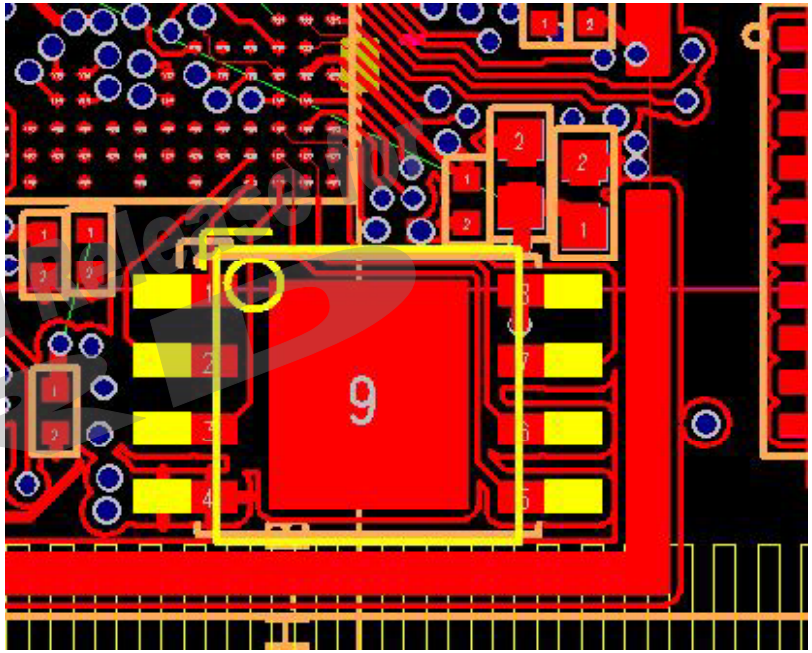


Memory should be placed as close to MT6252 as possible.

MT6252 Memory Layout design notice



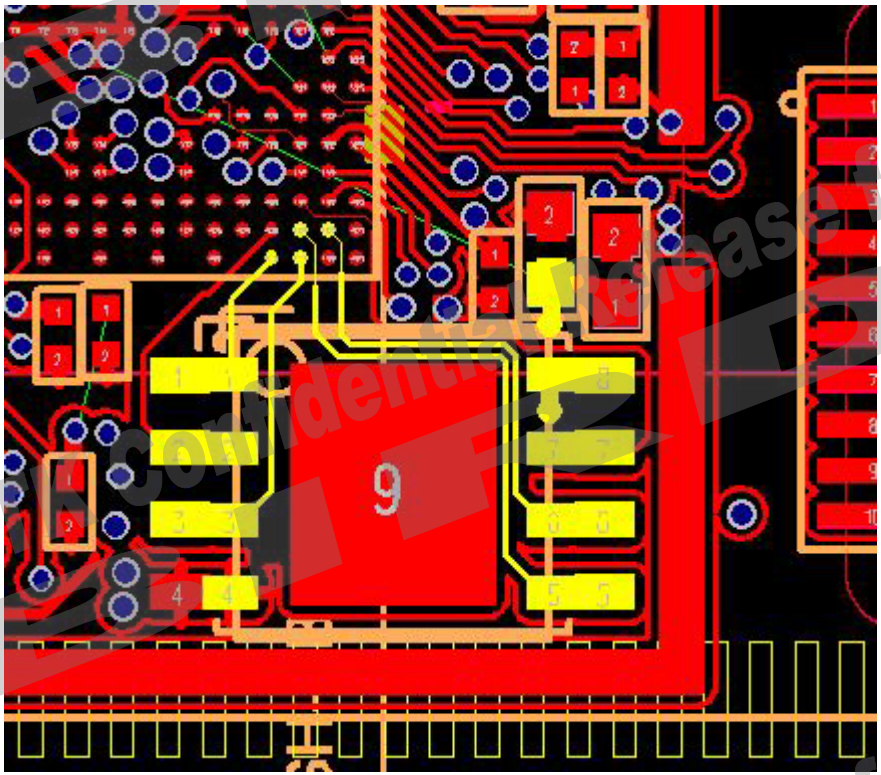
WSON



TSOP

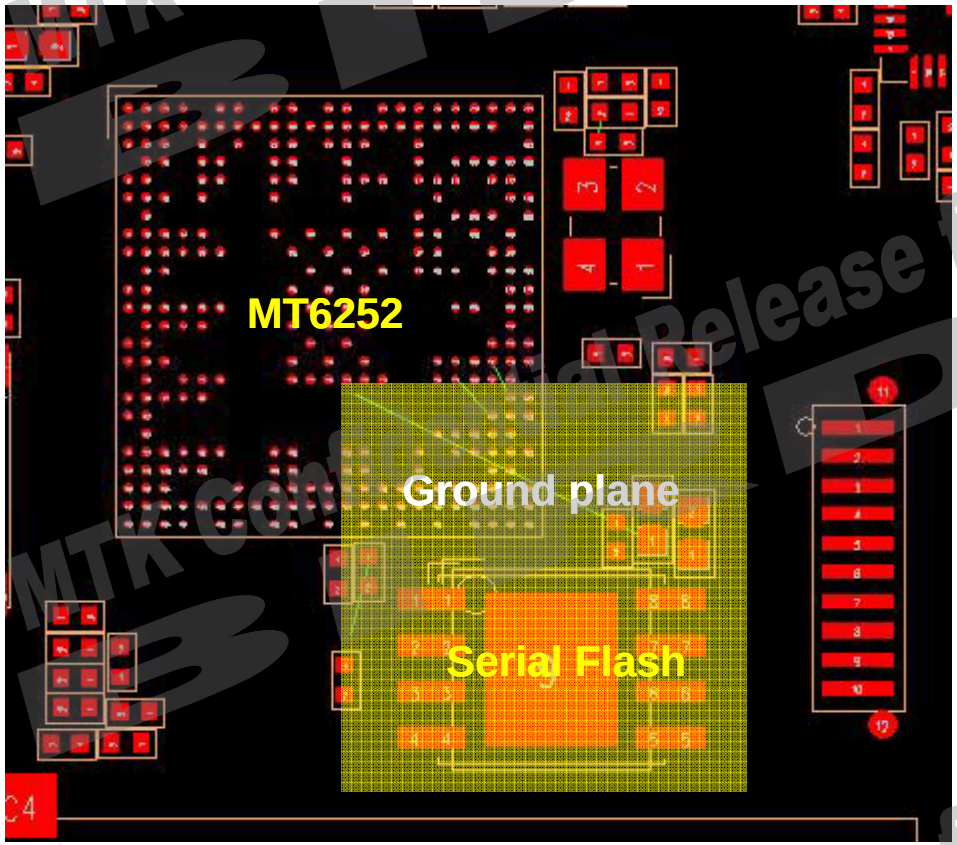
There are 2 packages(WSON and TSOP) on serial flash.
It's recommended that these 2 packages should be reserved on your PCB.
Their pins are fully compatible but pin locations are slightly shifted.
Please overlap the pins for SMT compatible.

MT6252 Memory Layout design notice



The traces of memory should not be crossed by other traces or power. (Nice to have)

MT6252 Memory Layout design notice



There should be a ground plane beneath the Serial Flash and QPI traces of MT6252. (Nice to have)

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MT6252 PMU Design Notice

2010/12

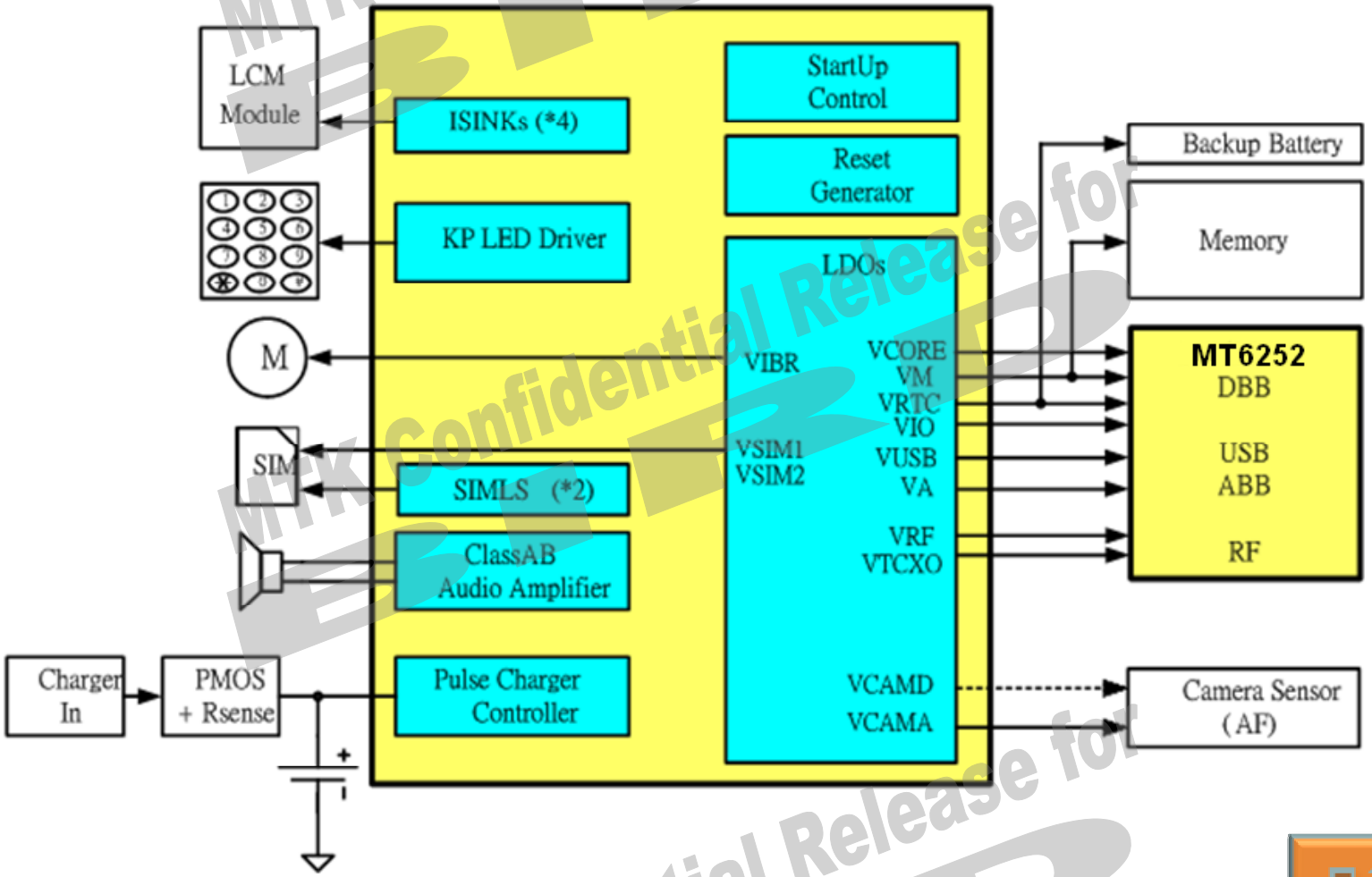
Content

- MT6252 Introduction
  - General description
  - Block diagram
  - LDO list
- Comparison
- Function Description
- Reference design
- Appendix

MT6252 Introduction – General description

- The MT6252 is built-in high performance power management IC.
- Highly integrated functions fulfill all power requirement in handset system
  - LDO
    - Analog LDO * 4
    - Digital LDO * 9
  - Audio Amplifier
    - Class-AB 0.7W@3.7V * 1
  - Charger controller
    - AC/USB
    - Pulse-Charger
  - Driver
    - Parallel LCM backlight LED 4
    - Keypad back-light * 1

MT6252 Introduction – Block Diagram



MT6252 LDO List

Regulator	Output Voltage (V)	Output Current (mA)	Output Components	Notes
VCORE	0.8~1.35	200	1uF	Far-end bypass cap
VM	1.8/2.9	150	4.7uF+1uF	Far-end bypass cap
VRF	2.8	150	2.2uF	Far-end bypass cap
VCAMA	1.5/1.8/2.5/2.8	150	2.2uF	Far-end bypass cap
VA	2.8	100	1uF	Far-end bypass cap
VTCXO	2.8	40	1uF	Far-end bypass cap
VCAMD	1.3/1.5/1.8/2.5/ 2.8/3.0/3.3	100	1uF	Far-end bypass cap
VIO	2.8	200	2.2uF	Far-end bypass cap; SS<40uS
VUSB	3.3	50	1uF	Far-end bypass cap
VSIM	1.8/3.0	30	1uF	Far-end bypass cap
VSIM2	1.3/1.5/1.8/2.5 2.8/3.0/3.3	30	1uF	Far-end bypass cap
VIBR	1.3/1.5/1.8/2.5/ 2.8/3.0/3.3	150	1uF	Far-end bypass cap
VRTC	2.8	2	1K + 100uF (可依需求修改)	Backup battery

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  - Power on timing
  - Driver
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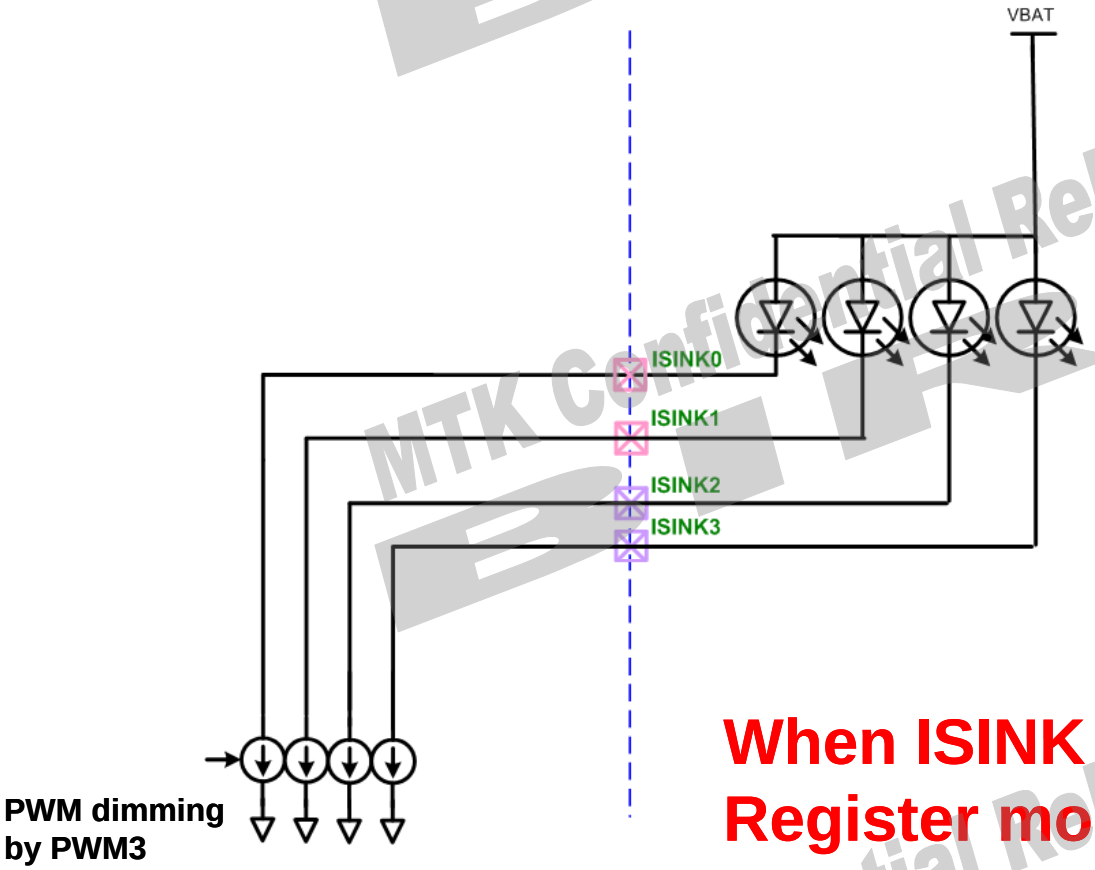
Function Description – Current sink for backlight

- Current sink for LCM backlight LED:
  - Max. 4 current sink
  - No external component required
  - Current balance between channels
  - Individual channel current/enable control
- Note 1 : Luminance become lower when low battery.
  - Please follow “Criteria: Vth = Vf + 0.25V” to avoid this issue
  - Ex.
    - Set VBAT low voltage shutdown at 3.5V
    - Select LED (Vf < 3.5 – 0.25 = 3.25V) will keep luminance equal under normal operation range.
- Note 2 : PWM should set higher to prevent LCM from flickering in low VBAT. PWM frequency > 20kHz is recommended to prevent both LCM flickering and audible noise.

Function Description – Current sink for backlight



Step 1 Current level setting by Register

RG_ISNK_STEP =>
000 : 4mA
001 : 8mA
010 : 12mA
011 : 16mA
100 : 20mA
101 : 24mA

Step 2 Current Controlled by PWM or Register

RG_ISINK_MODE => 0: PWM mode
PWM Dimming controlled by PWM3

RG_ISINK_MODE => 1: Register mode
RG_ISINK_EN Turn on ISINK Channel

When ISINK control by Register mode, It could be controlled independently

Function Description – Current sink for backlight (SW Control)

83010980h	PMIC_ISINK0_CON0
83010990h	PMIC_ISINK1_CON0
830109A0h	PMIC_ISINK2_CON0
830109B0h	PMIC_ISINK3_CON0

PMIC_ISINKX_CON0

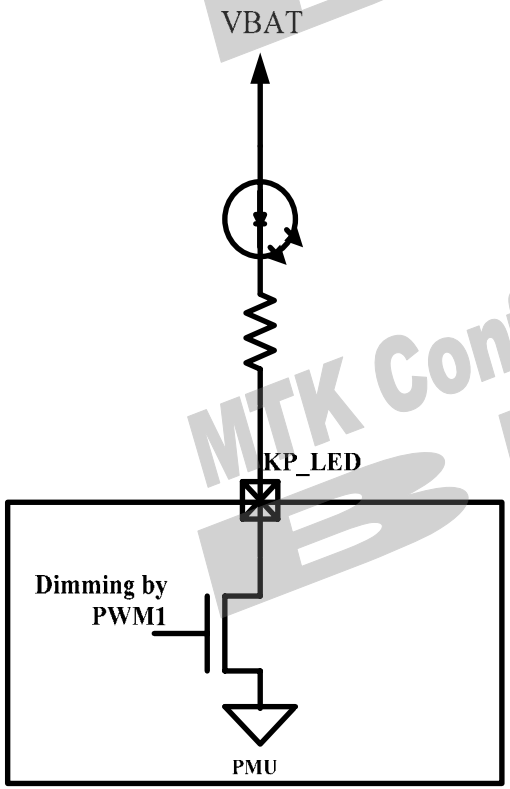
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										RG_ISINKX_STEP					RG_ISINKX_MODE	RG_ISINKX_EN
Type										RW					RW	RW
Reset										0					0	0

RG_ISINKX_STEP Coarse 6 step current level for ISINK, 000:4mA ~ 101:24mA, 4mA per step

RG_ISINK0_STEP[6:4]	000	001	010	011	100	101	110	111
ISINK0 current (mA)	4	8	12	16	20	24	-	-

RG_ISINKX_MODE ISINKX PWM MODE SEL
1 : Register control mode (see the RG_ISINK0_EN to turn-on)
0 : PWM mode, (controlled by PWM3)

Function Description - KP_LED Driver



Step 1 Current level setting by Register

RG_KPLED_SEL =>
000 : 1X
001 : 2X
010 : 3X
011 : 4X
100 : 5X
101 : 6X
110 : 7X
111 : 8X

Step 2 Current Controlled by PWM or Register

RG_KPLED_MODE => 0: PWM mode
PWM Dimming controlled by PWM1

RG_KPLED_MODE => 1: Register mode
RG_KPLED_EN Turn on ISINK Channel

Function Description - KP_LED Driver(SW Control)

0h PMIC_KPLED_CON0 PMIC_KPLED_CON0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						RG_KPLED_SFSTREN	RG_KPLED_SFSTRTC			RG_KPLED_SEL					RG_KPLED_MODE	RG_KPLED_EN
Type						RW	RW			RW					RW	RW
Reset						0	0			0					0	0

RG_KPLED_SEL 3 bits for KPLED current adjustment.
8 steps in total. The minimal current should be no less than 60mA at <111> step.

RG_KPLED_SEL[2:0]	000	001	010	011	100	101	110	111
KPLED current	1X	2X	3X	4X	5X	6X	7X	8X

RG_KPLED_MODE KPLED enable mode select

0 pwm mode, controlled by hardware **PWM1** output signal

1 Register control mode (see the KPLED_EN to turn-on)

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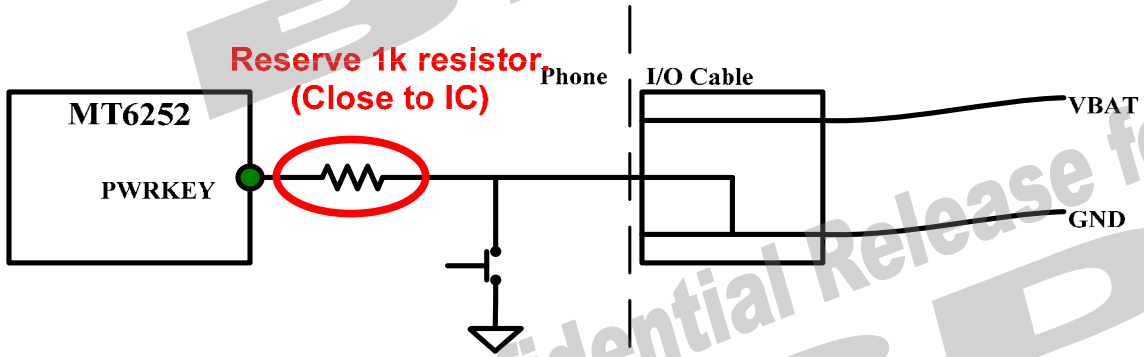
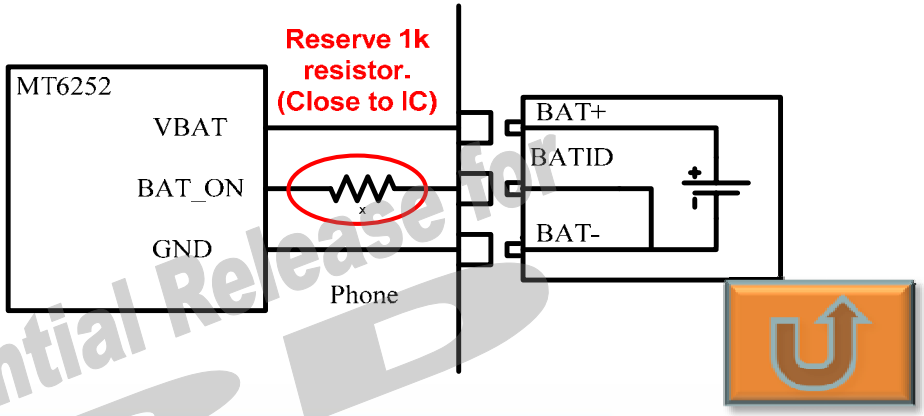
Reference design - Schematic
IC Protection: PWRKEY and BAT_ON

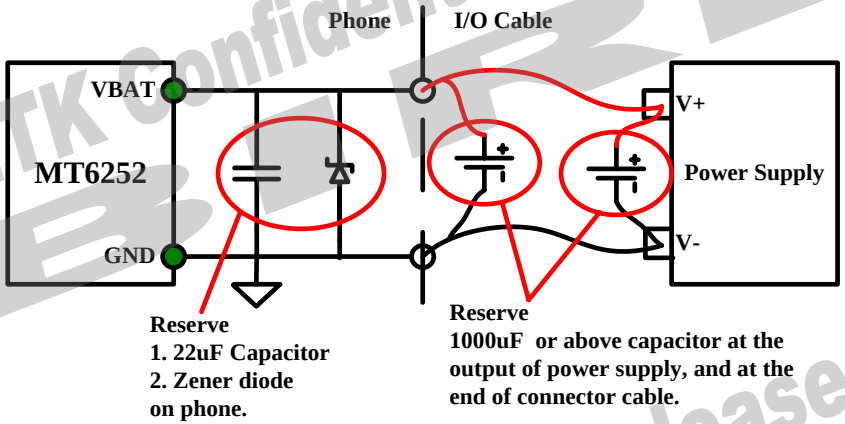


Please reserve 1k resistor on phone PCB to protect **PWRKEY** no matter if PWRKEY connect to any I/O connector or not.

Please reserve 1k resistor on phone PCB to protect **BAT_ON** pin if BAT_ON is used to detect battery.



Reference design - Schematic IC Protection: VBAT



MT6252 has lower VBAT voltage rating. (Max. 4.3V.) Some protection should reserve to prevent the damage by voltage surge.

•Design notice in Phone side:

1. At least 22uF capacitor. (Included RF PA input capacitor)
2. Add Zener diode (5.1V/500mW) to protect the IC against low frequency voltage surge. Put it between battery connector and MT6252.

Notice: If using IO connector or test point to supply VBAT for download, manufacture, or repair, should let VBAT trace passing zener diode and 22uF capacitor before entering IC.

Notice: Using 5.1V zener will introduce some leakage when VBAT = 4.2V.

•Design notice in Power Supply side:

Add 1000uF (or above) capacitor at the output of the power supply to reduce the voltage bounce caused by long power cable. And the power cable should be as short as possible.

Also add 1000uF (or above) capacitor at the end of power cable (near phone side).

Zener Diode Selection Guideline

Selection Guideline

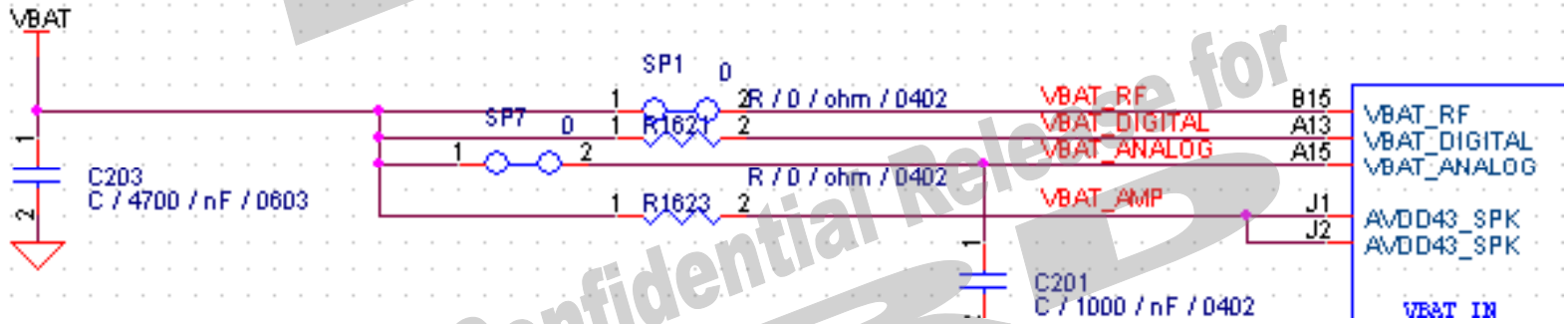
- 500mW zener diode has lower ZZT than 200mW and can sink more exceptional surge voltage/current.
- MT6252 must selcet 5.1V/500mW zener to enhance VBAT pin protection.
- Ir<100uA @Vr=4.2V, Ta=25 ° C, Using 5.1V zener will introduce some leakage when VBAT = 4.2V. Large Ir current will introduce more leakage current.

Zener Diode Validation List

- For design in,please notice the parts shipping delivery time.
- The latest validation list, please access the MTK BBS web.

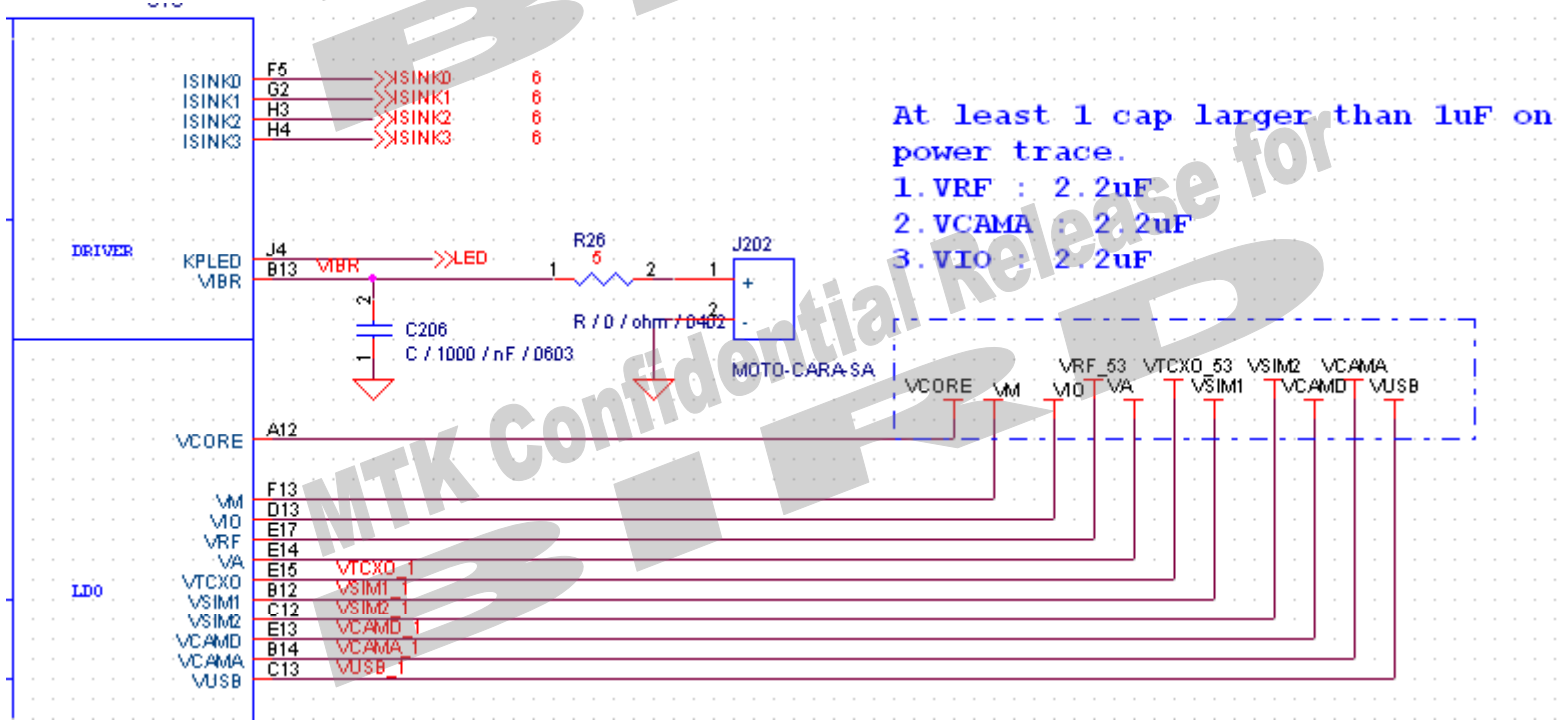
Item	Vendor	Part number	Power (Watts)	Package	IR(uA) @VR=4.2V	Contact Window
1	On semi	MMSZ5231BT1G	500mW	SOD123	9	Tony Kao, 886-2-23761153 886-987-265-997 Email: tony.kao@onsemi.com
2	JIANGSU CHANGJIANG (长电科技)	MMSZ5231B	500mW	SOD123	72	Mr. Chan 0510-86858061 13601525970 E-mail: cyz@cj-elec.com
3	Prisemi	PZ3D4V2H	500mW	SOD323	11.5	Bull Tang Mobile:13502888931 Email: bull1975@gmail.com
4	Prisemi	PZ5D4V2H	500mW	SOD523	4.85	
5	Vishay	MMSZ4689-V	500mW	SOD123	7	Mike_Wang 886-911313660 mike.wang@Vishay.com

Reference design - Schematic
VBAT Input Filter



- All bypass cap. should be as close to MT6252 IC as possible
- Recommend reserve 0 ohm between VBAT pin & VBAT_RF, VBAT_ANALOG for analog LDO quality.

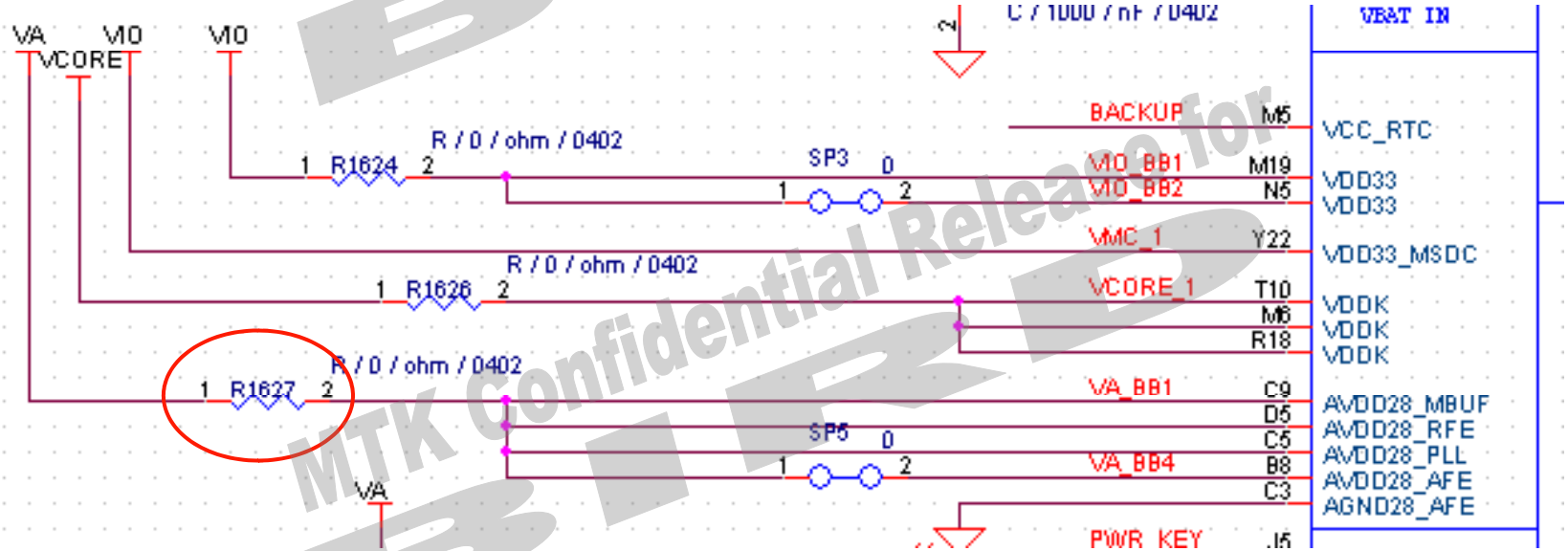
Reference design - Schematic
Bypass Capacitor



- At least 1 cap larger than 1uF on power trace

  VRF, VCAMA, VIO larger than 2uF

Reference design - Schematic
Bypass Capacitor for AVDD and VDD



- Reserve 0 ohm resistor for audio quality.

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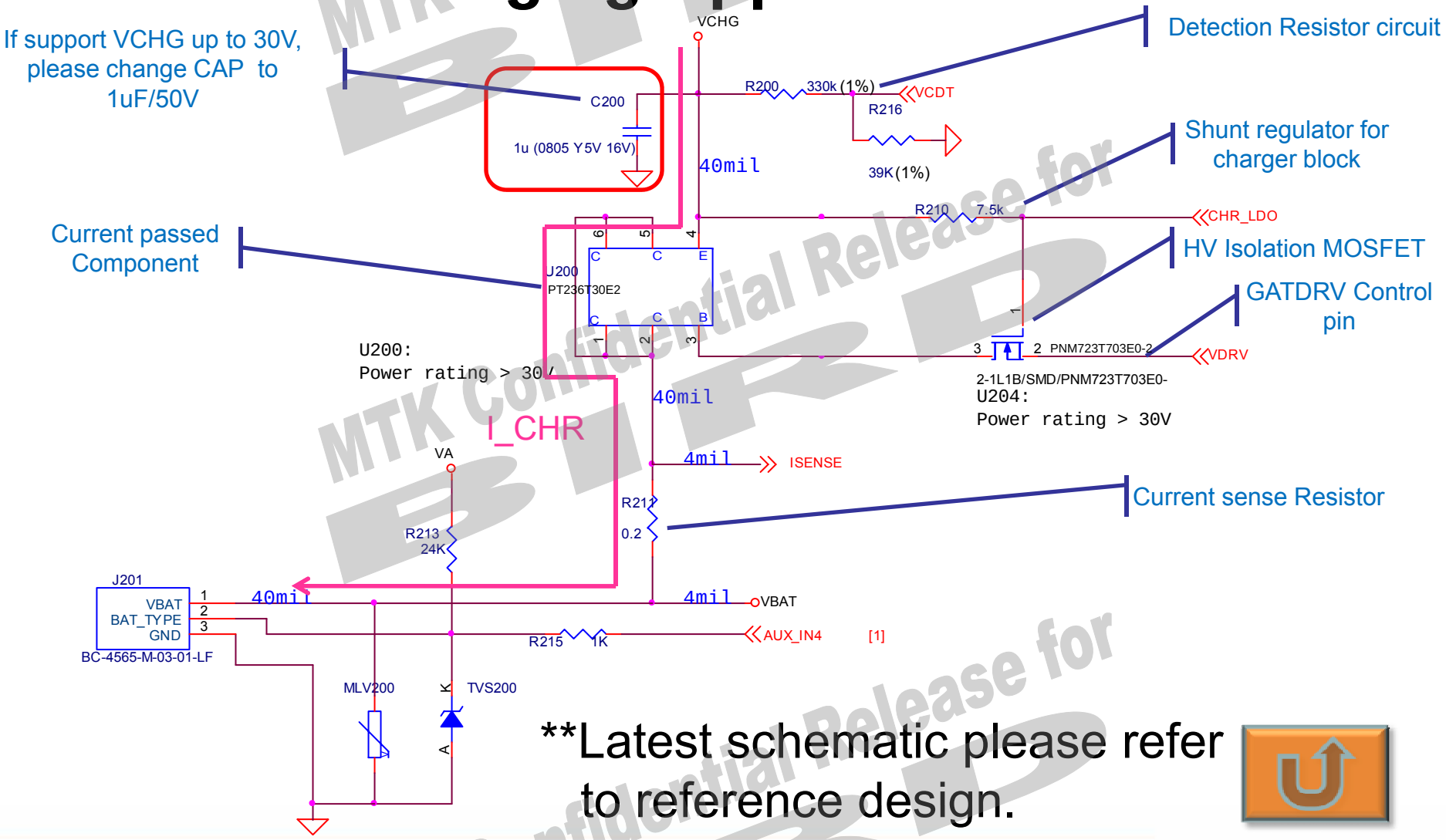
Design Notice - Pulse Charging

MT6252 Charging Feature Comparison

Chip / Feature	MT6253	MT6235	MT6252
Charging type	CC-CV	CC-CV	Pulse Charging
Maximum charger input voltage	9V	9V	30V
Support battery type	Li-ion	Li-ion	Li-ion
VCHG OVP	7V	7V	10.5V (Default off)
CV	4.2V	4.2V	4.2V comparator
CC	160mV/R	160mV/R	160mV/R
Pre_ charge	24mV/R	20mV/R	20mV/R
Battery OVP	4.3V	4.3V	4.35V
Watchdog timer	Yes	Yes	Yes
Pre-charge safety timer	NO	NO	50 minutes
Passed element	P-MOSFET +SD	P-MOSFET +SD	BJT+ N-MOSFET
Pre-charge/CC overlap	Yes	No	Yes

MT6252 Charging Application Circuit



**Latest schematic please refer to reference design.

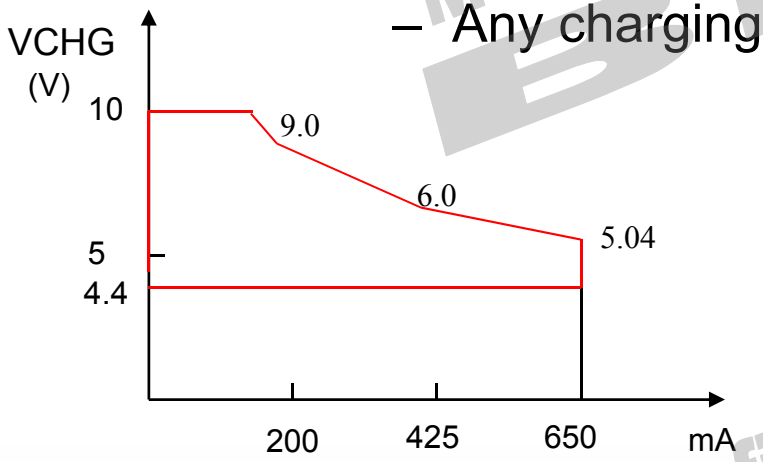
BJT Validation List

- For design in, please notice the parts shipping delivery time.
- The latest validation list, please access the MTK BBS web.

Item	Vendor	Part number	Power (Watts)	Package	hFE (min)	hFE (max)	Ic	Contact Window
1	ST	STTB818	1.2	SOT23-6L(TSOP6)	100	NC.	3A	Peter lui peter.liu@st.com 02-23762971
2	On semi	NSS35200MR6T1G	1	TSOP6	100	400	2A	Tony Kao, tony.kao@onsemi.com 886-2-23761153 886-987-265-997
3	NXP	PBSS5350D	0.7	SC-74(SOT-457)	200	NC.	3A	Mag Cheng mag.cheng@nxp.com "+886-987-49186 +886-2-8170-9076 (Direct)
4	Presemi	PT236T30E2	1.2	SOT23-6L(TSOP6)	100	NC.	3A	Bull Tang 13502888931 bull1975@gmail.com

BJT Power Dissipation and Charge Current

- Charger BJT selection
  - Max. charger voltage 10V
  - Max. battery charge current (0.72C for Li-ion 900mAHr)
  - Max. power dissipation of external BJT (1W),Duty=8/(8+1)
    - (Vchg-3.3)*0.65*0.88 < 1 ➔ Vchg < 5.04V, (I=0.65A)
    - (Vchg-3.3)*0.425*0.88 < 1 ➔ Vchg < 6.0V, (I=0.425A)
    - (Vchg-3.3)*0.20*0.88 < 1 ➔ Vchg < 9.0V (I=0.20A)
  - Any charging time VCHG > VBAT + 0.2 ➔ VCHG > 4.4 V



Pulse Charging

- Feature
  - Maximum input voltage up to 30V
  - Support low cost linear and Nokia adaptor charger(9.3V)
  - Meet 2010 China charger standard(12V OVP)
  - CC mode current control
  - Constant current pre-charging
  - Charger OVP and battery OVP
  - Pre-charge/CC safety timer
  - Watchdog timer

Design Notice – Charge Current Setting

		MT6223	MT6235		MT6253	MT6252
Sense Resistor		0.2 Ohm	0.2 Ohm	0.1 Ohm	0.2 Ohm	0.2 Ohm
Pre-Charge		62.5	100	200	50	100
CC	0	62.5	62.5	125	50	100
	1	90	90	180	87.5	200
	2	150	150	300	150	400
	3	225	225	450	225	425
	4	300	300	600	300	550
	5	450	450	900	450	650
	6	650	X	X	650	700
	7	800	X	X	800	800

Design Notice – SW Setting Notice

- Must set TRUE for “enable checking charging voltage while charging” in Chr_parameter.c

```
bmt_customized_struct  bmt_custom_chr_def =
{
xxxxxxxxxxxxx
```

KAL_FALSE, /* enable checking temperature while charging */

KAL_TRUE /* enable checking charging voltage while charging */

This should be TRUE.

Nokia adaptor charger(9.3V)

- Nokia adaptor has much type adaptor and different out put voltage. For 2-mm DC charging adaptor, the output open voltage will reach 9.3V.
- For HV input adaptor, must care charger OVP and BJT power dissipation.
- Configure charger OVP for Nokia Charger

  Step 1.SW OVP

  - ✓ Modify Chr_parameter.c ,

    ~~6500000~~ 10500000,/*VCHARGER_HIGH*/

  Step 2 .HW OVP

  - ✓ Please contact MTK to modify HW OVP for SW patch

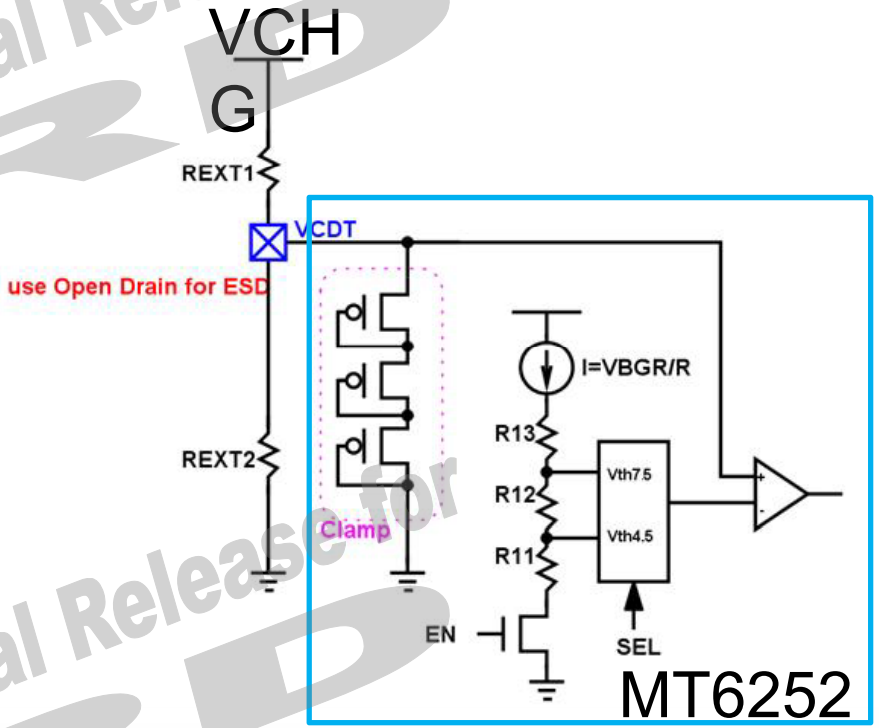
    (default is 7V)
- BJT power dissipation.
  - BJT Power Dissipation and Charge Current page

Pins Description

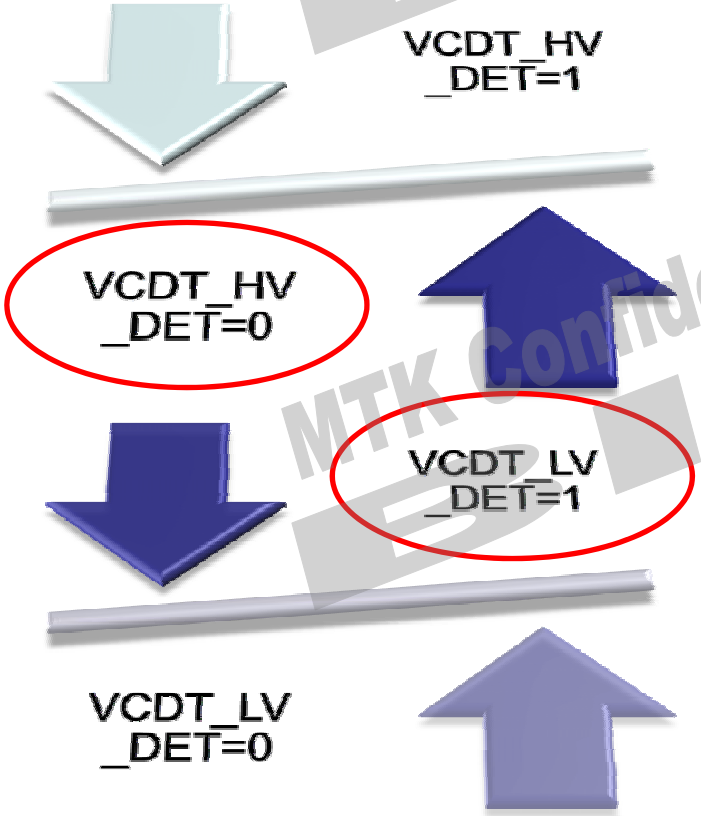
Pin	Function
VCDT	Charger detect, the V_CHG detection threshold voltage is 4.3V at charge off state
CHR_LDO	Charger power supply source and it's a 2.8V shunt regulator
VDRV	Charge passed element control pin
BATSNS	Battery voltage sense pin
ISENSE	Current sense pin
BATON	Battery detection pin. If this pin is large than 2.5V will disable charging.

Charge Detection

- Charger detect, the detection threshold voltage is 4.3V at charge off state.
- Charger over voltage protection HW default is disable, SW can customize. (Default is 7.5V)



Charger Detection



VCDT_HV_VTH (valid if VCDT_HV_EN=1)

CHRDET

VCDT_LV_VTH (always valid)

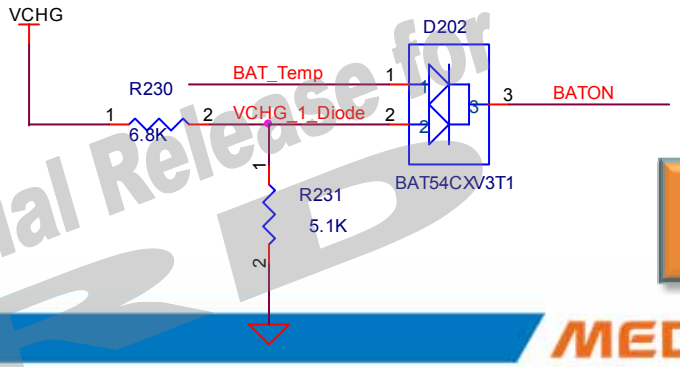
Charger OVP

- Charger over voltage protection HW default is disable.

  After power on, SW will configure “VCDT_HV_VTH”

	Min	Typical	Max
09	5.7	6	6.3
10	6.175	6.5	6.825
11	6.65	7	7.35
12	7.125	7.5	7.785
13	8.075	8.5	8.93
14	9.025	9.5	9.97
15	9.975	10.5	11.02

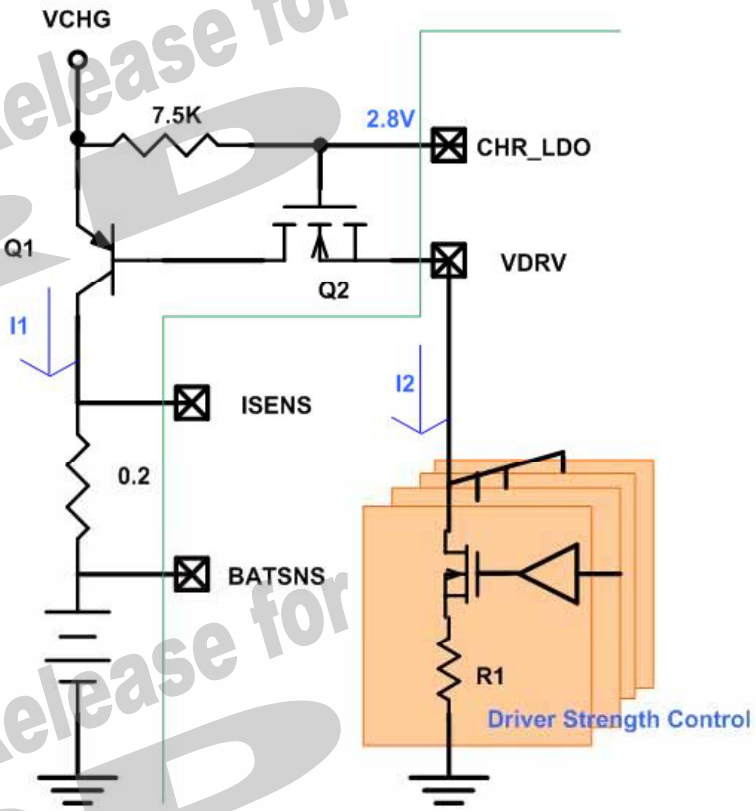
- Other, adding below circuitry to increase a OVP path .
  - BATON toggle threshold is 2.5V.



VDRV Driving Control

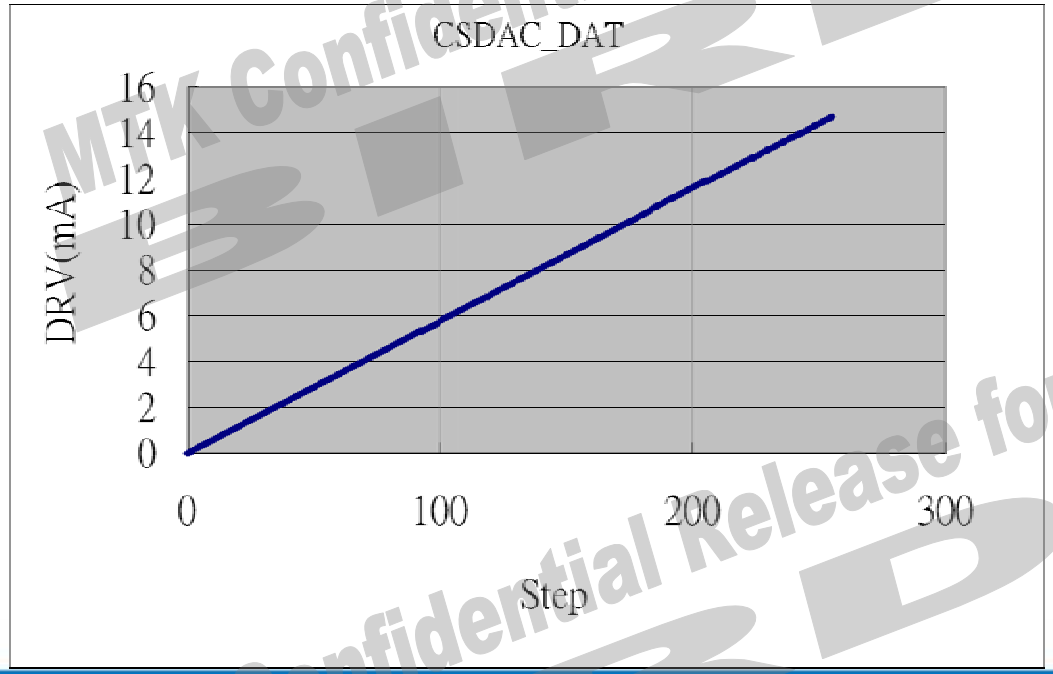
- If Q1 does not go into saturation, $I_1=\beta_1 x I_2$.
- Assume I_1=450mA, β_1=200

  => I_2=2.25mA
- If Q1 goes into saturation, look up the characteristic table to get the relationship between I_1 and I_2.
- Build in 256 steps CSDAC for current driving control.



CSDEC

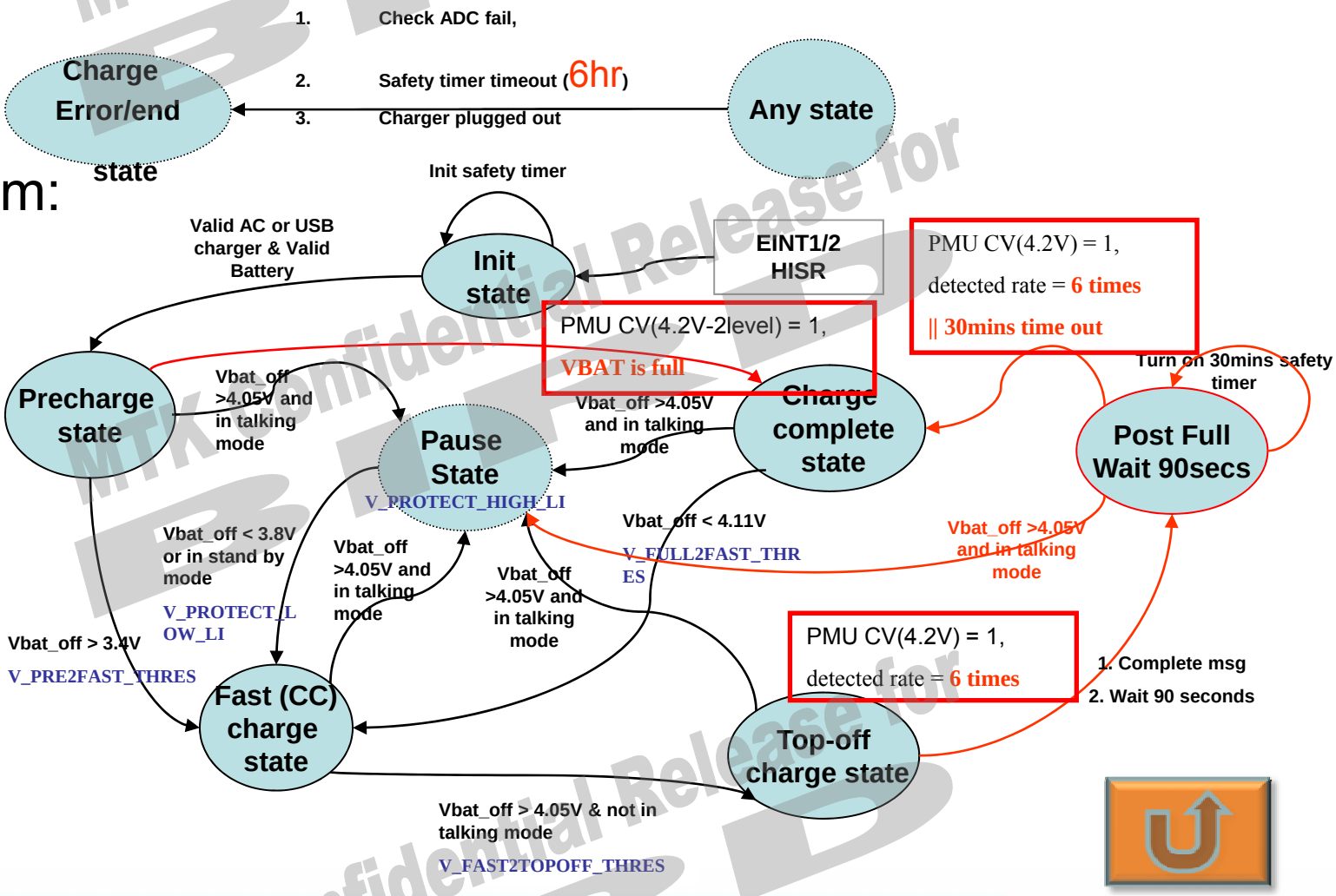
- Charge current =β_1*I_CSDEC
  - I_CSDEC (maximum)=14.8mA.
  - I_CSDEC selection
    - 1 LSB =55uA. Current step = 55uA*200(β_1)=11mA
- DC Current Gain(β) must be 100~300 at Ic=0.5A



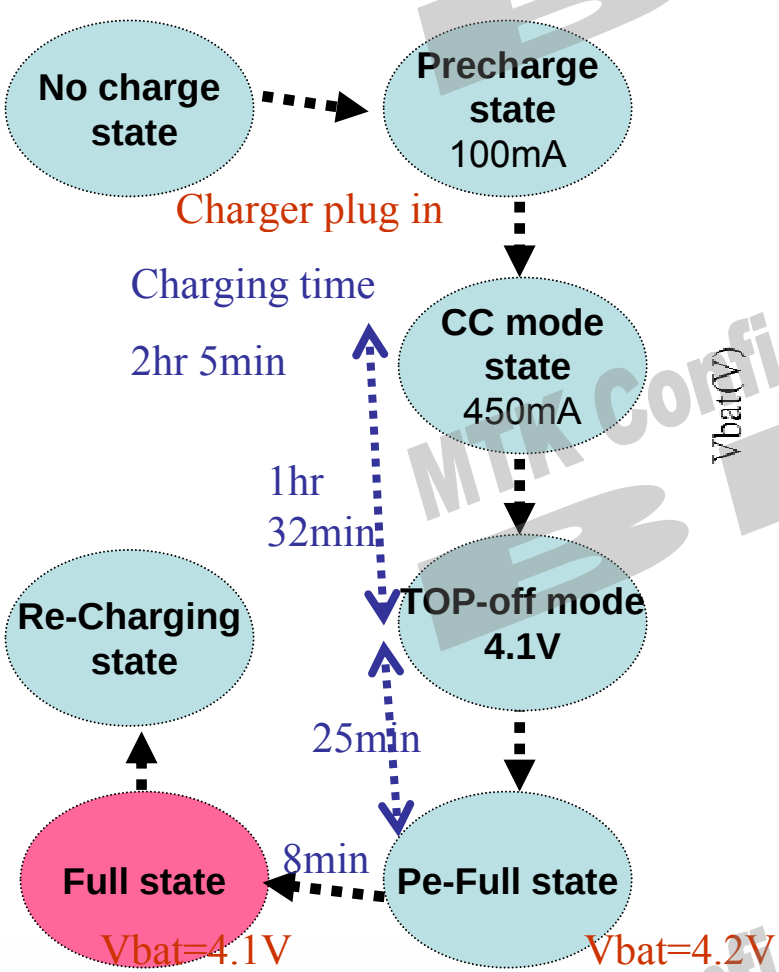
New Charging State

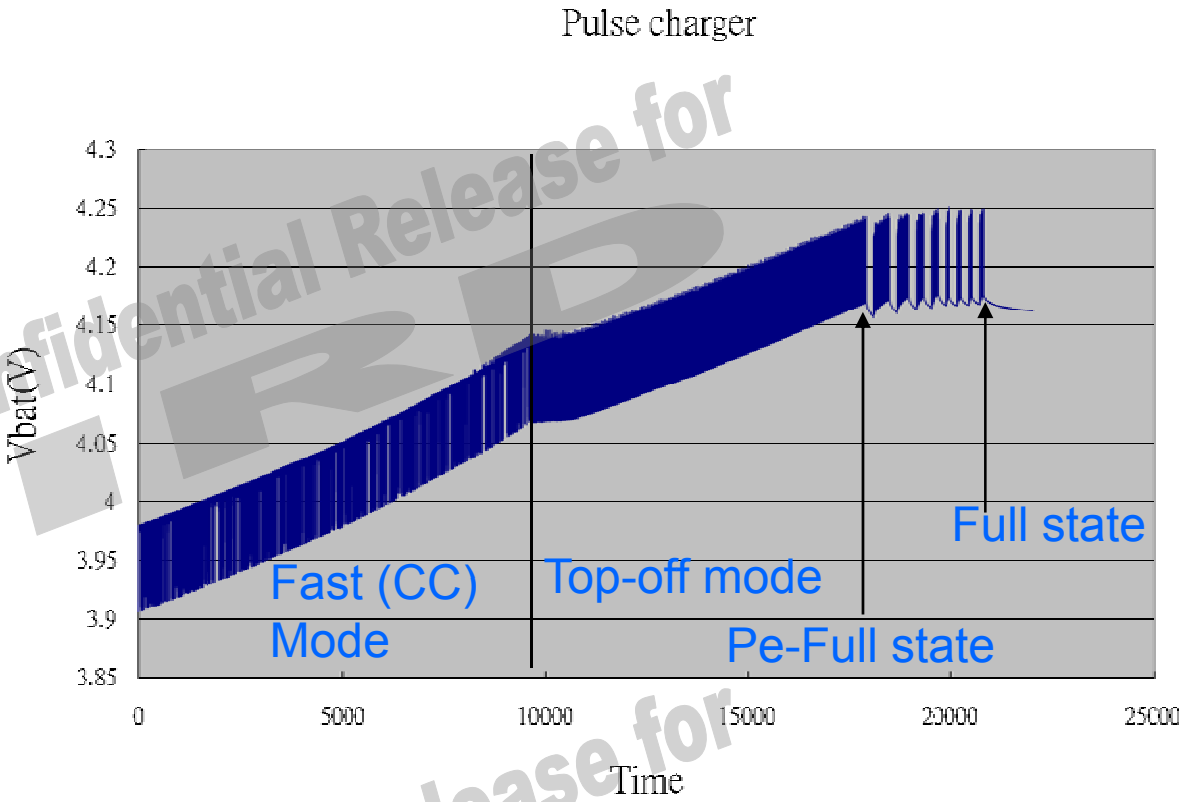
- Please refer to pulse charging SW customize programming guide for customization. (Please contact with MTK)

State diagram:



Pulse Charge Charging Curve





Application Limitation

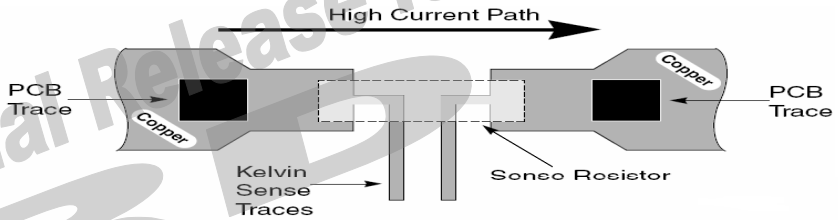
- Must have “Off duty” to detect charger plug-out.
  - Otherwise has reverse current and can’t detect charger plug-out
- BJT (DC Current Gain) will effect current step and accurate
  - Smaller “DC Current Gain” get more accurate.
  - Too small “DC Current Gain” to charge up zero voltage battery.
    - Vbat <1V, CSDEC will limit at 4 step(0.23mA).

Component Selection Glide

- U200:Current passed Component----PT236T30E2
  - hFE (DC Current Gain) is 100~300 (Typical 200 @-20~80 ^{0}C) at Ic=0.5A
  - For thermal dissipation concern, the U200 power dissipation must be large than 1W.
  - VCE(Collector-Emitter Voltage) ≥30V
  - Ic >0.8A (Depend on application)
- U204 N-MOS---PNM723T703E0-2
  - Vgs threshold <1.5V @Id=0.1mA
  - VDS>30V (Depend on application)
  - RDS (ON) <10 ohm @ID = 10 mA, VGS = 2.5 V
- C200 (VCHG input cap)
  - If want to support VCHG up to 30V, please change CAP to 1uF/50V.

Charger Layout Notice:

- C216 CHR_LDO decouple cap close to IC.
- R211 (Current sense resistor)close battery connector and trace is 40mil(star connect to connector)
- The exposed pad of the U200(Current passed component) should connect to a large copper ground plane to get good thermal performance.
- ISENSE and BATSNS should be connected as the below figure.
- The trace from Rsense to battery connector should not share with other VBAT traces.
- ISENSE/BATSNS should be routed as differential traces which are away from noisy signals.

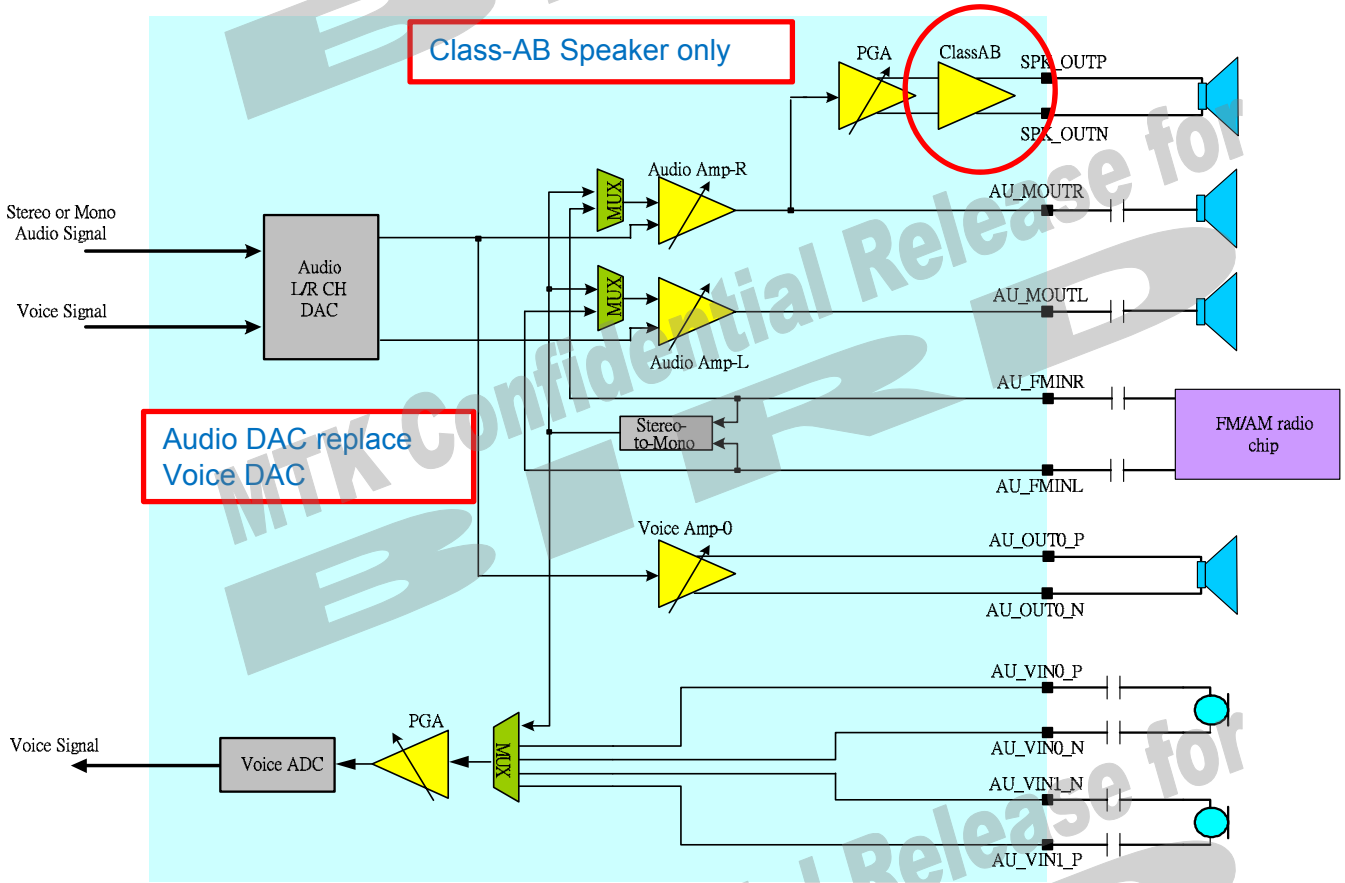


Confidential B

Design Notice – Audio

Design Notice – Audio (1/9)

- **Audio Block diagram :**



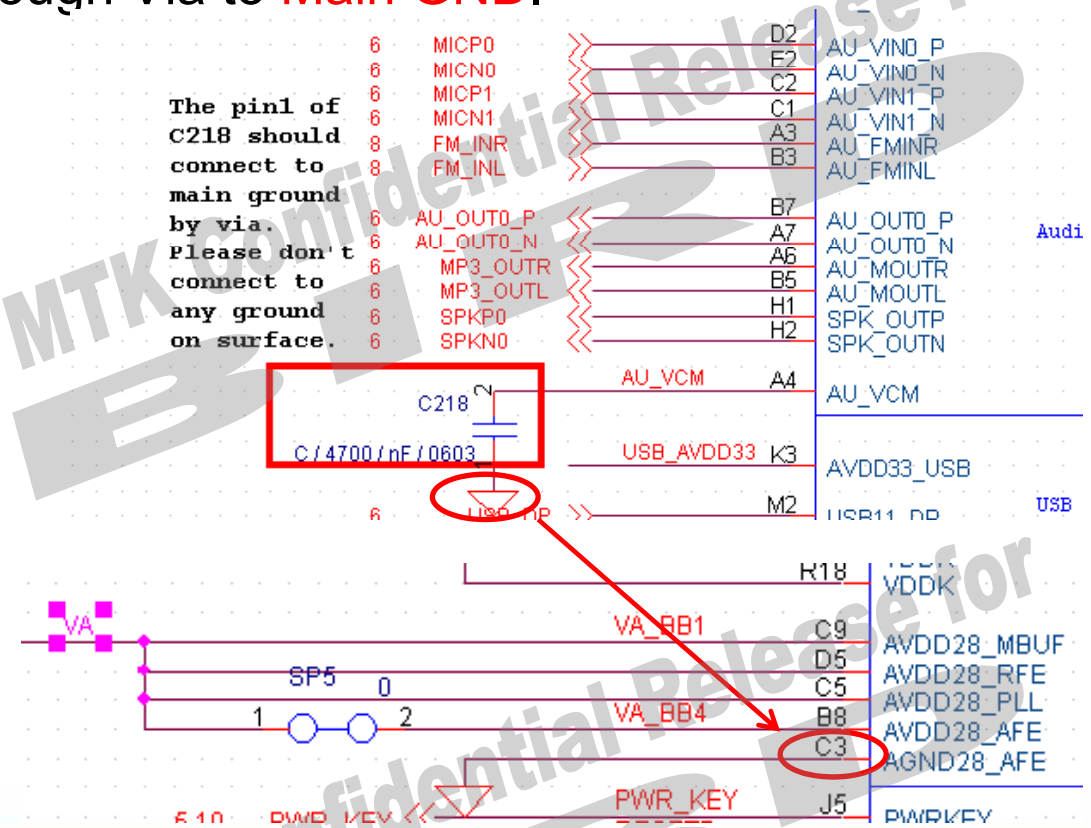
Design Notice – Audio (2/9)

- **MT6252/6253/6236 compare:**

		MT6253	MT6236	MT6252
MIC	gain range (dB)	-20 ~ +43	-20 ~ +43	1~49 dB
	gain step size	2dB	2dB	2dB
voice buffer 0	gain range (dB)	-22 ~ +8	-22 ~ +8	-16 ~ 8 dB
	gain step size	2dB	2dB	2dB
	Engineer mode range	0 ~ 255	0 ~ 255	0 ~ 255
audio buffer	gain range (dB)	-22 ~ +23	-22 ~ +23	-22 ~ 17 dB
	gain step size	3dB	3dB	3dB
	Engineer mode range	0 ~ 255	0 ~ 255	0 ~ 255
SPK AMP	Amp Type	ClassAB/D	ClassD	ClassAB
	gain range (dB)	0~21 (Class-AB) 6~27 (Class-D)	12/18dB	0~22.5dB
	gain step size	3dB	x	1.5dB

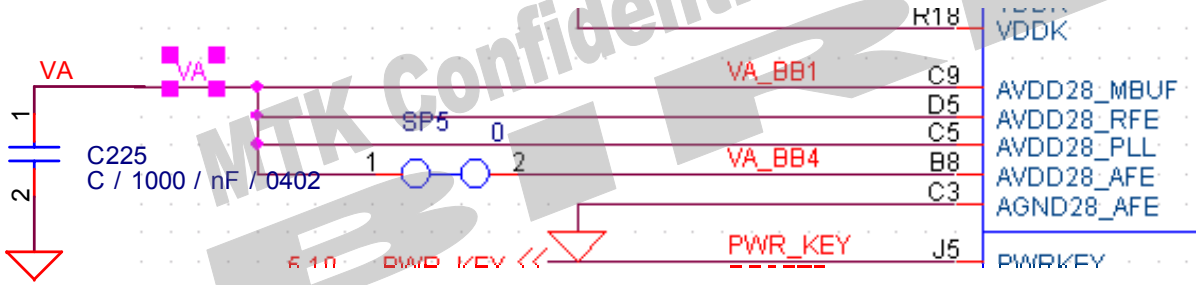
Design Notice – Audio (3/9)

- **Audio Signal schematic and layout :**
  - The signal of Audio block should shielding by GND
  - C218 GND net should connect to C3(AGND28_AFE) pad first then direct through Via to Main GND.



Design Notice – Audio (4/9)

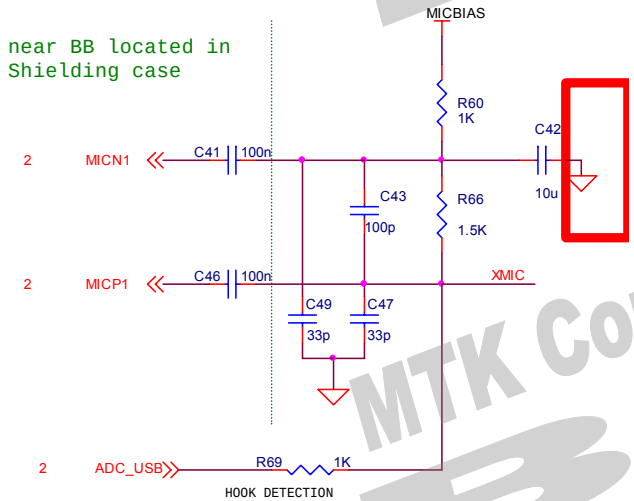
- **Audio Power schematic and layout :**
  - C225 GND side should connect to AGND28_AFE first then short to main GND and close to ball C9



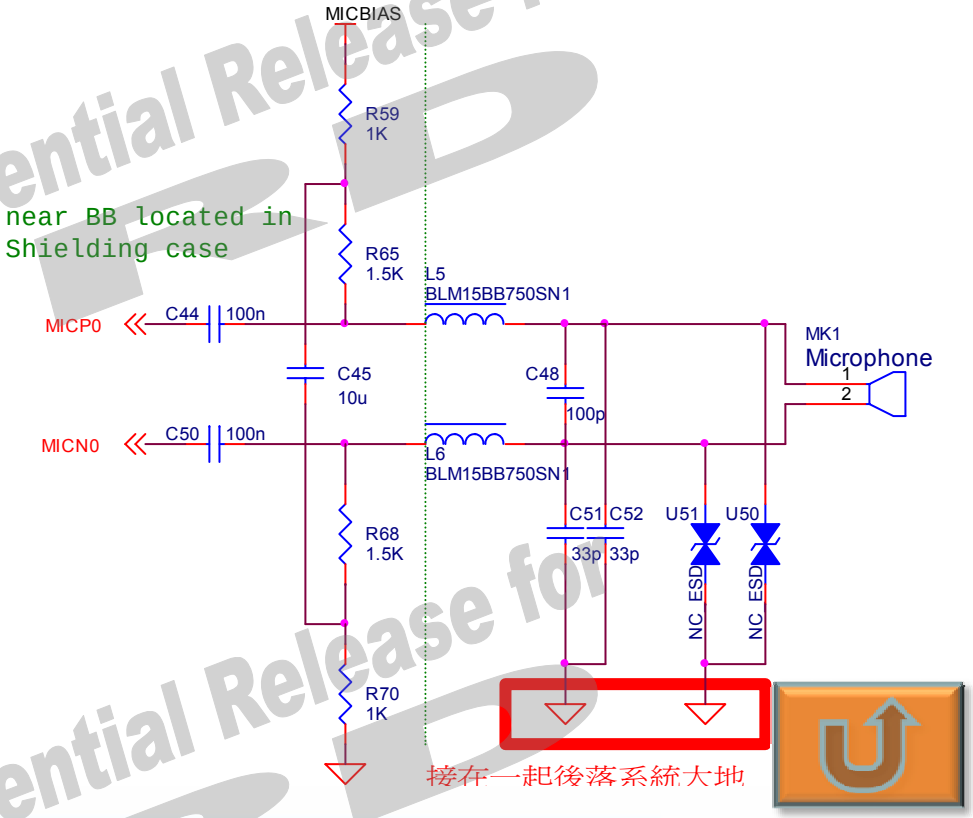
Design Notice – Audio (5/9)

- **Audio Power schematic and layout :**
  - C41 , C46 , C53 , C56 , R71 , R72 , R59 , R65 , R68 , R70 , C45 , C44 , C50 須靠近BB , 並放在shielding case 裡面

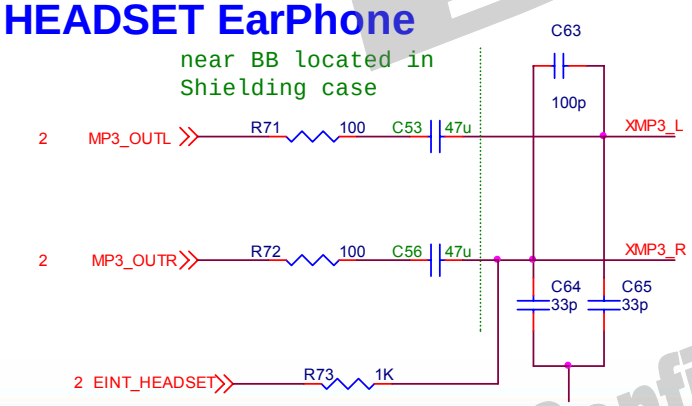
HEADSET MICOPHONE



HANDSET MICOPHONE



HEADSET EarPhone

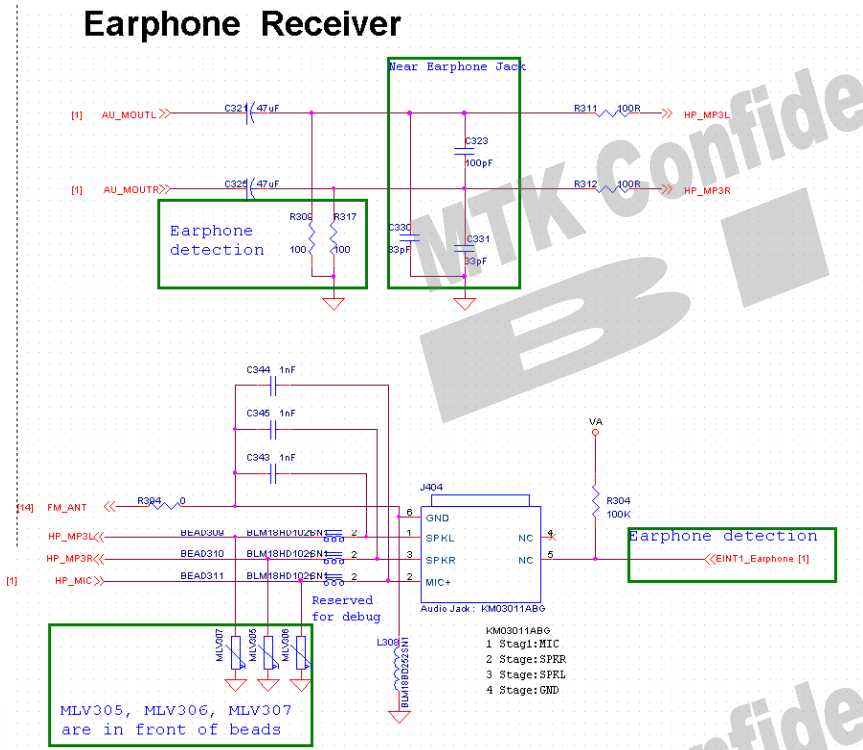


Design Notice – Audio (6/9)

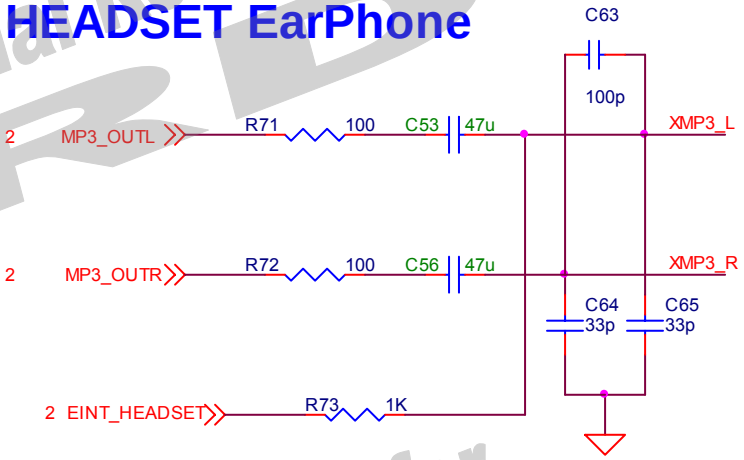
- **Audio Jack :**
  - An extra interrupt pin of audio jack for the earpiece detection can get better THD+N (from 71dB to 76dB)

● Step 1 : **Not plug-in** earphone (Audio Jack pin 3-5 connected)
EINT1 **pull low** through Audio Jack (pin 3-5 connection) to R317 to GND.
● Step 2 : **Plug-in** earphone (Audio Jack pin 3-5 dis-connected)
EINT 1 **pull high** .

Earphone Receiver



HEADSET EarPhone



● connect EINT to MP3_OUT for cost effective solution
● connect to L channel to avoid POP noise when use internal SPK Amp

Design Notice – Audio (7/9)

- **Audio Jack :**
  - In previous page, EINT status is from **Low**(earphone plug out) to **High** (earphone plug-in), so please confirm auxmain.c to fit hardware application

•Example for EINT status is from Low (plug out) to High (plug-in)

```
kal_bool            aux_state = LEVEL_LOW;
                    :
                    :
void AUX_EINT_HISR(void)
{
ilm_struct *aux_ilm;

 if (aux_state == LEVEL_HIGH)
 {
  #ifdef AUX_DEBUG
dbg_print(" Interrupt: Plugout \n\r");
 #endif
```

•Example for EINT status if from High (plug out) to Low (plug in)

```
kal_bool            aux_state = LEVEL_HIGH;
                    :
                    :
void AUX_EINT_HISR(void)
{
 ilm_struct *aux_ilm;

 if (aux_state == LEVEL_LOW)
 {
 #ifdef AUX_DEBUG
dbg_print(" Interrupt: Plugout \n\r");
#endif
```

Design Notice – Audio (8/9)

- **Internal Class-AB : Audio Amplifier Power Output**

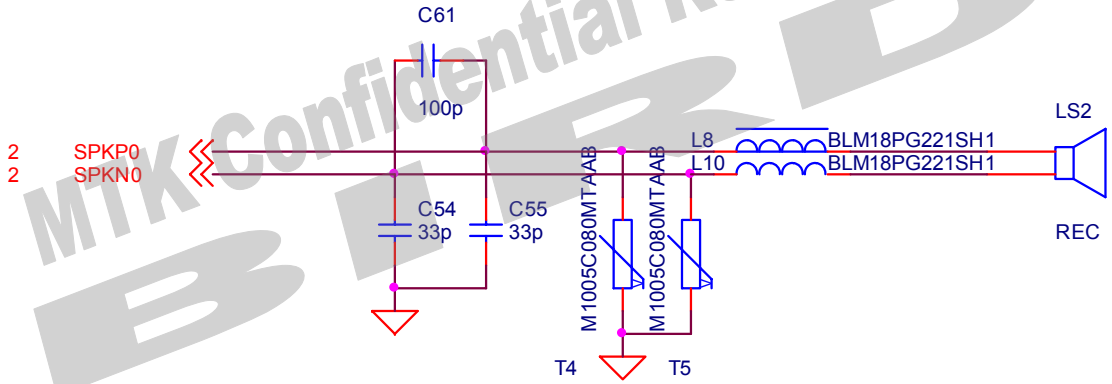
	MT6252 Class-AB Amplifier	
Pout Maximun output power	THD+N=10%, VDD=4.2V RL = 8Ω	1.0W
	THD+N=10%, VDD=3.3V RL = 8Ω	650mW
	THD+N=1%, VDD=4.2V RL = 8Ω	850mW
	THD+N=1%, VDD=3.6V RL = 8Ω	500mW

- Although MT6252 class-AB power output is 0.85W at 8 Ω , because congenital power source limitation is 4.2V from VBAT , but compare with other discrete amplifiers , MT6252 equal other amplifier in performance.

Design Notice – Audio (9/9)

- **Internal Class-AB Audio Amplifier :**
  - The trace width of SPK_P and SPK_N should be greater than 25 mil
  - The Net of SPK_P and SPK_N should be shielded by GND
  - Please select Bead for Amp output filter which R_{DC} < 0.1ohm and Rated Current > 1.1A

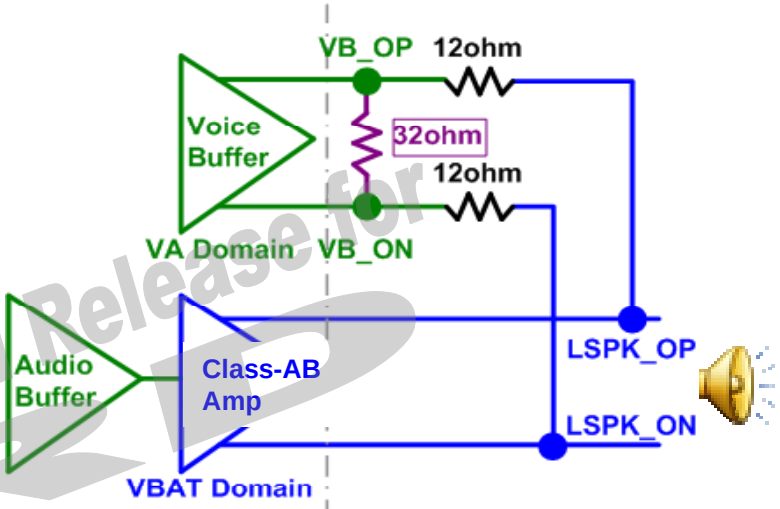
LOUD SPEAKER



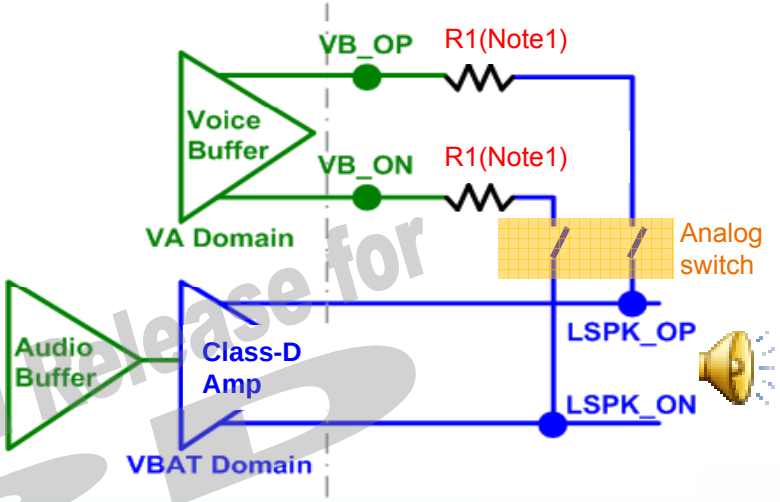
Vendor	P/N	Rdc(ohm)	Rate current(mA)
Murata	BLM18PG221SH1	0.1	1400
	BLM15PD800SN1	0.07	1500
	BLM18KG221SN1	0.05	2200
	BLM18KG331SN1	0.08	1700
	BLM18SG221TN1	0.04	2500
	BLM18SG331TN1	0.07	1500
	BLM18EG221SN1	0.05	2000
TDK	MPZ1608S221A	0.05	2200
	MPZ1608S331A	0.08	1700
	MPZ1608Y221B	0.1	1500

Notice for 2-on-1 speaker application

- Class-AB (MT6252 build-in amp)
  - **Adding one "32ohm" between (VB_OP, VB_ON)** to limit the voltage level at (VB_OP, VB_ON)



- Class-D (external amp)
  - **"2 analog switches"** should be put **between VB_OP/ON and LSPK_OP/ON**
  - **Note1: The R1+Ron of the analog switch should equal to 12ohm**

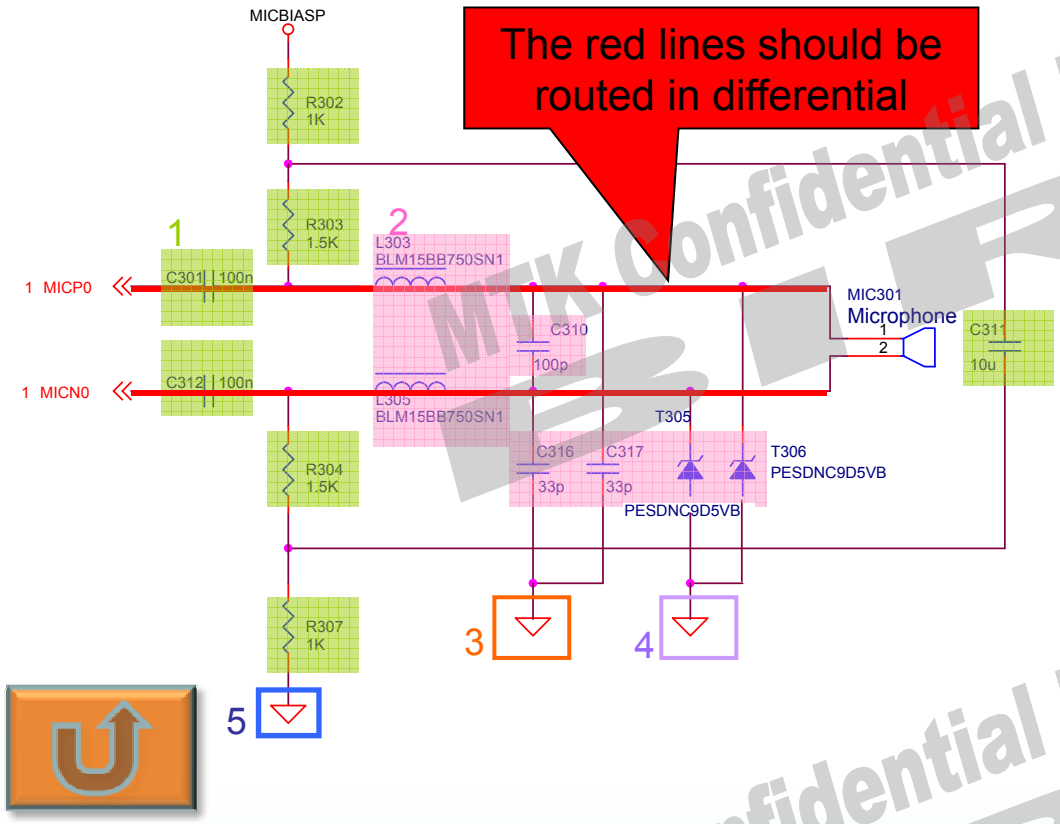


Confidential B

MT6252 design note- Speech

Microphone application circuit note

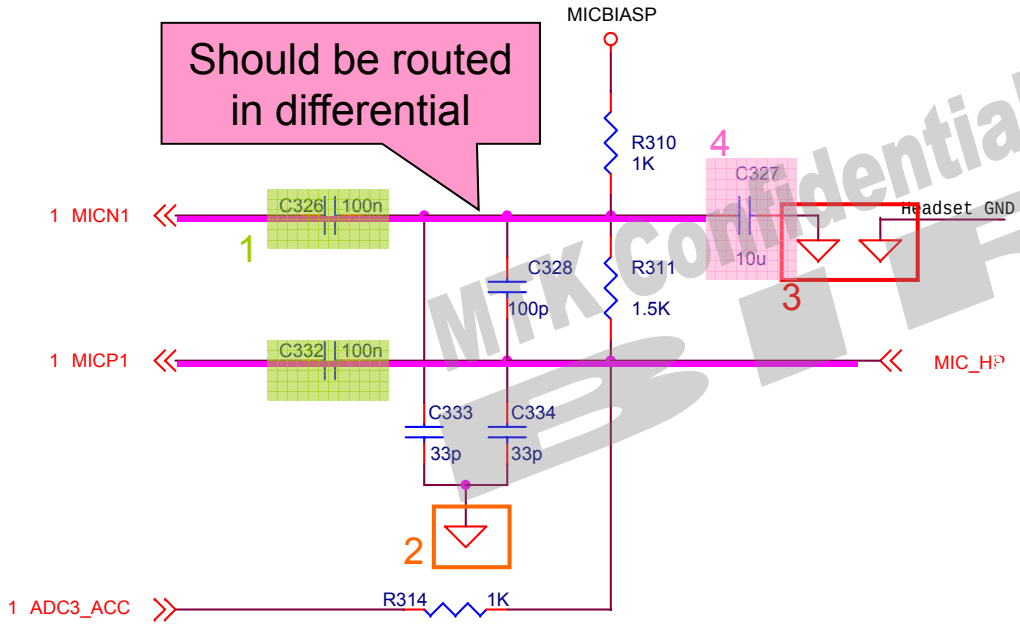
- Layout consideration-Normal mode



1. R302, R303, R304, R307, C311, C301 and C312 should be put **close to the BB chip**
   - R302, R303, R304, R307, C311 should be put as close as possible
2. L303, L305, C310, C316, C317, T305 and T306 should be **close to the microphone**
3. GND of **C316 and C317** should be connected **together** and then to the GND
4. GND of **T305 and T306** should be connected **together** and then to the GND
5. GND of **R307**should connect to the **main GND by a single via**

Microphone application circuit note

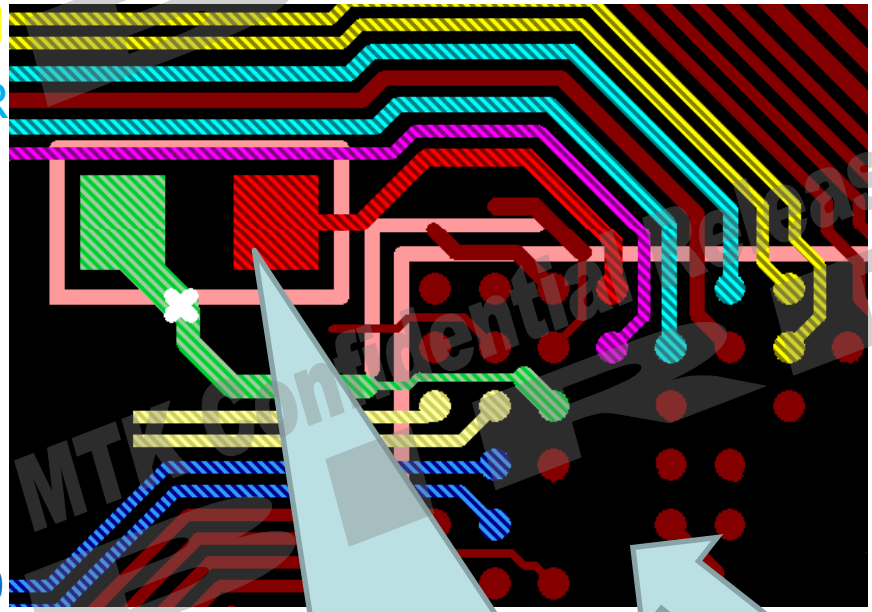
- Layout consideration-Headset mode



1. **C326, C332, R311, R310** should be put **close to BB**
2. The **GND of C333 and C334** should **connect together and then connect to the GND**
3. The **GND of C327 and headset** should **connect together and then to the main GND by single via**
4. **C327** should be put **close to microphone**

Placement and routing Example

AU_OUT0_P/N
MP3_OUTL/R
AU_MIC_BIAS
MICP1/N1
MICP0/N0



1. AU_VCM cap should be **as close as** to the BB chip
2. The GND of AU_VCM should be connected to **pin C3 first**, and then connect to the main GND by **single via**

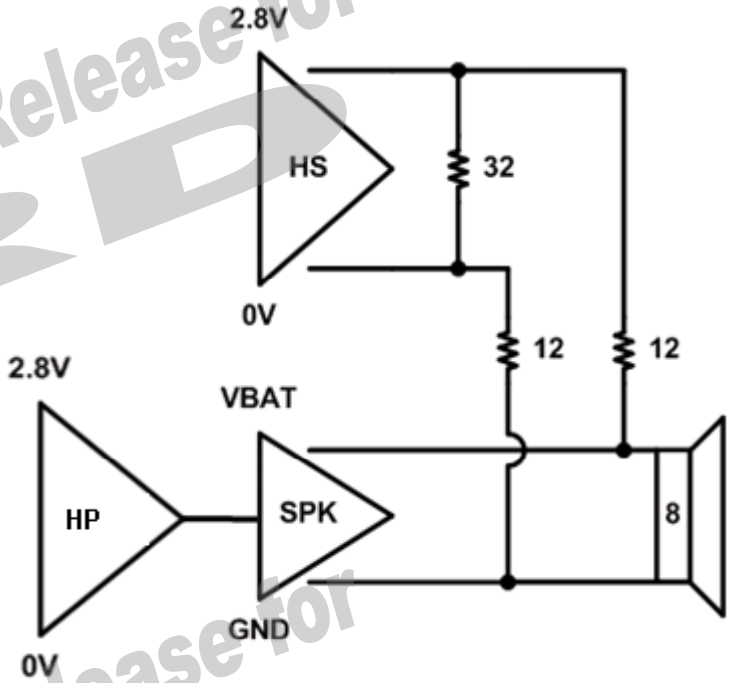
	1	2	3	4	5	6	7	8
A	NC	NC	AU_FMINR	AU_VCM		AU_MOUTR	AU_OUT0_N	
B	NC	APC	AU_FMINL	AU_MICBIAS	AU_MOUTL	DRV	AU_OUT0_P	AVDD28_AFE
C	AU_VIN1_N	AU_VIN1_P	AGND28_AFE		AVDD28_PLL		BATON	
D		AU_VIN0_P	AUX_IN4		AVDD28_RFE	VCDT		
E	XP	AU_VIN0_N			RESETB	AUX_IN5		
F	YP	XM	YM		ISINK0			

Layout rule

- The AU_VCM cap should be put close to the BB chip, the trace should be as short as possible
  - Prevent cross-over with power signal
  - Prevent to route it in parallel with other traces
- The GND of AU_VCM cap should be connected to the ball C3 first and then connected system GND with single via to make sure the GND is clear
  - For 6-layers PCB, the system GND is the GND plan of the PCB
  - For 4-layers PCB, the system GND is the GND that has largest GND area (top or bottom layer)
  - The via should be far-way from the high power signal, especially for VBAT (please see the case study in the next slide)

2-in-1 application circuit

- 2 resistor 12Ω are used to construct the equivalent 32Ω load at HS
- A resistor 32Ω is needed to avoid the current leakage from SPK amp output to the HS (voice buffer)



Confidential B

Image Sensor Design Notice

Parallel Image Sensor Interface

BB Chip (Pin definition)	Camera side
CMVREF	VSYNC
CMHREF	HSYNC
CMPCLK	PCLK
CMMCLK	MCLK
SDA	SIOD
SCL	SIOC
CMRST	RESETB
CMPDN	PWDN
CMDAT0~CMDAT7	DATA0 ~ DATA7

Serial Image Sensor Interface

BB Chip (Pin definition)	Camera side
MCLK	Master Clock
CSD	SPI Data Output
CSK	SPI Clock Output
SDA	I2C Data Output
SCL	I2C Clock Output
CAMRST	Reset
CMPDN	PWDN

Sensor Module Selection

Sensor Module Selection

Camera Reference Circuit

For Parallel Sensor :

EMI filter cap. max. loading is 30pf

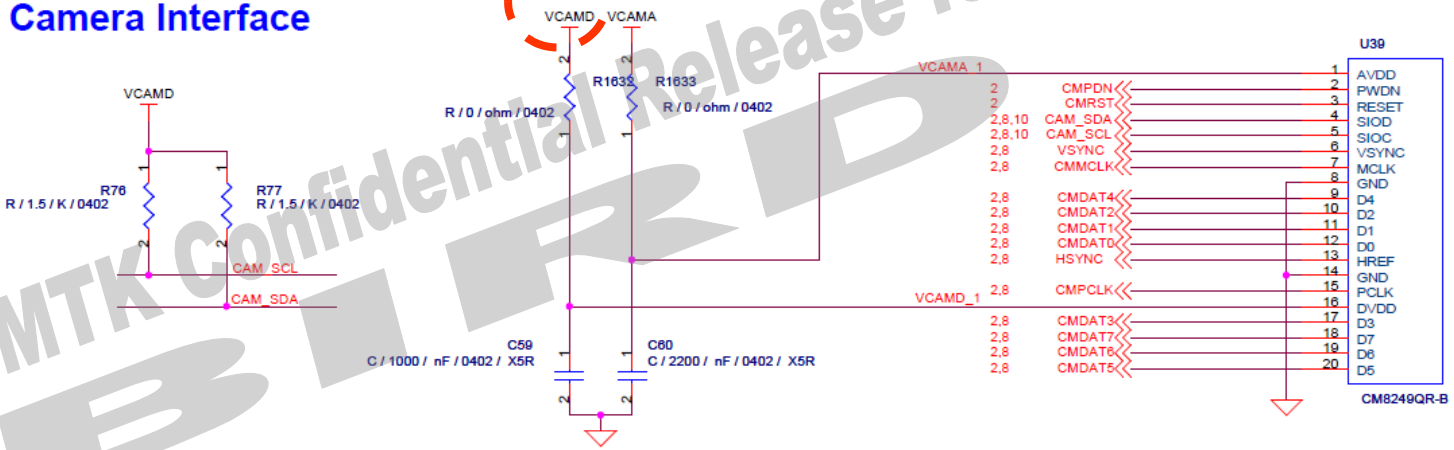
For Serial sensor :

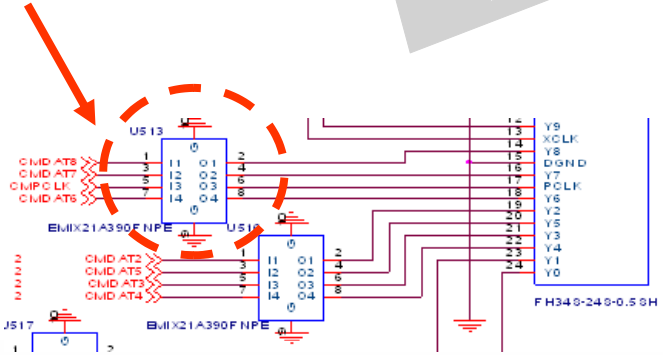
EMI filter cap. max. loading is 30pf

Please check VCAMD Current can meet sensor requirement or not.

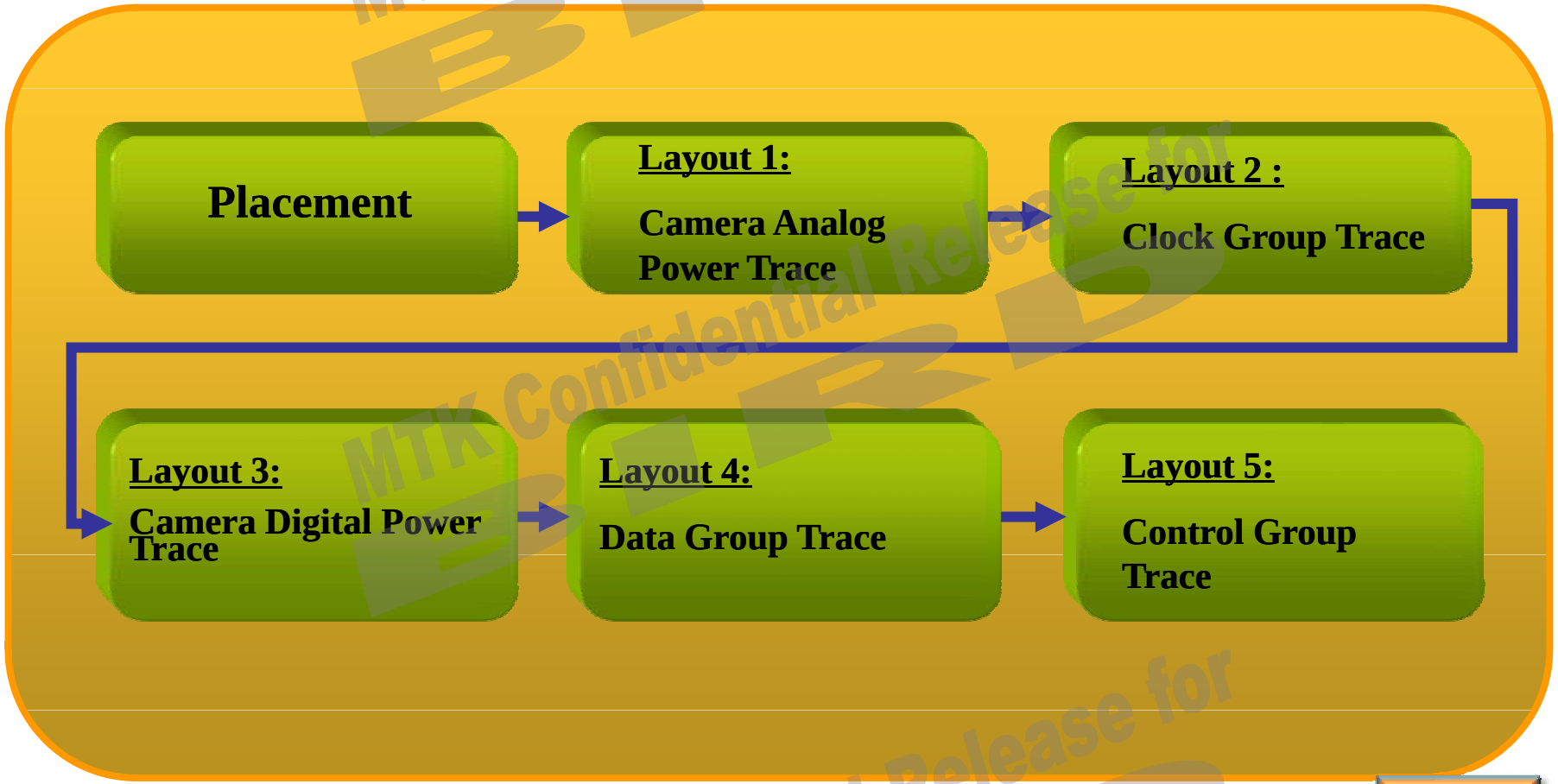
VCAMD Imax = 100mA

Camera Interface





PCB Design Flow

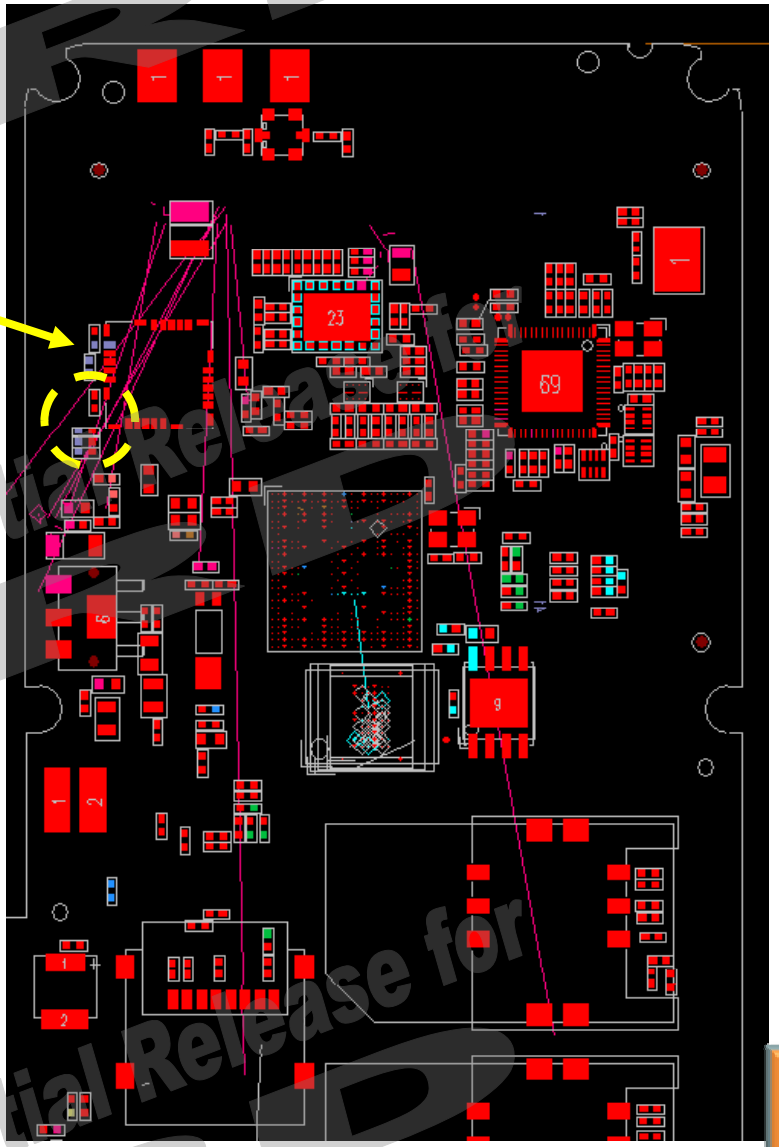


Design Notice – Image Sensor

- **PCB Component Placement recommend :**

➢To minimize RF radiation interference, do not place the sensor module near or beneath the antenna.

➢The sensor module's power supplies(inductors , beads , resistors , capacitors) should be placed as close as possible to the connect



Design Notice – Camera

- **General Routing recommend :**

➢With minimum trace lengths, route high-speed clock and high-speed data differential pairs first.

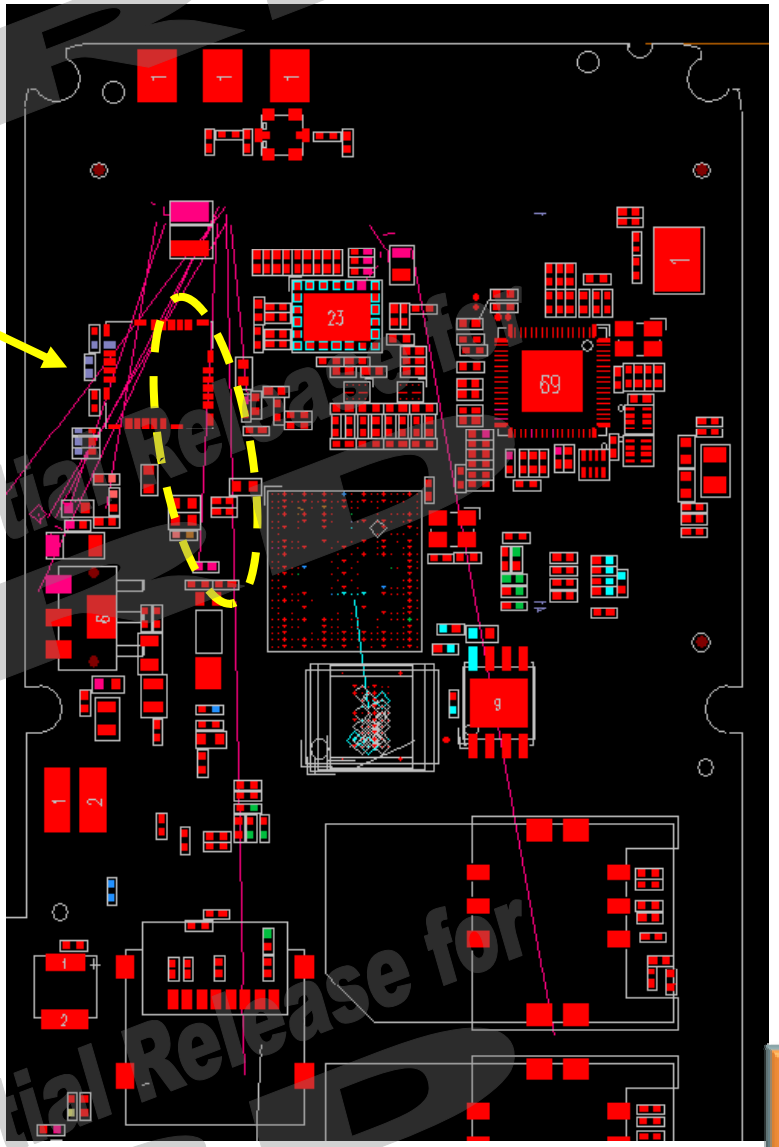
➢Route signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.

➢When it becomes necessary to turn 90 ° , use two 45 ° turns or an arc instead of making a single 90 ° turn. This reduces reflections on the signal by minimizing impedance discontinuities.

➢Do not route signal traces under crystals, oscillators, clock synthesizers, magnetic devices.

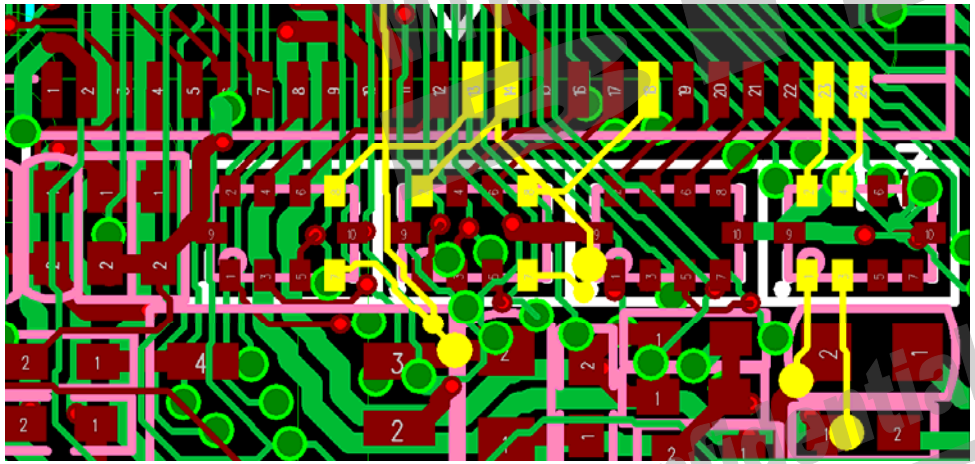
➢Route all traces over continuous planes

➢Keep all signals clear of the core logic set.



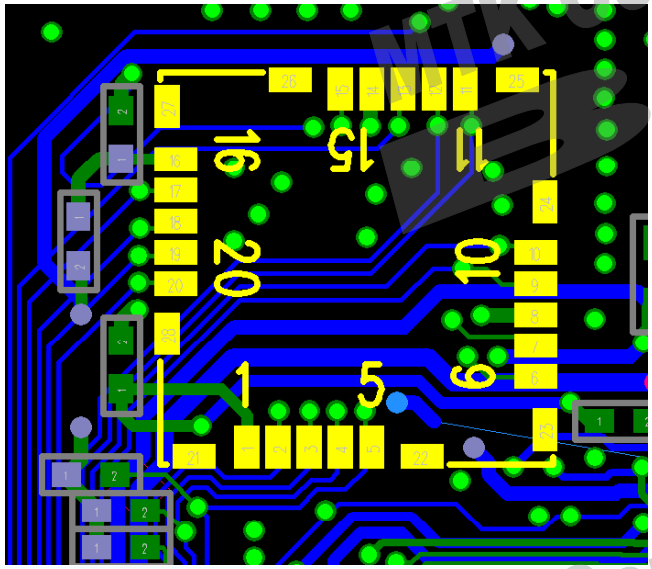
Design Notice – Camera

- **General Routing recommend :**



1.EMIF shall be placed as close as camera connector.

2.Don’t routing the trace to cross EMIF input and output. (L1 & L2)



3.Reduce the routing trace on top layer.
4.Don’t routing the unrelated signal on L2 pad.
(GND signal is OK)

Design Notice – Single Camera

- **Single Image Sensor Interface :**

The Image Sensor interface is divided up into three groups summarized in below that each group has special routing guidelines. The interconnecting lengths in the controller package should be calculated for the length matching.

Group	Signal Name	Description
Data	DQ[0:7] CMVREF CMHREF	Image sensor data[0:7] input Image sensor vertical reference signal input Image sensor horizontal reference signal input
Clock	MCLK PCLK	Image sensor master clock output Image sensor pixel clock input
Control	SCL SDA CMRST CMPDN CMFLASH	I2C clock output I2C data input/output Image sensor reset signal output Image sensor power down signal output Image sensor Flash signal output

Design Notice – Single Camera

- **PCB Layout Design Notice (1/3) (nice to have)**

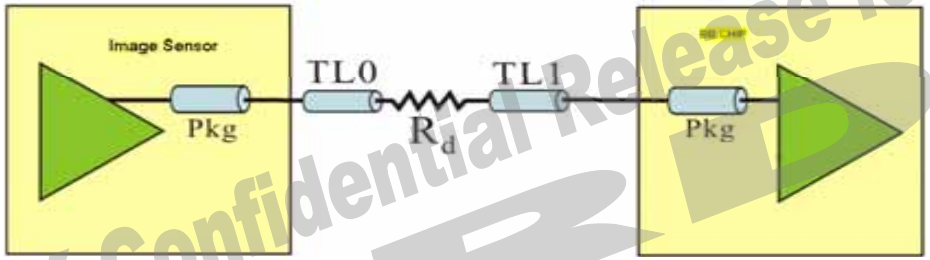
This section states the layout recommendations for the image sensor data group routing. Refer to below figure for the data group topology and below table for the routing guidelines. Data group shall be routed surround with ground plan

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Image Sensor Data)	W = 4-mil, S ≥ 4-mil.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Max. TL0 (BB ball to Image Sensor Connect)	4,800 mils
Length matching	Max. (Trace length) − 500mil ≤ (Trace length) ≤ Max. (Trace length)
Remark	Data Group shall be routed surround with ground plan

Design Notice – Single Camera

- **PCB Layout Design Notice (2/3)** (high priority-Must!!)

This section states the layout recommendations for the Image Sensor clock signals. Refer to below figure for the clock topology and below table for the routing guidelines. Each clock shall be routed surround with ground plan. The R_d is optional that could be different from 0 or 22 Ω if the different controller I/O is designed or the different driving strength is assigned.



Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground plane.
Main trace patterns (MCLK PCLK)	W = 4-mil, S ≥ 4-mil.Surround the CLK with ground plan.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Damping resistor (R_d)	Optional, 0 or 22 Ω (Near the Image Sensor).
Max. (TL0 + TL1)	4,500 mils
Length matching for Data-to-PCLK	(PCLK length − 500-mil) ≤ DQ length ≤ (PCLK length + 500-mil)
Remark	Each clock shall be routed surround with ground plan (high priority) [MCLK , PCLK]

Design Notice – Single Camera

- **PCB Layout Design Notice (3/3) (nice to have)**

This section states the layout recommendations for the Image Sensor control signals. Refer to below figure for the control topology and below table for the routing guidelines.

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns	W = 4-mil, S ≥ 4-mil.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Max. TL0	6000 mils
Remark	Control Group shall be routed surround with ground plan

Design Notice – Dual Camera

- **Dual Image Sensor Interface :**

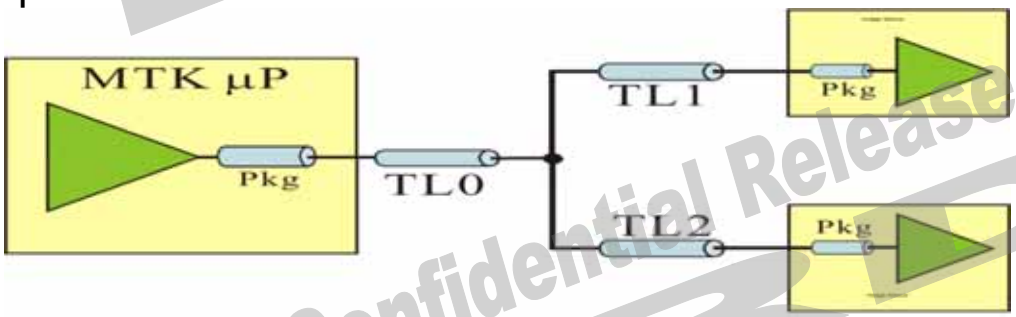
The Image Sensor interface is divided up into three groups summarized in below that each group has special routing guidelines. The interconnecting lengths in the controller package should be calculated for the length matching.

Group	Signal Name	Description
Data	DQ[0:7] CMVREF CMHREF	Image sensor data[0:7] input Image sensor vertical reference signal input Image sensor horizontal reference signal input
Clock	MCLK PCLK	Image sensor master clock output Image sensor pixel clock input
Control	SCL SDA CMRST CMPDN CMFLASH	I2C clock output I2C data input/output Image sensor reset signal output Image sensor power down signal output Image sensor Flash signal output

Design Notice – Dual Camera

- **PCB Layout Design Notice (1/3) (nice to have)**

This section states the layout recommendations for the dual camera image sensor data group routing. Refer to below figure for the data group topology and below table for the routing guidelines. Data group shall be routed surround with ground plan

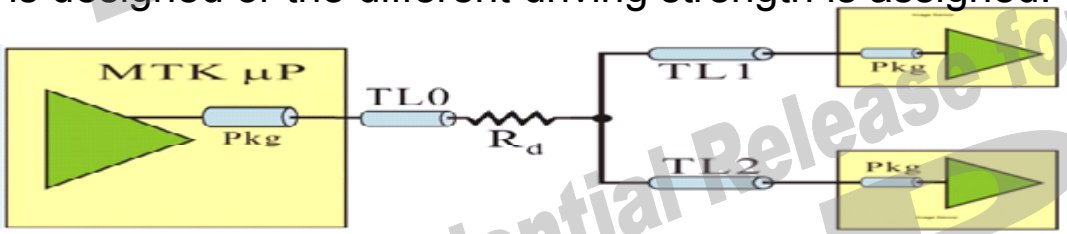


Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Image Sensor Data)	W = 4-mil, S ≥ 4-mil.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Max. TL0 + TL1 (BB ball to Main Image Sensor Connect)	4,800 mils
Max. TL1 (Branch points to Sub Image Sensor Connect)	1,500 mils
Length matching(TL0+TL1)	Max. (Trace length) − 500mil ≤ (Trace length) ≤ Max. (Trace length)
Remark	Data Group shall be routed surround with ground plan

Design Notice – Dual Camera

- **PCB Layout Design Notice (2/3)** (high priority-Must!!)

This section states the layout recommendations for the Image Sensor clock signals. Refer to below figure for the clock topology and below table for the routing guidelines. Each clock shall be routed surround with ground plan. The R_d is optional that could be different from 0 or 22 Ω if the different controller I/O is designed or the different driving strength is assigned.

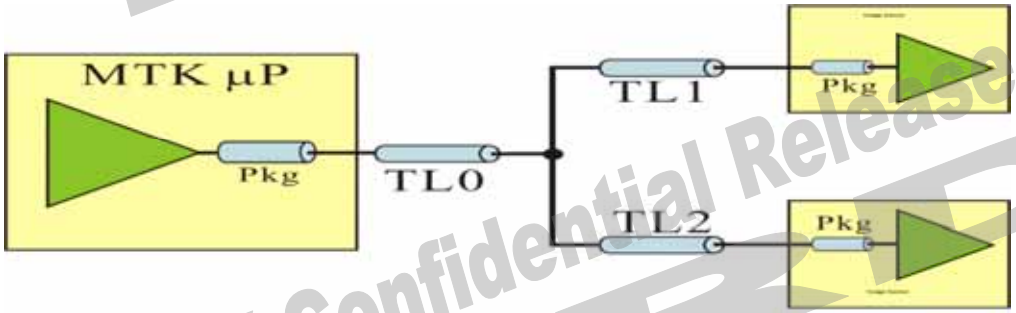


Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground plane.
Main trace patterns (MCLK PCLK)	W = 4-mil, S ≥ 4-mil.Surround the CLK with ground plan.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Damping resistor (R_d)	Optional, 0 or 22 Ω (Near the Image Sensor).
Max. TL0 + TL1 (BB ball to Main Image Sensor Connect)	4,500 mils
Max. TL1 (Branch points to Sub Image Sensor Connect)	1,500 mils
Length matching for Data-to-PCLK(TL0+TL1)	(PCLK length − 500-mil) ≤ DQ length ≤ (PCLK length + 500-mil)
Remark	Each clock shall be routed surround with ground plan (high priority) [MCLK, PCLK]

Design Notice – Dual Camera

- **PCB Layout Design Notice (3/3) (nice to have)**

This section states the layout recommendations for the dual Image Sensor control signals. Refer to below figure for the control topology and below table for the routing guidelines.



Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns	W = 4-mil, S ≥ 4-mil.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Max. TL0 + TL1 (BB ball to Main Image Sensor Connect)	6,000 mils
Max. TL1 (Branch points to Sub Image Sensor Connect)	2,000 mils
Remark	Control Group shall be routed surround with ground plan

Design Notice – Serial Camera

- **Serial Image Sensor Interface :**

  The Image Sensor interface is divided up into three groups summarized in below that each group has special routing guidelines. The interconnecting lengths in the controller package should be calculated for the length matching.

Group	Signal Name	Description
SPI	CSD CSK	Image sensor SPI data output Image sensor SPI CLK output
Clock	MCLK	Image sensor master clock output
Control	SCL SDA CMRST	I2C clock output I2C data input/output Image sensor reset signal output

Design Notice – Serial Camera

- **PCB Layout Design Notice (1/3) (nice to have)**

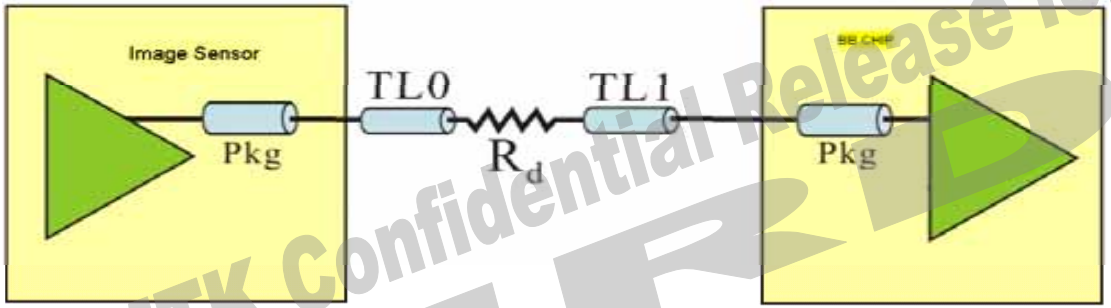
This section states the layout recommendations for the image sensor SPI group routing. Refer to below figure for the data group topology and below table for the routing guidelines. Data group shall be routed surround with ground plan

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Image Sensor Data)	W = 4-mil, S ≥ 4-mil.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Max. TL0 (BB ball to Image Sensor Connect)	6,000 mils
Length matching in PCB	100 mils.
Remark	SPI Group shall be routed surround with ground plan

Design Notice – Serial Camera

- **PCB Layout Design Notice (2/3)** (high priority-Must!!)

This section states the layout recommendations for the Image Sensor clock signals. Refer to below figure for the clock topology and below table for the routing guidelines. Each clock shall be routed surround with ground plan. The R_d is optional that could be different from 0 or 22 Ω if the different controller I/O is designed or the different driving strength is assigned.



Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground plane.
Main trace patterns (MCLK PCLK)	W = 4-mil, S ≥ 4-mil.Surround the CLK with ground plan.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Damping resistor (R_d)	Optional, 0 or 22 Ω (Near the Image Sensor).
Max. (TL0 + TL1)	6,000 mils
Remark	Each clock shall be routed surround with ground plan (high priority) [MCLK, CSK]

Design Notice – Serial Camera

- **PCB Layout Design Notice (3/3) (nice to have)**

This section states the layout recommendations for the Image Sensor control signals. Refer to below figure for the control topology and below table for the routing guidelines.

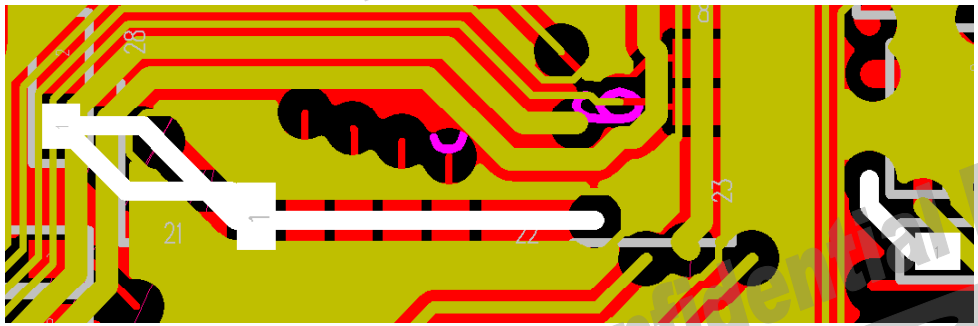
Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns	W = 4-mil, S ≥ 4-mil.
Break-out/Break-in area (under the BGA package area)	W ≥ 3-mil, S ≥ 3-mil.
Max. TL0	6000 mils
Remark	Control Group shall be routed surround with ground plan

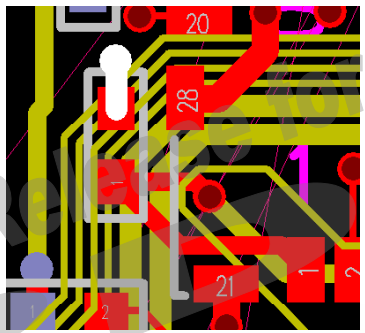
Design Notice – Camera

- **Analog Power Routing (high priority-Must)**

This section states the layout recommendations for the image sensor Analog power routing. Refer to below table for the routing guidelines. Analog Power shall be routed surround with ground plan

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Analog Power)	W ≥ 12-mil, S = 4-mil with GND trace.
Remark	Analog power must be routed surround with ground plan De-couple cap shall connect to main ground directly.



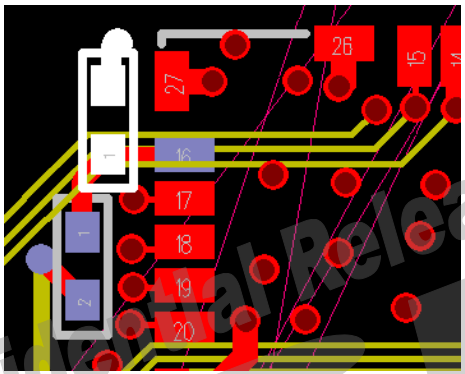


Design Notice – Camera

- **Digital Power Routing**

This section states the layout recommendations for the image sensor digital power routing. Refer to below table for the routing guidelines. Digital Power shall be routed surround with ground plan

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Digital Power)	W ≥ 12-mil, S = 4-mil with GND trace.
Remark	Digital power shall be routed surround with ground plan. De-couple cap shall connect to main ground directly. (Must)



Camera bus configuration.

2.8V I2C		MODE selection	Driving	Pull up	Pull down
CAM_SCL	URXD2	GPIO22 = 3	GPIO22	GPIO22	GPIO22
CAM_SDA	UTXD2	GPIO23 = 3	GPIO23	GPIO23	GPIO23
CAM_SCL	KCOL4	GPIO3 = 3	GPIO3	GPIO3	GPIO3
CAM_SDA	KCOL5	GPIO4 = 3	GPIO4	GPIO4	GPIO4
CAM_SCL	GPIO70	GPIO70 = 4	GPIO70	GPIO70	GPIO70
CAM_SDA	KROW7	GPIO45 = 4	GPIO45	GPIO45	GPIO45

1.8V I2C		MODE selection	Driving	Pull up	Pull down
CAM_SCL	UCTS1_B	GPIO24 = 2	GPIO24	GPIO24	GPIO24
CAM_SDA	URTS1_B	GPIO25 = 2	GPIO25	GPIO25	GPIO25
CAM_SCL	ED7 (L only)	GPIO_SPMODE1[10:8] = 5	ACIF_CON1[30:28]	EMI_IOB[4]	EMI_IOB[5]
CAM_SDA	ED6 (L only)	GPIO_SPMODE1[6:4] = 5	ACIF_CON1[30:28]	EMI_IOB[4]	EMI_IOB[5]

2.8V Parallel sensor		MODE selection	Driving	Pull up	Pull down
CMRST	CMRST	GPIO60 = 1	GPIO60	GPIO60	GPIO60
CMPDN	CMPDN	GPIO57 = 1	GPIO57	GPIO57	GPIO57
CMMCLK	CMMCLK	GPIO58 = 1	GPIO58	GPIO58	GPIO58
CMPCLK	CMPCLK	GPIO59 = 1	GPIO59	GPIO59	GPIO59
CMHREF	CMHREF	GPIO56 = 1	GPIO56	GPIO56	GPIO56
CMVREF	CMVREF	GPIO55 = 1	GPIO55	GPIO55	GPIO55
CMDATA0~7	CMDAT0~7	GPIO47-54 = 1	GPIO47-54	GPIO47-54	GPIO47-54

1.8V Serial sensor		MODE selection	Driving	Pull up	Pull down
CMMCLK	EA12	GPIO_SPMODE0[25:24] = 2	ACIF_CON0[30:28]	ACIF_CON1[16]	ACIF_CON1[17]
CSK	EA13	GPIO_SPMODE0[27:26] = 2	ACIF_CON0[30:28]	ACIF_CON1[16]	ACIF_CON1[17]
CSD	EA14	GPIO_SPMODE0[29:28] = 2	ACIF_CON0[30:28]	ACIF_CON1[16]	ACIF_CON1[17]
CMPDN	EA15	GPIO_SPMODE0[31:30] = 2	ACIF_CON0[30:28]	ACIF_CON1[16]	ACIF_CON1[17]

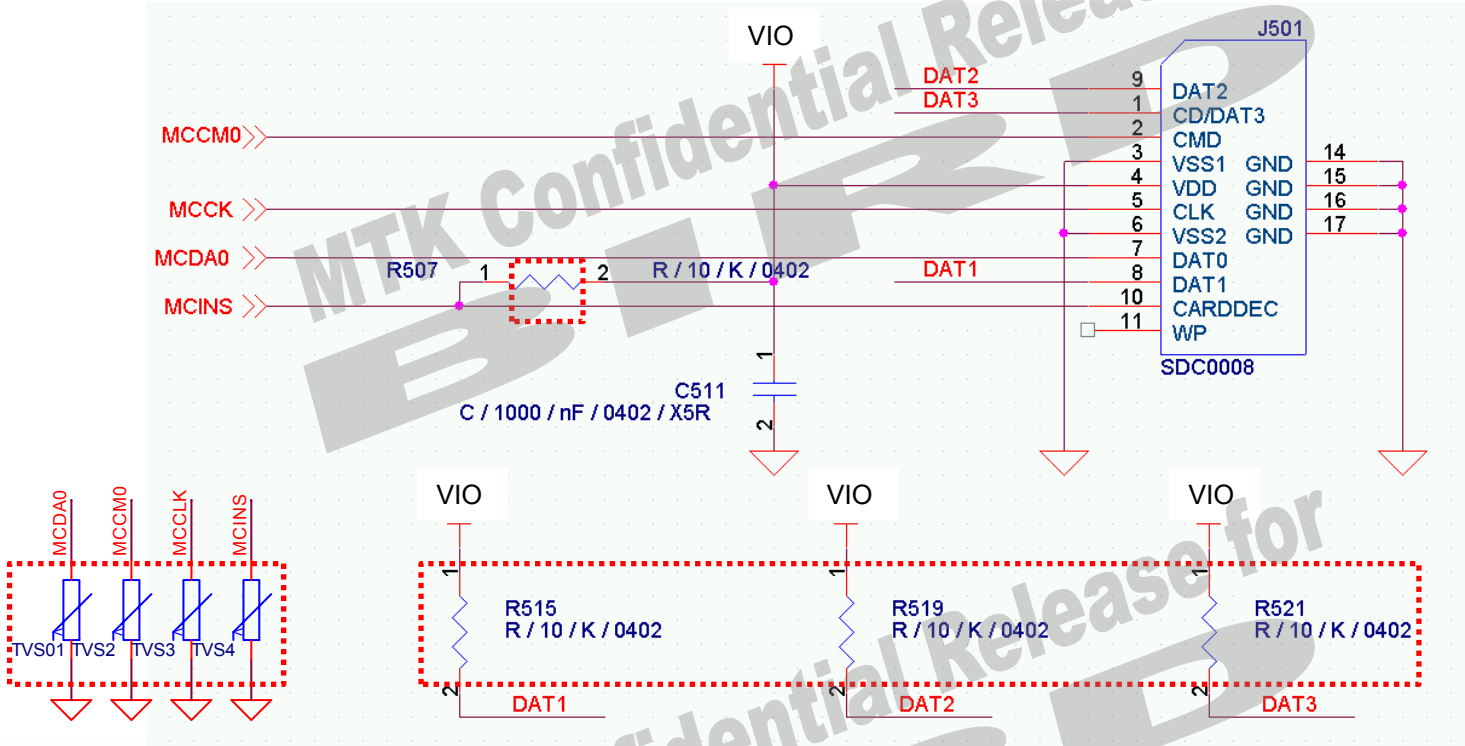
2.8V Serial sensor		MODE selection	Driving	Pull up	Pull down
CMMCLK	CMMCLK	GPIO58 = 1	GPIO58	GPIO58	GPIO58
CSK	CMPCLK	GPIO59 = 2	GPIO59	GPIO59	GPIO59
CSD	CMDAT0	GPIO47 = 2	GPIO47	GPIO47	GPIO47
CMPDN	CMPDN	GPIO57 = 1	GPIO57	GPIO57	GPIO57

Confidential B

MT6252 MSDC Design Notice V0.3

Connector with Card Detection Pin

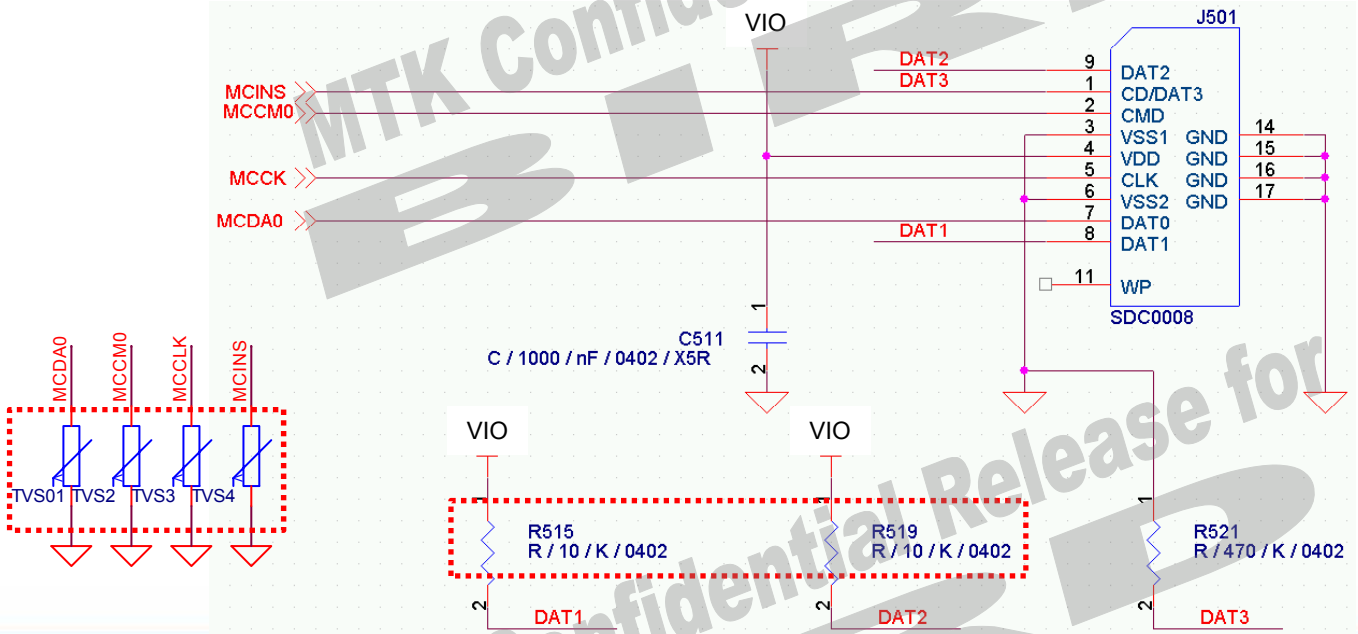
1. Reserve external PU resistors for DAT1/2/3 & MCINS in connector side
2. Reserve ESD protection device on CMD/CLK/DAT/MCINS with Cap < 15pF
3. VIO must always be on for hot plug detection



Connector without Card Detection Pin

- Use DAT3 for hot-plug detection

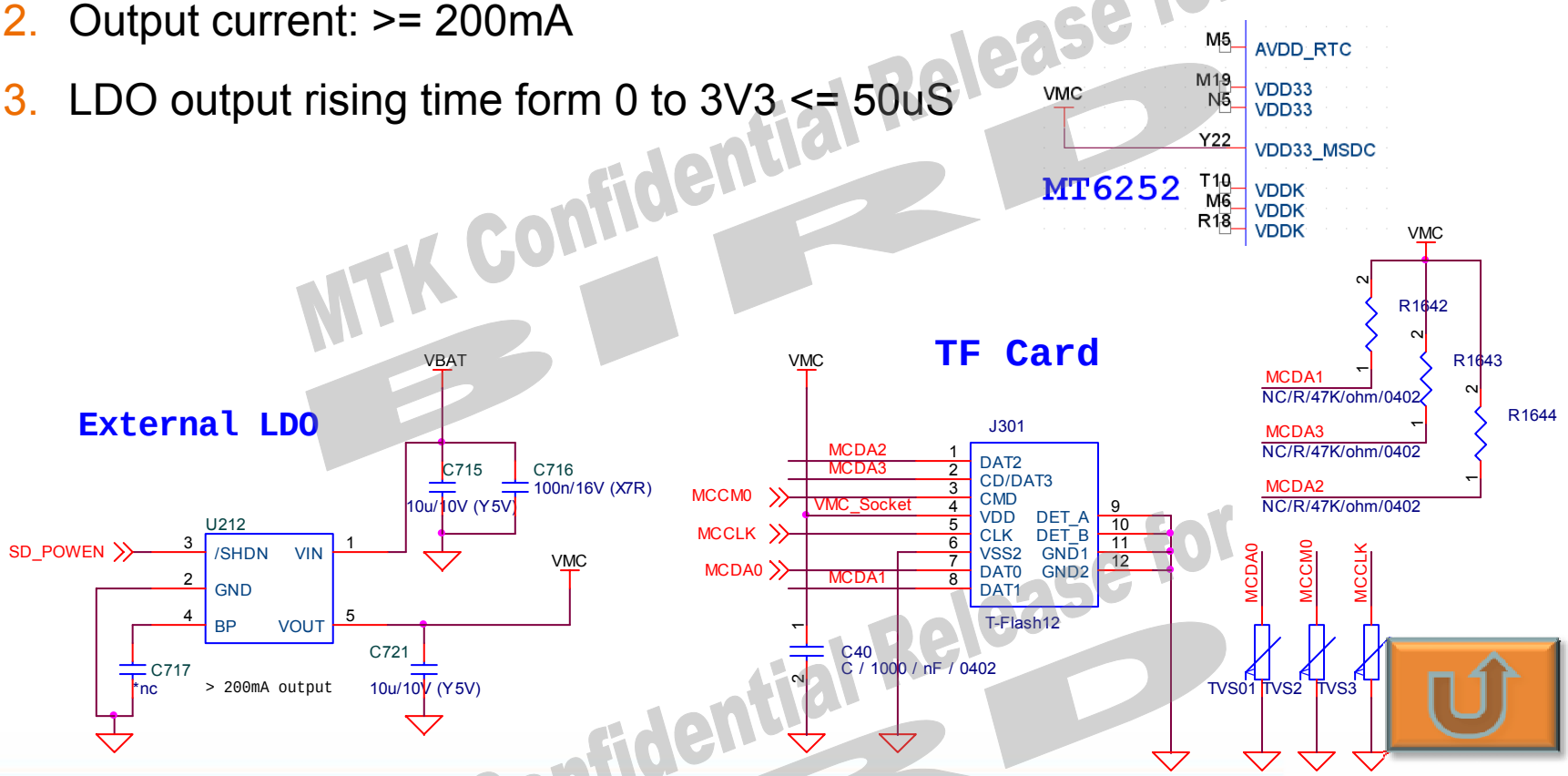
1. Reserve external PU resistors for DAT1/2 in connector side
2. Reserve ESD protection device on CMD/CLK/DAT/MCINS with Cap < 15pF
3. DAT3 must be PD with external 470Kohm resistor
4. Compile option for DAT3 detection: __MSDC_TFLASH_DAT3_1BIT_HOT_PLUG__
5. VIO must always be on for hot plug detection



Better T-card Compatibility

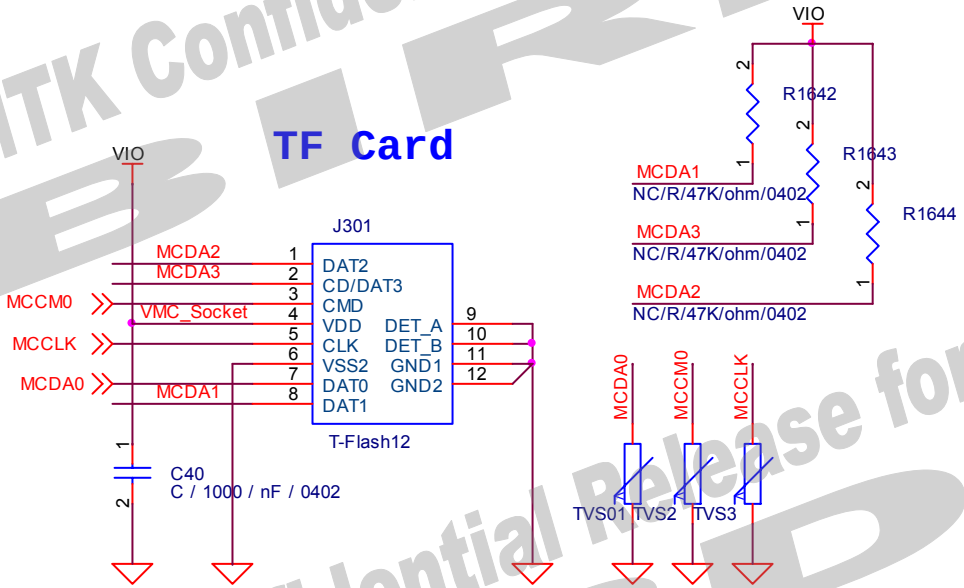
An external LDO for T-card (and MT6252 VDD33_MSDC) is suggested

1. Output voltage: 3V3
2. Output current: >= 200mA
3. LDO output rising time form 0 to 3V3 <= 50uS



MT6252 Example Circuit

1. Reserve external PU resistors for DAT1/2/3 in connector side
2. Reserve ESD protection device on CMD/CLK/DAT with Cap < 15pF



Layout Guidelines

1. DAT, CMD, CLK 一起走
2. 若無法全部一起走，優先順序為: ((DAT + CLK) + CMD)
3. CLK 左右要包GND，避免受到干擾
4. DAT, CMD, CLK 線長最大誤差控制在1000mil以內 (預估time difference在 160pS以內)

Confidential B

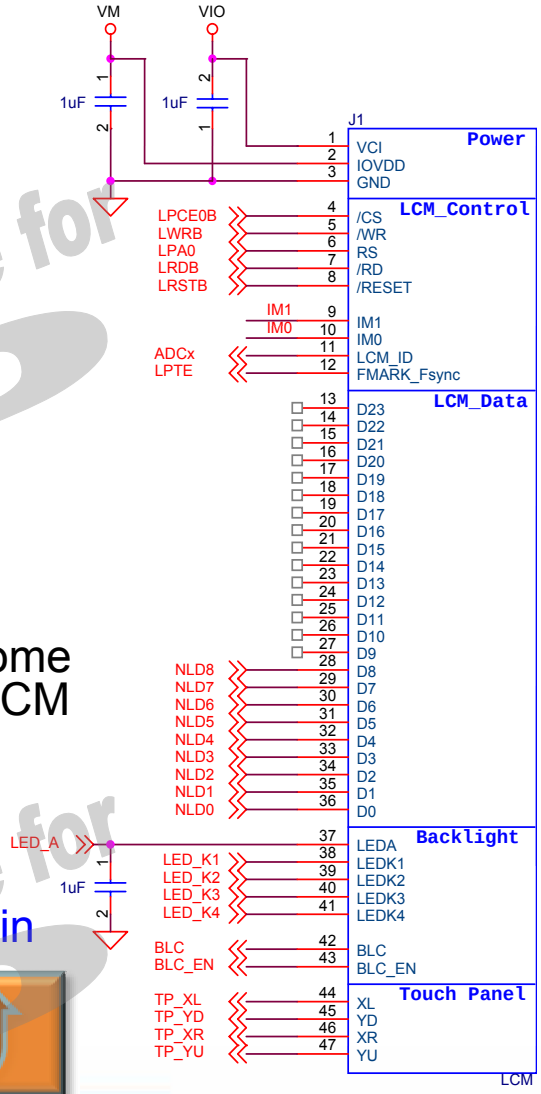
MT6252 LCM Design Notice

LCM Design Note – Overview

- Display Resolution
  - Support up to Main QVGA (main display) + QVGA (sub display)
- Interface
  - Supports CPU 8/9/16 bit interface
  - Dedicated HW tearing free control
- Power
  - Support **1.8v** IO level LCM (**6252 only support 1.8V I/O**)
  - Support Parallel-4 LCM backlight controller
- Dual display feature is supported
  - Parallel 8/9 (main) + Parallel 8/9 (sub)
  - Parallel 8/9 (main) + SPI (sub)

LCM Design Note – Parallel Interface

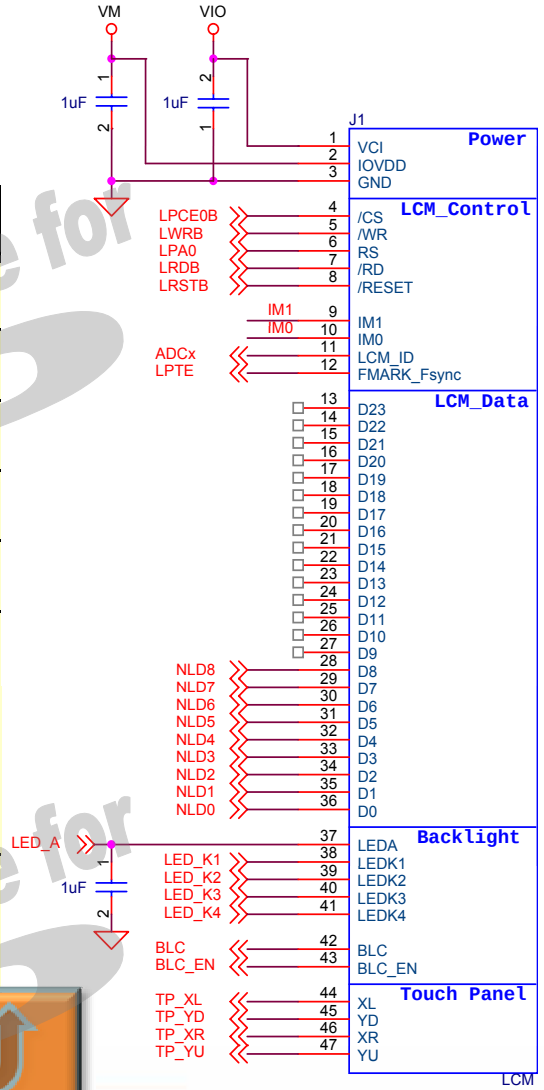
- Power
  - VCI : connect to 2.8v for LCM analog power
  - IOVDD : connect to 1.8v depends on LCM IO level
    - LCM IO level should follow EMI bus power level
- LCM Control
  - All LCM control pin are reserved at BB side
  - IM[1:0] : Interface Mode should reference IOVDD level
  - LCM_ID pin connetc to Aux_ADC for
- LCM Data
  - All LCM data pin are reserved at BB side
  - For 8 bit interface, some LCM use lower byte D[7:0], some use D[23:16]. Be sure data pin connect to the correct LCM pins.
- Backlight
  - Connect backlight anode to VBAT with a bypass cap
  - Connect backlight cathod to BB dedicated ISINK[0:3] pin
- Touch Panel
  - Connect to dedicated 4-wire R-type TP pin



LCM Design Note – Parallel Interface

- Parallel Interface Pin List

MT6252 (Pin definition)		LCM side
LPCE0B	Y19	/CS
LWRB	Y13	/WR
LPA0	Y14	RS
LRDB	AA13	/RD
LRSTB	AC5	/RESET
NLD8~NLD0	W20, AA21, Y21, AB22, W18, Y20, AA17, Y17, AA14	Note1
NLD15~NLD9	AB23, V21, T19, Y10, Y9, AA10, AA9	
LPTE	AC4	FMARK / F_Sync

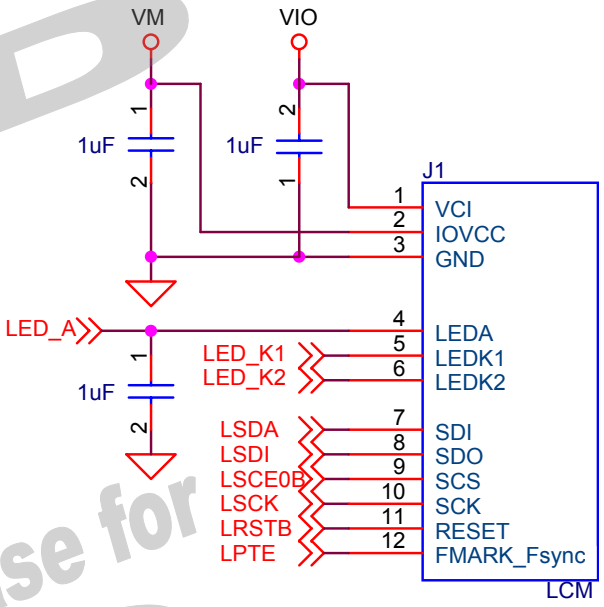


Note 1 : Check the correct data pins from LCM spec.

LCM Design Note – Serial Interface

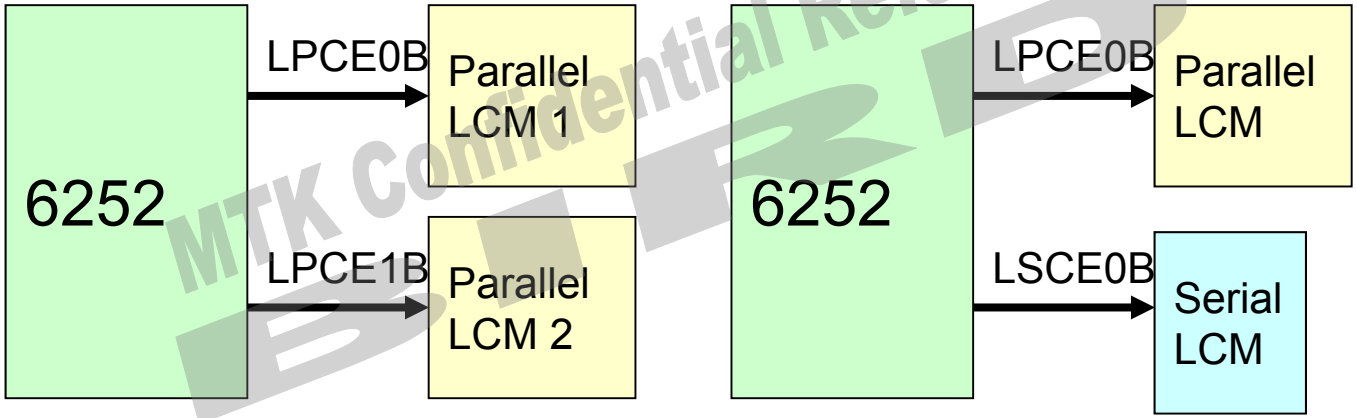
- Sometimes ULC LCM don't support F_Sync function. If supported, please connect to BB LCD_TE(pin AC4)

MT6252 (Pin definition)		LCM side
LSDA (EA4)	AA17	SDI
LSDI (EA6)	Y20	SDO
LSCK (EA3)	AA14	SCK
LRSTB	AC5	RESET
LSCE0B	Y19	SCS
LCD_TE	AC4	FMARK / F_Sync



LCM Design Note – Dual LCM

- Dual LCM mode



Supporting 1.8V I/O LCM Vendor Survey

No	Vendor	On-going 2.8v/1.8v compatible LCM Percentage	Vendor’ s feedback
1	Truly	> 90%	• 华南地区产品超过一半的OEM型号能兼容2.8V/1.8V • 华东、华北地区客户的产品绝大部分都可以兼容2.8/1.8V。 • 之前较早时期的显示模组，能够同时兼容2.8V/1.8V的比例会少一些 • 标准品超过90%会做2.8V/1.8V的IOVCC兼容(仅在某款产品是在依据某一客户具体要求而开的标准品中才会出现仅仅支持2.8V的情况) • OEM型号，则看客户的要求，之前部分客户的主板只能提供一个电压给LCM，要求的FPC pin数量尽量少会做成仅支援2.8V的方式。
2	WistronOPT	> 90%	• 新開發產品全面支援2.8v/1.8v兼容
3	BYD	TBD	目前的产品都尽可能将IO Power Supply单独接口，但是由于个别客户早期的主板只保留了1个2.8V Power Supply的供应，LCD产品不得不将IOVCC与VCI连接在一起使用。这种单电源供应产品不是很多，大部分集中在小尺寸产品上。
4	BOE	~ 81%	目前我司LCM是有一些在接口上只有一路电压（即2.8V)，当然这些产品应用的手机平台不全部是MTK的。对于这个问题，我司后续与客户进行项目沟通时会传递这个信息，尽量在新项目中采用分开电压的设计。
5	Tainma (SH)	~90%	绝大部分产品都是2.8v/1.8v IO compatible。
6	Varitronix	TBD	
7	SHARP	TBD	
8	LGD	100%	• There is no LGD panel and Module spec supporting 2.8V Iovcc only. • 2.8v/1.8v io compatible is the normal D-IC spec for Vcc and Iovcc.

MTK LCM IO Level Trend

- **不建議與建議的LCM Module Spec**
  - This LCM has only “One Power Pins” (no separated VCI and IOVCC power pins)
  - Supply voltage allows 3V only which means IO level **can’t** support 1.8V

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta=25±5°C, VDD=VDDIO=3.0V, GND=0V.

Table 5

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage (Logic)	VDD-GND		-	3.0	-	V
Supply voltage (LCD)	VLCD	Ta=-20°C, Note 1, VDD=3.0V	-	TBD	-	V
		Ta=+25°C, Note 1, VDD=3.0V	-	TBD	-	V
		Ta=+70°C, Note 1, VDD=3.0V	-	TBD	-	V
Supply Current (Logic & LCD)	IDD	All mode, VDD =3.0V	-	TBD	-	mA
Input high voltage	V_{IH}	VDD=3.0V	0.8VDDIO	-	VDDIO	V
Input low voltage	V_{IL}		GND	-	0.2VDDIO	V
Supply voltage of white LED backlight	VLED	Forward current =30mA	3.0	3.2	3.4	V
Luminance of backlight		Number of LED dies=2	3000	3500	-	cd/m²

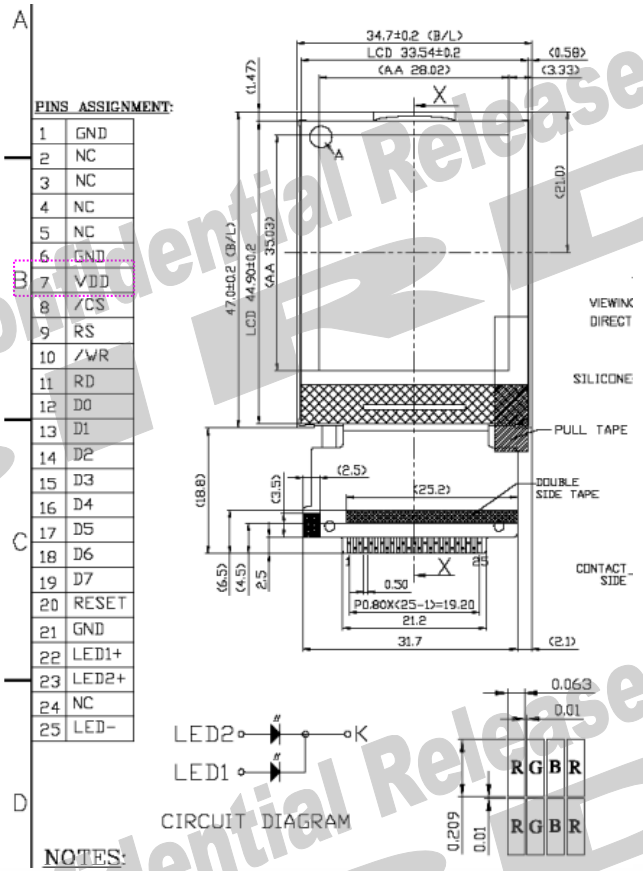
Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

$VDD_{,typical}$ = 3V

Non-separate

power pin

Only one pin



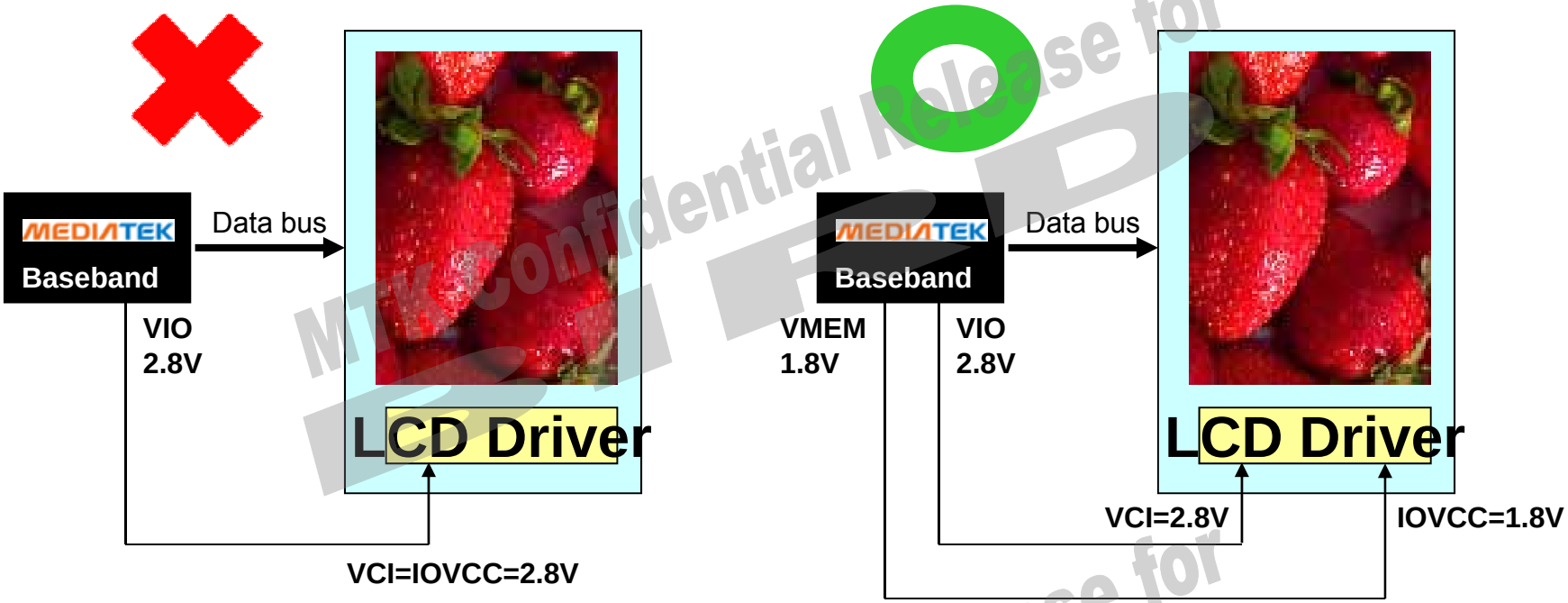
Separate

power pin

Pin	Pin Name
1	GND
2	LED A
3	LED K1
4	LED K2
5	LED K3
6	VCI
7	DNC
8	NCS
9	TE
10	NRESET
11	SDI
12	NRD/E
13	NWR/RNW/SCL
14	DB17
15	DB16
16	DB15
17	DB14
18	DB13
19	DB12
20	DB11
21	DB10
22	IM2
23	IM1
24	SDO
25	IOVCC
26	XL
27	YU
28	XR
29	YD
30	GND

MTK LCM IO Level Trend

- MTK recommend LCM connection



MEDIATEK

MT6252 RF Design Note

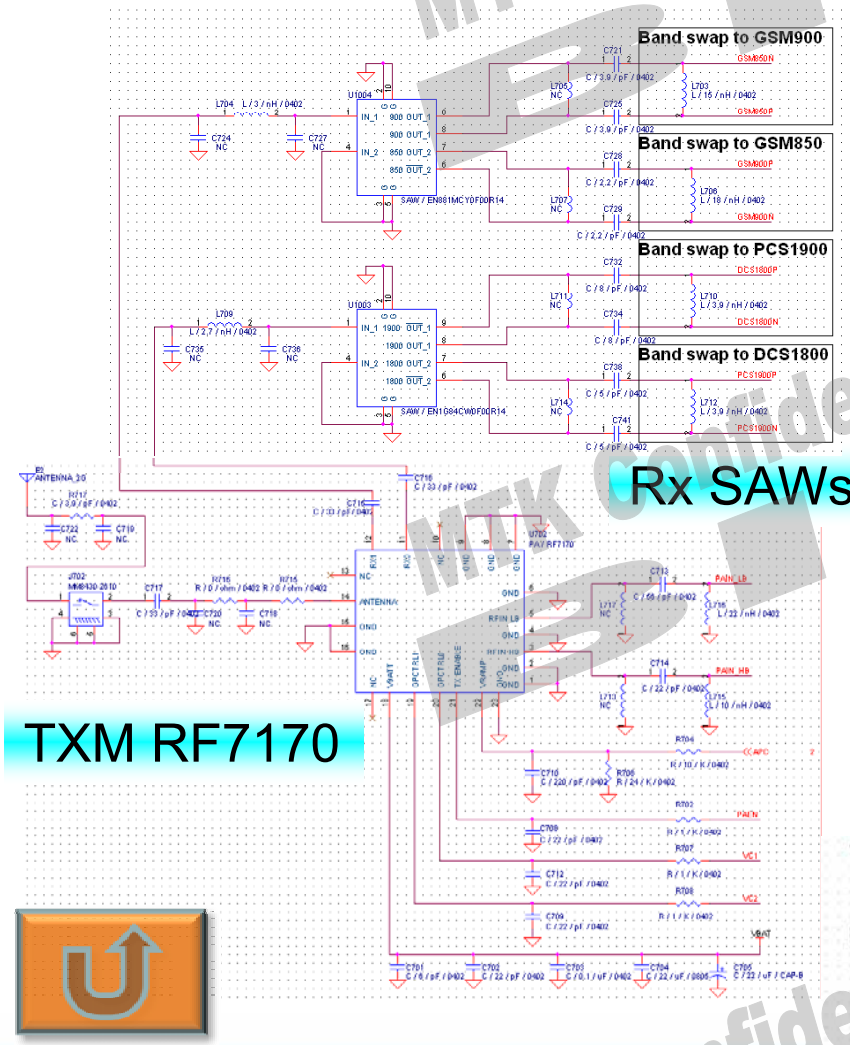
Outline

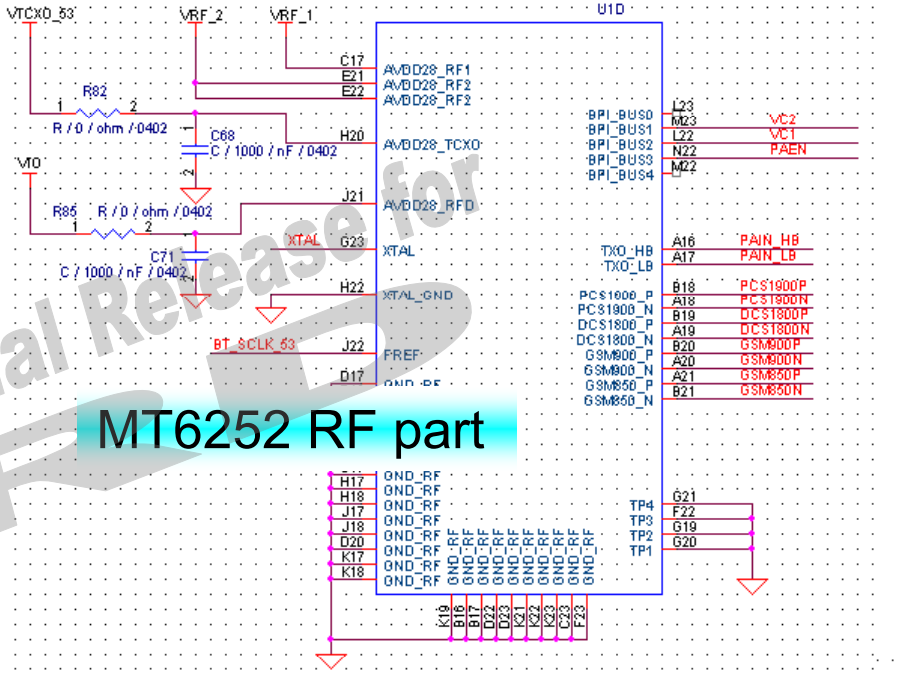
- Reference design
- META tools
- Key RF components
- Modify BPI and timing for MT6252

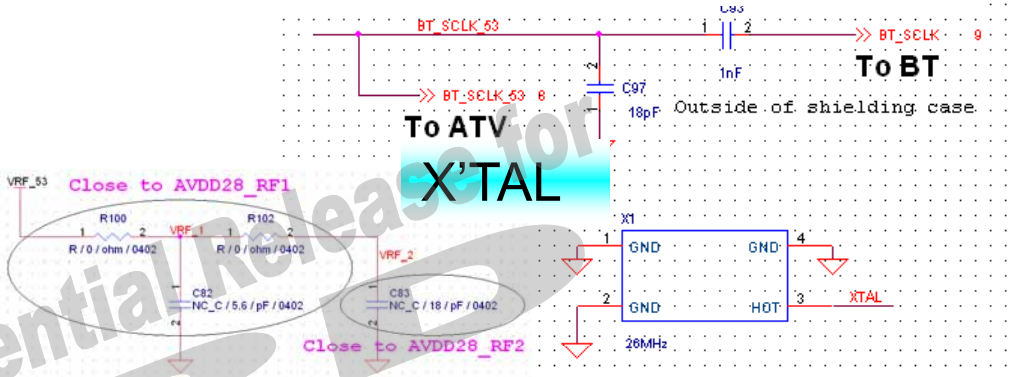
Confidential B

Reference Design

Quad-band Schematic







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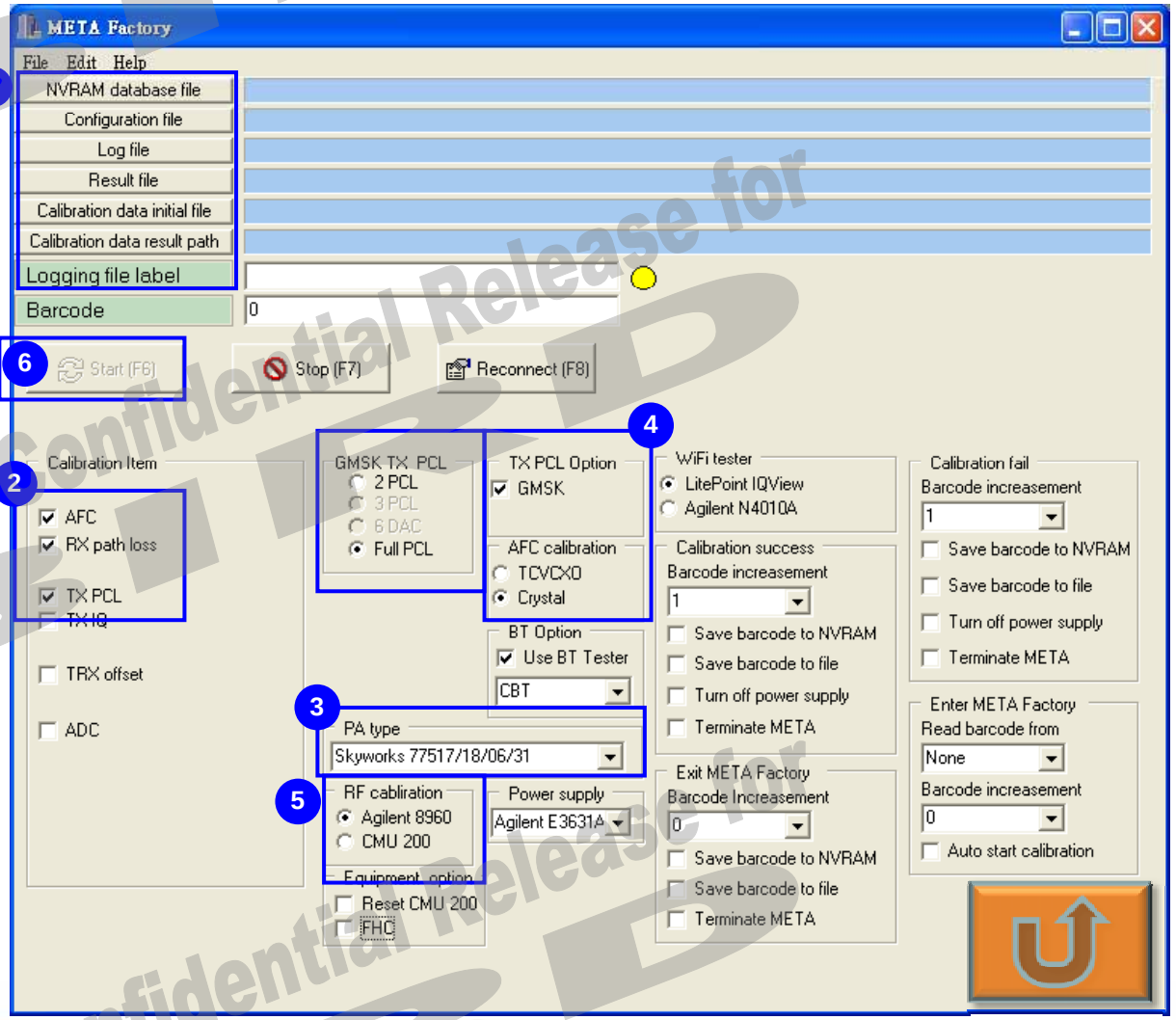
META Tools

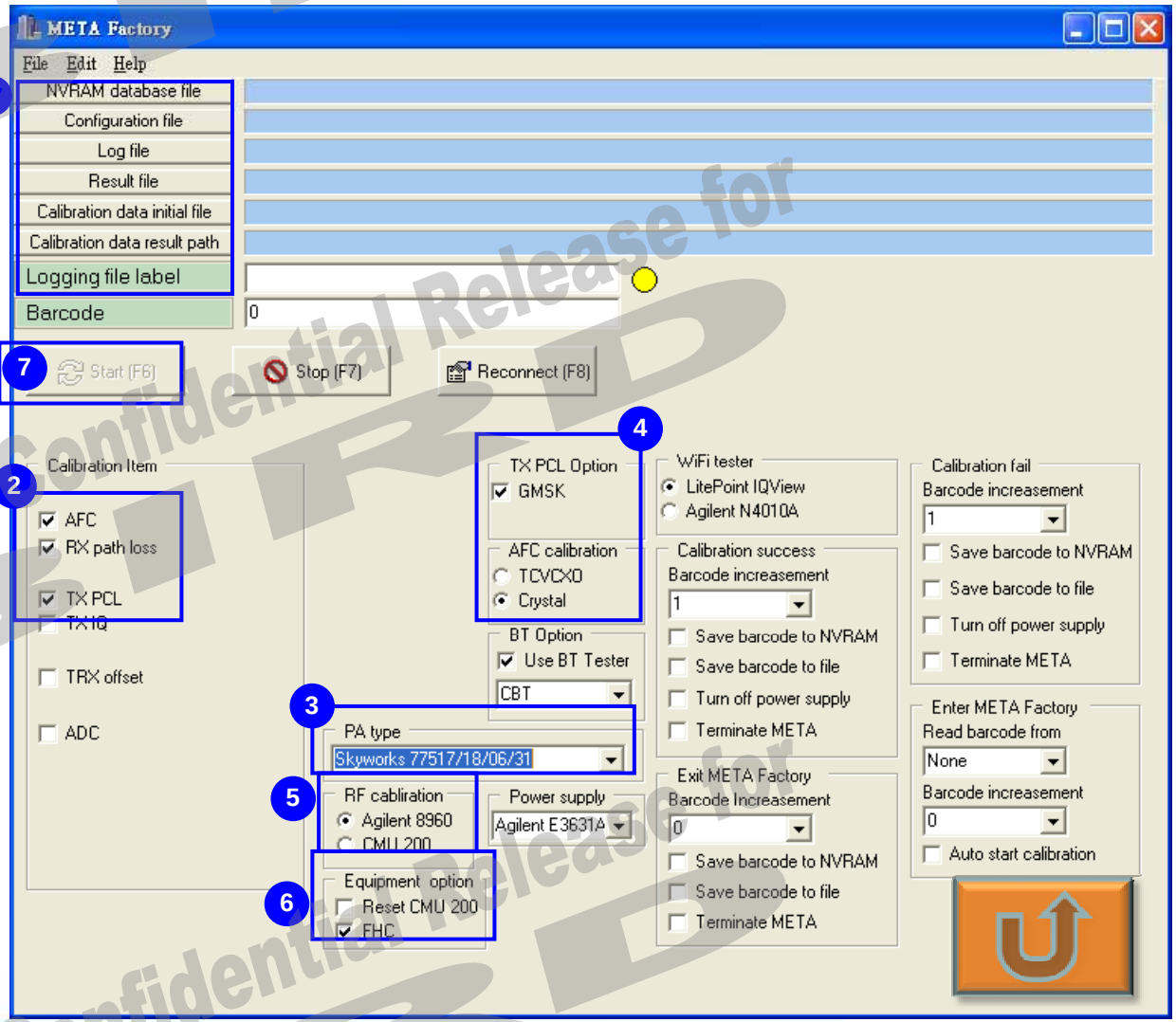
META Factory Calibration UI (Traditional)

1. Setting files :
•NVRAM DB
•CFG file (input file)
•LOG file
•RST file
•INI file (input file)
•CAL file
•Barcode
2. Calibration items :
•AFC
•RX path loss
•TX PCL
3. PA type and PCL :
•Select PA type in the scroll bar
4. Other settings :
•Select GMSK and/or EPSK mode
•AFC type is Crystal
5. Select instrument :
•Select CMU or 8960
•De-select Reset CMU200
6. Start calibration



META Factory Calibration UI (FHC)

1. Setting files :
•NVRAM DB
•CFG file (input file)
•LOG file
•RST file
•INI file (input file)
•CAL file
•Barcode
2. Calibration items :
•AFC
•RX path loss
•TX PCL
3. PA type:
•Select PA type in the scroll bar
4. Other settings :
•Select GMSK and/or EPSK mode
•AFC type is Crystal
5. Select instrument :
•Select CMU or 8960
•De-select Reset CMU200
6. Select FHC
7. Start calibration



Calibration File and Initial Files

Calibration file (traditional calibration)

MT6252.CFG

Initial file (traditional calibration)

MT6252.ini

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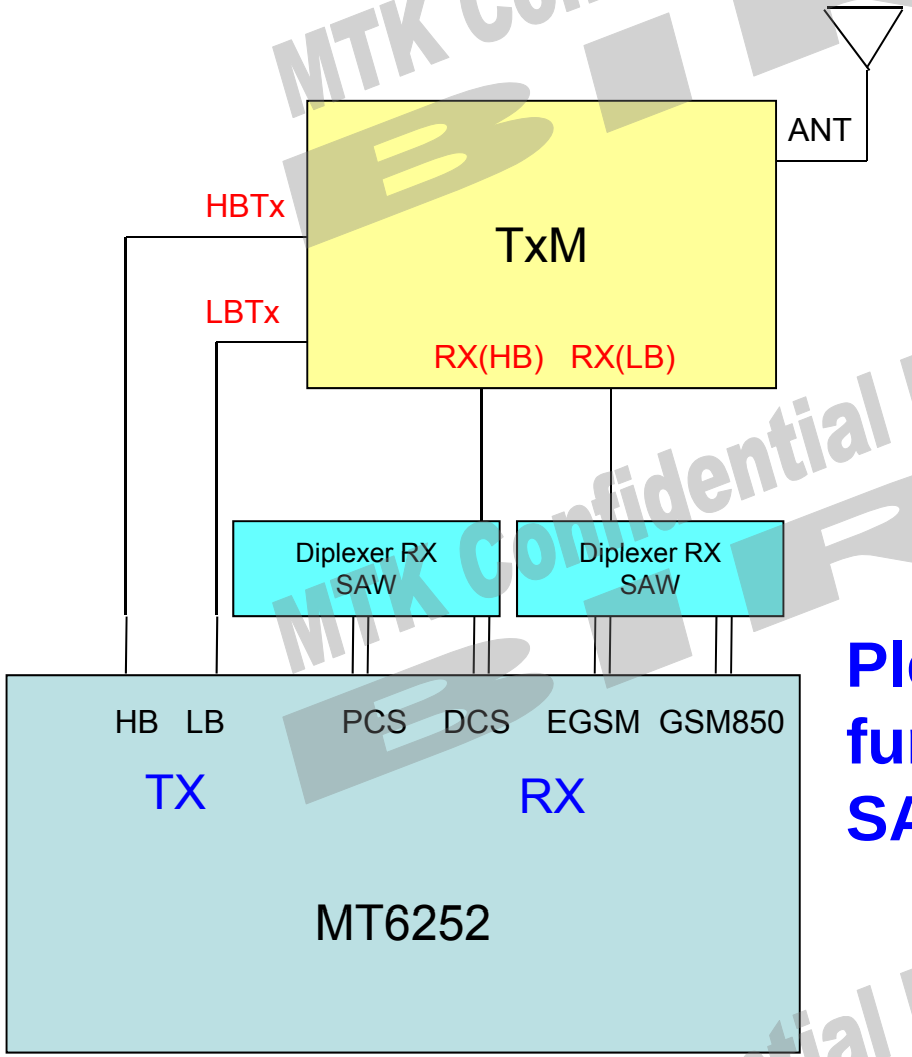
Key RF Components

Key RF Components: Evaluation

- RX SAW
  - Characteristics: Insertion loss/Attenuation
  - System performance: Sensitivity/Blocking test
- TX SAW
  - Characteristics: Insertion loss/Attenuation
  - System performance: Tx output power/Tx noise in Rx band
- ASM (Antenna Switch Module)
  - Characteristics: Insertion loss/Harmonics attenuation/Isolation
  - System performance: under normal and extreme condition
    - RMS and peak phase error/Frequency error/ORFS/Switching transient
    - Sensitivity
    - Spurious emission
- FEM (Front-End Module; ASM with RX SAW)
  - Characteristics: Insertion loss/Attenuation/Isolation
  - System Performance: Under normal and extreme conditions
    - RMS and peak phase error/Frequency error/ORFS/Switching transient
    - Sensitivity/Blocking
    - Spurious emission

PinOut of MT6252 (Same as MT6253)



PCB Layout Sketch

Please turn on SWAP function for diplexer SAW usage

RX SAWs (MT6252)

•Diplexer SAW (The target is these RF external components should be the same as 6253, but this qualify schedule is TBD)

Vendor	Part Number	Support Bands	Type	Size(mm2)	RF Chip	Qualified
Murata	SAWEN881MCX0F00R14 SAWEN1G84CV0F00R14	850/900 1800/1900	1 in 4 out	1.8x1.4	MT6253	
Fujitsu	FAR-G5KM-942M50-Y4NY FAR-G6KM-1G9600-Y4NZ	850/900 1800/1900	1 in 4 out	1.8x1.4	MT6253	
SAMSUNG	SFWM81DY102 SFWG42MY002	850/900 1800/1900	1 in 4 out	1.8x1.4	MT6253	
EPCOS	No products, checking develop schedule with engineers	850/900 1800/1900	1 in 4 out	1.8x1.4	MT6253	
Hitachi Media	No products, checking develop schedule with engineers	850/900 1800/1900	1 in 4 out	1.8x1.4	MT6253	

TX Modules (MT6252)(Schedule TBD)

PA/TxM Components Qualified for MT6253				
Type	**Vendor**	**Part Number**	**Size (mm^2)**	**Band Supported**
Tx Module	RFMD	RF7170	6.63 x 5.24	Semi-Quad

•Note：The target is these RF external components should be the same as 6253, but this qualify schedule is TBD

Crystal (MT6252) (Schedule TBD)

Qualified Crystal Components					
Vendor	**Part Number**	**Freq. (MHz)**	**CL (pF)**	**Size (mm^2)**	**Status**
TXC	7M26000028	26	7.5	3.2 x 2.5	Approved

- Note: Don't use MT6139/MT6140's, AD6548 Crystal for MT6252.
- Note : The target is these RF external components should be the same as 6253, but this qualify schedule is TBD

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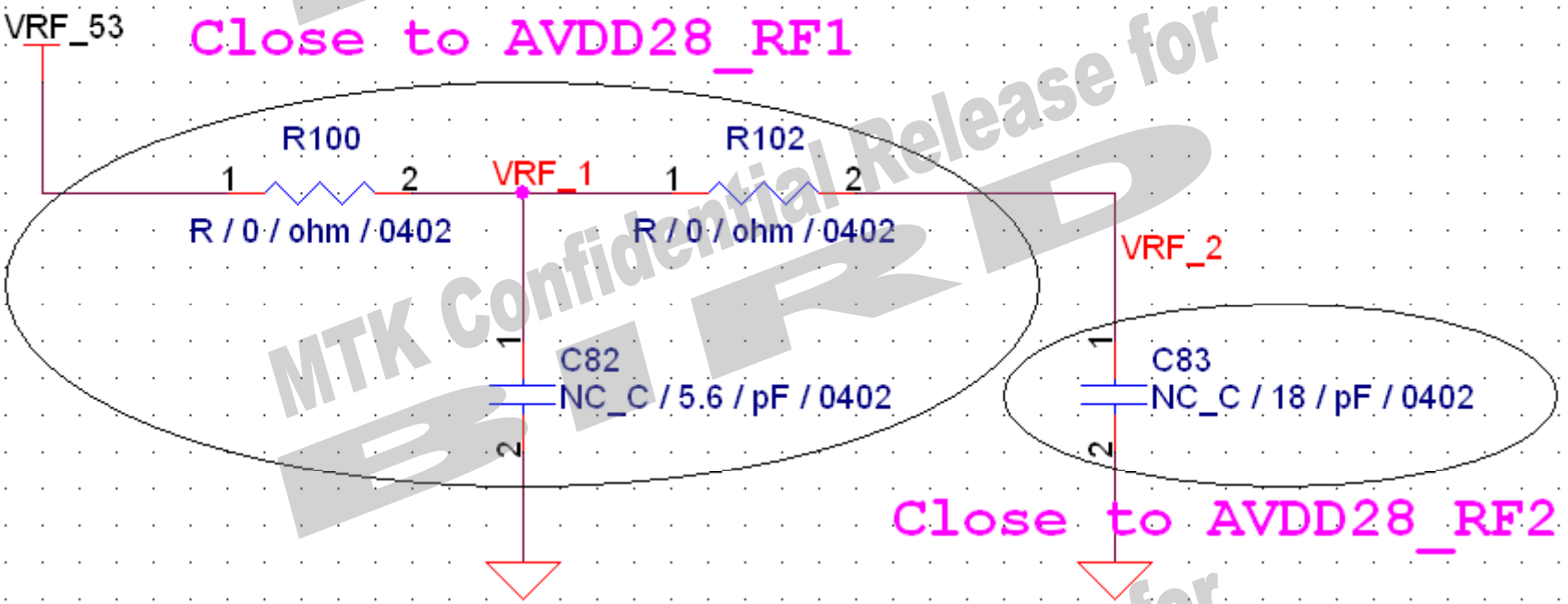
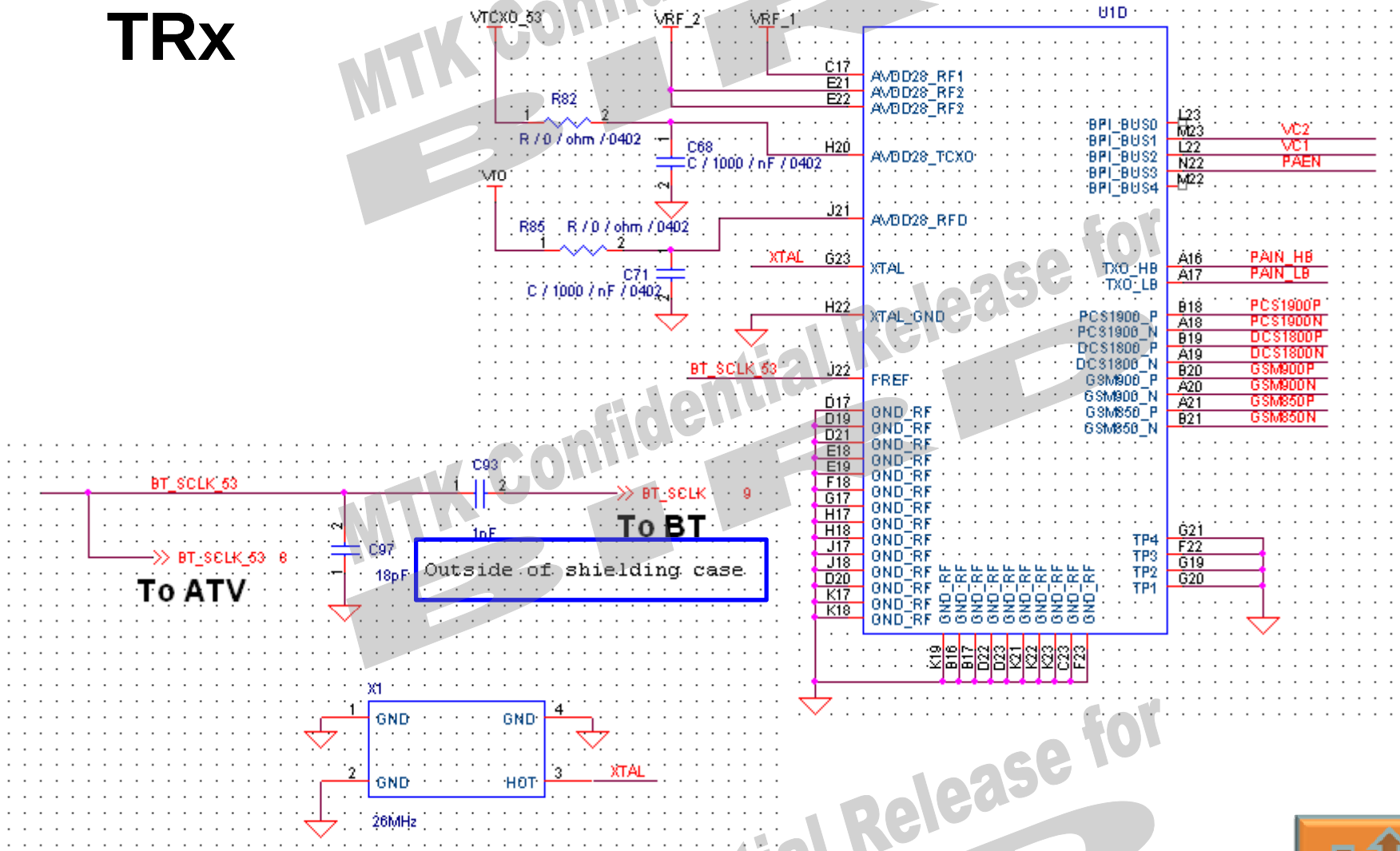
MT6252 Reference Phone

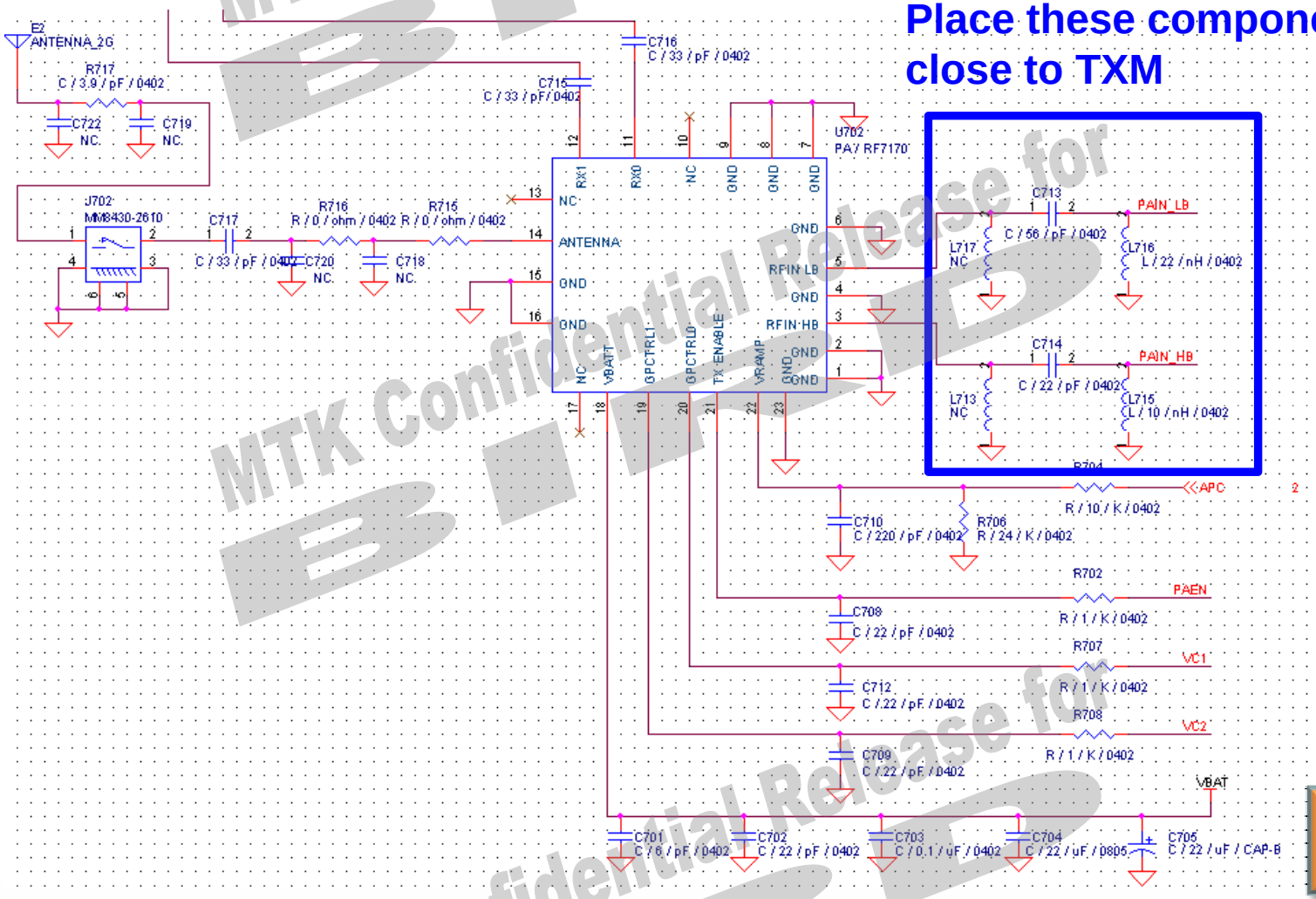
VRF / VRF1 & VRF2



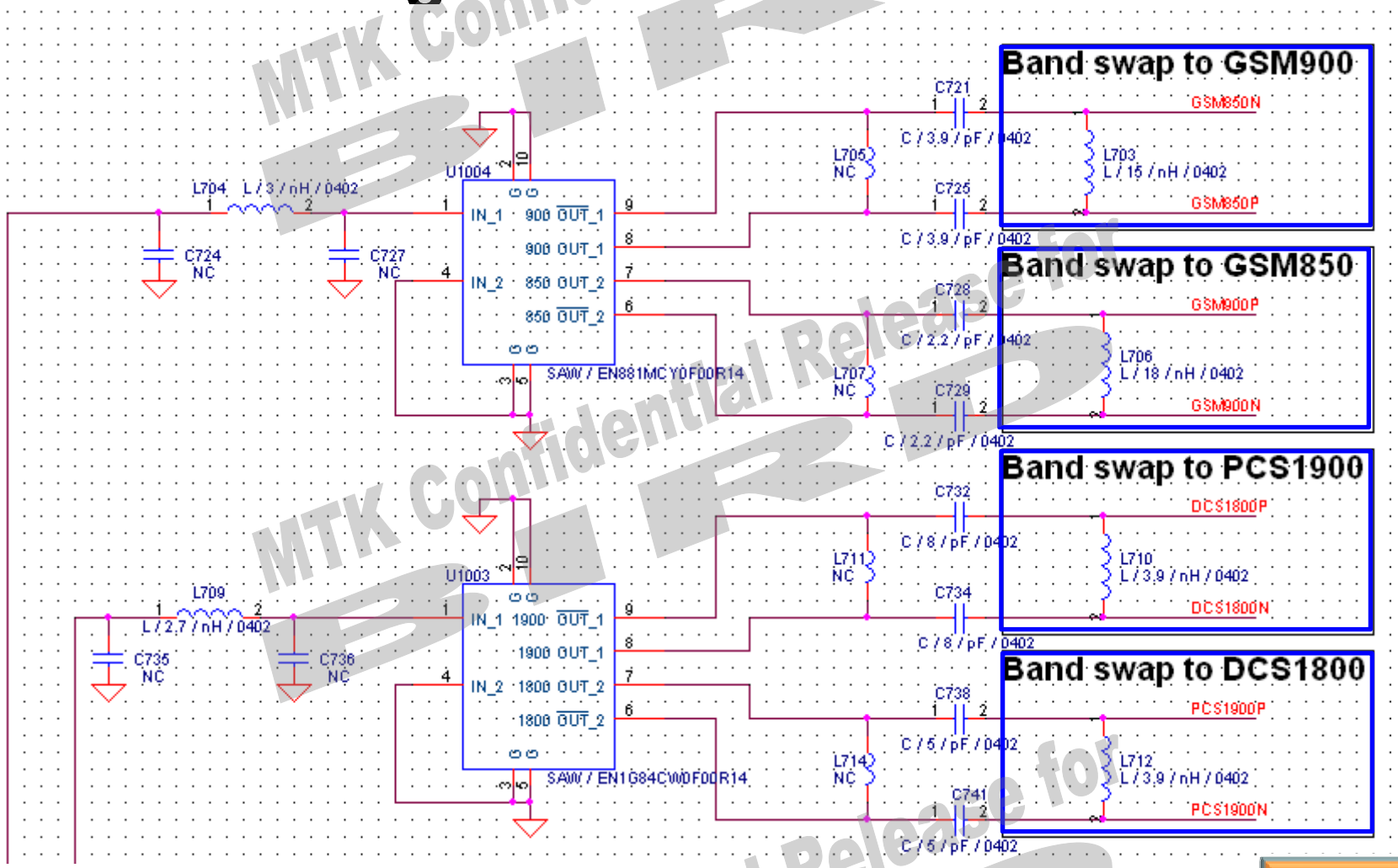
TRx



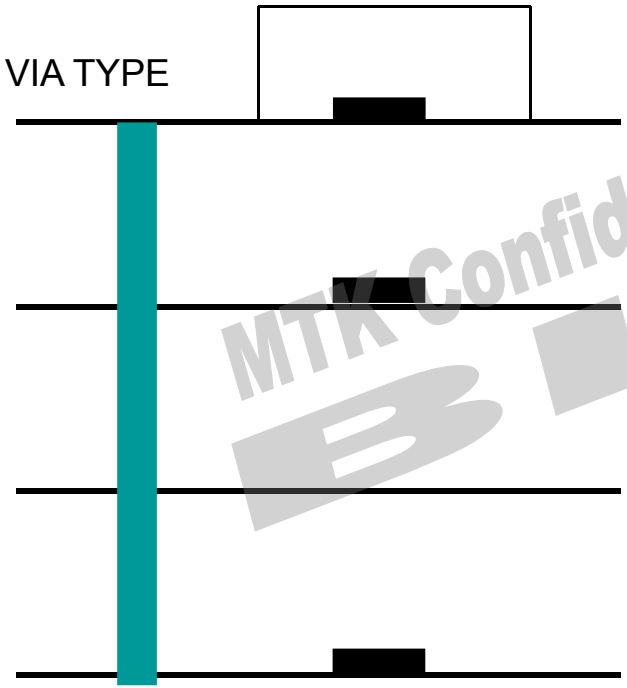
TXM



RX matching



Stack Up (4 Layers)



TOP (L1)

⇒ TOP layer RF trace
(Microstrip line, Ref. GND plane: L2)

L2

⇒ L2 RF trace,
(strip line, Ref. GND plane: L1 or L3)
⇒ control line

L3

⇒ Power line

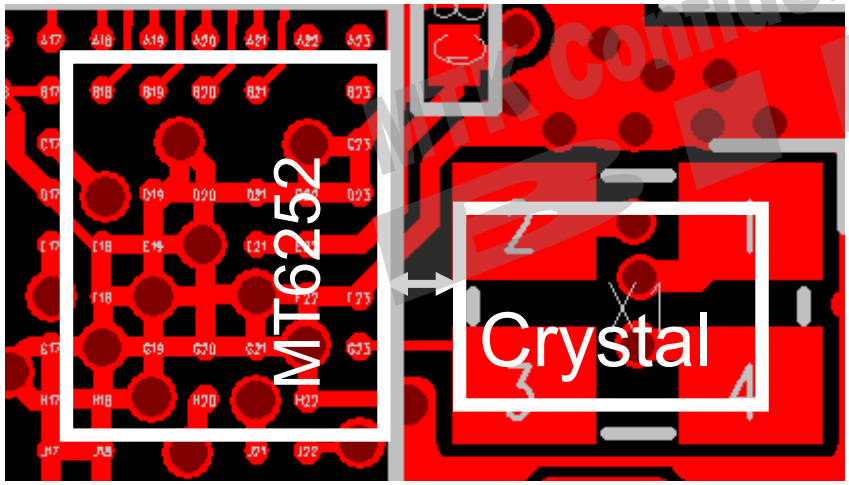
BOTTOM (L4)

⇒ Bottom layer RF trace
(Microstrip line, Ref. GND plane: L3)

Layout Rule

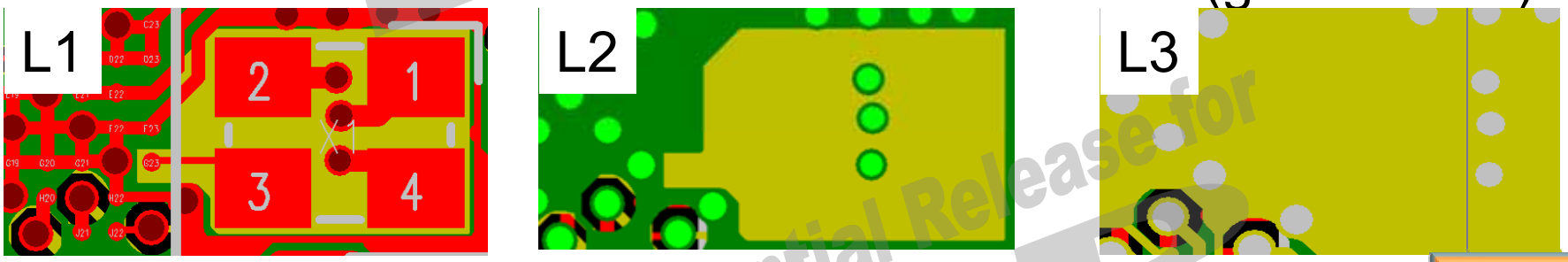
MT6252 PCB RF layout rules		
	Done	Item
1	☐	Crystal place as close as possible to MT6252 PIN XTAL (G23)
2	☐	Crystal and its trace directly refer to global ground , keep out L1&L2 ground
3	☐	Crystal ground pin directly connect to global ground , do not connect to other layer GND
4	☐	PIN XTAL_GND (H22) is directly connected to global ground
5	☐	PIN FREF (J22) should be shielded in inner layer, and its via should keep far away from Pin XTAL(G23) and trace
6	☐	Control signals of ASM or Front-end Module do not cross the antenna port or PA outputs
7	☐	Keep RF trace as 50Ω
8	☐	Keep good differential property of RX differential trace
9	☐	Avoid GND split under MT6252 , especially for L2
10	☐	AVDD28_RF1 (C17) & AVDD28_RF2 (E21&E22) bypass cap. place as close as possible to MT6252
11	☐	GND of AVDD28_RF1 (C17) & AVDD28_RF2 (E21 & E22) decoupling cap is directly connected to global ground
12	☐	Place AVDD28_TCXO (H20) bypass cap. as close as possible to MT6252
13	☐	Place AVDD28_RFD (J21) bypass cap. as close as possible to MT6252
14	☐	For Camera, LCM, and MSDC, the clock and data should have better GND protection. Avoid power trace or other trace routing parallel with clock and data.
15	☐	Place memory as close as possible to MT6252

1. Crystal place as close as possible to MT6252 PIN XTAL (G23)

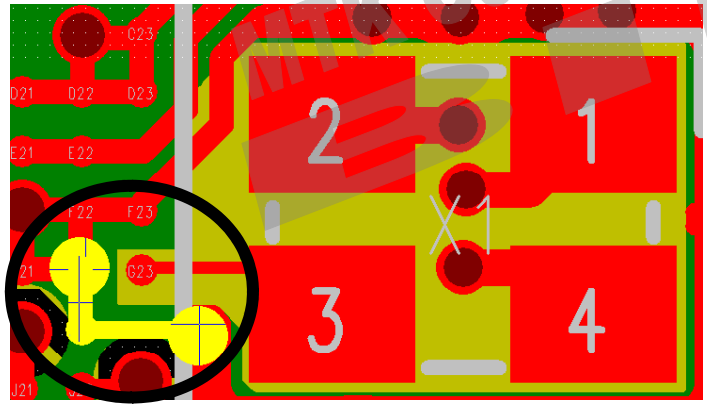


2. Crystal and its trace directly refer to global ground , keep out L1&L2 ground

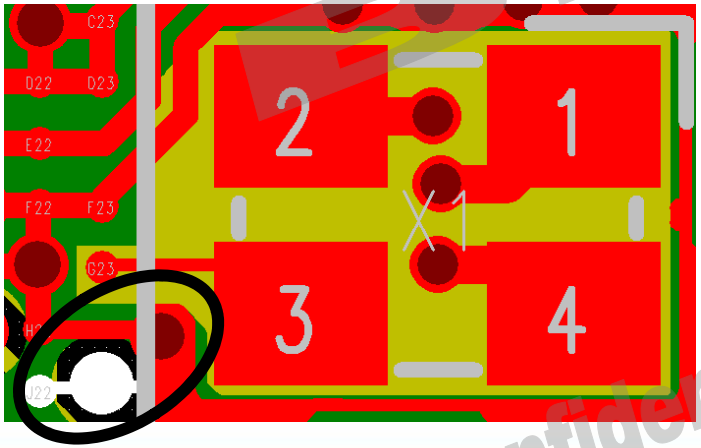
3. Crystal ground pin directly connect to global ground , do not connect to other layer GND



4. PIN XTAL_GND (H22) is directly connected to global ground

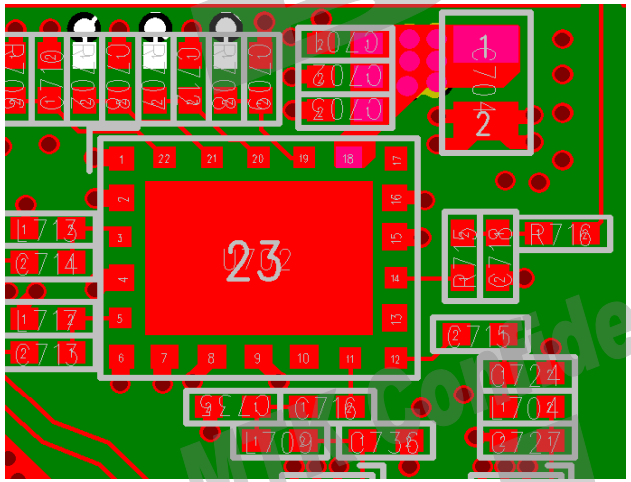


5. PIN FREF (J22) should be shielded in inner layer, and its via should keep far away from Pin XTAL(G23) and trace



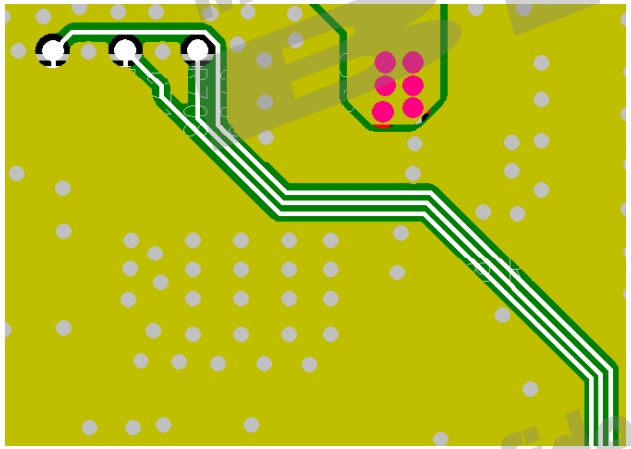
6. Control signals of ASM or Front-end Module do not cross the antenna port or PA outputs

L1



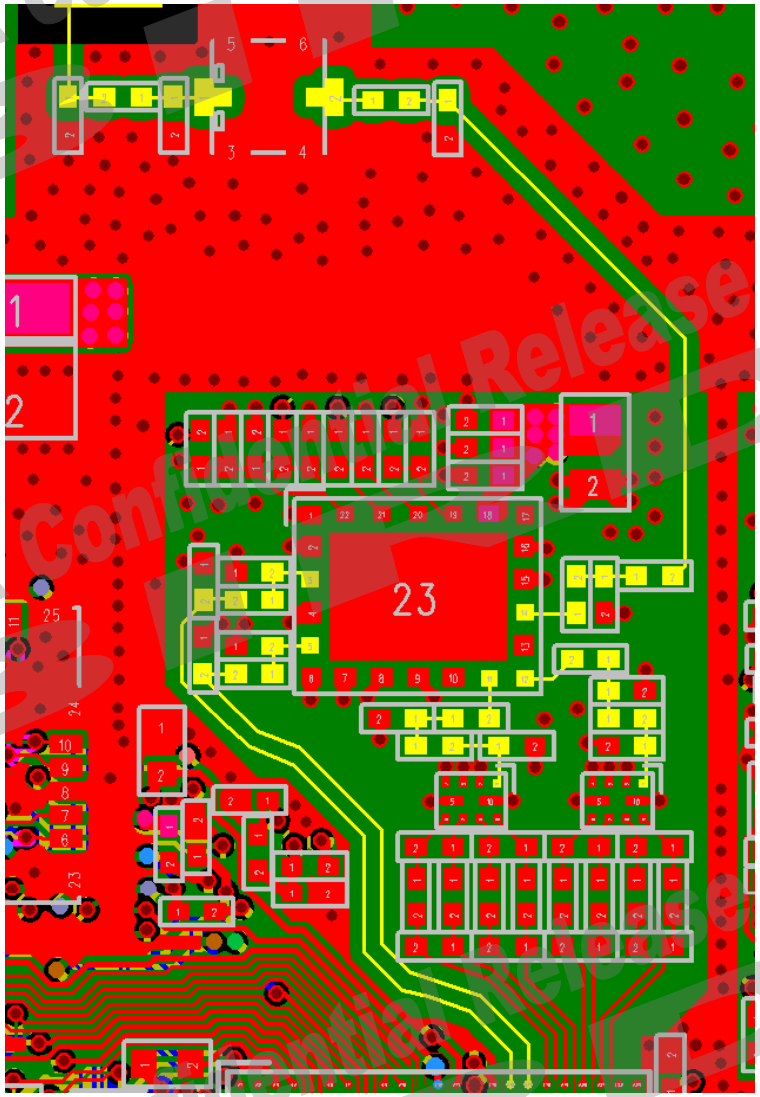
L2

L3

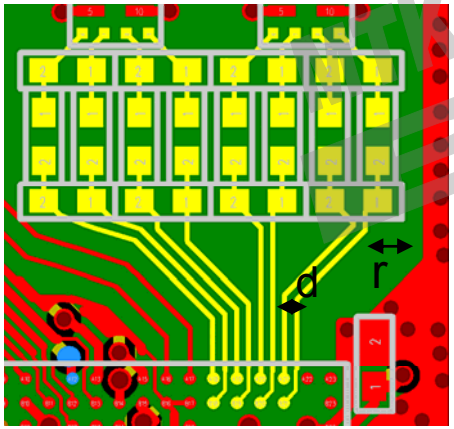


L4

7. Keep RF trace as 50Ω

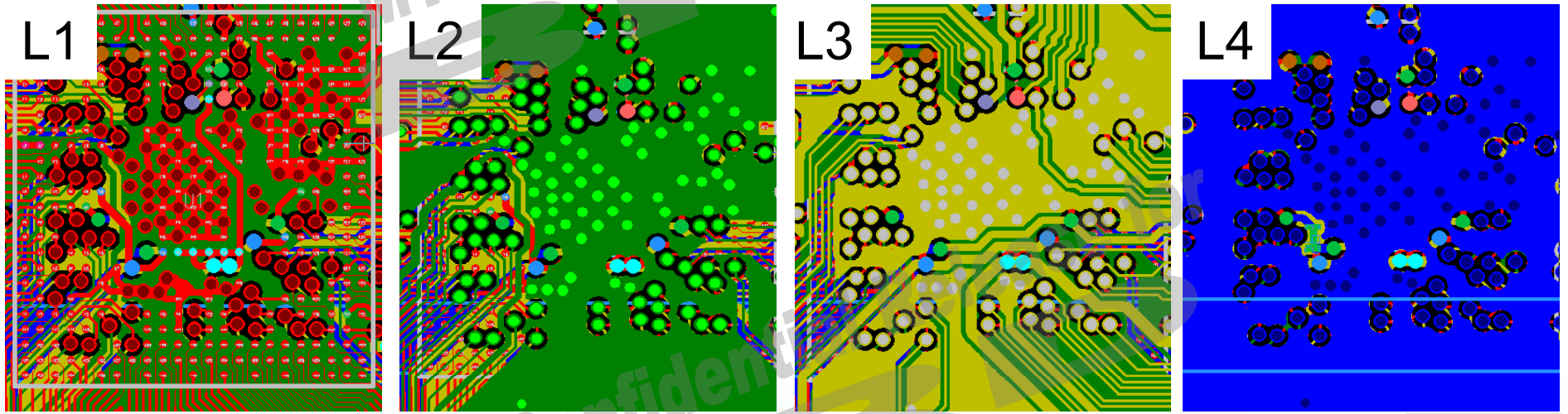


8. Keep good differential property of RX differential trace

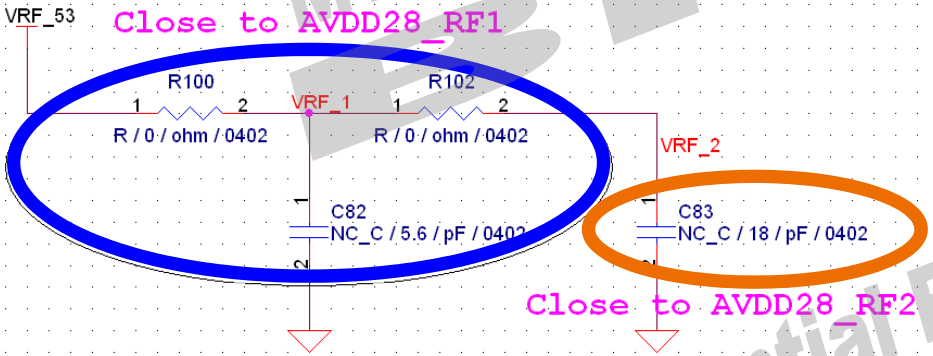


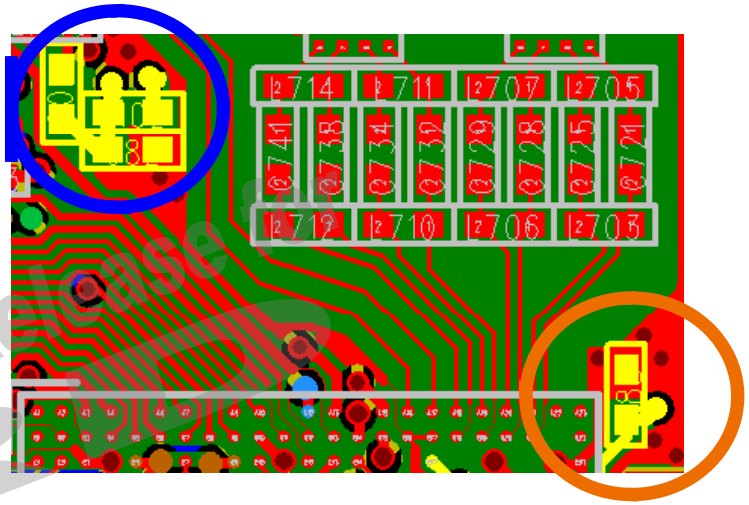
a. Trace length keep the same between the differential pair
b. GND keep at least larger than 4 time of differential pair distance, r>4xd

9. Avoid GND split under MT6252 , especially for L2



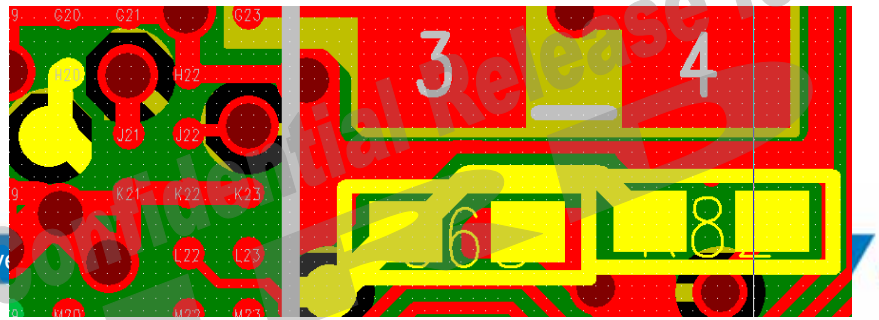
10. AVDD28_RF1 (C17) & AVDD28_RF2 (E21&E22) bypass cap. place as close as possible to MT6252





11. GND of AVDD28_RF1 (C17) & AVDD28_RF2 (E21 & E22) decoupling cap is directly connected to global ground

12. Place AVDD28_TCXO (H20) bypass cap. as close as possible to MT6252



13. Place AVDD28_RFD (J21) bypass cap. as close as possible to MT6252

14. For Camera, LCM, and MSDC, the clock and data should have better GND protection. Avoid power trace or other trace routing parallel with clock and data.

15. Place memory as close as possible to MT6252

MEDIATEK

Modify BPI and Timing for MT6252

Before prepare

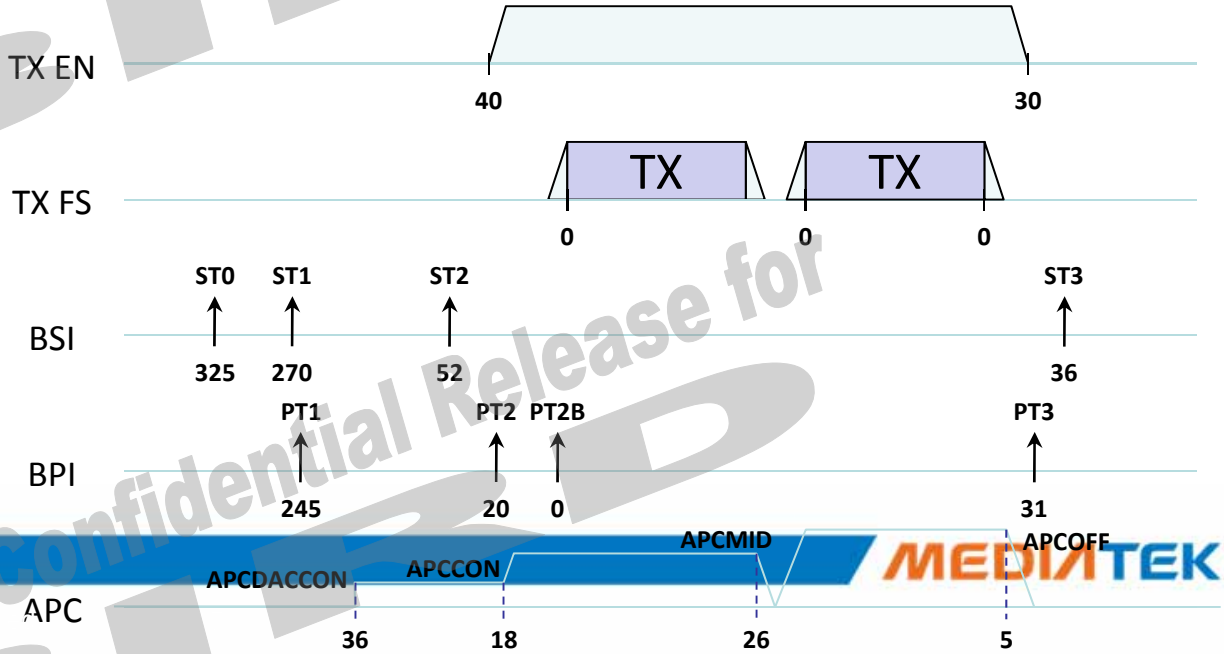
- L1_custom_rf .h file
- PA control logic and schematic of RF module
- Due the BPI amount of MT6252 is less than MT6253, it is necessary to modify “Vlogic” pin to BPI_BUS 1
- Defunded function of BPI

BSI/BPI Event Timing: TX

ST0 (325 Qb) Standby mode	ST1 (280 Qb) Warm-up mode	ST2 (52 Qb) TX mode	ST3 (36 Qb) TX sleep mode
• CW2: Set TRX, band, Nfrc, mode = 010 • CW57: Set AFC value • CW4: optimize performance by band	• CW1: SX N divider	• CW133: Enter TX mode	• CW2: mode=000, TRX=10

PT1 (245 Qb) Dummy	PT2 (20 Qb) Dummy	PT2B (0 Qb) TX mode	PT3 (31 Qb) Return to idle
• Idle	• Idle	• TRSW, Band SW, PA EN	• Idle

- BSI CLK=26MHz
- Send CW2 first in ST0



BSI/BPI Event Timing: RX

SR0 (213 Qb)
Standby mode

- CW2: Set TRX, band, Nfrc, mode = 010
- CW57: Set AFC value

SR1 (148 Qb)
Warm-up mode

- CW1: SX N divider

SR2 (71 Qb)
TX mode

- CW96: RX gain

SR3 (0 Qb)
TX sleep mode

- CW2: mode=000, TRX=10

PR1 (40 Qb)
Dummy

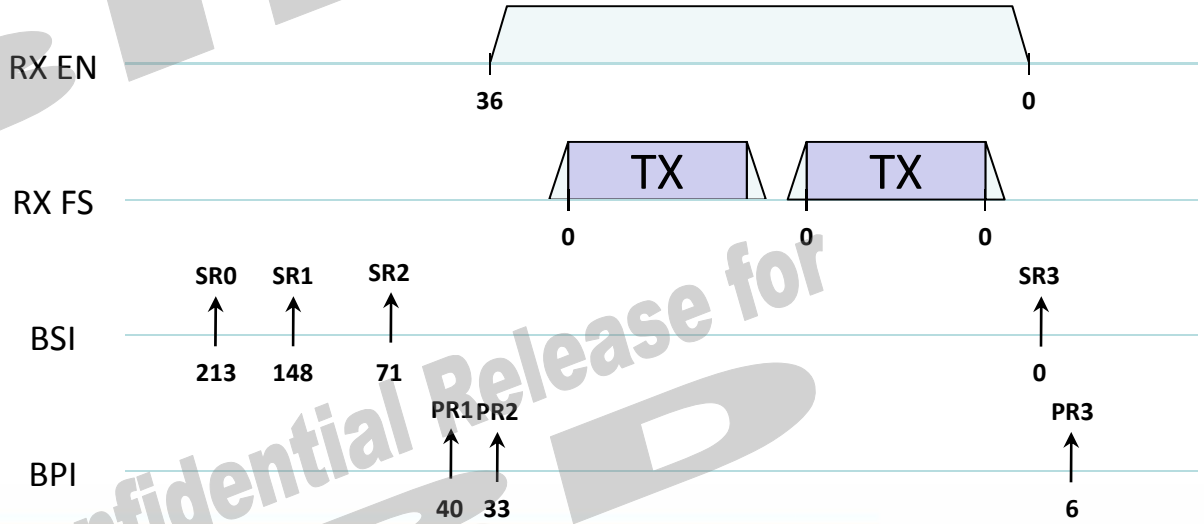
- Idle

PR2 (33 Qb)
Dummy

- TRSW, Band SW, PA EN

PR3 (6 Qb)
Return to idle

- Idle



.h file form


```
#define   QB_SR0
#define   QB_SR1
#define   QB_SR2
#define   QB_SR3
#define   QB_SR2M
#define   QB_PR1
#define   QB_PR2
#define   QB_PR3
#define   QB_ST0
#define   QB_ST1
#define   QB_ST2
#define   QB_ST3
#define   QB_PT1
#define   QB_PT2
#define   QB_PT2B
#define   QB_PT3
#define   QB_APCON
#define   QB_APCMID
#define   QB_APCOFF
#define   QB_APCDACON
#define   TX_PROPAGATION_DELAY
```

Modify Timing

```
213
148
 71
  0
 44
 40
 33
  6
325
280
 52
 36
245
 20
  0
 35
 18
 26
  9
 99
 43
```

```
#define   PDATA_GSM850_PR1
#define   PDATA_GSM850_PR2
#define   PDATA_GSM850_PR3
#define   PDATA_GSM850_PT1
#define   PDATA_GSM850_PT2
#define   PDATA_GSM850_PT2B
#define   PDATA_GSM850_PT3
#define   PDATA_GSM_PR1
#define   PDATA_GSM_PR2
#define   PDATA_GSM_PR3
#define   PDATA_GSM_PT1
#define   PDATA_GSM_PT2
#define   PDATA_GSM_PT2B
#define   PDATA_GSM_PT3
#define   PDATA_DCS_PR1
#define   PDATA_DCS_PR2
#define   PDATA_DCS_PR3
#define   PDATA_DCS_PT1
#define   PDATA_DCS_PT2
#define   PDATA_DCS_PT2B
#define   PDATA_DCS_PT3
#define   PDATA_PCS_PR1
#define   PDATA_PCS_PR2
#define   PDATA_PCS_PR3
#define   PDATA_PCS_PT1
#define   PDATA_PCS_PT2
#define   PDATA_PCS_PT2B
#define   PDATA_PCS_PT3
```

Modify BPI

```
PDATA_IDLE
0x2
PDATA_IDLE
PDATA_IDLE
PDATA_IDLE
0x12
PDATA_IDLE
PDATA_IDLE
0x2
PDATA_IDLE
PDATA_IDLE
PDATA_IDLE
0x12
PDATA_IDLE
PDATA_IDLE
0x3
PDATA_IDLE
PDATA_IDLE
PDATA_IDLE
0x13
PDATA_IDLE
PDATA_IDLE
0x3
PDATA_IDLE
PDATA_IDLE
PDATA_IDLE
0x13
PDATA_IDLE
```

Timing

For MT6252		For MT6253	
QB_SR0	213		
QB_SR1	148	QB_SR1	213
QB_SR2	71	QB_SR2	71
QB_SR3	0	QB_SR3	0
QB_SR2M	44	QB_SR2M	44
QB_PR1	245	QB_PR1	245
QB_PR2	33	QB_PR2	33
QB_PR3	6	QB_PR3	6
QB_ST0	325		
QB_ST1	280	QB_ST1	213
QB_ST2	52	QB_ST2	110
QB_ST3	36	QB_ST3	23
QB_PT1	245	QB_PT1	245
QB_PT2	20	QB_PT2	20
QB_PT2B	5	QB_PT2B	5
QB_PT3	35	QB_PT3	29
QB_APCON	18	QB_APCON	18
QB_APCMID	26	QB_APCMID	26
QB_APCOFF	9	QB_APCOFF	9
QB_APCDACON	99	QB_APCDACON	99
TX_PROPAGATION_DELAY	43	TX_PROPAGATION_DELAY	43

*The difference between APC off and PT3 is 26QB

BPI

For MT6252

```
PDATA_GSM850_PR1        PDATA_IDLE
PDATA_GSM850_PR2        0x2
PDATA_GSM850_PR3        PDATA_IDLE
PDATA_GSM850_PT1        PDATA_IDLE
PDATA_GSM850_PT2        PDATA_IDLE
PDATA_GSM850_PT2B       0x12
PDATA_GSM850_PT3        PDATA_IDLE
PDATA_GSM_PR1           PDATA_IDLE
PDATA_GSM_PR2           0x2
PDATA_GSM_PR3           PDATA_IDLE
PDATA_GSM_PT1           PDATA_IDLE
PDATA_GSM_PT2           PDATA_IDLE
PDATA_GSM_PT2B          0x12
PDATA_GSM_PT3           PDATA_IDLE
PDATA_DCS_PR1           PDATA_IDLE
PDATA_DCS_PR2           0x3
PDATA_DCS_PR3           PDATA_IDLE
PDATA_DCS_PT1           PDATA_IDLE
PDATA_DCS_PT2           PDATA_IDLE
PDATA_DCS_PT2B          0x13
PDATA_DCS_PT3           PDATA_IDLE
PDATA_PCS_PR1           PDATA_IDLE
PDATA_PCS_PR2           0x3
PDATA_PCS_PR3           PDATA_IDLE
PDATA_PCS_PT1           PDATA_IDLE
PDATA_PCS_PT2           PDATA_IDLE
PDATA_PCS_PT2B          0x13
PDATA_PCS_PT3           PDATA_IDLE
```

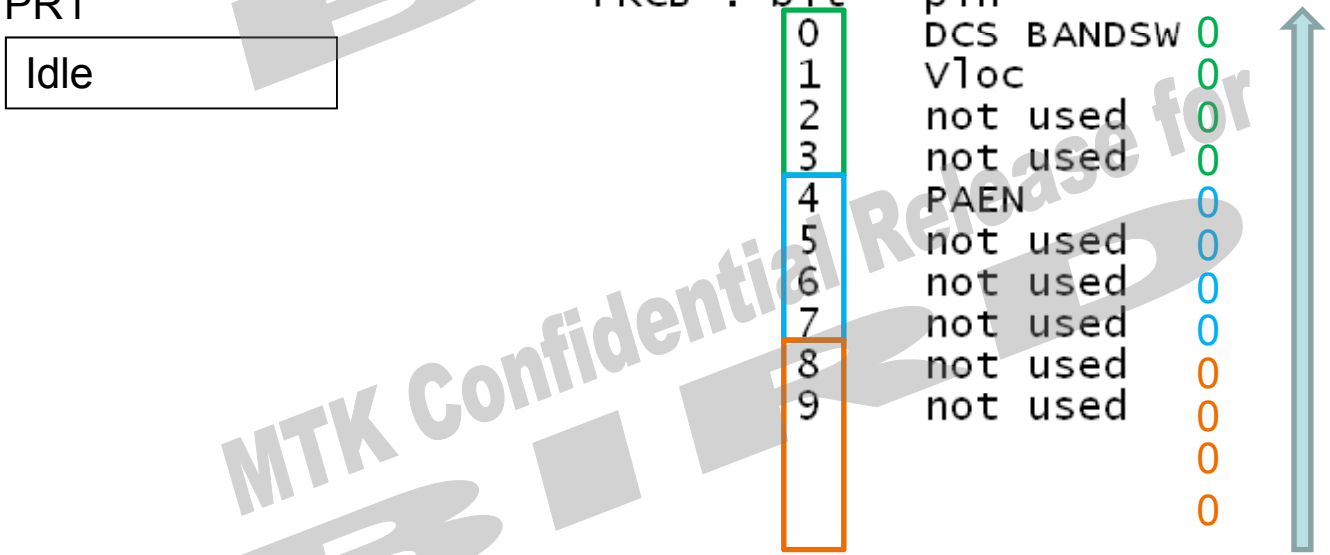
For MT6253

```
PDATA_GSM850_PR1        ( 0x000
PDATA_GSM850_PR2        ( 0x002
PDATA_GSM850_PR3        ( 0x000
PDATA_GSM850_PT1        ( 0x000
PDATA_GSM850_PT2        ( 0x002
PDATA_GSM850_PT2B       ( 0x012
PDATA_GSM850_PT3        ( 0x000
PDATA_GSM_PR1           ( 0x000
PDATA_GSM_PR2           ( 0x002
PDATA_GSM_PR3           ( 0x000
PDATA_GSM_PT1           ( 0x000
PDATA_GSM_PT2           ( 0x002
PDATA_GSM_PT2B          ( 0x012
PDATA_GSM_PT3           ( 0x000
PDATA_DCS_PR1           ( 0x000
PDATA_DCS_PR2           ( 0x003
PDATA_DCS_PR3           ( 0x000
PDATA_DCS_PT1           ( 0x000
PDATA_DCS_PT2           ( 0x003
PDATA_DCS_PT2B          ( 0x013
PDATA_DCS_PT3           ( 0x000
PDATA_PCS_PR1           ( 0x000
PDATA_PCS_PR2           ( 0x003
PDATA_PCS_PR3           ( 0x000
PDATA_PCS_PT1           ( 0x000
PDATA_PCS_PT2           ( 0x003
PDATA_PCS_PT2B          ( 0x013
PDATA_PCS_PT3           ( 0x000
PDATA_INIT                0x000
PDATA_IDLE                0x000
```

Example for GSM_PR1

PR1

Idle



Binary: 0000 0000 0000 → Hexadecimal: 000

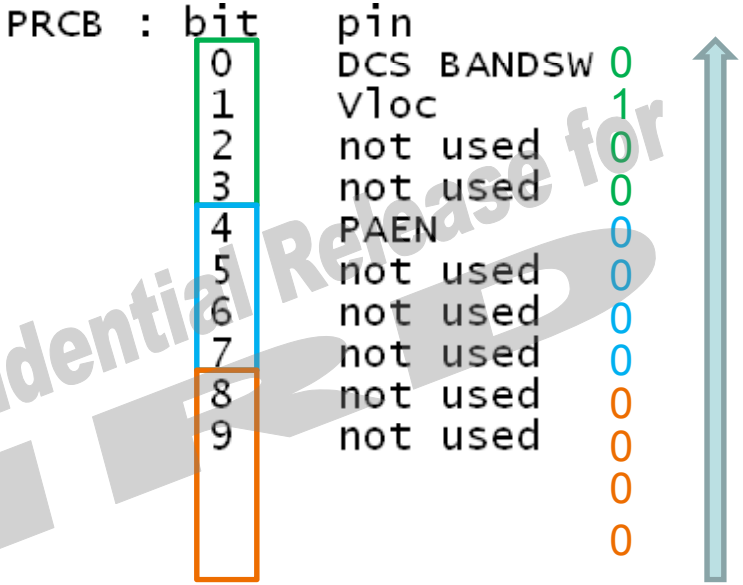
Transform

PDATA_GSM_PR1 PDATA_IDLE

Example for GSM_PR2

PR2

TRSW, Band SW



Binary: 0000 0000 0010 → Hexadecimal: 2

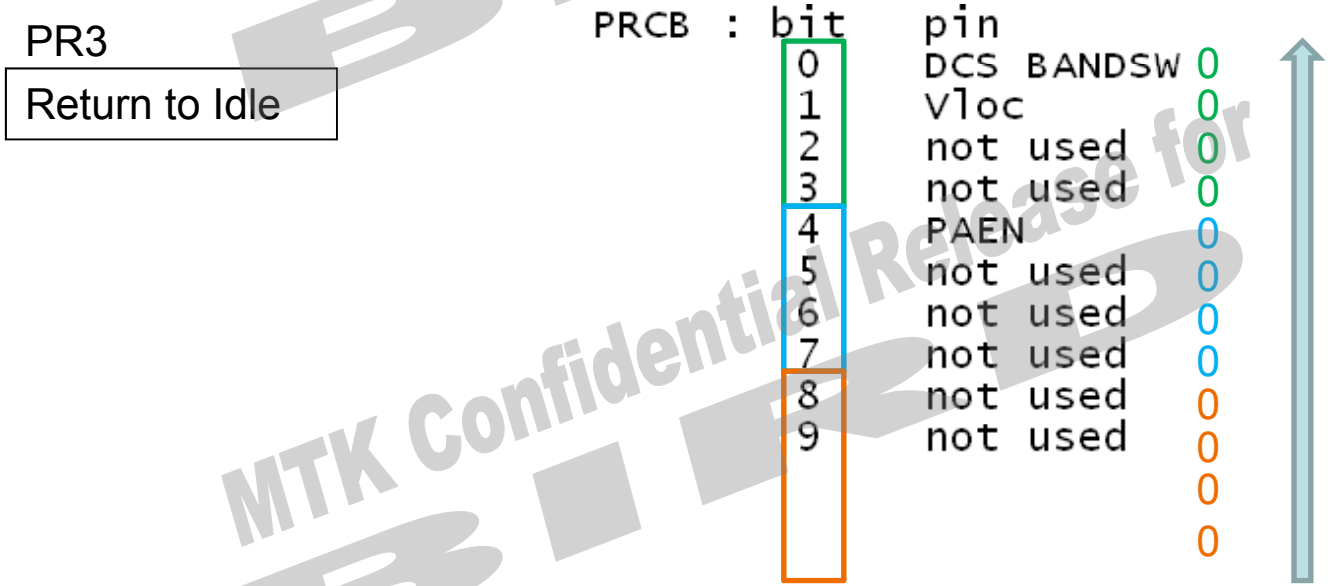
Transform

PDATA_GSM_PR2 0x2

Example for GSM_PR3

PR3

Return to Idle



Binary: 0000 0000 0000 → Hexadecimal: 000

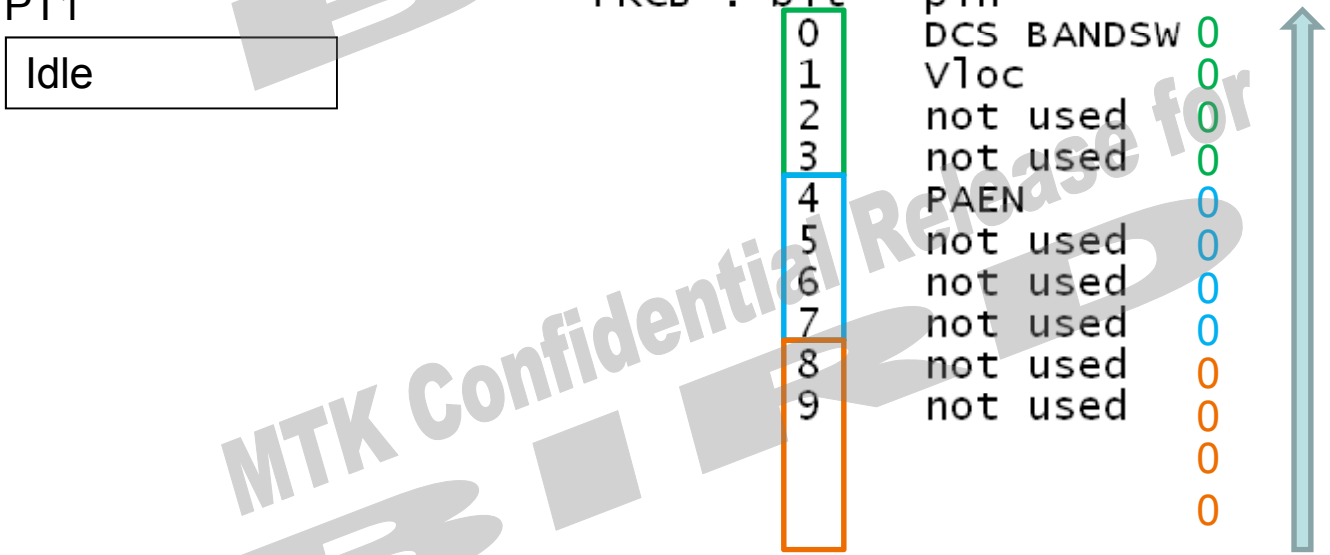
Transform

PDATA_GSM_PR3 PDATA_IDLE

Example for GSM_PT1

PT1

Idle



Binary: 0000 0000 0000 → Hexadecimal: 000

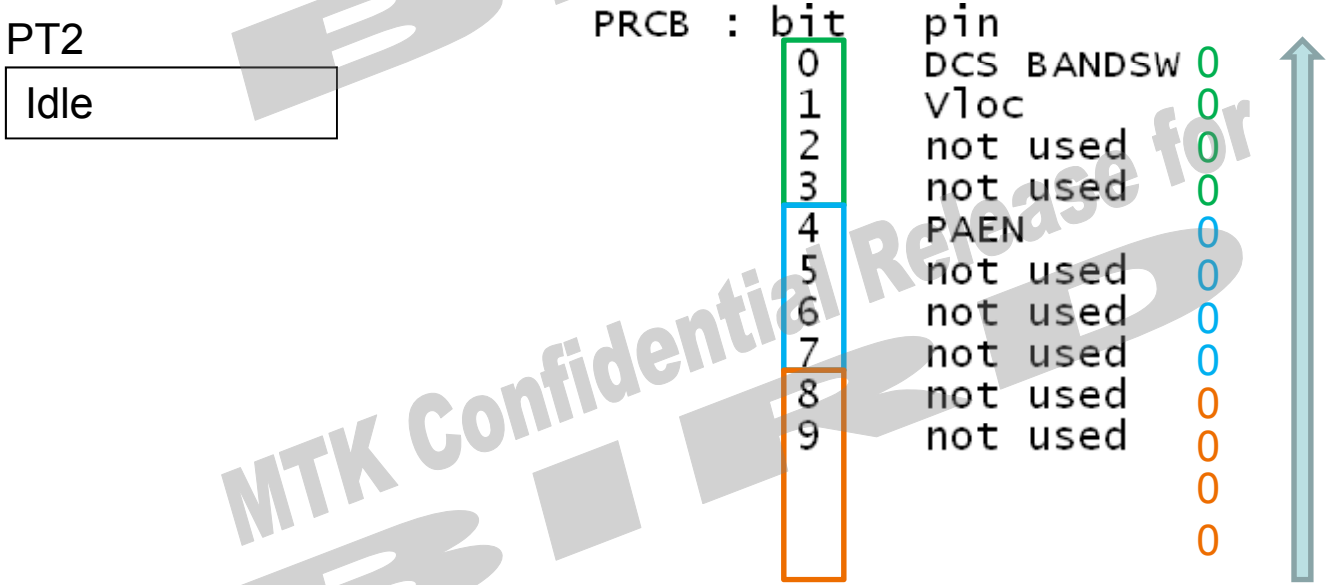
Transform

PDATA_GSM_PT1 PDATA_IDLE

Example for GSM_PT2

PT2

Idle



Binary: 0000 0000 0000 → Hexadecimal: 000

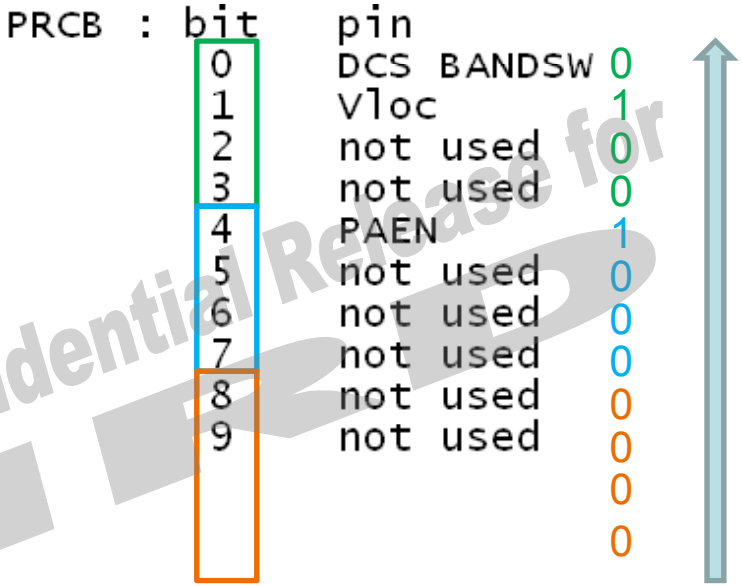
Transform

PDATA_GSM_PT2 PDATA_IDLE

Example for GSM_PT2B

PT2B

TRSW
BANDSW_DCS
PAEN on



Binary: 0000 0001 0010 → Hexadecimal: 12

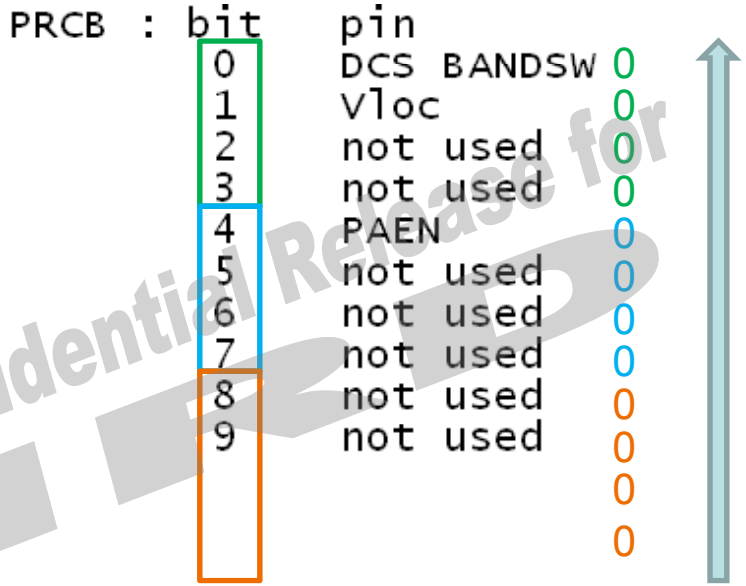
Transform

PDATA_GSM_PT2B 0x12

Example for GSM_PT3

PT3

Return to Idle



Binary: 0000 0000 0000 → Hexadecimal: 000

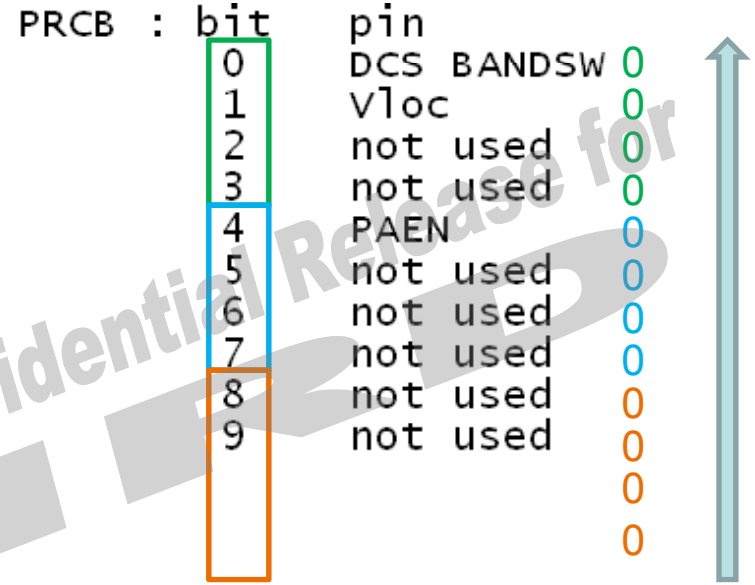
Transform

PDATA_GSM_PT3 PDATA_IDLE

Example for DCS_PR1

PR1

Idle



Binary: 0000 0000 0000 → Hexadecimal: 000

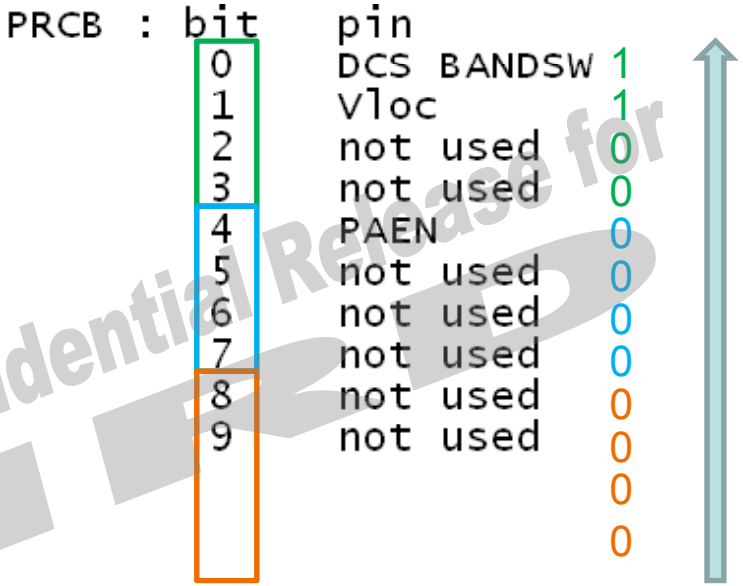
Transform

PDATA_DCS_PR1 PDATA_IDLE

Example for DCS_PR2

PR2

TRSW, Band SW



Binary: 0000 0000 0011 → Hexadecimal: 3

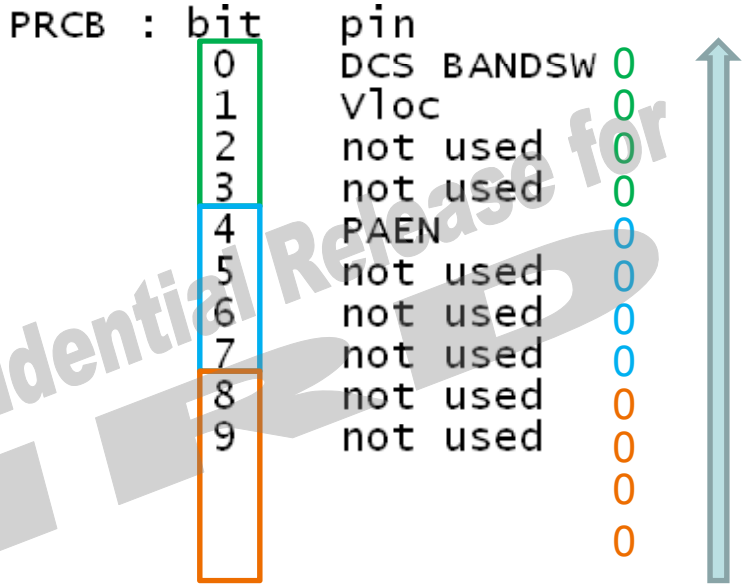
Transform

PDATA_DCS_PR2 0x3

Example for DCS_PR3

PR3

Return to Idle



Binary: 0000 0000 0000 → Hexadecimal: 000

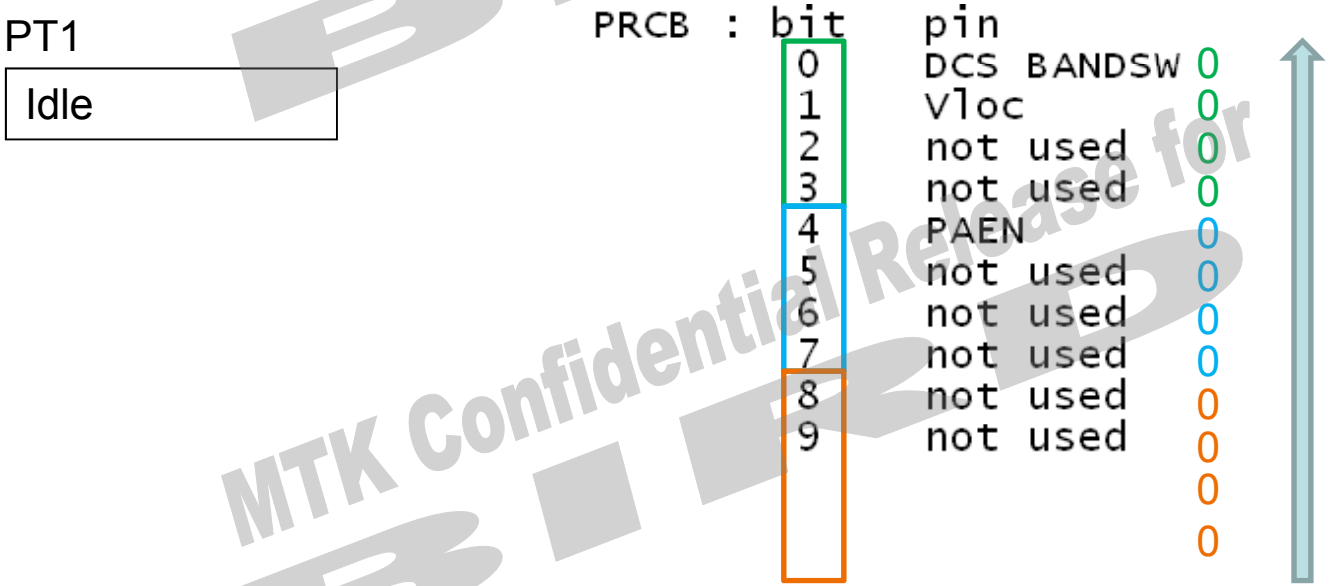
Transform

PDATA_DCS_PR3 PDATA_IDLE

Example for DCS_PT1

PT1

Idle



Binary: 0010 0000 0000 → Hexadecimal: 000

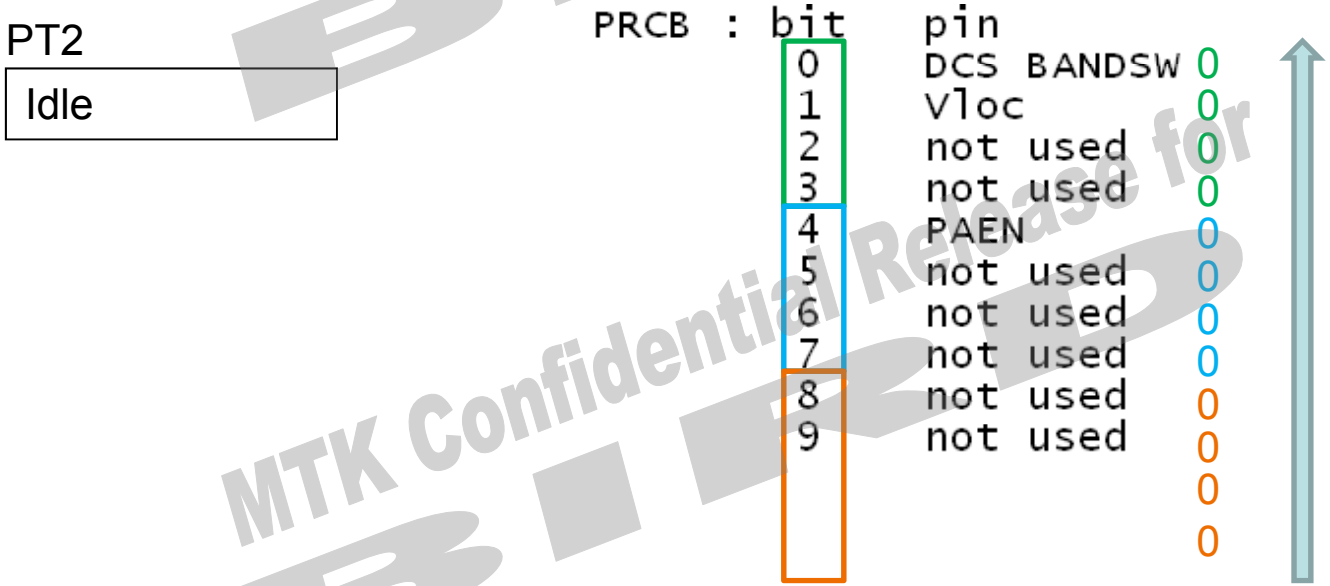
Transform

PDATA_DCS_PT1 PDATA_IDLE

Example for DCS_PT2

PT2

Idle



Binary: 0000 0000 0000 → Hexadecimal: 000

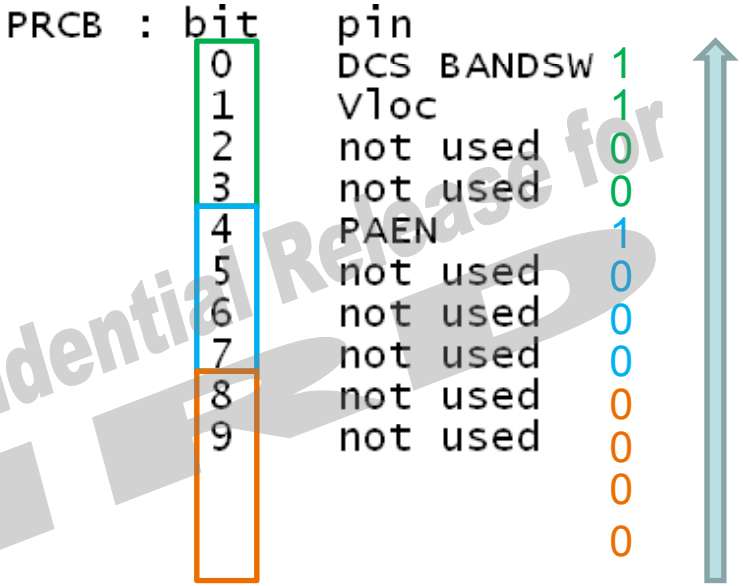
Transform

PDATA_DCS_PT2 PDATA_IDLE

Example for DCS_PT2B

PT2B

TRSW
BANDSW_DCS
PAEN on



Binary: 0000 0001 0011 → Hexadecimal: 13

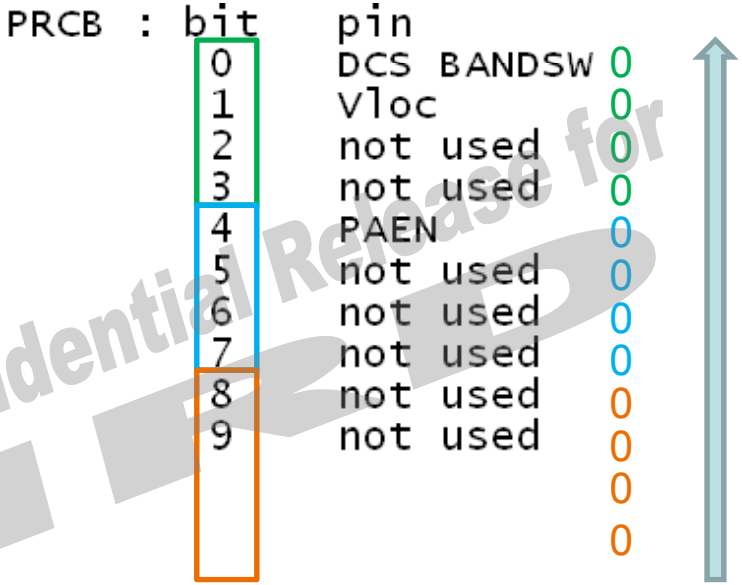
Transform

PDATA_DCS_PT2B 0x13

Example for DCS_PT3

PT3

Return to Idle



Binary: 0000 0000 0000 → Hexadecimal: 000

Transform

PDATA_DCS_PT3 PDATA_IDLE

Summery

- Timing
  - The unit of timing is QB
  - The difference between APC off and PT3 is 26QB
  - Due the transceiver architecture deference, SR timing have to be modified.

- BPI
  - BPI is expressed by hexadecimal, but edited by binary

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