18 DUSART: Infra-Red Interface

The IFR module is a configurable CODEC designed for the transmission and reception of infra-red data frames. Input signals should be demodulated externally before being supplied to the device for decoding. The IFR transmit data output signal may be provided both modulated and unmodulated. For a modulated output signal, the IFR transmit data output controls the PWM2 timer, and the output from this timer is the modulated data output. For an unmodulated output signal, the normal IFR transmit data output is used.

The module is designed to be flexible, supporting current consumer protocols (RC-5, ASK, PPM) and potentially future infra-red protocols via a programmable register interface. Some support is also provided for low-rate IrDA. For specific details of these interfaces and the related terminology used in this section, refer to the relevant standards documents.

It should be emphasised that while this module provides programmable operations and parameters for infra-red link operation via a register interface, it is the application software which implements a given protocol.

18.1 Overview

An outline structure of the IFR controller module is shown in below. The IFR function is part of the Dual USART. Either USART may be configured for use with the IFR, depending upon port availability. Data and control flow between the IFR and other DUSART modules is shown.

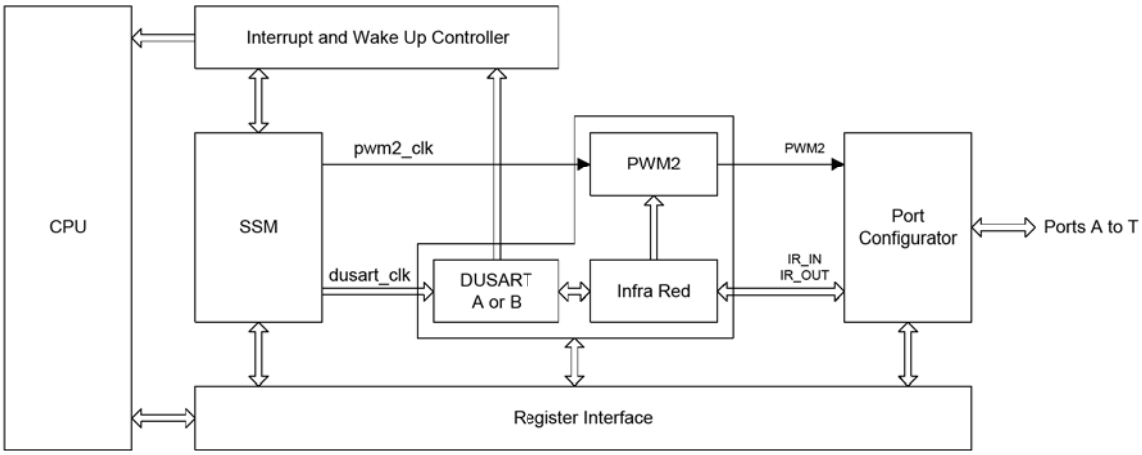


Figure 36: DUSART configuration for Infra-Red Interface

18.2 Initialisation

Initialisation of the Infra Red interface is achieved using the relevant DUSART clock and reset signals, see the DUSART and SSM sections.

18.3 Operation

The operation of the IFR module is controlled by a finite state machine. The state machine responds to processor controls and commands to generate and receive frames of 'consumer infra-red' or IrDA format data. To allow as much flexibility as possible, no specific infra-red format is defined as part of the IFR module. Instead, a generic frame format is defined as a template which may be adapted to many of the most popular infra-red frame types.

The state machine provides the generic frame sequence in the form of one or more lead-in periods, several bit periods of data, one or more lead-out periods and a handover period before the start of the next frame.

Figure 37 below shows an example structure of the 'generic' frame. Each period or data bit is represented by a number of symbols (samples) A of polarity pol_A, followed by a number of symbols B of polarity pol_B. The descriptions of the bit fields in the IFR module registers later in this chapter refer to this generic frame format.

The state machine preloads the IFR counters with the number of symbols in each period, and monitors signals from the datapath during transmit and receive. After the lead-out phase is complete, the FSM waits until the IFR counter module signals that the frame counter has reached zero before returning to the idle state, ready for another frame to be transmitted or received. Any signal activity during this time is lost.

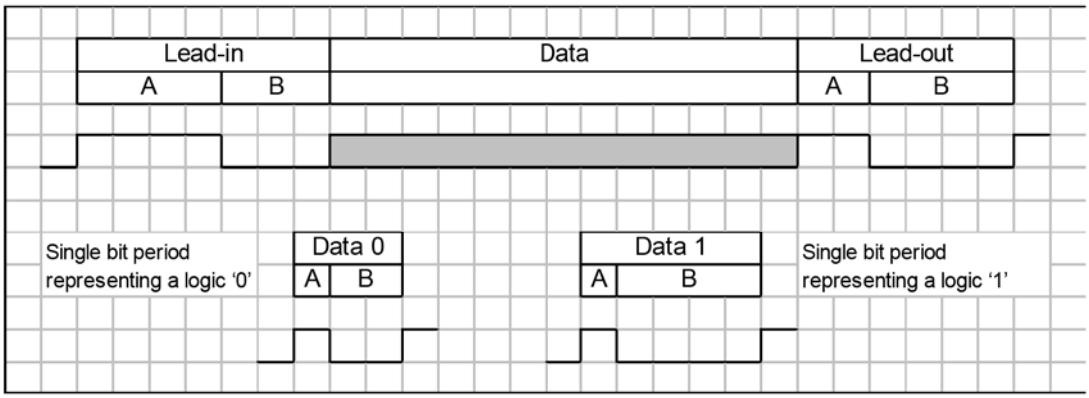


Figure 37: Generic IFR frame format

To begin a frame transfer, initialise all the IFR related configuration registers, and then write to the ***dusart.ir_ctrl*** register. The ***ifr_en*** bit must first be set. If this bit is ever cleared, the IFR control state machine returns to the idle state. At the same time, the ***mode*** bit is set or cleared to indicate the data direction. Finally (and in a separate register write cycle), write a '1' to the ***start_frame*** bit. This triggers the beginning of the lead-in phase (or the scan for lead-in start, if in receive mode). The ***start_frame*** control bit is a pulse trigger, so it is not necessary to clear it to zero before the next frame.

18.4 IFR Counters

The IFR module includes 3 counters:

- Frame counter: a 10-bit down counter that counts at the symbol strobe rate and stops at zero. This counter is preloaded with the total number of symbols in the frame, as stored in the ***dusart.ir_len_cfg*** register.
- Symbol counter: a 7-bit down counter that counts at the symbol strobe rate and stops at zero. This counter is loaded with the number of 'symbols per bit' of lead-in, data and lead-out periods. The load values for each of these phases in the generic frame format are stored in the ***dusart.ir_ldin_cfg***, ***dusart.ir_d0_cfg***, ***dusart.ir_d1_cfg*** and ***dusart.ir_ldout_cfg*** registers.
- Sample counter: an 8-bit down counter that counts at the sample strobe rate and stops at zero. This counter is provided as part of the pulse shaping function.

During the lead-in and lead-out periods, a thresholding mechanism may be used. This allows a certain level of tolerance to be applied to the initial lead-in and lead-out pulse widths, and is useful when scanning for the start of the first input frame. As the symbol counter is a down counter, the threshold values held in the ***dusart.ir_thresh_cfg*** register are the counter values *below* which the lead-in 'a' or lead-out 'a' phase is accepted. Once this threshold is reached, the IFR state machine waits for the correct input signal polarity to start the 'b' phase of lead-in or lead-out. Thresholding is disabled when the threshold register values are set to zero. This is the default condition following a reset.

18.5 IFR Datapath

The IFR datapath contains a receiver/detector, a pulse shaper and a selection of polarity multiplexers. It is controlled directly by the IFR control state machine.

18.5.1 Receiver / Detector

The receiver/detector is a 6-bit shift and match register. The incoming data is shifted into the register, preprocessed (masked) and compared with two match registers, one representing logic '1', the other logic '0'. A match indicates that the associated bit value has been detected. The match pattern and mask pattern for logic one and zero are defined in the registers ***dusart.ir_rx_d1_cfg*** and ***dusart.ir_rx_d0_cfg*** respectively. Matching takes place only for those bits in the ***match*** field that correspond to '0' bits in the ***mask*** field. Bits set to '1' in the ***mask*** field are treated as don't care in the ***match*** field. The following example illustrates the detection sequence:

Example: An input data frame represents the bit value '1' by the 3 symbols '100', and the bit value '0' by the 2 symbols '10'. The IFR module configuration registers should be set as follows:

```
// Set match field for data = 1 to 000100b
fd.dusart.ir_rx_d1_cfg.match = 0x04;
// Set mask field for data = 1 to 111000b: match bits 2-0
fd.dusart.ir_rx_d1_cfg.mask = 0x38;

// Set match field for data = 0 to 000100b
fd.dusart.ir_rx_d0_cfg.match = 0x04;
// Set mask field for data = 1 to 111001b: match bits 2,1 only
fd.dusart.ir_rx_d0_cfg.mask = 0x39;

// Set up bit config register
// Symbols per bit for a 1 = 3
fd.dusart.ir_rx_bit_cfg.sym1 = 3;
// Symbols per bit for a 0 = 2
fd.dusart.ir_rx_bit_cfg.sym0 = 2;
// Symbols per bit (initial) = 3
fd.dusart.ir_rx_bit_cfg.sym_init = 3;
// Priority = 1
```

Initially three symbols are shifted into the shift register (defined by the ***sym_init*** field in the ***dusart.ir_rx_bit_cfg*** register). The first transmitted bit value is '0', the three symbols being '101' (the final symbol being the first of the next bit). This triggers a 'data0' match (the least significant symbol is a don't care), but not a 'data1' match. The data value '0' is therefore detected. Two further symbols (defined by the ***sym0*** field in the ***dusart.ir_rx_bit_cfg*** register) are then shifted in and the process repeated for the next bit.

The next transmitted bit value is '1', the three bits now being '100'. This triggers a match for both 'data0' and 'data1'. A check of the ***priority*** field (true) indicates that in this instance the data value '1' is detected. Three further symbols (defined by the ***sym1*** field in the ***dusart.ir_rx_bit_cfg*** register) are then shifted in and the process is repeated for the next bit.

This sequence repeats until all of the data bits of the frame are detected.

	Shift Register ⇐		
Initial state	000000		
Shift in 3 symbols	000101	mask0 → *000100* mask1 → *000101*	match0 = TRUE match1 = FALSE **Detected = '0'**
Shift in 2 symbols	010100	mask0 → *000100* mask1 → *000100*	match0 = TRUE match1 = TRUE priority_1 = TRUE **Detected = '1'**

18.5.2 Pulse Shaper

The pulse shaper is useful, particularly in IrDA modes of operation, in increasing the frequency/phase tolerance of the receiver to the incoming signal. An incoming pulse can be detected, and where necessary extended to a minimum pulse width, prior to further processing. The 8-bit sample counter in the IFR counter module is provided to maintain up to 255 sample periods of minimum pulse duration. The ***dusart.ir_rx_cfg*** configuration register provides the necessary enable and minimum_pulse_duration values in the ***en*** and ***min_pulse*** fields.

A further feature, bitwise synchronisation, is included to improve the frequency error tolerance of incoming data streams. By taking advantage of some frame formats that begin each bit period with the same data transition (edge), the USART symbol strobe may be resynchronised several times within the frame data portion. This feature is enabled by setting the ***bit_sync_en*** field in the ***dusart.ir_rx_bit_cfg*** register.

18.5.3 Polarity Controls

All of the signal polarities for the lead-in, data0, data1 and lead-out A and B phases are configurable via the following registers:

- ***dusart.ir_ldin_cfg***
- ***dusart.ir_d0_cfg***
- ***dusart.ir_d1_cfg***
- ***dusart.ir_ldout_cfg***

Each has polarity_a and polarity_b configuration settings in the ***a_pol*** and ***b_pol*** fields, which apply for both transmit and receive data directions.

At each stage of the transmit or receive frame, the IFR state machine determines which of the polarity configuration registers is selected for the current stage of the frame.

18.6 Infra-Red Interface Registers

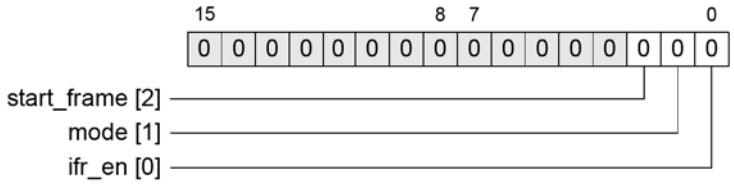
The Infra-Red Interface contains the following registers:

Address	Name	Reset	Type	Page
0xFD00	***dusart.ir_ctrl***	0x0000	RW	18-5
0xFD02	***dusart.ir_sts***	0x0000	R	18-6
0xFD04	***dusart.ir_int_en***	0x0000	RW	18-6
0xFD06	***dusart.ir_int_dis***	0x0000	W	18-7
0xFD08	***dusart.ir_int_clr***	0x0000	W	18-7
0xFD0A				
0xFD0C	***dusart.ir_ldin_cfg***	0x0000	RW	18-8
0xFD0E	***dusart.ir_d0_cfg***	0x0000	RW	18-8
0xFD10	***dusart.ir_d1_cfg***	0x0000	RW	18-9
0xFD12	***dusart.ir_ldout_cfg***	0x0000	RW	18-9
0xFD14	***dusart.ir_thresh_cfg***	0x0000	RW	18-10
0xFD16	***dusart.ir_len_cfg***	0x0000	RW	18-10
0xFD18	***dusart.ir_rx_cfg***	0x0000	RW	18-11
0xFD1A	***dusart.ir_rx_bit_cfg***	0x0000	RW	18-11
0xFD1C	***dusart.ir_rx_d0_cfg***	0x0000	RW	18-12
0xFD1E	***dusart.ir_rx_d1_cfg***	0x0000	RW	18-12
0xFD20	***dusart.ir_frame_cfg***	0x0000	RW	18-13

Table 50: Infra-Red Interface registers

18.6.1 dusart.ir_ctrl

Address: 0xFD00 Reset: 0x0000 Type: RW



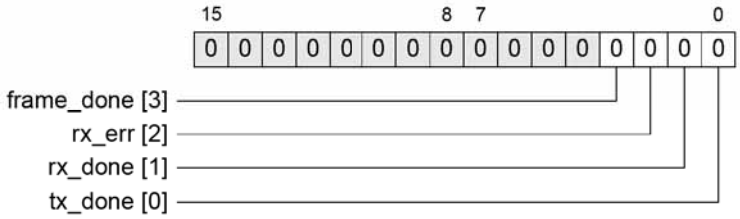
The main control register for the IFR.

The register contains the following fields.

Bits	Field	Type
2	**start_frame:** Enables frame transmission or reception. This bit should only be set when the IFR module is in the IDLE state.	RW
1	**mode:** The mode of operation. This bit is sampled when the IFR is in the IDLE state and ***start_frame*** is '1'. Subsequent changes are not read until the next ***start_frame*** pulse. This field can have one of the following values. '0': rx: Infra-red peripheral configured as a receiver. '1': tx: Infra-red peripheral configured as a transmitter.	RW
0	**ifr_en:** Enables the IFR module. The IFR may be returned to the IDLE state at any time by resetting this bit to '0'.	RW

18.6.2 dusart.ir_sts

Address: 0xFD02 Reset: 0x0000 Type: R



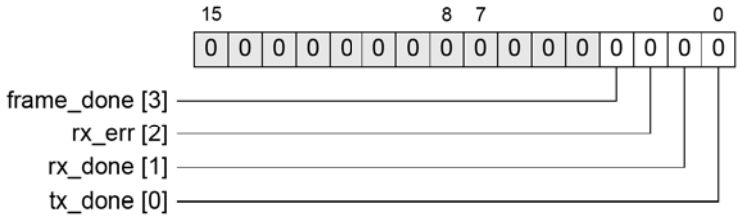
The transmit, receive and control interrupt status of the IFR.

The register contains the following fields.

Bits	Field	Type
3	**frame_done:** The entire frame, consisting of lead-in, data, lead-out and handover periods, is complete.	R
2	**rx_err:** A receive error has been detected. A receive error occurs if an unexpected symbol value (or sequence of values in the case of data matching) is detected during the lead-in b, data or lead-out b portions of a frame.	R
1	**rx_done:** The data portion of the frame has been received.	R
0	**tx_done:** The data portion of the frame has been transmitted.	R

18.6.3 dusart.ir_int_en

Address: 0xFD04 Reset: 0x0000 Type: RW



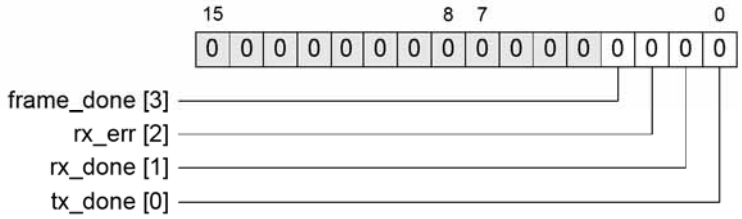
Register ***dusart.ir_int_en*** enables the interrupt events described in the ***dusart.ir_sts*** register. It forms a set/clear pair with the ***dusart.ir_int_dis*** register. Setting a bit to '1' enables the interrupt for that bit. Reading this register returns the current value of the interrupt enable control for each bit.

The register contains the following fields.

Bits	Field	Type
3	**frame_done:** Enables the frame complete interrupt.	RW
2	**rx_err:** Enables the receive error interrupt.	RW
1	**rx_done:** Enables the receive complete interrupt.	RW
0	**tx_done:** Enables the transmit complete interrupt.	RW

18.6.4 dusart.ir_int_dis

Address: 0xFD06 Reset: 0x0000 Type: W



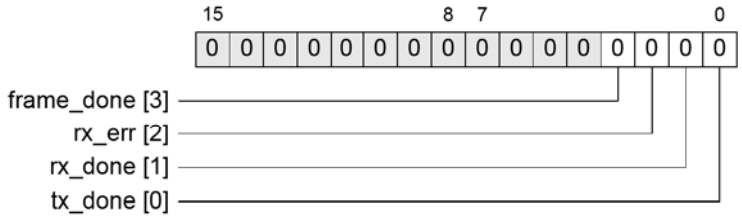
Register ***dusart.ir_int_dis*** disables the interrupt events described in the ***dusart.ir_sts*** register. It forms a set/clear pair with the ***dusart.ir_int_en*** register. Setting a bit to '1' disables the interrupt for that bit. If an interrupt is disabled, no interrupt is generated for that event, but the value of the interrupt status register is still updated. Reading this register returns zero.

The register contains the following fields.

Bits	Field	Type
3	**frame_done:** Disables the frame complete interrupt.	W
2	**rx_err:** Disables the receive error interrupt.	W
1	**rx_done:** Disables the receive complete interrupt.	W
0	**tx_done:** Disables the transmit complete interrupt.	W

18.6.5 dusart.ir_int_clr

Address: 0xFD08 Reset: 0x0000 Type: W



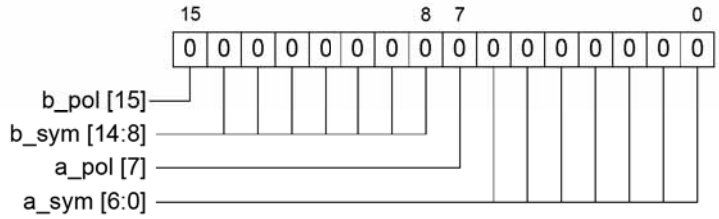
Register ***dusart.ir_int_clr*** clears the interrupt events described in the ***dusart.ir_sts*** register. Setting a bit to '1' clears the corresponding bit in the status register.

The register contains the following fields.

Bits	Field	Type
3	**frame_done:** Clears the frame complete interrupt.	W
2	**rx_err:** Clears the receive error interrupt.	W
1	**rx_done:** Clears the receive complete interrupt.	W
0	**tx_done:** Clears the transmit complete interrupt.	W

18.6.6 dusart.ir_ldin_cfg

Address: 0xFD0C Reset: 0x0000 Type: RW



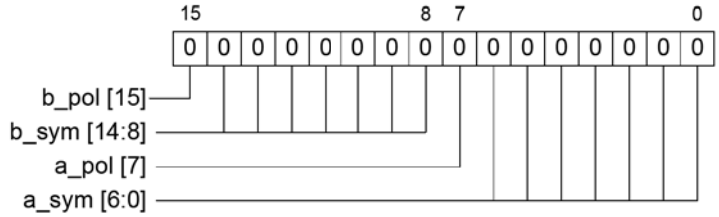
The ***dusart.ir_ldin_cfg*** register holds the polarity and duration (number of symbols) of each phase (a and b) within the lead-in part of a transmitted or received frame.

The register contains the following fields.

Bits	Field	Type
15	**b_pol:** The polarity of symbols in the lead-in 'b' phase. '0': The signal at the pin is low (logic 0). '1': The signal at the pin is high (logic 1).	RW
14:8	**b_sym:** The number of symbol strobes in the lead-in 'b' phase.	RW
7	**a_pol:** The polarity of symbols in the lead-in 'a' phase. '0': The signal at the pin is low (logic 0). '1': The signal at the pin is high (logic 1).	RW
6:0	**a_sym:** The number of symbol strobes in the lead-in 'a' phase.	RW

18.6.7 dusart.ir_d0_cfg

Address: 0xFD0E Reset: 0x0000 Type: RW



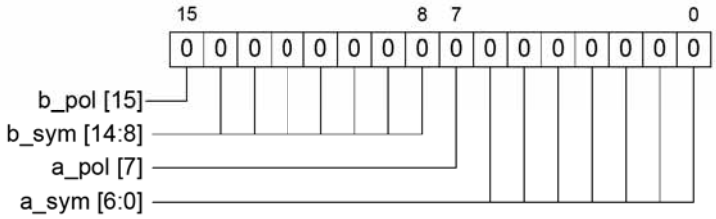
The d0 configuration register holds the polarity and duration (number of symbols) of each phase (a and b) within data = 0 parts of a transmitted frame. For received frames, data bits are decoded according to the values in the ***ir_rx_bit_cfg***, ***ir_rx_d0_cfg*** and ***ir_rx_d1_cfg*** registers.

The register contains the following fields.

Bits	Field	Type
15	**b_pol:** The polarity of symbols in the data = 0 'b' phase. '0': The signal at the pin is low (logic 0). '1': The signal at the pin is high (logic 1).	RW
14:8	**b_sym:** The number of symbol strobes in the data = 0 'b' phase.	RW
7	**a_pol:** The polarity of symbols in the data = 0 'a' phase. '0': The signal at the pin is low (logic 0). '1': The signal at the pin is high (logic 1).	RW
6:0	**a_sym:** The number of symbol strobes in the data = 0 'a' phase.	RW

18.6.8 dusart.ir_d1_cfg

Address: 0xFD10 Reset: 0x0000 Type: RW



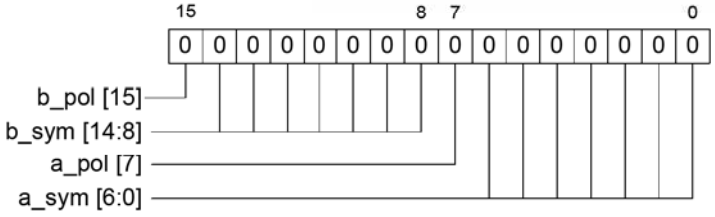
The d1 configuration register holds the polarity and duration (number of symbols) of each phase (a and b) within data = 1 parts of a transmitted frame. For received frames, data bits are decoded according to the values in the ***ir_rx_bit_cfg***, ***ir_rx_d0_cfg*** and ***ir_rx_d1_cfg*** registers.

The register contains the following fields.

Bits	Field	Type
15	**b_pol:** The polarity of symbols in the data = 1 'b' phase. '0': The signal at the pin is low (logic 0). '1': The signal at the pin is high (logic 1)	RW
14:8	**b_sym:** The number of symbol strobes in the data = 1 'b' phase.	RW
7	**a_pol:** The polarity of symbols in the data = 1 'a' phase. '0': The signal at the pin is low (logic 0). '1': The signal at the pin is high (logic 1).	RW
6:0	**a_sym:** The number of symbol strobes in the data = 1 'a' phase.	RW

18.6.9 dusart.ir_ldout_cfg

Address: 0xFD12 Reset: 0x0000 Type: RW



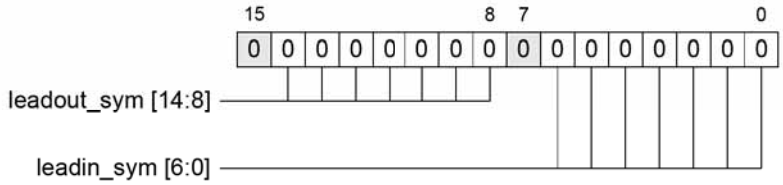
The ***dusart.ir_ldout_cfg*** register holds the polarity and duration (number of symbols) of each phase (a and b) within the lead-out part of a transmitted or received frame.

The register contains the following fields.

Bits	Field	Type
15	**b_pol:** The polarity of symbols in the lead-out 'b' phase. '0': The signal at the pin is low (logic 0). '1': The signal at the pin is high (logic 1).	RW
14:8	**b_sym:** The number of symbol strobes in the lead-out 'b' phase.	RW
7	**a_pol:** The polarity of symbols in the lead-out 'a' phase. '0': The signal at the pin is low (logic 0). '1': The signal at the pin is high (logic 1).	RW
6:0	**a_sym:** The number of symbol strobes in the lead-out 'a' phase.	RW

18.6.10 dusart.ir_thresh_cfg

Address: 0xFD14 Reset: 0x0000 Type: RW



The symbol counters count from the initial ***a_sym*** and ***b_sym*** values down to zero. It is conceivable that in receive mode, a tolerance is required when scanning for the beginning of a frame. Threshold values allow a minimum symbol count value, beyond which the first ‘a’ phase of lead-in or lead-out is accepted. If an unexpected symbol polarity is detected before this threshold is reached, a false trigger is assumed and the count down is re-initialised.

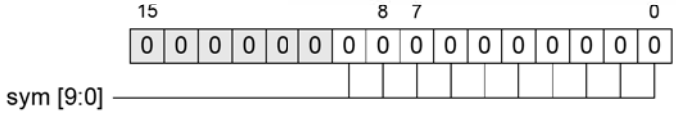
As an example, a lead-in 'a' count value of eight (in the ***a_sym*** field) with a threshold value of six (in the ***leadin_sym*** field) implies a minimum lead-in 'a' pulse width of three symbols. The lead-in ‘a’ phase is accepted at any time after the symbol counter has counted down from eight to six.

The register contains the following fields.

Bits	Field	Type
14:8	**leadout_sym:** Threshold below which the lead-out ‘a’ phase is accepted and the IFR begins to scan for the start of the lead-out ‘b’ phase.	RW
6:0	**leadin_sym:** Threshold below which the lead-in ‘a’ phase is accepted and the IFR begins to scan for the start of the lead-in ‘b’ phase.	RW

18.6.11 dusart.ir_len_cfg

Address: 0xFD16 Reset: 0x0000 Type: RW



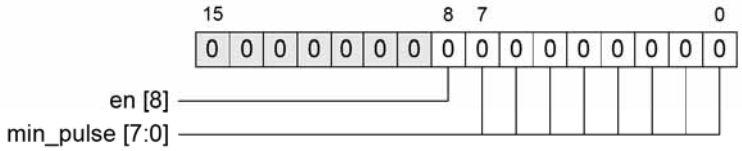
The frame counter measures the number of symbols in the entire frame. This is the sum of lead-in symbols (multiplied by the number of lead-in loops), data symbols, lead-out symbols (multiplied by the number of lead-out loops) and any symbols of handover or guard time after the final lead-out repetition.

The register contains the following field.

Bits	Field	Type
9:0	**sym:** The total number of symbols representing a single frame.	RW

18.6.12 dusart.ir_rx_cfg

Address: 0xFD18 Reset: 0x0000 Type: RW



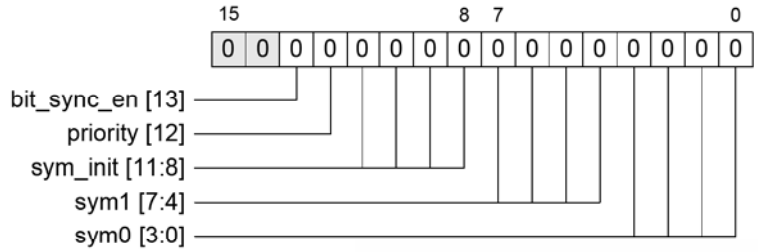
The pulse shaper allows received pulses to be extended. An example use is in IrDA mode where a minimum pulse width is allowed; internally extending the received pulse width to always be at least 3/16 of a bit period can increase the receiver's tolerance to frequency drift.

The register contains the following fields.

Bits	Field	Type
8	**en:** When set, extends each pulse to the minimum pulse duration. Any pulse longer than the set duration is unaffected.	RW
7:0	**min_pulse:** The width, in sample periods, to which a narrow pulse is extended.	RW

18.6.13 dusart.ir_rx_bit_cfg

Address: 0xFD1A Reset: 0x0000 Type: RW



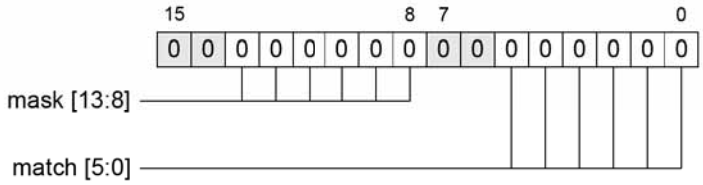
Bit detection configuration data for receive mode.

The register contains the following fields.

Bits	Field	Type
13	**bit_sync_en:** Allows resynchronisation within a frame. Useful in consumer IR modes where every bit period begins with an edge. Synchronisation is enabled following detection of the longer (in terms of symbols per bit) of the two bits.	RW
12	**priority:** If the initial correlation results in a positive match of both logic '0' and '1', choose which output value to select. If the ***sym1*** field is greater than the ***sym0*** field, set the priority to '1'. If the ***sym1*** field is less than the ***sym0*** field, set the priority to '0'.	RW
11:8	**sym_init:** The number of symbols to read before making an initial correlation at the beginning of the receive data period.	RW
7:4	**sym1:** The number of consecutive symbols required to represent a received '1' data bit.	RW
3:0	**sym0:** The number of consecutive symbols required to represent a received '0' data bit.	RW

18.6.14 dusart.ir_rx_d0_cfg

Address: 0xFD1C Reset: 0x0000 Type: RW



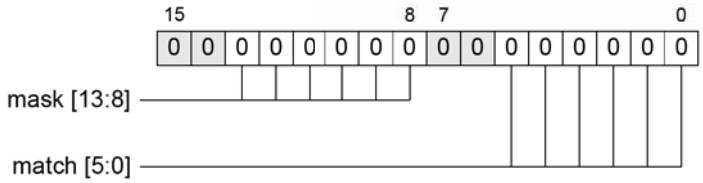
Correlation values and don't care fields for input '0' data bits.

The register contains the following fields.

Bits	Field	Type
13:8	**mask:** Don't care bits. Set bits in this field to '1' to ignore the corresponding bits in the match field.	RW
5:0	**match:** Compare value with shifted input data. If the input data shift register is the same as the match register (ignoring the mask bit positions), then there is a match.	RW

18.6.15 dusart.ir_rx_d1_cfg

Address: 0xFD1E Reset: 0x0000 Type: RW



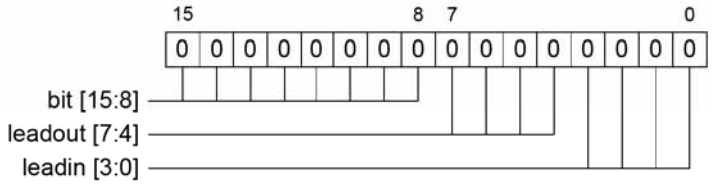
Correlation values and don't care fields for input '1' data bits.

The register contains the following fields.

Bits	Field	Type
13:8	**mask:** Don't care bits. Set bits in this field to '1' to ignore the corresponding bits in the match field.	RW
5:0	**match:** Compare value with shifted input data. If the input data shift register is the same as the match register (ignoring the mask bit positions), then there is a match.	RW

18.6.16 dusart.ir_frame_cfg

Address: 0xFD20 Reset: 0x0000 Type: RW



Configuration for higher level counters - bits per frame, number of lead-in cycles and number of lead-out cycles.

The register contains the following fields.

Bits	Field	Type
15:8	**bit:** The total number of data bits carried by the frame.	RW
7:4	**leadout:** The number of lead-out cycles.	RW
3:0	**leadin:** The number of lead-in cycles. A lead-in count of zero is not recommended in receive mode, as symbol synchronisation then occurs at the beginning of the data period. This may cause some data corruption or loss of the first frame.	RW