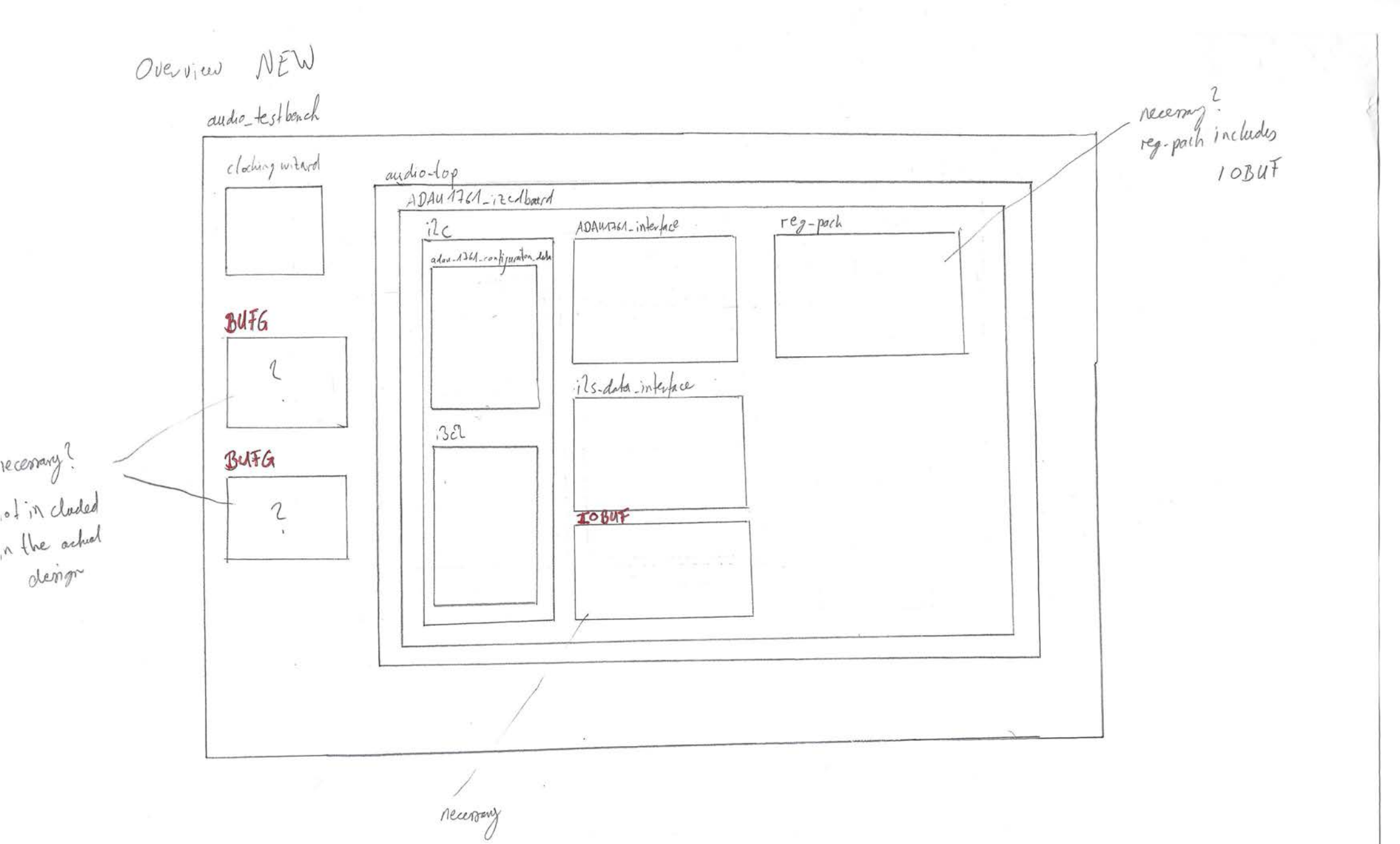
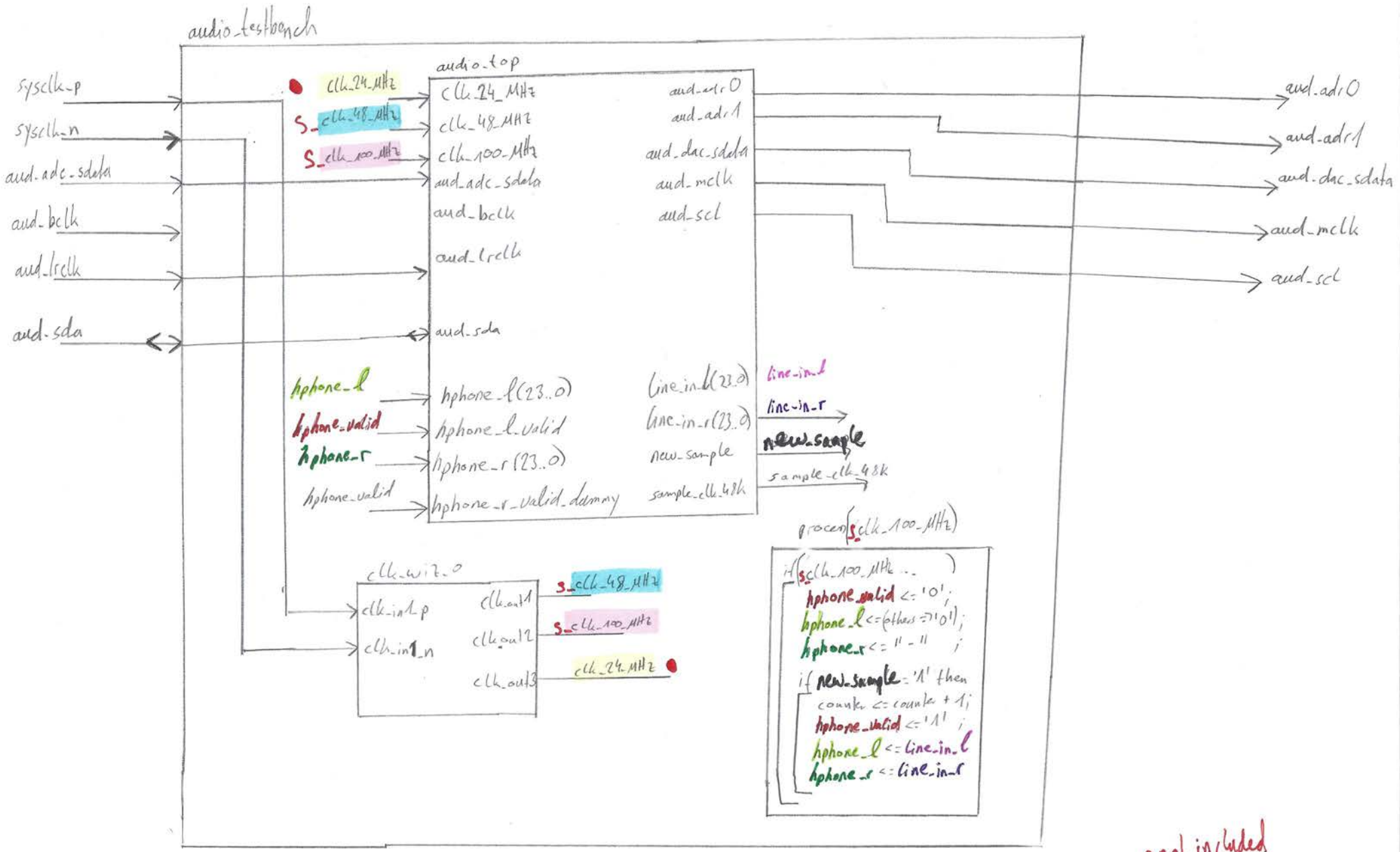
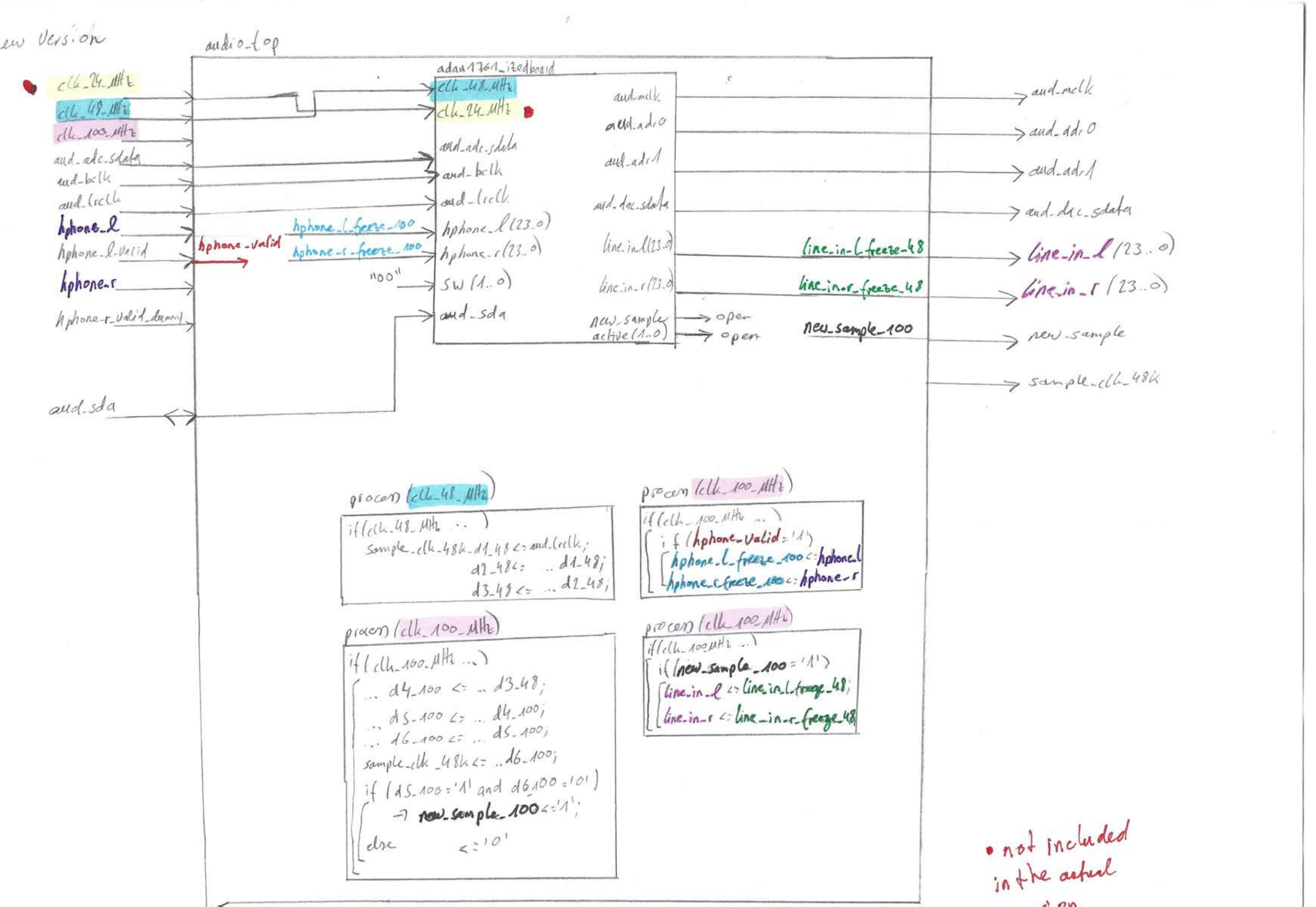
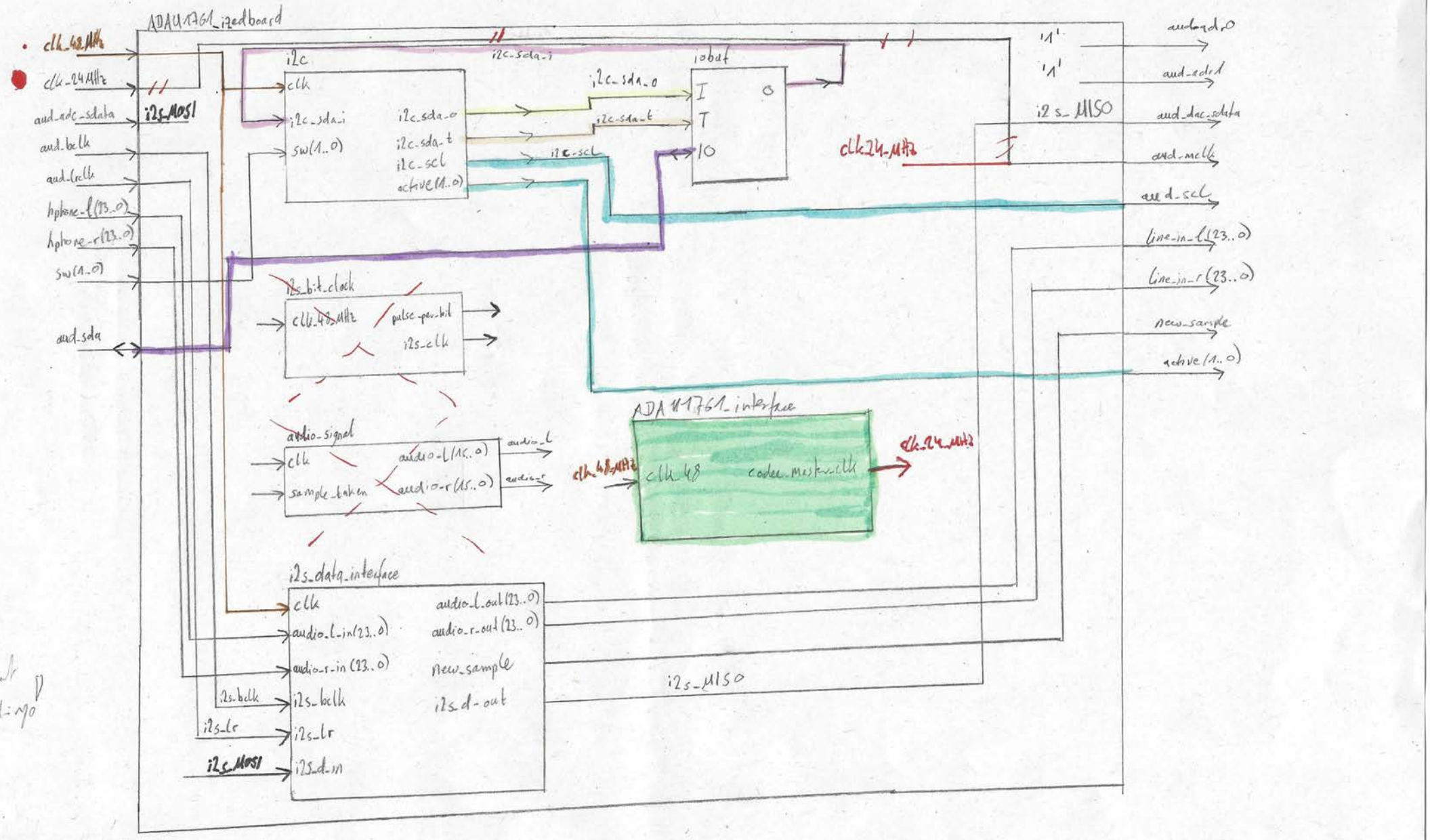

Overview NEW
audio_testbench
clocking wizard
audio_top
ADAU1761_izedboard
i2c
adau_1761_configuration_data
ADAU1761_interface
reg_pack
i2s_data_interface
IOBUF
BUFG
?
BUFG
?
necessary?
not included in the actual design
necessary?
reg_pack includes IOBUF
necessary

ew version .

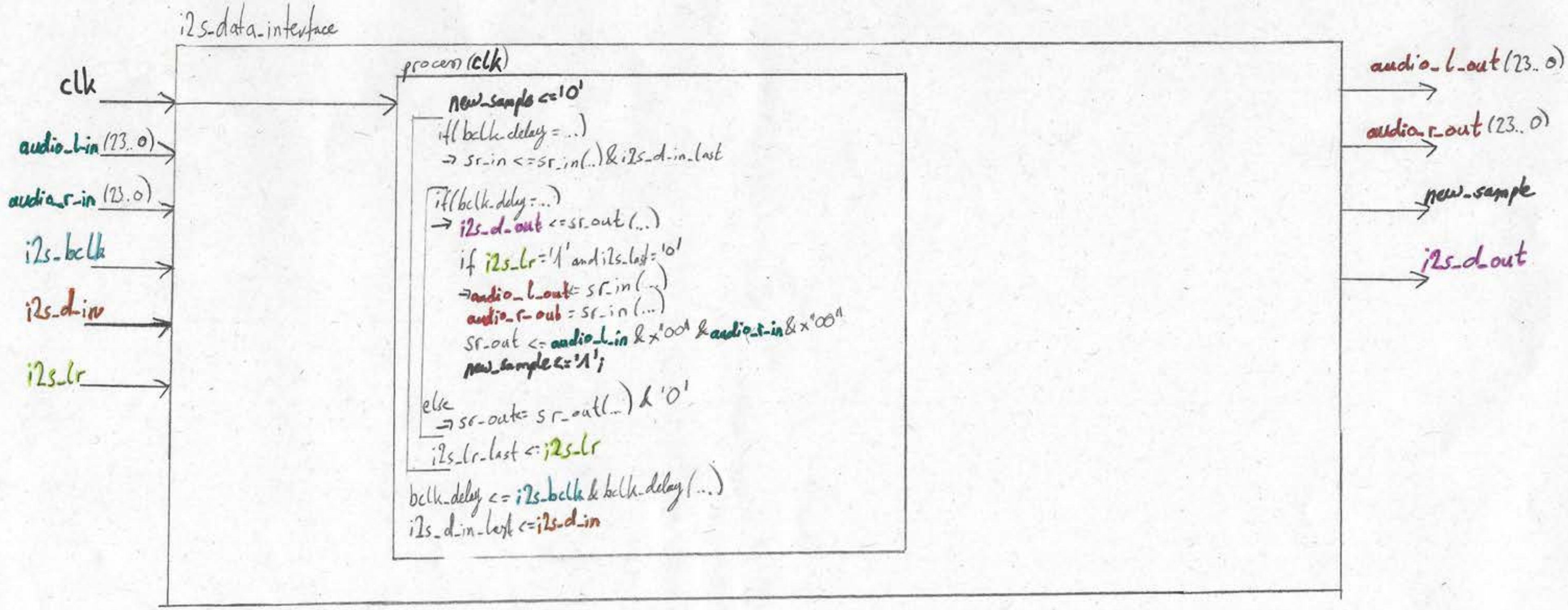


● not included in the actual version.


ew Version
audio_top
adau1761_izedboard
clk_24_MHz
clk_48_MHz
clk_100_MHz
aud_adc_sdata
aud_bclk
aud_lrclk
hphone_l
hphone_l_valid
hphone_r
hphone_r_valid_dummy
aud_sda
hphone_valid
hphone_l_freeze_100
hphone_r_freeze_100
"00"
SW(1..0)
hphone_l(23..0)
hphone_r(23..0)
aud_mclk
aud_adr0
aud_adr1
aud_dac_sdata
line_in_l(23..0)
line_in_r(23..0)
new_sample_active(1..0)
open
open
line_in_l_freeze_48
line_in_r_freeze_48
new_sample_100
aud_mclk
aud_adr0
aud_adr1
aud_dac_sdata
line_in_l (23..0)
line_in_r (23..0)
new_sample
sample_clk_48k
process (clk_48_MHz)
if(clk_48_MHz ...)
sample_clk_48k_d1_48 <= aud_lrclk;
d2_48 <= ... d1_48;
d3_48 <= ... d2_48;
process (clk_100_MHz)
if(clk_100_MHz ...)
if (hphone_valid='1')
hphone_l_freeze_100 <= hphone_l
hphone_r_freeze_100 <= hphone_r
process (clk_100_MHz)
if(clk_100_MHz ...)
... d4_100 <= ... d3_48;
... d5_100 <= ... d4_100;
... d6_100 <= ... d5_100;
sample_clk_48k <= ... d6_100;
if (d5_100='1' and d6_100='0')
→ new_sample_100 <='1';
else <='0'
process (clk_100_MHz)
if(clk_100_MHz ...)
if(new_sample_100='1')
line_in_l <= line_in_l_freeze_48;
line_in_r <= line_in_r_freeze_48;
• not included in the actual design



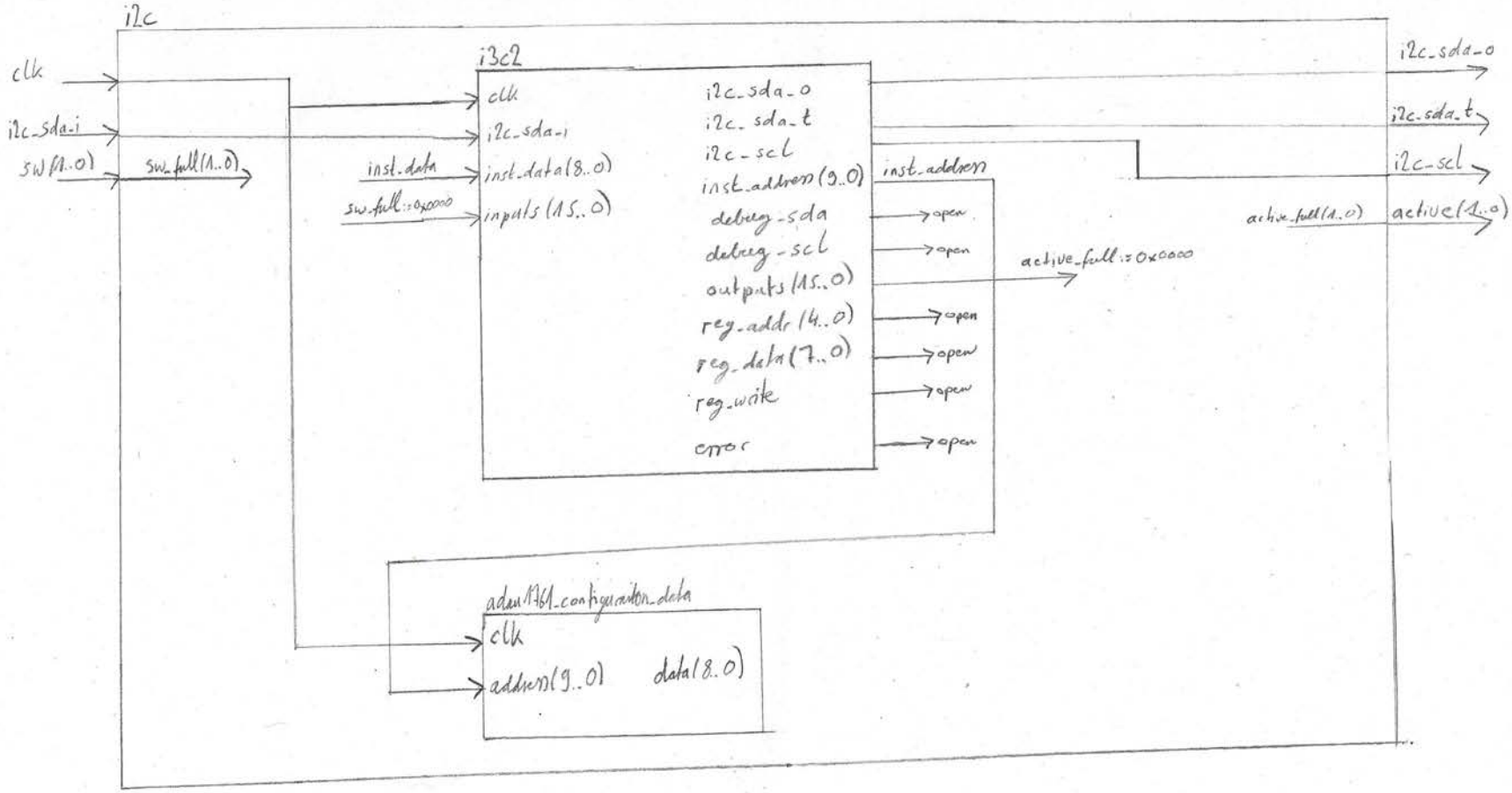
• not included in the actual design

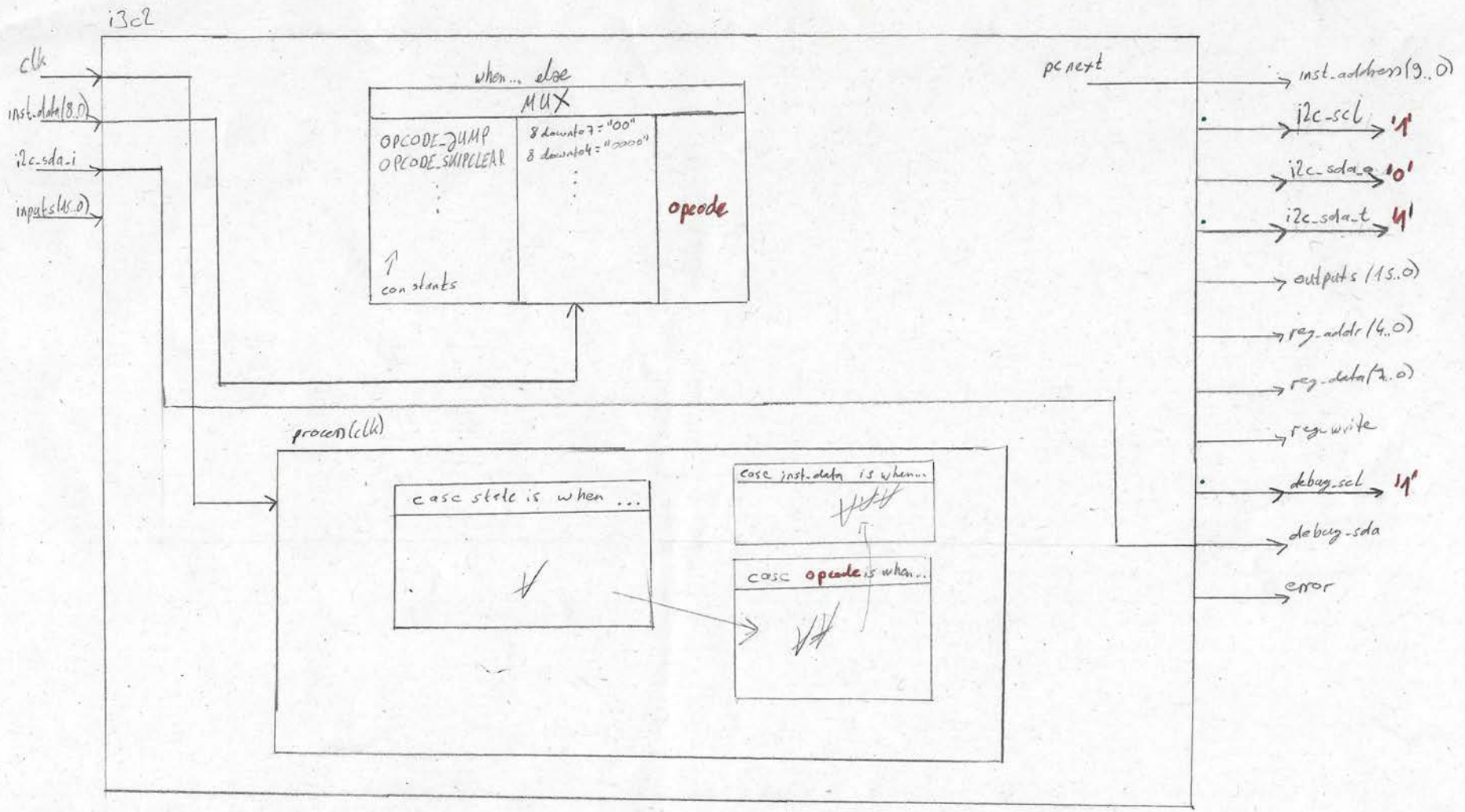


Signal bit-counter (5..0) := 0 ? nicht verwendet

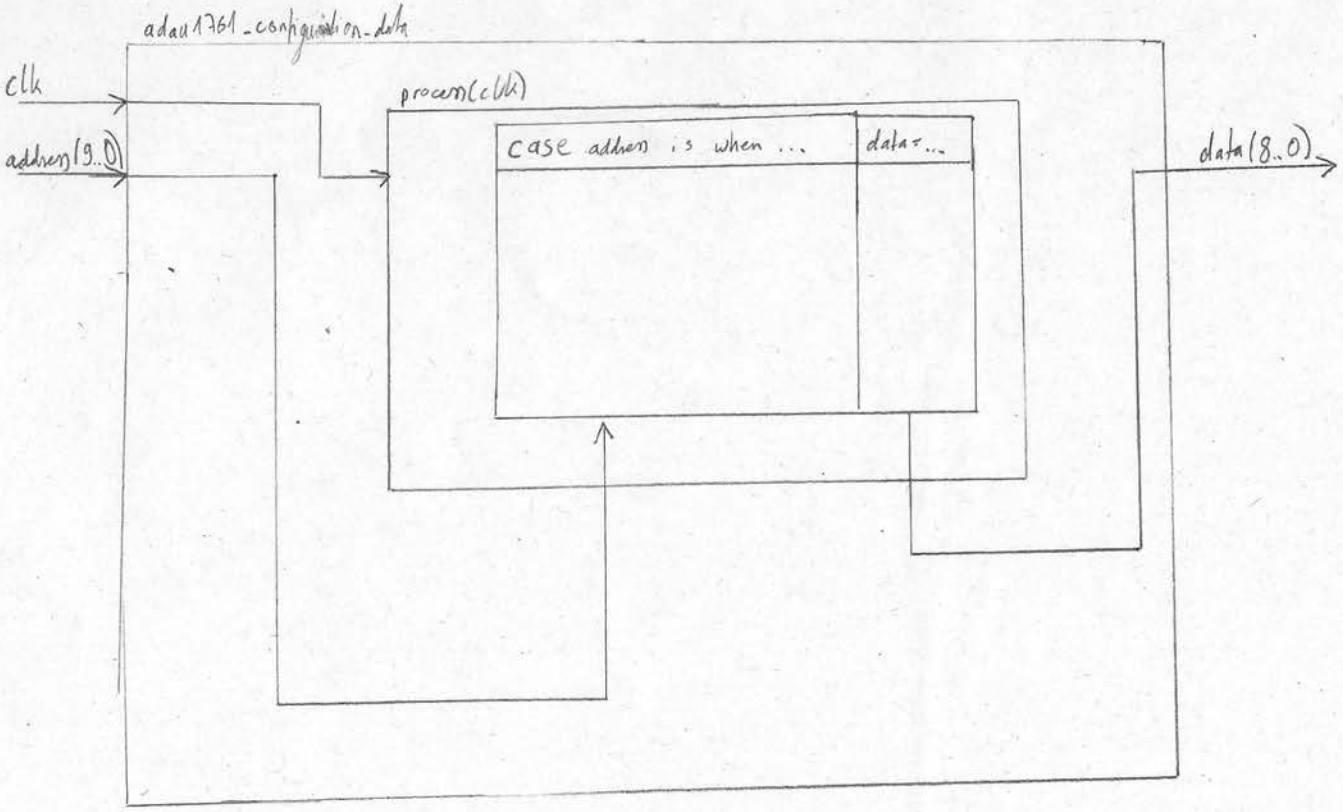
Signal bclk-delay (9..0) := 0
Signal lr-delay (9..0) := 0
sr-in (126..0) := 0
sr-out (63..0) := 0

i2s-lr-last := 0
i2s-d-in-last := 0


i2c
clk
i2c_sda_i
sw(1..0)
sw_full(1..0)
i3c2
clk
i2c_sda_i
inst_data
inst_data(8..0)
sw_full=0x0000
inputs(15..0)
i2c_sda_o
i2c_sda_t
i2c_scl
inst_address(9..0)
debug_sda
debug_scl
outputs(15..0)
reg_addr(4..0)
reg_data(7..0)
reg_write
error
open
inst_address
active_full=0x0000
active_full(1..0)
i2c_sda_o
i2c_sda_t
i2c_scl
active(1..0)
adau1761_configuration_data
clk
address(9..0)
data(8..0)



in case ... is when ... : clk_divide (7..0)
i2c_stalled
bit count (7..0)


adau1761_configuration_data
clk
address(9..0)
process(clk)
case address is when ...
data<...
data(8..0)