RF Application Note

Wireless Products

CAR RADIO

FM Receiver with Frequency Synthesizer TUA 4401K

WS LIN AE CE MCH B R. EMSLANDER TEL.: ..49 89 234 24465 2000-07-21

General Description:

The TUA 4401K is a carradio IC using BICMOS technology. The combination of an analog FM receiver and a digital PLL synthesizer on the same chip reduces the overall pin count in comparison of two separate ICs and in addition the number of necessary external components. This gives the flexibility both for high performance and low cost applications. The recommended applications for this device are FM only carradios and background receivers, capable for all world standards.

1. Frontend

Features:

- strictly symmetrical RF sections
- high level, high impedance mixer input with improved dynamic range
- high input / output 3rd order interception point
- balanced or unbalanced use of the mixer
- bus controlled AGC threshold
- 2 pin LO with improved low phase noise, internally coupled to PLL
- PLL with fast acquisition mode
- resolution 100kHz, 50kHz, 25kHz, 12.5kHz, 10kHz, and 6.25kHz
- high running crystal oscillator (61.5 MHz) to avoid interference with bus controlled adjustment

2. IF amplifier, demodulator, and STOP informations

Features:

- low noise amplifier
- gain adjust with DC control voltage or serial bus possible
- 7 stage IF limiter with extended signalstrength range suitable for the IF frequency range 10.7 MHz ... 21.4 MHz
- signalstrength DC and ADC output available
- low distortion coincidence demodulator (using short loop AFC principle) with MPX output
- multipath detector with analog output and ADC output
- IF counter for search tuning stop with selectable IF center frequency and window width and programmable thresholds for signalstrength and multipath evaluation
- STS informations -in window- , -below- , -beyond- available

3. I²C bus

- I²C bus (2 wire, fast mode device with 400 kbit/s)
- bus interface with low threshold voltage Schmitt trigger inputs for interfacing 3 V or 5 V microprocessors

Circuit Description:

The TUA 4401K is a one chip FM car radio system consisting of RF frontend, gain adjustable IF amplifier, FM-IF limiter amplifier, demodulator, PLL synthesizer, IF counter for STS and ADC's for fieldstrength and multipath detector. The serial bus is a I²C type.

1. FM frontend

The frontend consists of a two pin varactor tuned oscillator, a double balanced mixer and a prestage AGC control circuit. The mixer has an improved intermodulation behaviour and converts the RF signal to the 10,7 MHz IF range. Two inputs allow both symmetrical and unsymmetrical operation.
The integrated AGC stage for prestage control drives MOSFETS as well as PIN diodes a with current driver. The AGC threshold can be set with a serial bus controlled 2 Bit DAC.

2. FM IF amplifier

After the mixer an IF amplifier is present for IF post amplification. Input and output impedance are both 330 Ohms for matching with ceramic filters. For adjusting the over all gain the IF amplifier gain can be adjusted with a serial bus controlled 4 Bit DAC.

3. FM limiter and demodulator

The FM IF amplifier includes a seven stage capacitive coupled limiter amplifier and a fieldstrength generator with high linearity and increased dynamic range. The coincidence demodulator has an additional AFC short loop circuit with integrated varactor diode in parallel to the external tank circuit to improve the distortion behavior in case of detuning.

4. Multipath detector

A multipath detector with analog output is available.

5. A/D converter for fieldstrength and multipath detector

The 7 bit A/D converter has two input channels and works as a successive approximation converter. The conversion time for both input signals is t = 32 µs. The 7-bit digital-words from both channels (14 bit) are read out together via bus into two bytes with the read subaddress 82H. The input voltage range for both channels is 0 ... V_{REFD5V}.

6. IF counter and multipath/fieldstrength evaluation for STS

FM center frequencies are available in two ranges set by bit D7 in subaddress 05H. For D7 = 1 the range of center frequency is 20.800 MHz ... 22.3875 MHz in 128 steps (12.5 kHz per step). For D7 = 0 the range of center frequency is 10.400 MHz ... 11.1937 MHz in 128 steps (6.25 kHz per step).
The gate time is adjustable in 8 steps from 320 µs ... 40.96 ms and the tolerance of the accepted count value, the window, is adjustable in 5 steps from +/- (6.25 kHz ... 100 kHz) for D7=0 in subaddress 05H and +/- (12.5 kHz ... 200 kHz) for D7 = 1 in subaddress 05H. The results IF_CENT and IF_WINDOW are read out via bus (read-subaddress 82H) or pins IF_CENT and IF_WINDOW.
If the IF frequency is in the preselected window, IF_CENT goes from high to low level. If the IF frequency is outside the preselected window, IF_CENT is high. The bit IF_WINDOW is a hint IF-frequency that is to low (IF_WINDOW = high) or is to high (IF_WINDOW = low).
In addition to the frequency measurement, thresholds for multipath and fieldstrength voltages can be programmed via bus (subaddress 0BH). IF_CENT will only go to low level in case of fieldstrength and multipath voltages are beyond the thresholds and the frequency is inside the window.
When setting the thresholds to zero multipath and fieldstrength evaluation is disabled.

7. Crystal oscillator

A master crystal oscillator provides all necessary clock frequencies for the whole IC. A 61.5 MHz crystal is used in 3rd harmonic mode. The oscillator frequency can be fine tuned with a serial bus controlled 4 bit D/A converter.
The crystal frequency is used as reference frequency for the PLL oscillator and IF counter. It is also used as clock for the ADC’s. Finally the crystal frequency divided by 6 (10.25 MHz) is available at a pin as low pass filtered voltage, it can be disabled with the serial bus.

8. Output ports

PORT_1 / 2 are NMOS Open drain outputs.

9. I²C Bus

The TUA 4401K supports the I²C bus protocol (2 wire). All bus pins (SCL, SDA) are Schmitt triggered input buffer for 3 V or 5 V microcontroller.
The bit stream begins with the most significant bit (MSB), is shifted in (write mode) on the low to high transition of CLK and is shifted out (read mode) on the high to low transition of CLK.

9.1 I²C bus mode

Data Transition:
Data transition on the pin SDA must only occur when the clock SCL is low. SDA transitions while SCL is high will be interpreted as start or stop condition.

Start Condition (STA):
A start condition is defined by a high to low transition of the SDA line while SCL is at a stable high level. This start condition must precede any command and initiate a data transfer onto the bus.

Stop Condition (STO):
A stop condition is defined by a low to high transition of the SDA while the SCL line is at a stable high level. This condition terminate the communication between the devices and forces the bus interface into the initial conditions.

Acknowledge (ACK):
Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will pull the SDA line to low level to indicate it has receive the 8 bits of data correctly.

Data Transfer Write Mode:
To start the communication, the bus master must initiate a start condition, followed by the 8bit chip address (write). The chip address for the TUA 4401K is fixed as ”1100110” (MSB at first). The last bit (LSB = A0) of the chip address byte defines the type of operation to be performed:
A0 = 1, a read operation is selected and A0 = 0, a write operation is selected. After this comparison the TUA 4401K will generate an ACK.
After this device addressing the desired subaddress byte and data bytes must be followed. The subaddresses determines which one of the 9 data bytes (00H ... 07H, 0BH) is transmitted first. At the end of data transition the master must be generate the stop condition.

Data Transfer Read Mode:
To start the communication in the read mode, the bus master must initiate a start condition, followed by the 8bit chip address (write: A0 = 0), followed by the sub address read (82H/83H), followed by the chip address (read: A0 = 1). After that procedure the 16bit/8bit data register 82H/83H is read out. After the first 8 bit read out, the microcontroller mandatory sends LOW during the ACK-clock. After the second 8 bit read out the microcontroller mandatory sends HIGH during the ACK-clock. At the end of data transition the master must generate the stop condition.

10. PLL Synthesizer

R / N Counter

The TUA 4401K has 2 identical 16bit counter for R and N path. Input frequency for the R counter is the buffered XTAL-frequency (61.5 MHz). Tuning steps can be selected by the 16bit R-counter from f_R= 6.25 kHz ... 100 kHz. Input frequency for the N-counter is the buffered LO-frequency (in FM mode 98.2 MHz ... 118.7 MHz).

Three State Phase Comparator

The phase comparator generates a phase error signal according to phase difference between f_R (R counter output) and f_N (N counter output).This phase error signal drives the charge pump current generator.

Charge Pump

The charge pump generates signed pulses of current. 4 current values are available.

Loop Amp

The integrated rail to rail loop amplifier allows an active loop filter design with external components. Two modes are available with status bit D11: high speed and normal mode.

Technical details:

Supply voltage	8 V to 9 V
Ambient temperature	-40 ... +85 °C

The following AC / DC characteristics refer to supply voltage V_S = 8.5 V ±5 % and T_{amb} = +25 °C.

Supply current	111 mA

Local oscillator

frequency range	50 ... 250 MHz

RF mixer

input frequency	f_{22-23}	60 ... 140 MHz
max. input RF level	V_{22-23}	min. 120 dBµV
3rd Intercept point	IP3	125 dBµV
mixer gain	V_{22-23} = 10 mV_{rms}; R_L = 330 Ω	12 dB
noise figure	R_{Gopt} = 500 Ω	6 dB
input impedance	R_{22-23} asym.	1.8 kΩ
input impedance	C_{22-23} asym.	2.5 pF
reference voltage	V_{27}	4.8 V

Prestage AGC outputs

AGC threshold range	V_{22-23}		15 ... 60 mV
AGC voltage for MOSFET	V_{21}	V_{22-23} = 0 mV	6.4 V
AGC voltage for MOSFET	V_{21}	V_{22-23} = 200 mV_{rms}	max. 0.1 V
AGC current	I_{24*}	V_{22-23} = 0 mV	13 mA
AGC current	I_{24*}	V_{22-23} = 200 mV_{rms}	max. 0.1 mA
integrator current	I_{21*}	V_{22-23} = 0 mV; V_m=3V	- 50 µA
integrator current	I_{21*}	V_{22-23} = 200 V; V_m=3V	+ 50 µA

IF amplifier

DC input voltage	V_{29}		3.7 V
input resistance	R_{29}		330 Ω
output resistance	R_{31}		330 Ω
voltage gain	A_{31-29}		max. 26 dB
voltage gain	A_{31-29}		min. 13 dB
noise figure	F	R_G = 330 Ω	7 dB

IF limiter amplifier / fieldstrength generator

input voltage	V_{34}	V_{37} -3 dB	25 µV_{rms}
AM suppression	A_{AM}	m = 30 %	80 dB
fieldstrength voltage	V_{38}	V_{34} = 0 mV_{rms}	max. 0.8 V
fieldstrength voltage	V_{38}	V_{34} = 1 mV_{rms}	1.9 V
fieldstrength voltage	V_{38}	V_{34} = 10 mV_{rms}	2.9 V
fieldstrength voltage	V_{38}	V_{34} = 200 mV_{rms}	4.2 V
fieldstrength dyn. range	V_{38dyn}		90 dB
fieldstrength linearity	V_{38lin}		± 1dB
fieldstrength temp. drift	V_{38temp}		max. ± 3dB

FM demodulator

AF output voltage	V_{37}	f_{IF} = 10.7 MHz ΔF = 75 kHz	typ. 600 mV_{rms}
AF output voltage	V_{37}	f_{IF} = 21.4 MHz ΔF = 75 kHz	typ. 300 mV_{rms}
THD	THD_{37}	ΔF = 75 kHz	typ. 0.3 %
THD detuned	THD_{37}	ΔF = 75 kHz ± 50 kHz	max. 0.8 %

*) Integrator currents are measured between the output pin (-pole of the measurement equipment) and a voltage source V_m (+ pole).

Multipath detector

attack current	I_{40*}	V_{39} = 350 V_{rms} ; V_m = 5 V	900 µA
recovery current	I_{40*}	V_{39} = 0 V ; V_m = 3.6 V	- 13 µA
start voltage	V_{41Def}	V_{39} = 0 V	4.7 V
detector characteristic	V_{41}	f_{39} = 200 kHz ; V_{39} = 40 mV_{rms}	V_{Def} - 2.8 V

Crystal oscillator

operating frequency	f_{10-11}	3rd harmonic	61.5 MHz
negative input impedance	Z_{10-11}	f = 61.5 MHz	- 250 Ω
negative input impedance	Z_{10-11}	f = 20.5 MHz	1.4 kΩ
spurious harmonics crystal	a_{sp}	f < 200 MHz	- 20 dB

Chargepump output (loopfilter input)

DC voltage	V_{PD_FM}	locked	2.5 V
DC current	$+/-I_{PD\_FM3}$		4 mA
DC current	$+/-I_{PD\_FM2}$		2 mA
DC current	$+/-I_{PD\_FM1}$		1 mA
DC current	$+/-I_{PD\_FM0}$		500 µA
tristate output current	$+/-I_{PD\_FMOFF}$		typ. 0.1 nA

Loop amplifier tuning voltage output (loopfilter output)

LOW output voltage	V_{PDA_L}	I_{TUNE} = 100 µA	max. 400 mV
HIGH output voltage	V_{PDA_H}	I_{TUNE} = -100 µA	min. $V_{VCC-0.5V}$
HIGH output current source	I_{PDA_H}	V_{TUNE} = 4 V	- 2.4 mA
LOW output current source	I_{PDA_L}	V_{TUNE} = 4 V	- 1.2 mA

PLL for synthesizer

PLL / VCO step size	f_{ref}	$f_{crystal}$ = 61.5 MHz	6.25 ... 100 kHz
N counter divider ratio	N	16 bit	2 ... 65535
R counter divider ratio	R	16 bit	2 ... 65535

Port outputs, IF_CENT, IF_WINDOW

LOW output voltage	V_P	I_P = 1 mA	typ. 100 mA
HIGH leackage current	I_{P_LEACK}	V_P = 5 V	max. 100 nA

I²C bus

H input voltage	V_{IH}	2.10 ... 5.50 V
L input voltage	V_{IL}	- 0.5 ... 0.90 V
hysteresis of Schmitt trigger inputs	I_{hys}	min. 0.3 V
input capacity	C_I	max. 5 pF

Reference Voltages

Ref voltage	V_6	4.5 ... 5.5 V
Ref voltage	V_7	2.7 ... 3.3 V

Demoboard:

The demoboard contains the single chip receiver TUA 4401K. This Integrated Circuit is designed using the latest BICMOS technology. The IC includes RF, IF, and PLL sections along with severed internal voltage and current supplies.

Surrounding the IC are the external RF stage for FM, the local oscillator, the IF filtering parts, and input and output matching for the different signals and control possibilities.

RF section

The FM input prestage amplifier uses the Siemens MOSFET tetrode BF1009S with internal fixed DC bias. Both gate 2 and the pin diode at the antenna input are controlled via the IC to limit the maximum RF input level at the FM mixer input. The RF circuit between the drain of the MOSFET and the mixer input is designed as a tracking circuit to provide image frequency rejection and suppress local oscillator radiation.
The AGC threshold has an internally controlled AGC starting point from V_{in} = 15 mV_{rms} to 60 mV_{rms} at the mixer input. The AGC time constant is given with

$$I * t = C * \Delta U.$$

I IC internal reference current I_{ref} = 50 µA
t time constant
C load capacity at pin 21
ΔU AGC voltage range at pin 21.

The local oscillator operates in the 100 MHz range.

The parameter for the RF / LOC OSC adjustment is the signal strength level. At the input frequency of 88 MHz the LOC OSC tuning voltage V_{TUN} is set to 2.58 V with L04. The prestage coils L01 and L03 have to be adjusted to maximum signal strength. At 106 MHz maximal signal strength is set with P01.

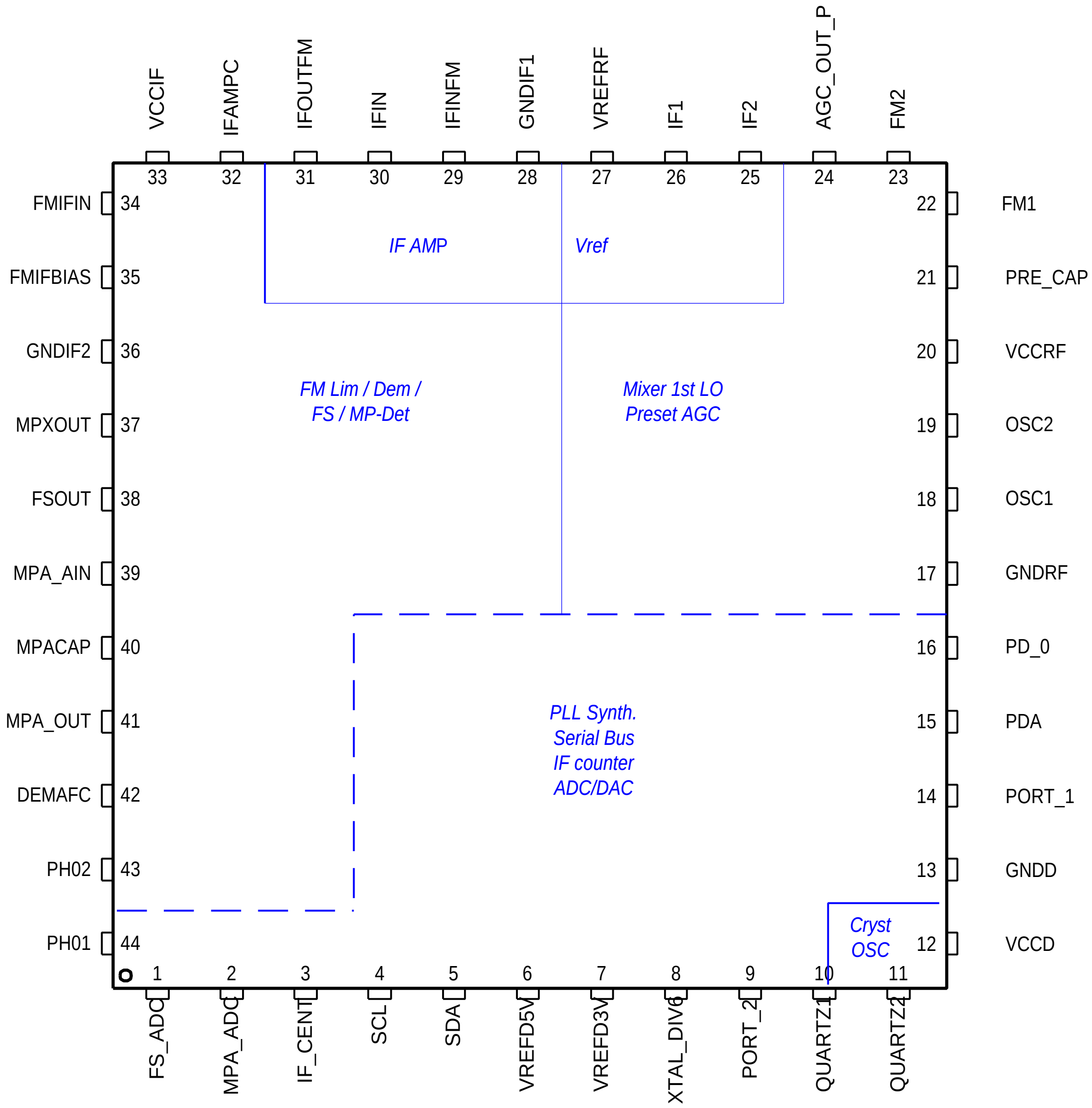
At the balanced mixer output (pins 25 and 26) there is a matching tank circuit (C_p = 120 pF) for the following ceramic filter. The double filtered IF signal is amplified in a preamplifier stage and then filtered again with a further ceramic filter. The gain of the IF amplifier in the range from 16 dB to 26 dB may be set via I^2C bus control.

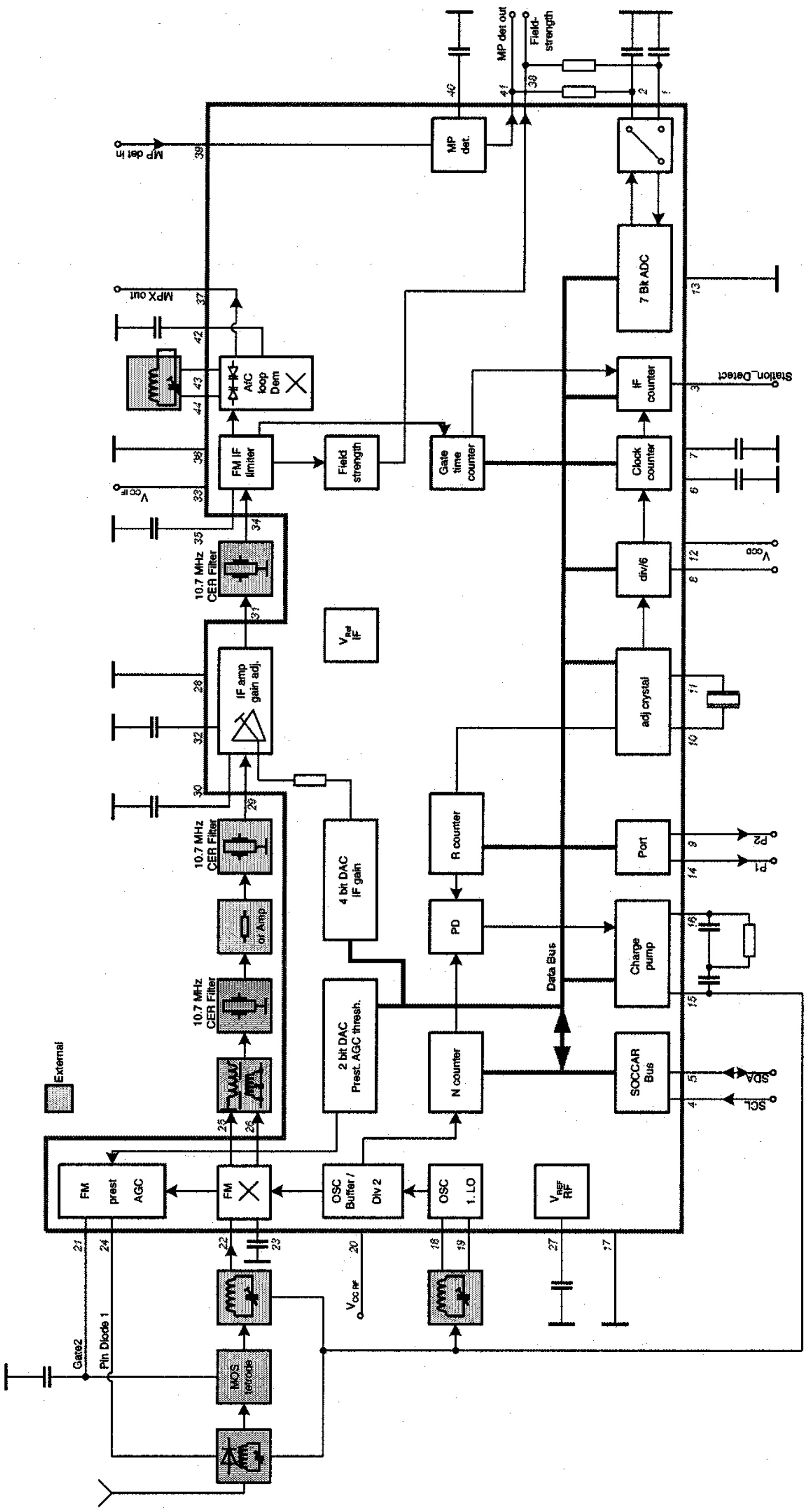
After passing the limiter amplifier the IF signal is demodulated. The demodulator has an automatic center tracking behavior. The total capacitance of the tank circuit is 120 pF, the resulting external part has to be C_{ext} = 82 pF. For a first adjustment the DC level at the AGC capacitor at pin 42 has to be adjusted to V_{AGC} = 3.35 V with the ferrite core of the tank circuit T102.

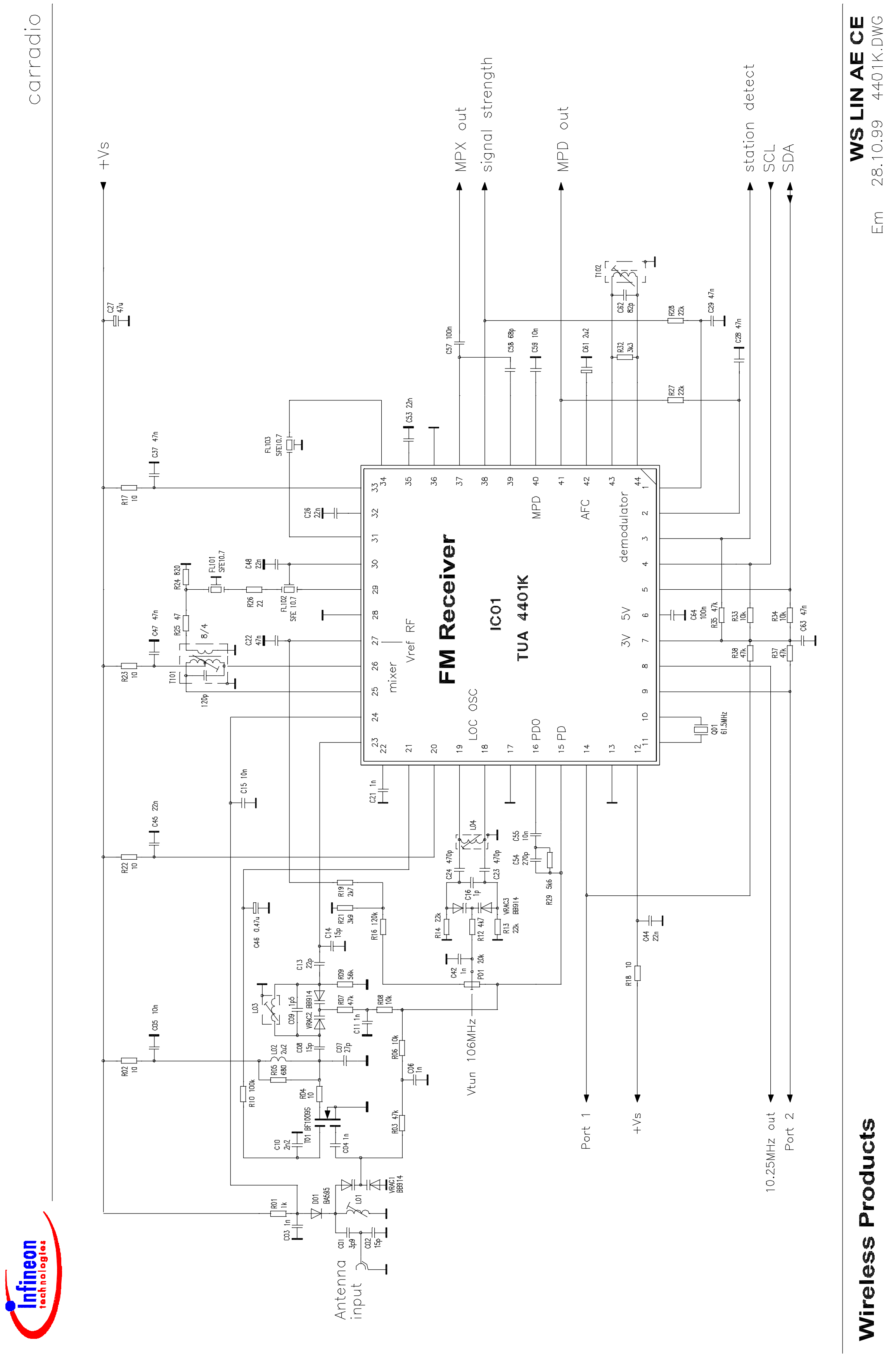
The demodulated MPX signal is supplied at the output pin 37.

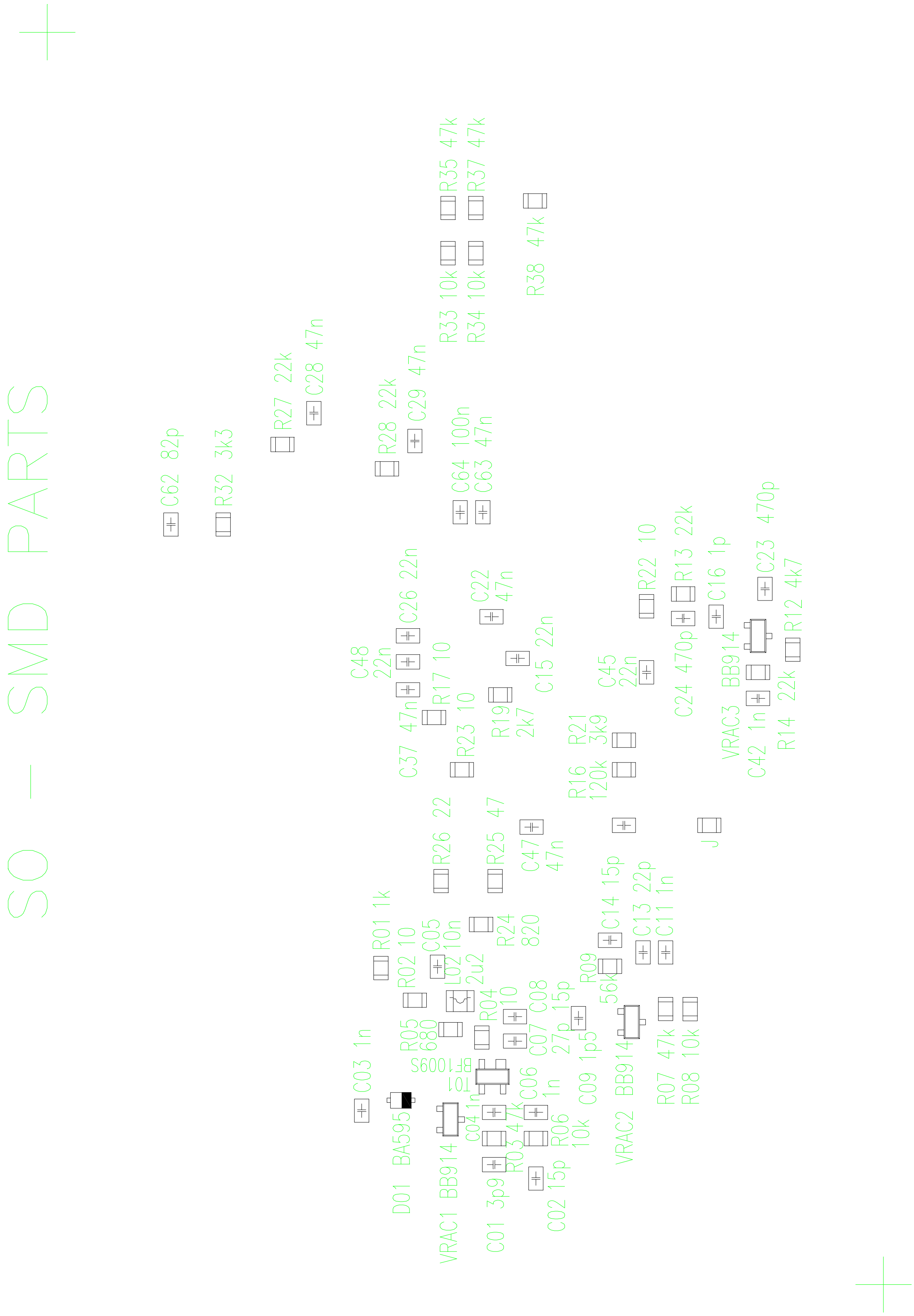
The IF_CENT output pin 3 (open collector) supplies a LOW level when the IF frequency is in the preselected window.

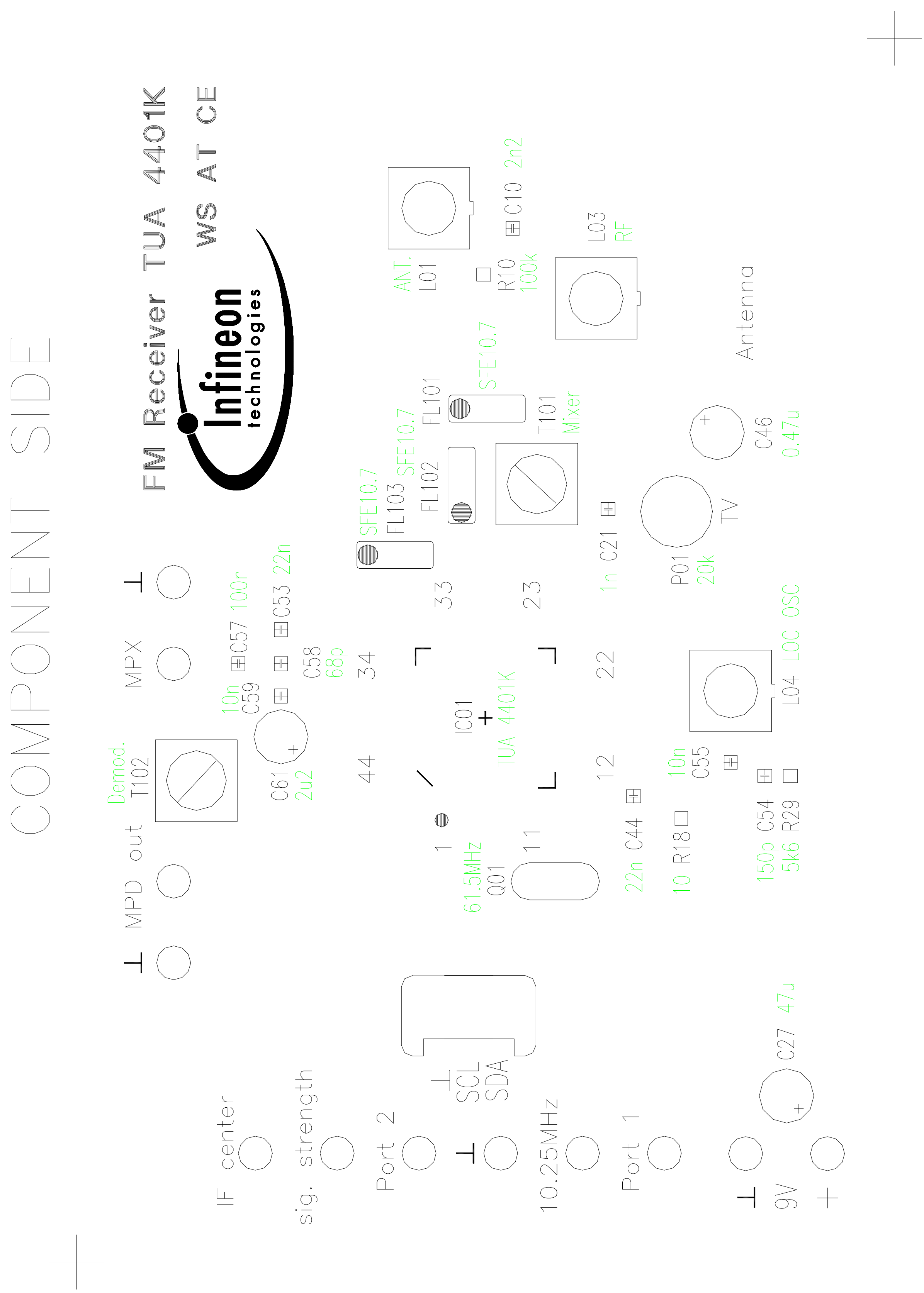
Enclosure:


VCCIF
IFAMPC
IFOUTFM
IFIN
IFINFM
GNDIF1
VREFRF
IF1
IF2
AGC_OUT_P
FM2
33
32
31
30
29
28
27
26
25
24
23
FMIFIN
34
FMIFBIAS
35
GNDIF2
36
MPXOUT
37
FSOUT
38
MPA_AIN
39
MPACAP
40
MPA_OUT
41
DEMAFC
42
PH02
43
PH01
44
22
FM1
21
PRE_CAP
20
VCCRF
19
OSC2
18
OSC1
17
GNDRF
16
PD_0
15
PDA
14
PORT_1
13
GNDD
12
VCCD
IF AMP
Vref
FM Lim / Dem /
FS / MP-Det
Mixer 1st LO
Preset AGC
PLL Synth.
Serial Bus
IF counter
ADC/DAC
Cryst
OSC
1
2
3
4
5
6
7
8
9
10
11
FS_ADC
MPA_ADC
IF_CENT
SCL
SDA
VREFD5V
VREFD3V
XTAL_DIV6
PORT_2
QUARTZ1
QUARTZ2


MP det out
Field-strength
MP det in
MP det.
MPX out
AfC loop Dem
FM IF limiter
Field strength
Gate time counter
7 Bit ADC
IF counter
Station_Detect
Clock counter
div/6
10.7 MHz CER Filter
IF amp gain adj.
adj crystal
4 bit DAC IF gain
R counter
Port
P2
P1
PD
Charge pump
Data Bus
2 bit DAC Prest. AGC thresh.
N counter
SOCCAR Bus
SDA
SCL
External
FM prest AGC
FM
OSC Buffer / Div 2
OSC 1. LO
Gate2
Pin Diode 1
MOS tetrode


carradio
+Vs
MPX out
signal strength
MPD out
station detect
SCL
SDA
WS LIN AE CE
28.10.99 4401K.DWG
Em
FM Receiver
IC01
TUA 4401K
mixer
Vref RF
LOC OSC
PDO
PD
MPD
AFC
demodulator
3V 5V
Vtun 106MHz
Port 1
+Vs
10.25MHz out
Port 2
Antenna input
Wireless Products


SO - SMD PARTS


COMPONENT SIDE
FM Receiver TUA 4401K
WS AT CE
ANT. L01
C10 2n2
R10 100k
L03 RF
Antenna
SFE10.7 FL101
T101 Mixer
C46 0.47u
SFE10.7 FL103
SFE10.7 FL102
1n C21
P01 20k
TV
MPX
C57 100n
C53 22n
10n C59
C58 68p
Demod. T102
C61 2u2
IC01 TUA 4401K
L04 LOC OSC
10n C55
MPD out
61.5MHz Q01
22n C44
10 R18
150p C54
5k6 R29
SCL
SDA
C27 47u
IF center
sig. strength
Port 2
10.25MHz
Port 1
9V

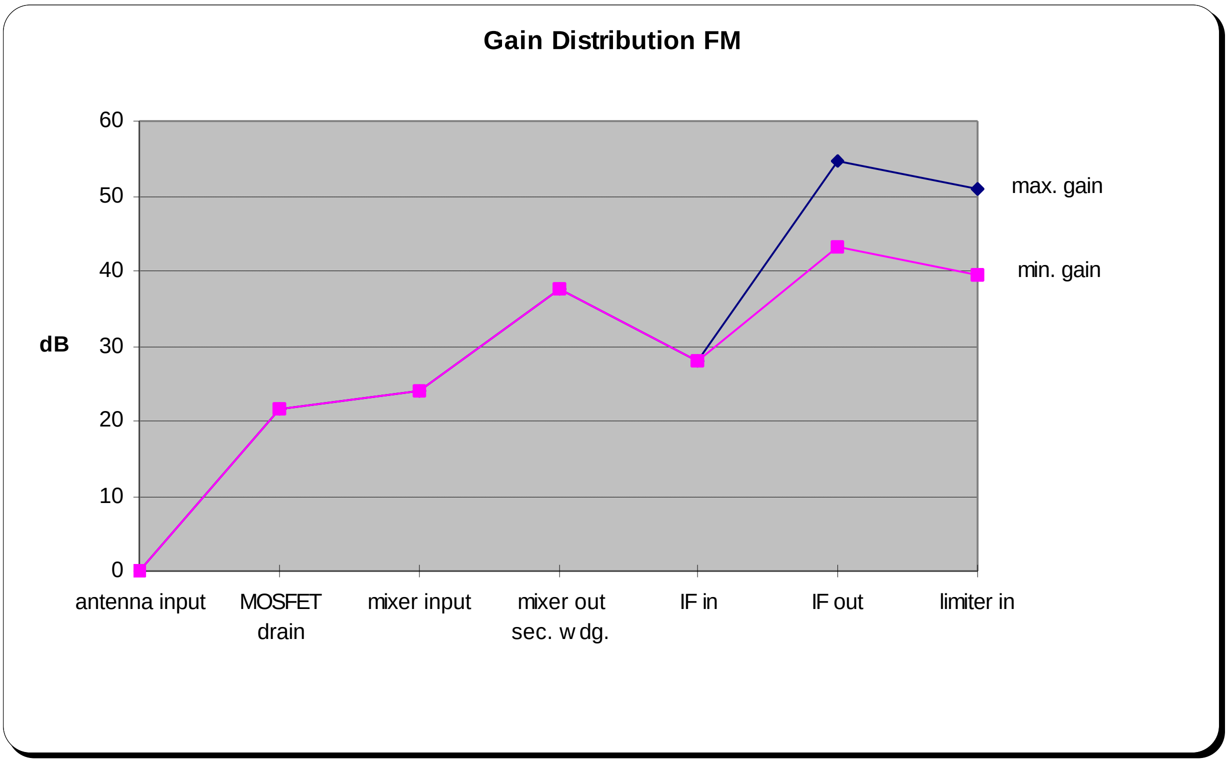
partlist for single chip receiver TUA 4401K

single chip receiver	IC01	TUA 4401K	Infineon
MOS tetrode	T01	BF1009S	Infineon
pindiode	D01	BA595	Infineon
varactor diode	VRAC1	BB914	Infineon
varactor diode	VRAC2	BB914	Infineon
varactor diode	VRAC3	BB914	Infineon
chip capacitor	C01	4p7	Siemens
chip capacitor	C02	15p	Siemens
chip capacitor	C03	1n	Siemens
chip capacitor	C04	1n	Siemens
chip capacitor	C05	10n	Siemens
chip capacitor	C06	1n	Siemens
chip capacitor	C07	27p	Siemens
chip capacitor	C08	15p	Siemens
chip capacitor	C09	1p5	Siemens
chip capacitor	C10	2n2	Siemens
chip capacitor	C11	1n	Siemens
chip capacitor	C13	22p	Siemens
chip capacitor	C14	15p	Siemens
chip capacitor	C15	10n	Siemens
chip capacitor	C16	1p	Siemens
chip capacitor	C21	1n	Siemens
chip capacitor	C22	47n	Siemens
chip capacitor	C23	470p	Siemens
chip capacitor	C24	470p	Siemens
chip capacitor	C26	22n	Siemens
chip capacitor	C28	47n	Siemens
chip capacitor	C29	47n	Siemens
chip capacitor	C37	47n	Siemens
chip capacitor	C42	1n	Siemens
chip capacitor	C44	22n	Siemens
chip capacitor	C45	22n	Siemens
chip capacitor	C47	47n	Siemens
chip capacitor	C48	47n	Siemens
chip capacitor	C53	22n	Siemens
chip capacitor	C54	270p	Siemens
chip capacitor	C55	10n	Siemens
chip capacitor	C57	100n	Siemens
chip capacitor	C58	68p	Siemens
chip capacitor	C59	10n	Siemens
chip capacitor	C62	82p	Siemens
chip capacitor	C63	47n	Siemens
chip capacitor	C64	100n	Siemens

chip resistor	R01	1k	Siemens
chip resistor	R02	10	Siemens
chip resistor	R03	47k	Siemens
chip resistor	R04	10	Siemens
chip resistor	R05	680	Siemens
chip resistor	R06	10k	Siemens
chip resistor	R07	47k	Siemens
chip resistor	R08	10k	Siemens
chip resistor	R09	56k	Siemens
chip resistor	R12	4k7	Siemens
chip resistor	R13	22k	Siemens
chip resistor	R14	22k	Siemens
chip resistor	R16	120k	Siemens
chip resistor	R17	10	Siemens
chip resistor	R19	2k7	Siemens
chip resistor	R21	3k9	Siemens
chip resistor	R22	10	Siemens
chip resistor	R23	10	Siemens
chip resistor	R24	820	Siemens
chip resistor	R25	47	Siemens
chip resistor	R26	22	Siemens
chip resistor	R27	22k	Siemens
chip resistor	R29	5k6	Siemens
chip resistor	R32	3k3	Siemens
chip resistor	R33	10k	Siemens
chip resistor	R34	10k	Siemens
chip resistor	R35	10k	Siemens
chip resistor	R36	47k	Siemens
chip resistor	R37	47k	Siemens
variable resistor	P01	20k	
elco	C27	47u	
elco	C46	0.47u	
elco	C61	2u2	

choke coil	L02	2u2	SIMID04	Siemens
RF input coil	L01	E528SNAS-100076		Toko
RF coil	L03	E528SNAS-100076		Toko
LOC OSC	L04	E528SNAS-100075		Toko
mixer transformer	T101	218FCS-2166N		Toko
demodulator	T102	600BNS-A1004HM		Toko
ceramic filter	FL101	SFE10.7MS3-A		Murata
		or: SK107M3-AE-20		Toko
ceramic filter	FL102	SFE10.7MS3-A		Murata
		or: SK107M3-AE-20		Toko
ceramic filter	FL103	SFE10.7MS3-A		Murata
		or: SK107M3-AE-20		Toko
crystal resonator	Q01	61.5MHz		e.g. Telequarz

FM (f_{in} = 95.2 MHz; V_G = 100 µV)



TUA 4401K - Software-Help

Enclosed to the application board you will find the PLL software and the connector cable. The software runs on Windows® 3.1, 95, and 98.

The attached cable connects the personal computer (desktop or laptop) via the parallelport with the application board.

The software may be started directly from the diskette with the *.exe file. The additional 4401K.car file includes all settings which are necessary to bring the receiver into a first normal mode. So it is recommended to load this file after starting the *.exe file. In the first window “System” via <Load Setup...> the 4401K.car should be activated. In the window “IC Prog.” in the field “Send sequence” with the button <Initialize> all pre-settings are transferred.

For special settings additional files may be saved on the disc.

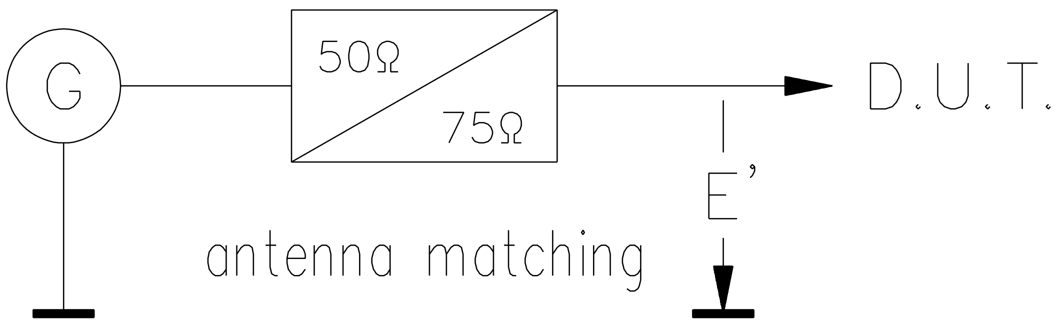
Important:

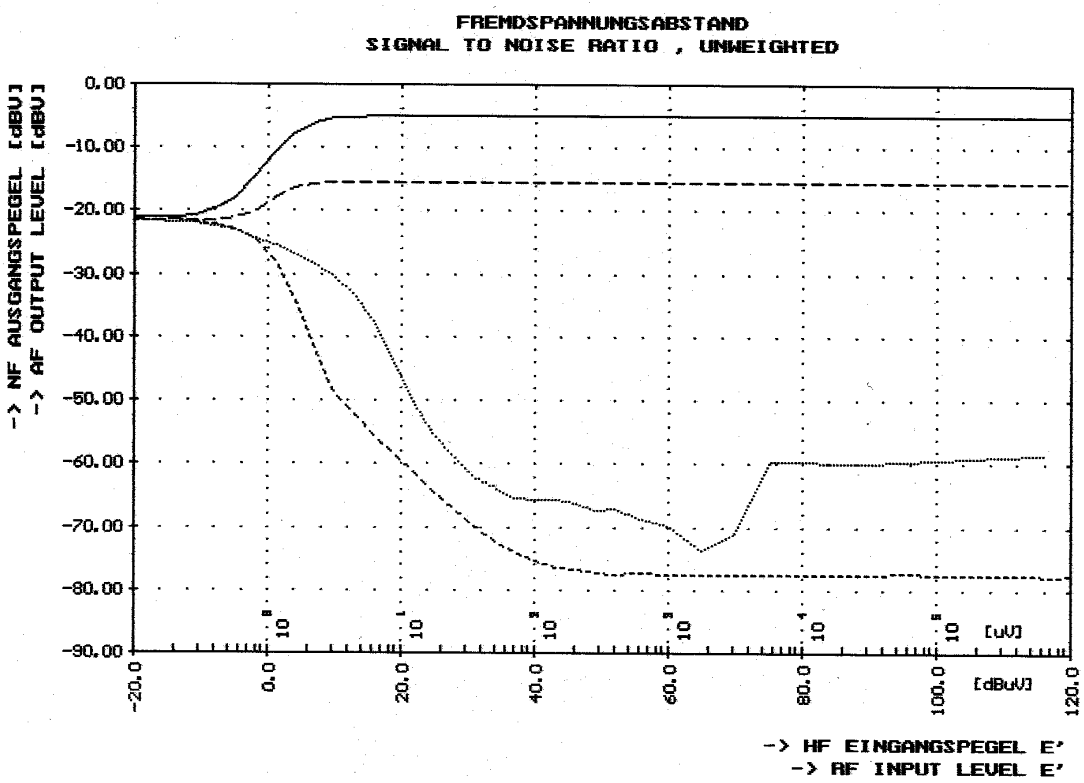
In a self written control software it is necessary at the very first time to transfer all bytes (bits) of the complete IC protocol, first initialisation. Hereby the useful bits may be set to ‘0’ or ‘1’ and the not used bits to ‘0’.

For further settings only the byte which has to be exchanged has to be transferred by sending the corresponding subaddress.

For every datatransfer START and STOP conditions are necessary (in I^2C mode and 3 wire mode).

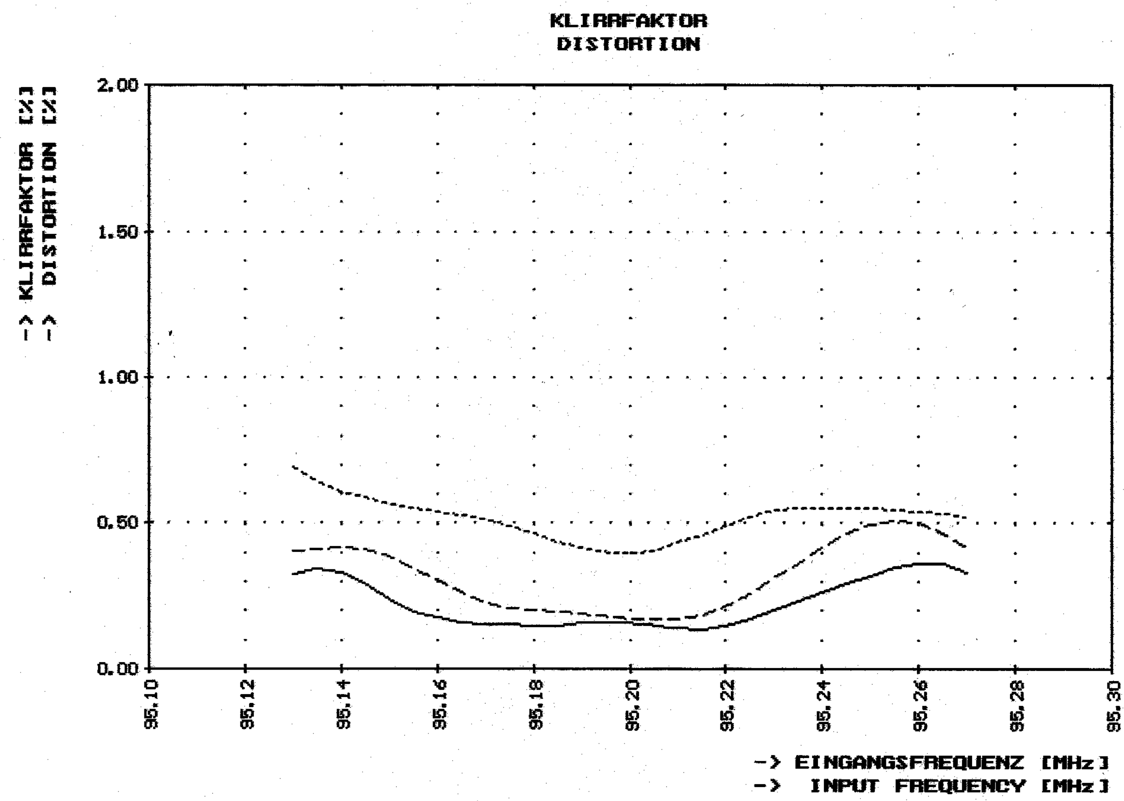
All measurements in the FM mode were done with the antenna matching adapter as shown in the following figure. The RF level in the measurement diagrams is identical with E' in the schematic diagram below. E' is the RF level at the open antenna plug.





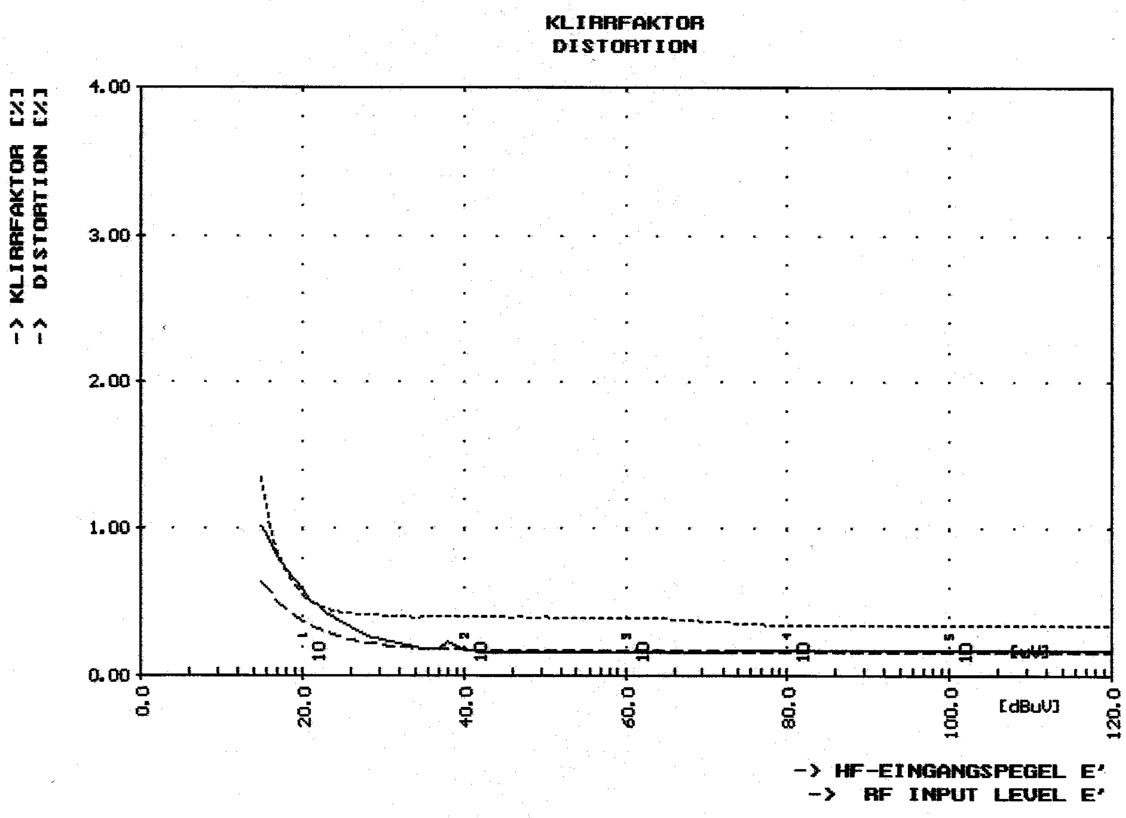
Vs =	8.5 V	±75.0 kHz	————
fmod=	1.0 kHz	±22.5 kHz	– – – –
f =	95.2 MHz	NOISE	- - - -
m =	80.0 %	AM SUPPR.	········
ΔMax=	72.646 dB		

measured with ext. 50us deemphasis



Us =	8.5 V	±22.5 kHz	————————
fmod=	1.0 kHz	±40.0 kHz	– – – – – – – –
E' =	1.0 mV	±75.0 kHz	- - - - - - - - - - - -

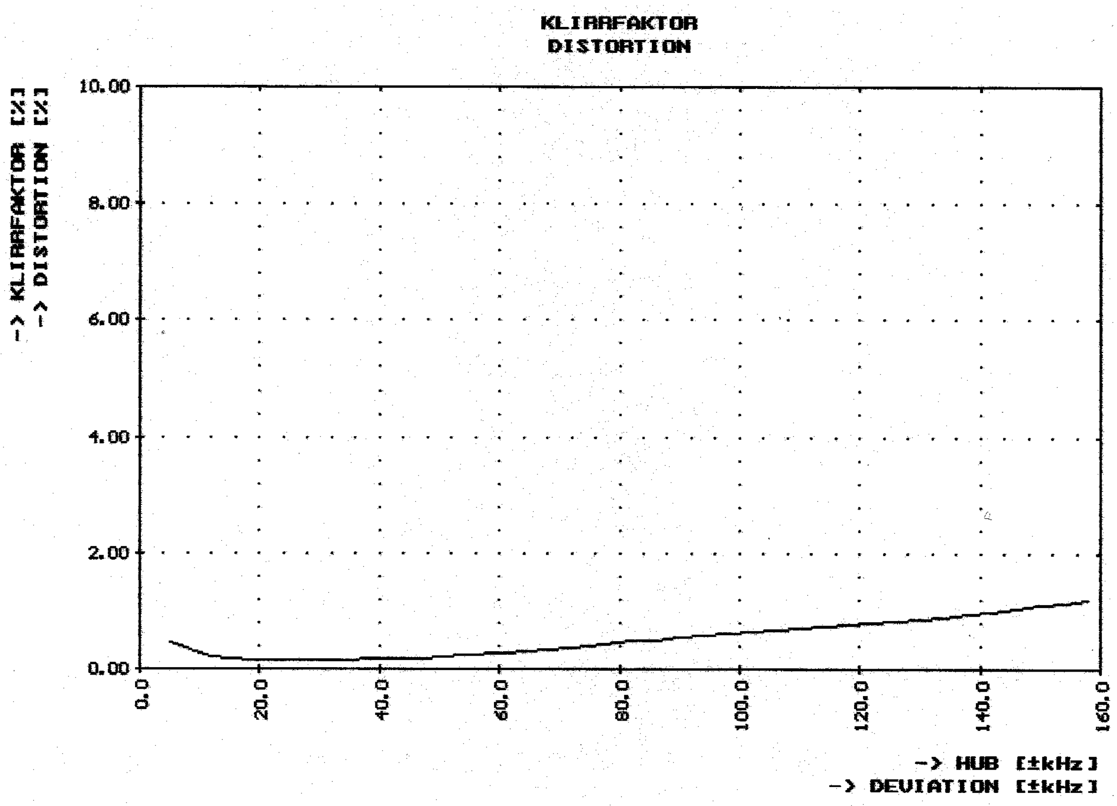
measured with ext. 50us deemphasis



Us = 8.5 V
fmod= 1.00 kHz
f = 95.2 MHz

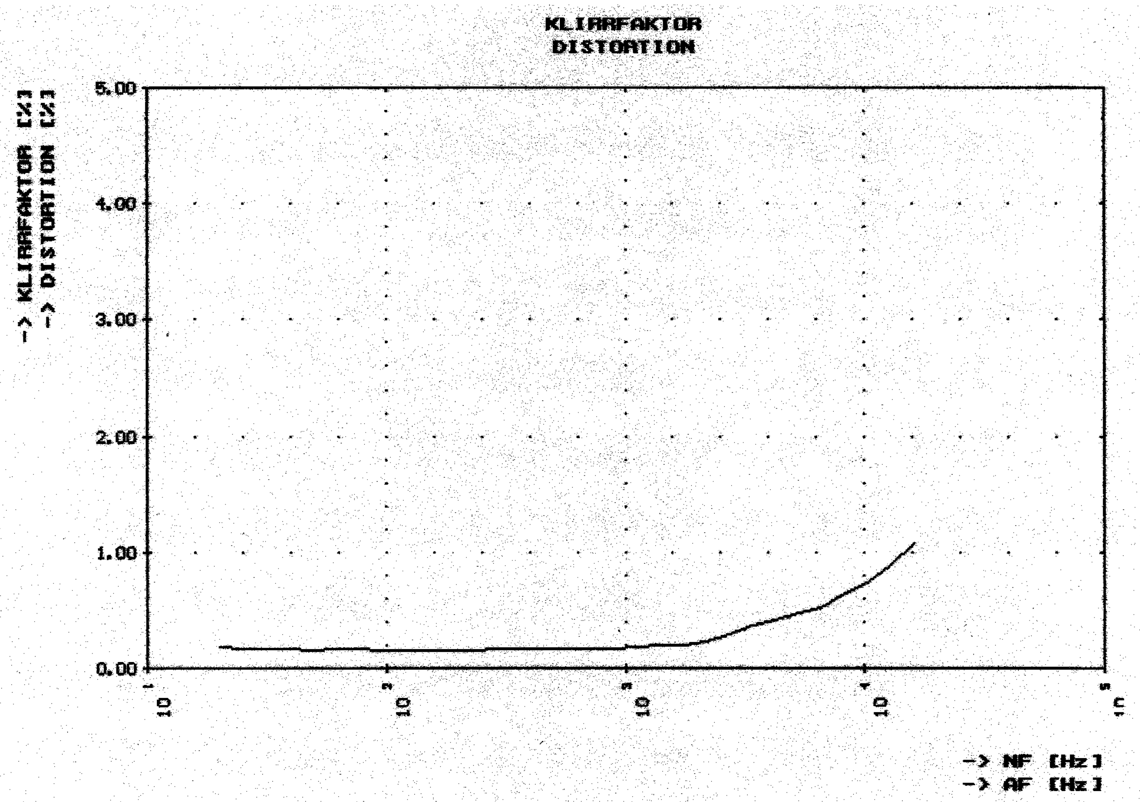
±22.5 kHz ————————
±40.0 kHz – – – – – – – –
±75.0 kHz - - - - - - - - - - -

measured with ext. 50us deemphasis



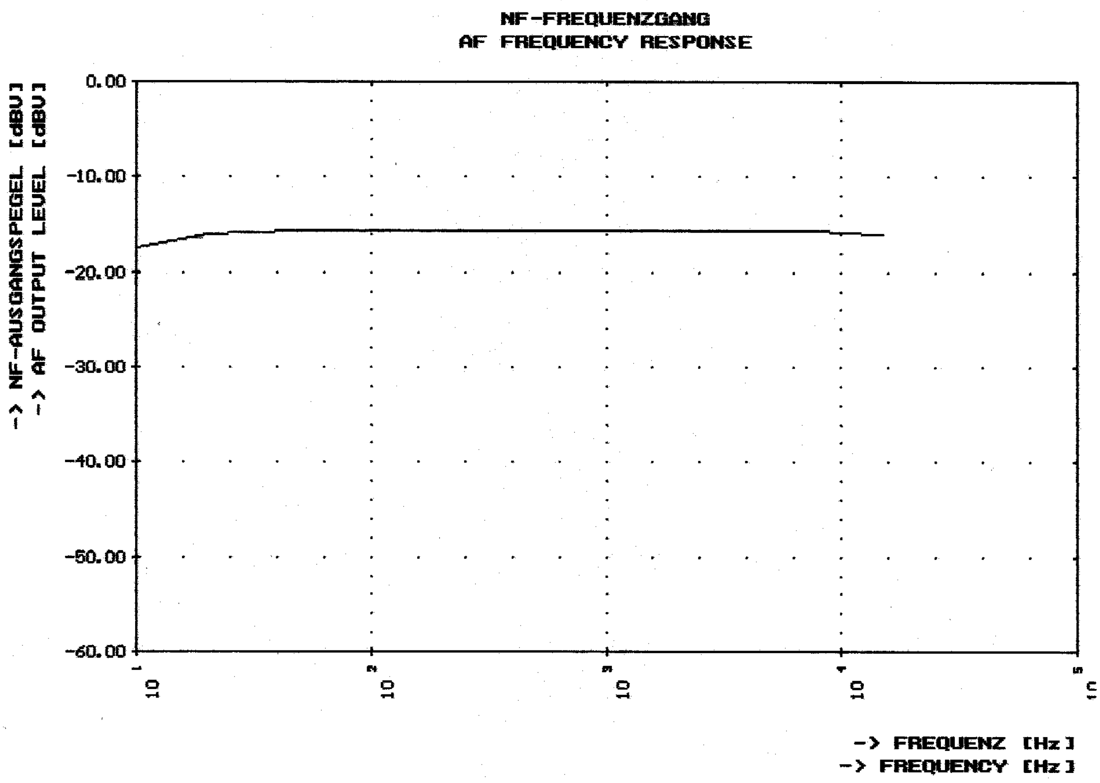
Us = 8.5 V
f = 95.2 MHz
E' = 1.0 mV
fmod= 1.00 kHz

measured with ext. 50us deemphasis



Vs = 8.5 V
f = 95.2 MHz
E' = 1.0 mV
Dev = ±22.5 kHz

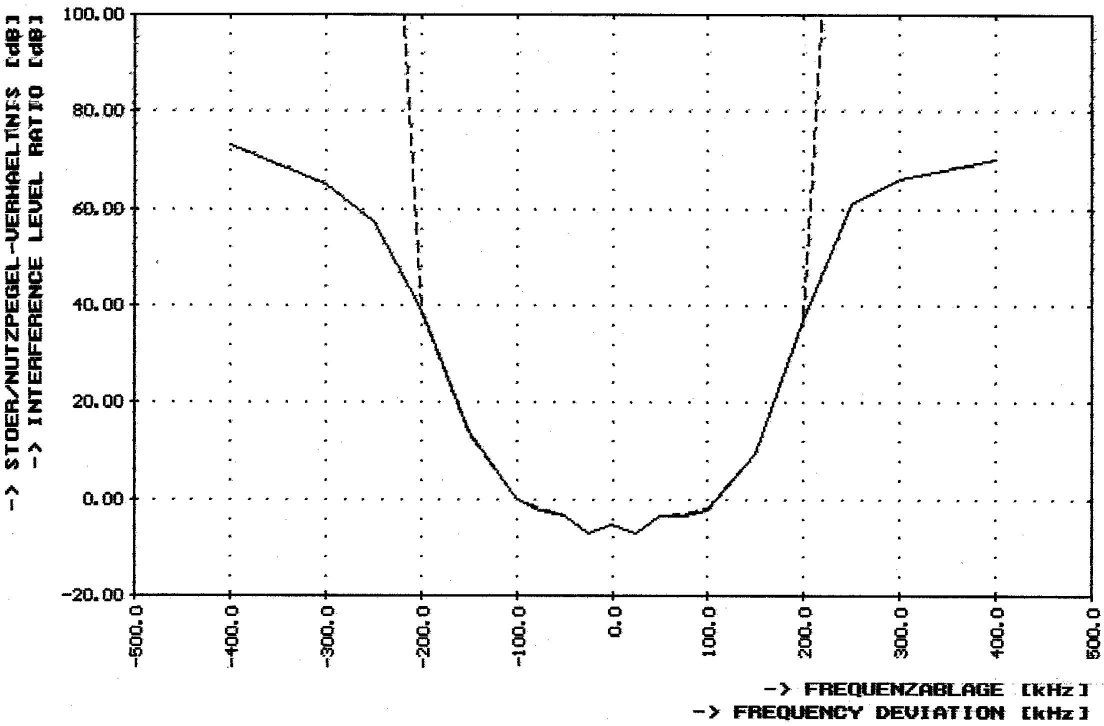
measured with ext. 50us deemphasis



Vs = 8.5 V
f = 95.2 MHz
Dev = ±22.5 kHz
E' = 1.0 mV
Preem= 50.0 µs

measured with ext. 50us deemphasis

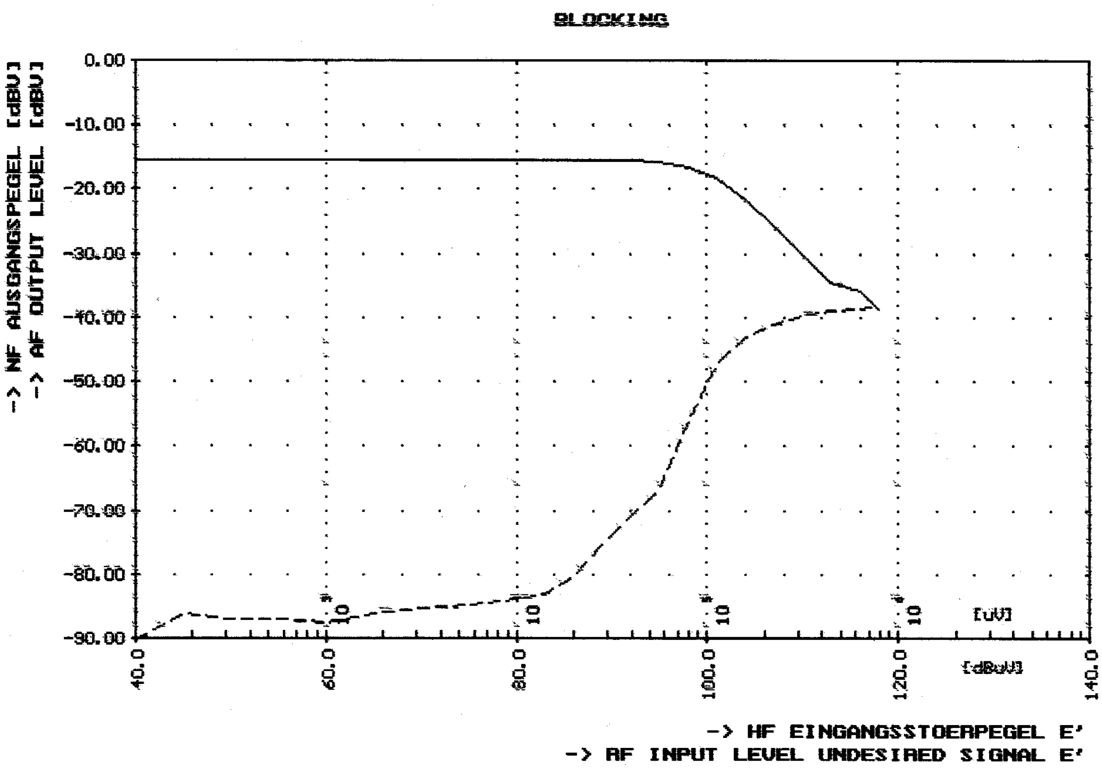
DYNAMISCHE SELEKTION
DYNAMIC SELECTION



Vs = 8.5 V
fmod= 1.0 kHz
f = 95.2 MHz
Dev = ±40.0 kHz
a = 30.0 dB
E'1 = 10.0 µV
E'2 = 1000.0 µV

DESIRED SIG. 1 ————————
DESIRED SIG. 2 - - - - - - - -

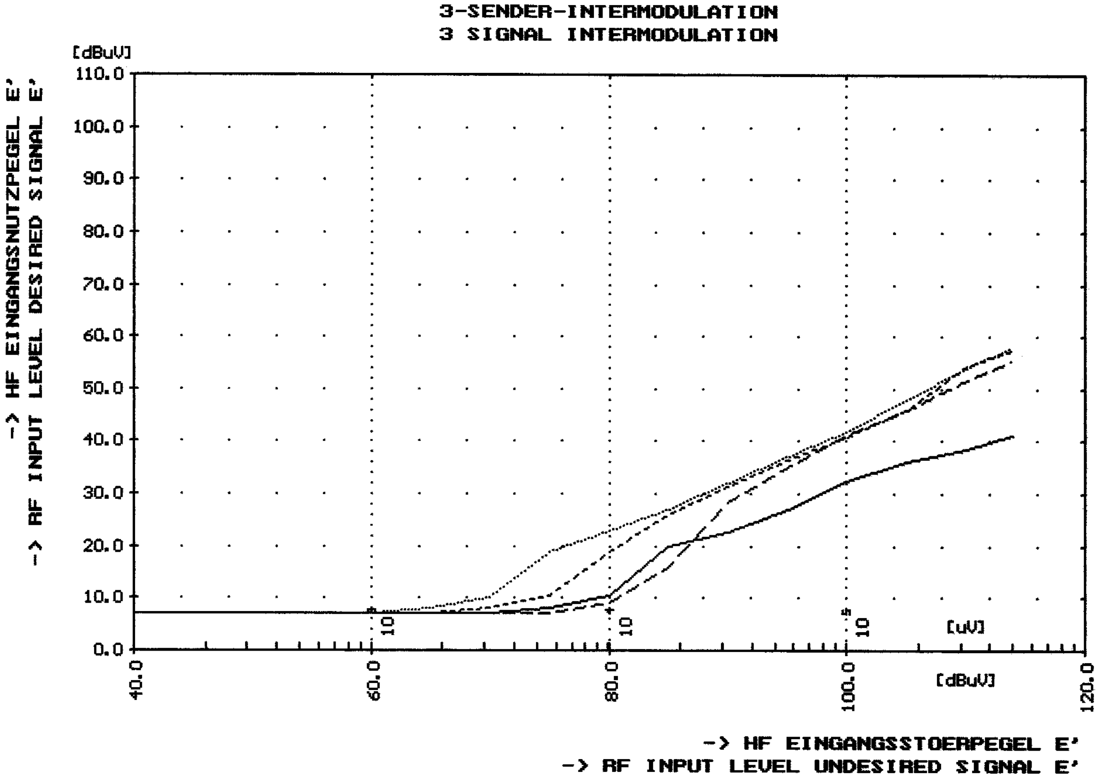
measured with ext. 50us deemphasis



Us = 8.5 V
fmod= 1.0 kHz
Dev = ±22.5 kHz
f = 95.550 MHz undesired
f = 95.200 MHz desired
E' = 20 µV desired
Audio Bandpass 1kHz

±22.5 kHz ————————
NOISE - - - - - - - - -

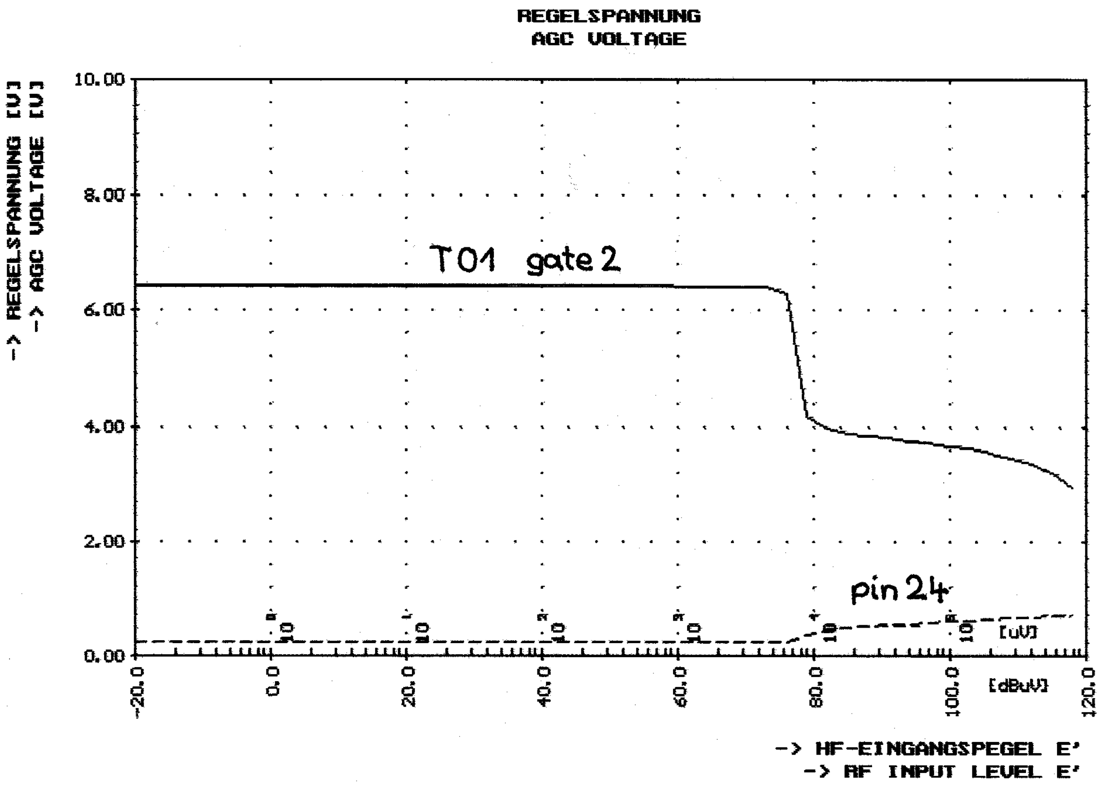
measured with ext. 50us deemphasis



Vs = 8.5 V
f = 95.20 MHz
fmod= 1.0 kHz
Dev = ±22.5 kHz
Reference THD -30dB

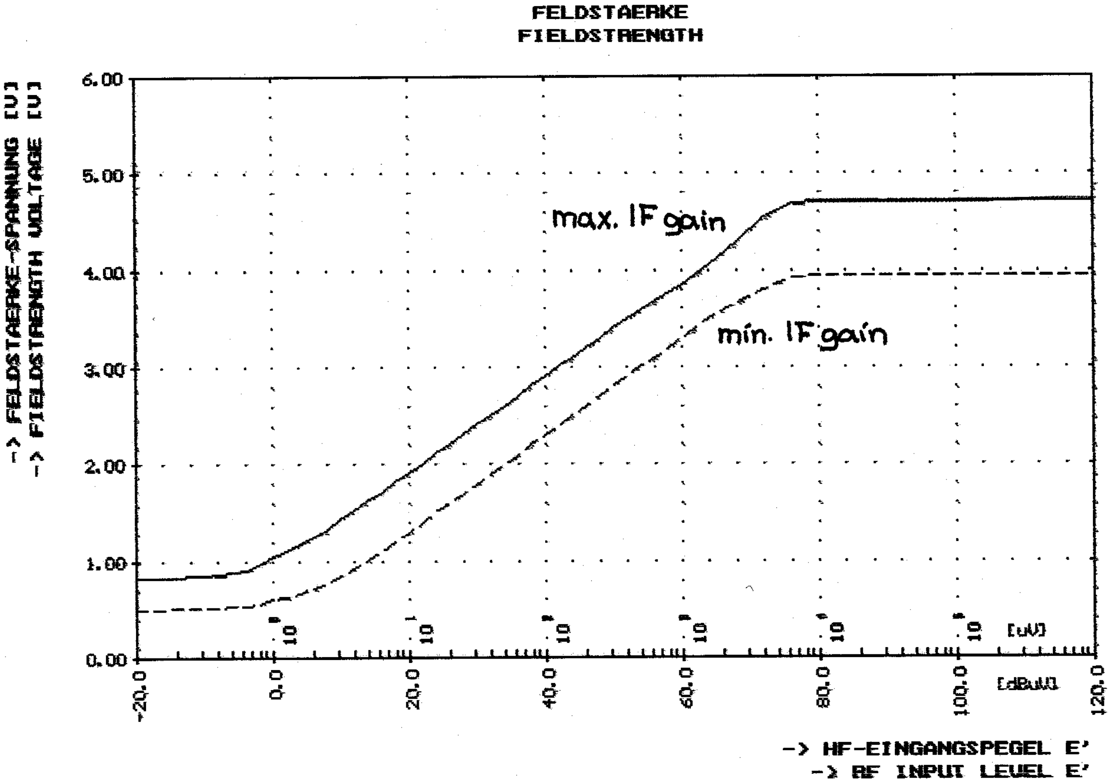
+2.0/+4.0MHz ————
-2.0/-4.0MHz – – – –
-0.8/-1.6MHz - - - -
+0.8/+1.6MHz ....

measured with ext. 50us deemphasis



Vs = 8.5 V

f = 95.200 MHz



Vs = 8.5 V

f = 95.2 MHz

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