# TMP117x High-Accuracy, Low-Power, Digital Temperature Sensor With SMBus™- and I²C-Compatible Interface

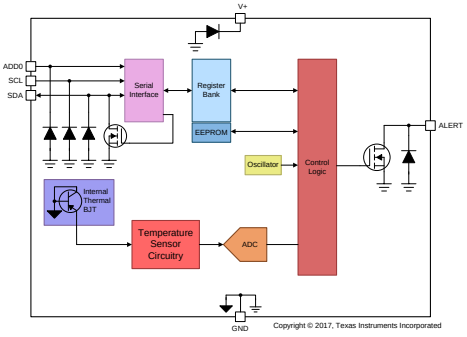
## 1 Features

- TMP117 High Accuracy Temperature Sensor
  - ±0.1°C (Maximum) From 25°C to +50°C
  - ±0.2°C (Maximum) From –40°C to +125°C
  - ±0.3°C (Maximum) From –55°C to +150°C
- TMP117M Medical Temperature Sensor
  - ±0.1°C (Maximum) From 30°C to +45°C
- TMP117N Industrial Temperature Sensor
  - ±0.2°C (Maximum) From –40°C to +125°C
- Temperature Operating Range: –55°C to +150°C
- Low Power Consumption:
  - 3.5-µA, 1-Hz Conversion Cycle
  - 250-nA Shutdown Current
- Supply Range: 1.8 V to 5.5 V
- 16-Bit Resolution: 0.0078°C (1 LSB)
- Programmable Temperature Alert Limits
- Digital Offset for System Correction
- General-Purpose EEPROM: 48 Bits
- NIST Traceability
- SMBus™, I²C Interface Compatibility

## 2 Applications

- Medical Grade: Meets ASTM E1112 and ISO 80601-2-56
- Environmental Monitoring and Thermostats
- Wearables
- Asset Tracking and Cold Chain
- Gas Meters and Heat Meters
- Test and Measurement
- RTDs Replacement: PT100, PT500, PT1000
- Cold-Junction Compensation of Thermocouples

### Functional Block Diagram




## 3 Description

The TMP117 is a high-precision digital temperature sensor. It is designed to exceed ASTM E1112 requirements for electronic patient thermometers. The TMP117 provides a 16-bit temperature result with a resolution of 0.0078°C and an accuracy of up to ±0.1°C across the temperature range of 25°C to 50°C with no calibration. The TMP117 is I²C- and SMBus™-interface compatible, has programmable alert functionality, and can support up to four devices on a single bus. Integrated EEPROM is included for device programming with an additional 48-bits memory available for general use.

The low power consumption of the TMP117 minimizes the impact of self-heating on measurement accuracy. The TMP117 operates from 1.8 V to 5.5 V and typically consumes 3.5 µA.

For non-medical applications, the TMP117 can serve as a single chip digital alternative to a Platinum RTD. With an accuracy of ±0.2°C accuracy from –55°C to 150°C, the TMP117 offers comparable if not better accuracy than can be achieved with a Class A RTD, while only using a fraction of the power of the power typically needed for a PT100 RTD. The TMP117 simplifies the design effort by removing many of the complexities of RTDs such as precision references, matched traces, complicated algorithms, and calibration.

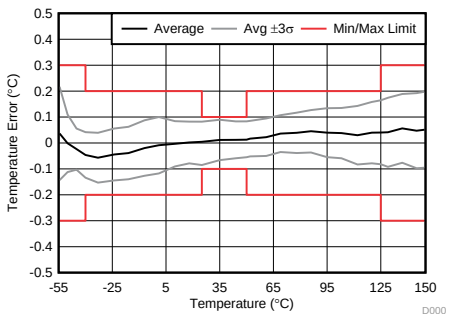
The TMP117 units are 100% tested on a production setup that is NIST traceable and verified with equipment that is calibrated to ISO/IEC 17025 accredited standards.

### Device Information(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TMP117 | WSON (6) | 2.00 mm × 2.00 mm |
| | DSBGA (6) | 1.00 mm × 1.60 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

### Temperature Accuracy

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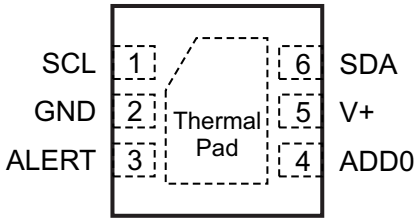
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

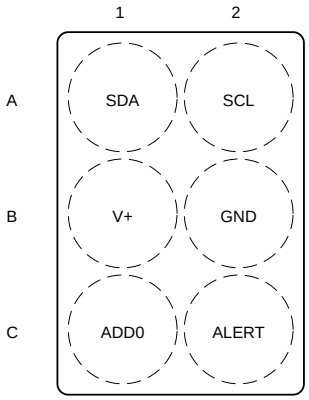
| DATE | REVISION | NOTES |
|---|---|---|
| June 2018 | * | Initial release. |

# 5 Pin Configuration and Functions

**DRV Package**
**6-Pin WSON**
**Top View**




**YFF Package**
**6-Pin DSBGA**
**Top View**




Not to scale

**Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | WSON | DSBGA | | |
| ADD0 | 4 | C1 | I | Address select. Connect to GND, V+, SDA, or SCL. |
| ALERT | 3 | C2 | O | Overtemperature alert or data-ready signal. Open-drain output; requires a pullup resistor. |
| GND | 2 | B2 | — | Ground |
| SCL | 1 | A2 | I | Serial clock |
| SDA | 6 | A1 | I/O | Serial data. Open-drain output; requires a pullup resistor. |
| V+ | 5 | B1 | I | Supply voltage: 1.8 V to 5.5 V |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | V+ | –0.3 | 6 | V |
| Voltage at | SCL, SDA, ALERT and ADD0 | –0.3 | 6 | V |
| Operating junction temperature, $T_J$ | | –55 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| V+ | Supply voltage | 1.8 | 3.3 | 5.5 | V |
| $T_A$ | Operating free-air temperature | –55 | | 150 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TMP116 DRV (WSON) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 68.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 70.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 9.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 38.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 38.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

minimum and maximum specifications are over -55°C to 150°C and V+ = 1.8 V to 5.5 V (unless otherwise noted); typical specifications are at $T_A$ = 25°C and V+ = 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TEMPERATURE TO DIGITAL CONVERTER** | | | | | | |
| Temperature accuracy(1) | TMP117M | 30°C to 45°C | -0.1 | ±0.05 | 0.1 | °C |
| | | 0°C to 85°C | -0.2 | ±0.1 | 0.2 | |
| | TMP117 | 25°C to 50°C | -0.1 | ±0.05 | 0.1 | |
| | | -55°C to 150°C | -0.2 | ±0.1 | 0.2 | |
| | TMP117N | -55°C to 150°C | -0.2 | ±0.1 | 0.2 | |
| DC power supply sensitivity | | One-shot mode, 8 Averages, $T_A$ = +25°C | | | 10 | m°C/V |
| Temperature resolution (LSB) | | | | 7.8125 | | m°C |
| Repeatability(2) | | (1) | | ±1 | | LSB |
| Long-term stability and drift | | 300 hours at 150°C(3) | | ±0.02 | | °C |

(1) V+ = 3.3 V, 8 Averages, 1Hz sampling
(2) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(3) Long term stability is determined using accelerated operational life testing at a junction temperature of 150°C.

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## Electrical Characteristics (continued)

minimum and maximum specifications are over -55°C to 150°C and V+ = 1.8 V to 5.5 V (unless otherwise noted); typical specifications are at $T_A$ = 25°C and V+ = 3.3 V.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Temperature cycling and hysteresis(4) | | 8 Averages | | ±1 | | LSB |
| **DIGITAL INPUT/OUTPUT** | | | | | | | |
| | Input capacitance | | | | 4 | | pF |
| $V_{IH}$ | Input logic high level | | | 0.7 (V+) | | | V |
| $V_{IL}$ | Input logic low level | | | | | 0.3 (V+) | V |
| $I_{IN}$ | Input current | | | -0.1 | | 0.1 | µA |
| $V_{OL}S$ | SDA output logic low level | | $I_{OL}$ = -3 mA | 0 | | 0.4 | V |
| $V_{OL}A$ | $\overline{\text{ALERT}}$ output logic low level | | $I_{OL}$ = -3 mA | 0 | | 0.4 | V |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current | | Active Conversion, serial bus inactive | | 135 | 220 | µA |
| $I_Q$ | Quiescent current | | Duty cycle 1 Hz, averaging mode off, serial bus inactive | | 3.5 | 4.5 | µA |
| | | | Duty cycle 1 Hz, 8 avgerages mode, serial bus inactive | | 16 | 22 | |
| | | | Duty cycle 1 Hz, averaging mode off, serial bus active, SCL frequency = 400 kHz | | 15 | | |
| $I_{SB}$ | Stanby current(5) | | Serial bus inactive, SCL and SDA = V+ | | 1.25 | 2.1 | µA |
| $I_{SD}$ | Shutdown current | | Serial bus inactive, SCL and SDA = V+, 25°C | | 0.15 | 0.5 | µA |
| | | | Serial bus inactive, SCL and SDA = V+, 125°C | | | 4 | µA |
| | | | Serial bus active, SCL frequency = 400 kHz | | 17 | | µA |
| $I_{EE}$ | EEPROM write quiescent current | | ADC conversion off; serial bus inactive | | 240 | | µA |
| $V_{POR}$ | Power-on-reset threshold voltage | | Supply going up | | 1.6 | | V |
| | Brownout detect | | Supply going down | | 1.1 | | V |
| | Reset Time | | Time required by device to reset | | 1.5 | | ms |
| | Conversion time | | One-shot mode | 13.5 | 15.5 | 17 | ms |

(4) Hysteresis is defined as the ability to reproduce a temperature reading as the temperature varies from room → hot →room→cold→room. The temperatures used for this test are -40°C, 25°C, and 150°C.
(5) Quiescent current between conversions

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## 6.6 Switching Characteristics

minimum and maximum specifications are over -55°C to 150°C and V+ = 1.8 V to 5.5 V (unless otherwise noted) typical specifications are at $T_A$ = 25°C and V+ = 3.3 V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **EEPROM** | | | | | |
| Programming time | | | 7 | | ms |
| Number of writes | | 1,000 | 50,000 | | Times |
| Data retention time | | 10 | 100 | | Years |

## 6.7 Two-Wire Interface Timing

minimum and maximum specifications are over –55°C to 150°C and V+ = 1.8 V to 5.5 V (unless otherwise noted)(1)

| | | FAST-MODE | | |
|---|---|---|---|---|
| | | MIN | MAX | UNIT |
| $f_{SCL}$ | SCL operating frequency | 1 | 400 | KHz |
| $t_{BUF}$ | Bus free time between STOP and START conditions | 1300 | | ns |
| $t_{HD;STA}$ | Hold time after repeated STRAT condition. After this period, the first clock is generated(2) | 600 | | ns |
| $t_{SU;STA}$ | Repeated START condition setup time | 600 | | ns |
| $t_{SU;STO}$ | STOP condition setup time | 600 | | ns |
| $t_{HD;DAT}$ | Data hold time | 0 | | ns |
| $t_{VD;DAT}$ | Data valid time(3) | | 0.9 | µs |
| $t_{SU;DAT}$ | Data setup time | 100 | | ns |
| $t_{LOW}$ | SCL clock low period | 1300 | | ns |
| $t_{HIGH}$ | SCL clock high period | 600 | | ns |
| $t_F$ – SDA | Data fall time | 20 × (V+ /5.5) | 300 | ns |
| $t_F$, $t_R$ – SCL | Clock fall and rise time | | 300 | ns |
| $t_R$ | Rise time for SCL ≤ 100 kHz | | 1000 | ns |
| | Serial bus timeout (SDA bus released if there is no clock) | 20 | 40 | ms |

(1) The master and device have the same V+ value. Values are based on statistical analysis of samples tested during initial release.
(2) The maximum $t_{HD;DAT}$ could be 0.9 µs for Fast-Mode, and is less than the maximum $t_{VD;DAT}$ by a transition time.
(3) $t_{VD;DATA}$ = time for data signal from SCL "LOW" to SDA output ("HIGH" to "LOW", depending on which is worse).

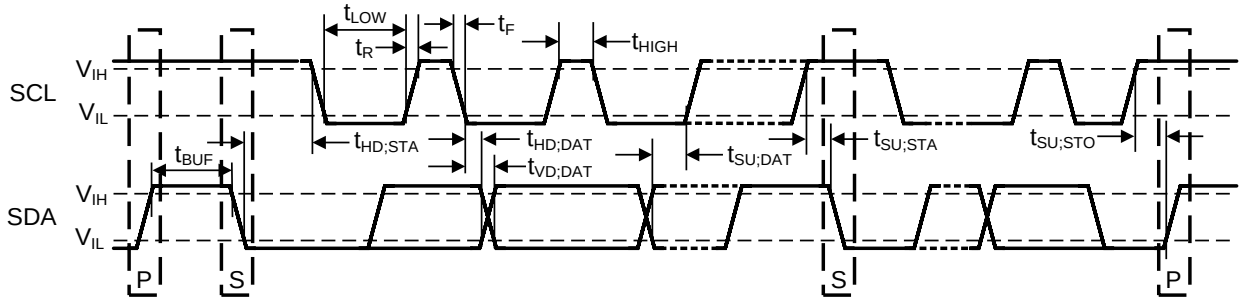


**Figure 1. Two-Wire Timing Diagram**

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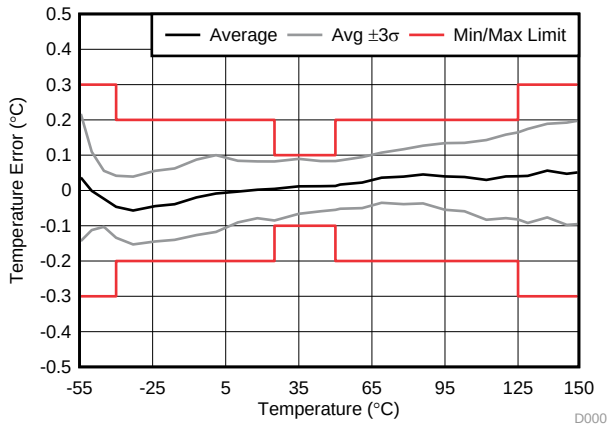
## 6.8 Typical Characteristics

at $T_A$ = 25°C, V+ = 3.3 V, and measurement taken in oil bath (unless otherwise noted)




1-Hz conversion cycle, 8 averages mode

**Figure 2. Temperature Error vs Temperature**

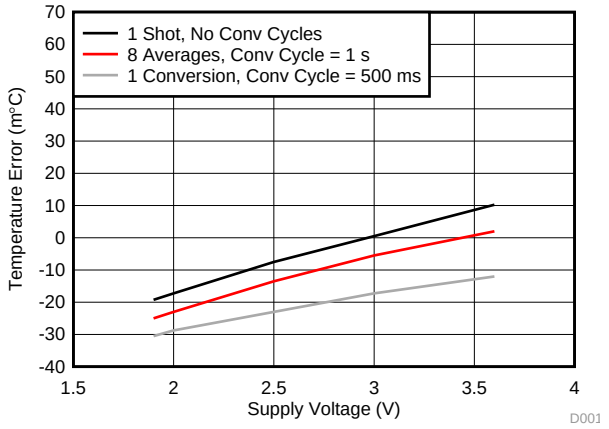
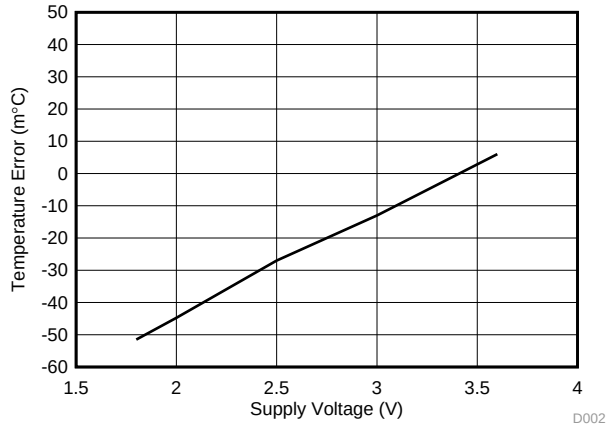



**Figure 3. Temperature Error vs Supply Voltage**




Continuous conversion, no conversion cycle in still air

**Figure 4. Temperature Error vs Supply Voltage**

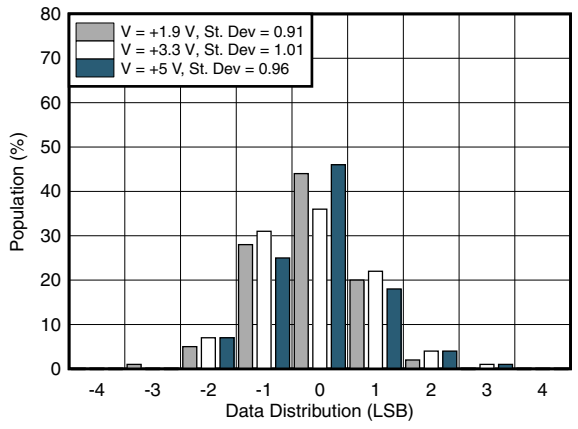



**Figure 5. Data Reading Distribution Over Supply Voltage (No Averaging)**

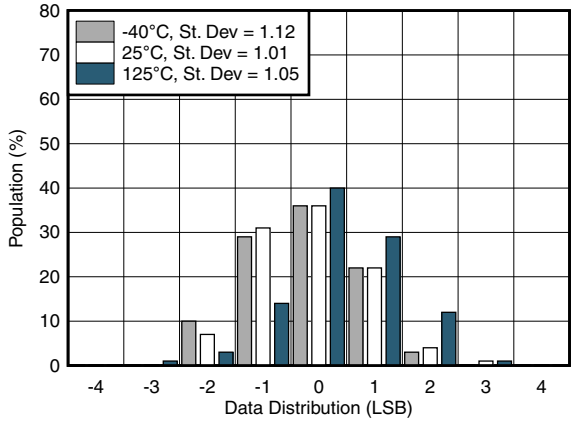
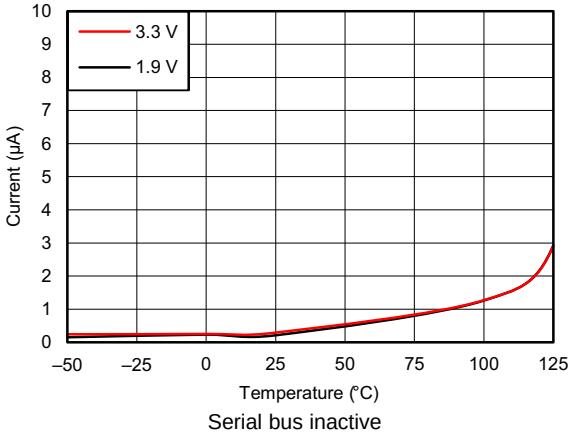



**Figure 6. Data Reading Distribution Over Temperature (No Averaging)**




Serial bus inactive

**Figure 7. Quiescent Current in Shutdown Mode**

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## Typical Characteristics (continued)

at $T_A$ = 25°C, V+ = 3.3 V, and measurement taken in oil bath (unless otherwise noted)

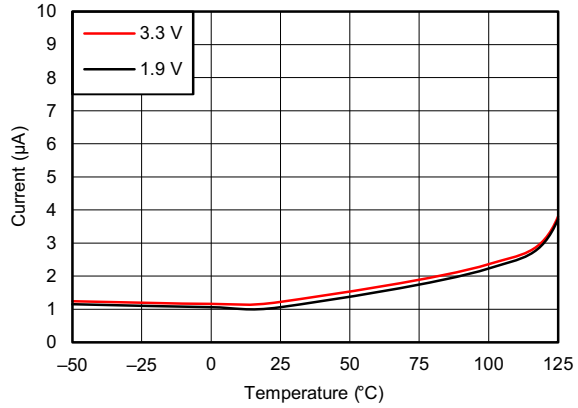


**Figure 8. Quiescent Current in Standby Mode**

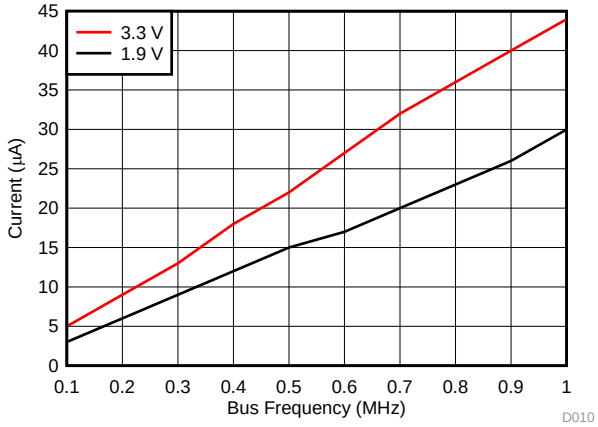


**Figure 9. Quiescent Current in Shutdown Mode**

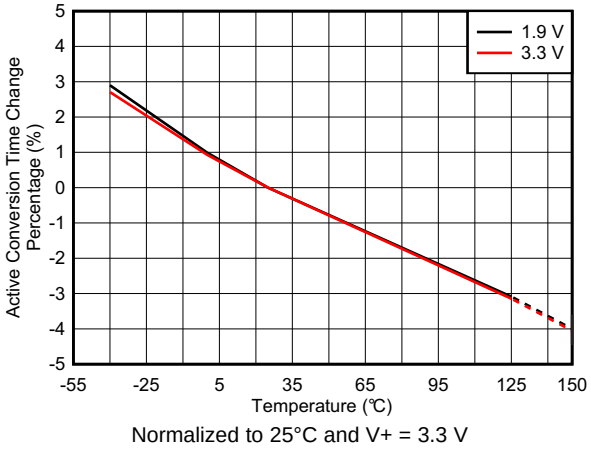


**Figure 10. Active Conversion Time vs Temperature**

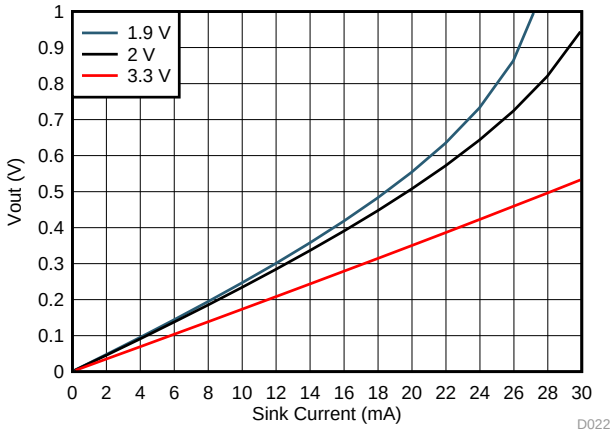


**Figure 11. ALERT Pin Output Voltage vs Pin Sink Current**

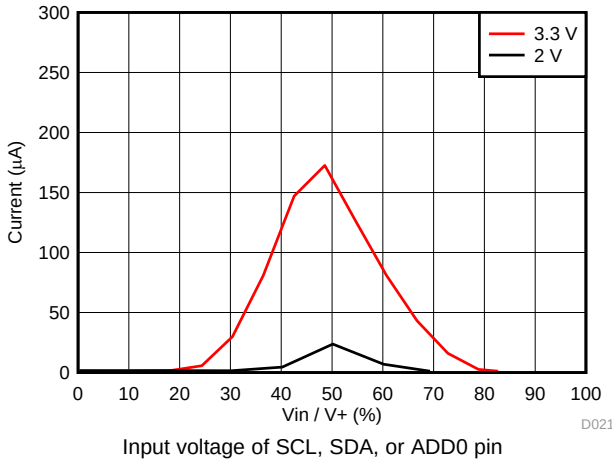


**Figure 12. Supply Current vs Input Cell Voltage**

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# 7 Detailed Description

## 7.1 Overview

The TMP117 is a digital output temperature sensor that is optimal for thermal-management and thermal-protection applications. The TMP117 is two-wire, SMBus, and $I^2C$ interface-compatible. The device is specified over an operating temperature range of –55°C to +125°C. Figure 13 shows a block diagram of the TMP117.

## 7.2 Functional Block Diagrams

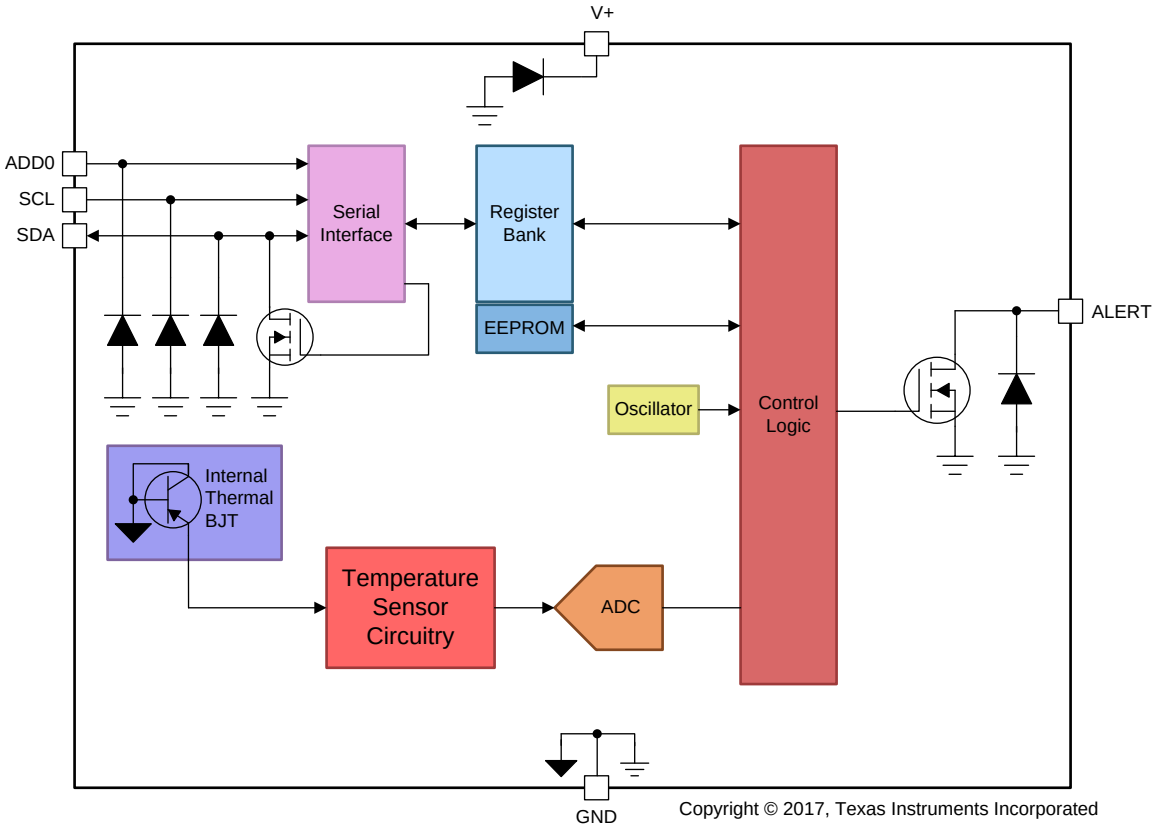


**Figure 13. Internal Block Diagram**

## 7.3 Feature Description

### 7.3.1 Power Up

After the supply voltage reaches within the operating range, the device requires 1.5 ms to power up before conversions begin. The device can be programmed to start up in shutdown mode as well. See the *EEPROM Programming* section for more information. The temperature register reads –256°C before the first conversion.

### 7.3.2 Temperature Result and Limits

At the end of every conversion, the device updates the temperature register with the conversion result. The data reading in the result register is in two's complement format, has a data width of 16 bits, and a resolution of 7.8125 m°C. Table 1 shows multiple examples of possible binary data that can be read from the temperature result register and the corresponding hexadecimal and decimal equivalents.

The TMP117 also has alert status flags and alert pin functionality that use the temperature limits stored in the low limit register and high limit register. The same data format used for the temperature result register can be used for data that are written to the high and low limit registers.

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## Feature Description (continued)

**Table 1. 16-Bit Temperature Data Format**

| TEMPERATURE (°C) | TEMPERATURE REGISTER VALUE (0.0078125°C RESOLUTION) | |
|---|---|---|
| | BINARY | HEX |
| –256 | 1000 0000 0000 0000 | 8000 |
| –25 | 1111 0011 1000 0000 | F380 |
| –0.1250 | 1111 1111 1111 0000 | FFF0 |
| –0.0078125 | 1111 1111 1111 1111 | FFFF |
| 0 | 0000 0000 0000 0000 | 0000 |
| 0.0078125 | 0000 0000 0000 0001 | 0001 |
| 0.1250 | 0000 0000 0001 0000 | 0010 |
| 1 | 0000 0000 1000 0000 | 0080 |
| 25 | 0000 1100 1000 0000 | 0C80 |
| 100 | 0011 0010 0000 0000 | 3200 |
| 255.9921 | 0111 1111 1111 1111 | 7FFF |

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## 7.4 Device Functional Modes

### 7.4.1 Temperature Conversions

The TMP117 can be configured to operate in various conversion modes by using the MOD[1:0] bits. These modes provide flexibility to operate the device in the most power efficient way necessary for the intended application.

#### *7.4.1.1 Conversion Cycle*

When the device is operating in continuous conversion mode (see the *Continuous Conversion Mode (CC)* section), every conversion cycle consists of an active conversion period followed by a standby period. The device typically consumes 135 µA during active conversion, and the device typically consumes 1.25 µA during the low-power standby period, as indicated in Table 1. Figure 14 shows a representative current consumption profile of a conversion cycle. The duration of the active conversion period and standby period can be configured using the CONV[2:0] and AVG[1:0] bits in the configuration register, thereby allowing the average current consumption of the device to be optimized based on the application requirements. Changing the conversion cycle period also affects the temperature result update rate because the temperature result register is updated at the end of every conversion.

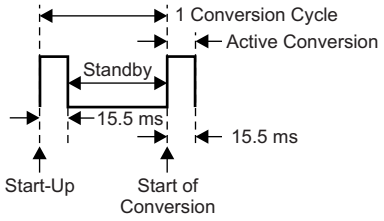


**Figure 14. Conversion Cycle Timing Diagram**

#### *7.4.1.2 Averaging*

Users can configure the device to report the average of multiple temperature conversions with the AVG[1:0] bits to improve noise in the conversion results. When the TMP117 is configured to perform averaging, the device executes the configured number of conversions. The device accumulates those conversion results and reports the average of all the collected results at the end of the process. As shown in the noise histograms of Figure 6 and , the temperature result output has a repeatability of approximately ±3 LSBs when there is no averaging and ±1 LSB when the device is configured to perform eight averages. As shown in Figure 15, engineer can achieve this improvement in noise performance with an increase in the active conversion time in a conversion cycle as a trade-off. Note that this outcome will increase the average active current consumption. For example, a single active conversion typically takes 15.5 ms, so if the device is configured to report an average of eight conversions, then the active conversion time is 124 ms (15.5 ms × 8). Use Equation 1 to factor in this increase in active conversion time to accurately calculate the average current consumption of the device. The average current consumption of the device can be decreased by increasing the amount of time the device spends in standby period as compared to active conversion. On reset, the device is configured to report an average of eight conversions with a conversion cycle time of 1 second.

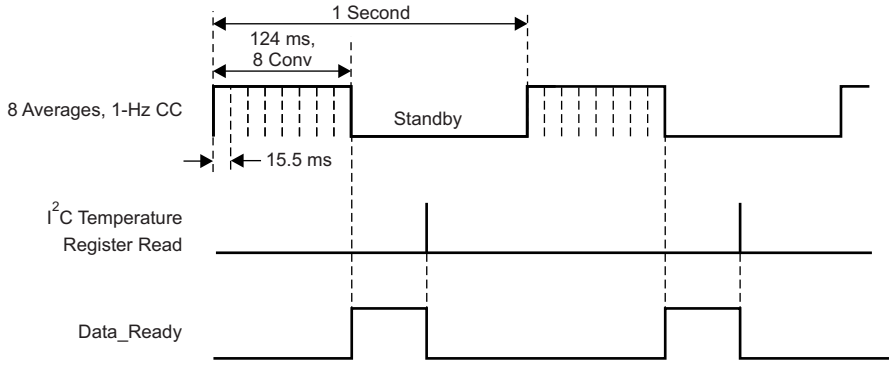


**Figure 15. Averaging Timing Diagram**

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## Device Functional Modes (continued)

Use Equation 1 to calculate the average current consumption of the device in continuous mode.

$$\frac{(\text{Active Current Consumption} \times \text{Active Conversion Time}) + (\text{Standby Current Consumption} \times \text{Standby Time})}{\text{Conversion Cycle Time}} \quad (1)$$

### 7.4.1.3 Continuous Conversion Mode (CC)

When the MOD[1:0] bits are set to 00 in the configuration register , the device operates in continuous conversion mode. The device continuously performs temperature conversions in this mode, as shown in Figure 14, and updates the temperature result register at the end of every conversion. As described in the *Conversion Cycle* section, every conversion cycle consists of an active conversion period followed by a standby period whose duration can be configured using the CONV and AVG bits in the configuration register based on the temperature accuracy, power consumption, and temperature update rate trade-offs of the application that the device is used in. At the end of a conversion, the Data_Ready flag in the configuration register is set. The user can read the configuration register or the temperature result register to clear the Data_Ready flag. Therefore, the Data_Ready flag can be used to determine when the conversion completes so that an external controller can synchronize reading the result register with conversion result updates. The user can set the DR/nAlert_EN bit in the configuration register to monitor the state of the Data_Ready flag on the ALERT pin.

### 7.4.1.4 Shutdown Mode (SD)

When the MOD[1:0] bits are set to 01 in the configuration register, the device instantly aborts the currently running conversion and enters a low-power shutdown mode. In this mode, the device powers down all active circuitry and can be used in conjunction with the OS mode to perform temperature conversions. In SD mode, the device typically consumes only 250 nA, which makes the TMP117 suitable for battery-operated systems and other low-power consumption applications.

### 7.4.1.5 One-Shot Mode (OS)

When MOD[1:0] bits are set to 11 in the configuration register to run a single conversion, referred to as a one-shot conversion. After the device completes a one-shot conversion, the device returns to the low-power shutdown mode. A one-shot conversion cycle only consists of active conversion time and no standby period, unlike CC mode. Thus, the duration of a one-shot conversion is only affected by the AVG bit settings. The CONV bits do not affect the duration of a one-shot conversion. Figure 16 shows a timing diagram for this mode with an AVG setting of 00. At the end of a one-shot conversion, the Data_Ready flag in the configuration register is set. The Data_Ready flag can thus be used to determine when the conversion completes. The user can perform an $I^2C$ read on the configuration register or temperature result register to clear the Data_Ready flag. The user can also set the DR/nAlert_EN bit in the configuration register to monitor the state of the Data_Ready flag on the ALERT pin.

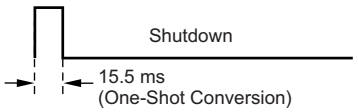


**Figure 16. One-Shot Timing Diagram**

### 7.4.2 Therm and Alert Functions

The built-in therm and alert functions of the TMP117 can alert the user if the temperature has crossed a certain temperature limit or if the device is within a certain temperature range. At the end of every conversion, the TMP117 compares the converted temperature result to the values stored in the low limit register and high limit register. The device then either sets or clears the corresponding status flags in the configuration register, as described in this section.

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## Device Functional Modes (continued)

### 7.4.2.1 Alert Mode

When the T/nA bit in the configuration register is set to 0, the device is in alert mode. In this mode, the device compares the conversion result at the end of every conversion with the values in the low limit register and high limit register. If the temperature result exceeds the value in the high limit register, the HIGH_Alert status flag in the configuration register is set. On the other hand, if the temperature result is lower than the value in the low limit register, the LOW_Alert status flag in the configuration register is set. As shown in Figure 17, the user can run an $I^2C$ read transaction on the configuration register to clear the status flags in alert mode.

When a user configures the device in alert mode, it affects the behaviour of the ALERT pin. The device asserts the ALERT pin in this mode when either the HIGH_Alert or the LOW_Alert status flag is set, as shown in Figure 17. The user can either run an $I^2C$ read of the configuration register (which also clears the status flags) or run an SMBus alert response command (see the *SMBus Alert Function* section) to deassert the ALERT pin. The polarity of the ALERT pin can be changed by using the POL bit setting in the configuration register.

This mode effectively makes the device behave like a window limit detector. Thus this mode can be used in applications where detecting if the temperature goes outside of the specified range is necessary.

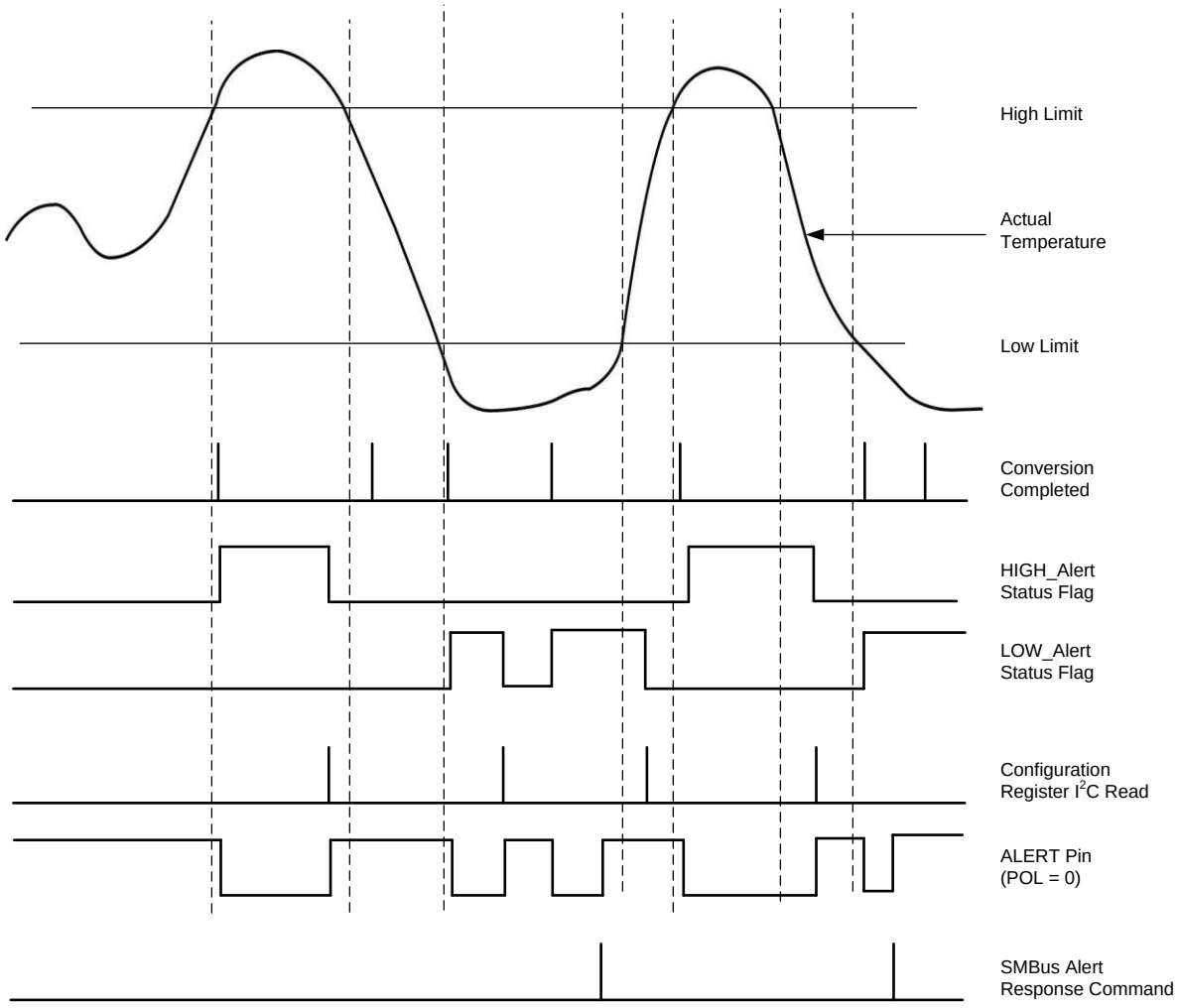


**Figure 17. Alert Mode Timing Diagram**

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## Device Functional Modes (continued)

### 7.4.2.2 Therm Mode

When the T/nA bit in the configuration register is set to 1 the device is in therm mode. In this mode, the device compares the conversion result at the end of every conversion with the values in the low limit register and high limit register and sets the HIGH_Alert status flag in the configuration register if the temperature exceeds the value in the high limit register. When set, the device clears the HIGH_Alert status flag if the conversion result goes below the value in the low limit register. Thus, the difference between the high and low limits effectively acts like a hysteresis. In this mode, the LOW_Alert status flag is disabled and always reads 0. Unlike the alert mode, $I^2C$ reads of the configuration register do not affect the status bits. The HIGH_Alert status flag is only set or cleared at the end of conversions based on the value of the temperature result compared to the high and low limits.

As in alert mode, configuring the device in therm mode also affects the behaviour of the ALERT pin. In this mode, the device asserts the ALERT pin if the HIGH_Alert status flag is set and deasserts the ALERT pin when the HIGH_Alert status flag is cleared. In therm mode, the ALERT pin cannot be cleared by performing an $I^2C$ read of the configuration register or by performing an SMBus alert response command. As in alert mode, the polarity of the active state of the ALERT pin can be changed if the user adjusts the POL bit setting in the configuration register.

Thus, this mode effectively makes the device behave like a high-limit threshold detector. This mode can be used in applications where detecting if the temperature has gone above a desired threshold is necessary. Figure 18 shows a timing diagram of this mode.

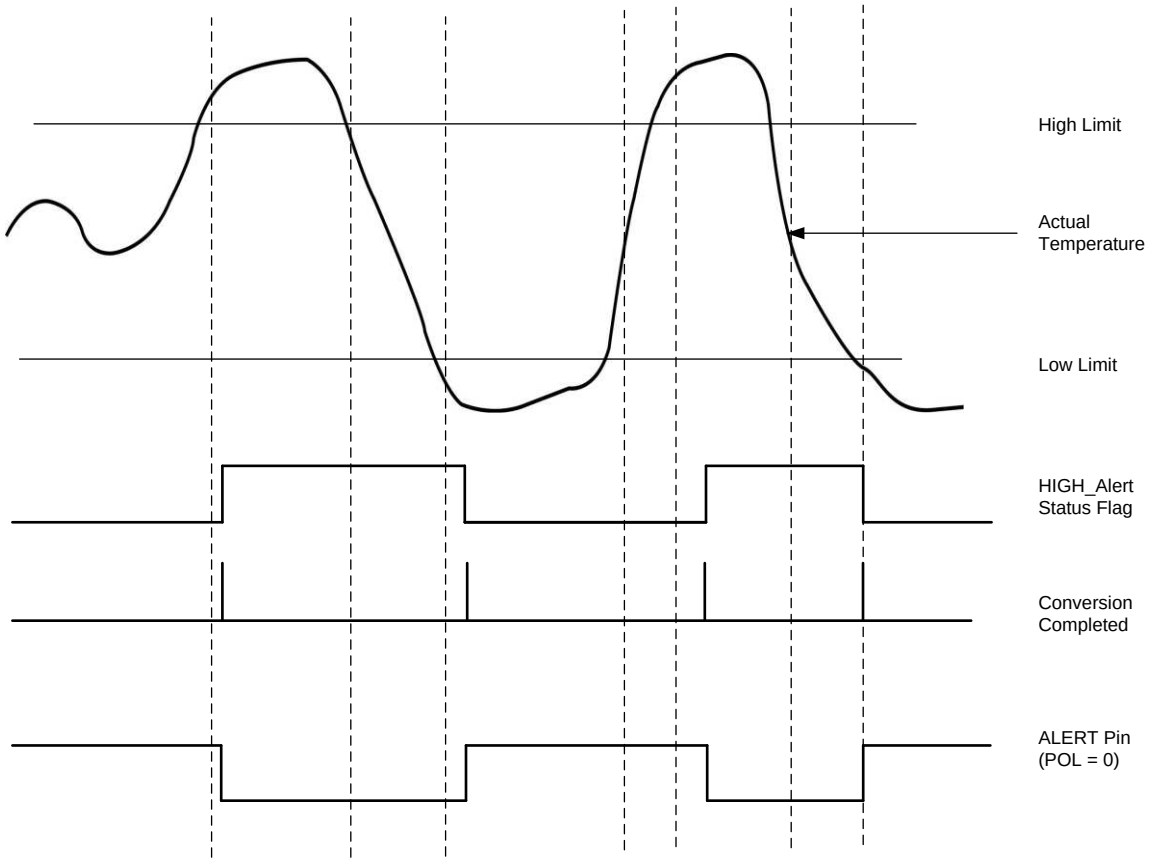


**Figure 18. Therm Mode Timing Diagram**

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## 7.5 Programming

### 7.5.1 EEPROM Programming

#### *7.5.1.1 EEPROM Overview*

The device has a user-programmable EEPROM that can be used for two purposes:

- Storing power-on-reset (POR) values of the high limit register, low limit register, conversion cycle time, averaging mode, conversion mode (continuous or shutdown mode), alert function mode (alert or therm mode), and alert polarity
- Storing four 16-bit locations for general-purpose use. See the EEPROM[4:1] registers for more information.

On reset, the device goes through a POR sequence that loads the values programmed in the EEPROM into the respective register map locations. This process takes approximately 1.5 ms. When the power-up sequence is complete, the device starts operating in accordance to the configuration parameters that are loaded from the EEPROM. Any $I^2C$ writes performed during this initial POR period to the limit registers or the configuration register are ignored. $I^2C$ read transactions can still be performed with the device during the power-up period. While the POR sequence is being executed, the EEPROM_Busy status flag in the EEPROM unlock register is set.

During production, the EEPROM in the TMP117 is programmed with reset values as shown in Table 3. The *Programming the EEPROM* section describes how to change these values. A unique ID is also programmed in the general-purpose EEPROM locations during production. This unique ID is used to support NIST traceability. The TMP117 units are 100% tested on a production setup that is NIST traceable and verified with equipment that is calibrated to ISO/IEC 17025 accredited standards. Only reprogram the general-purpose EEPROM[4:1] locations if NIST traceability is not desired.

#### *7.5.1.2 Programming the EEPROM*

To prevent accidental programming, the EEPROM is locked by default. When locked, any $I^2C$ writes to the register map locations are performed only on the volatile registers and not on the EEPROM.

Figure 19 illustrates a flow chart describing the EEPROM programming sequence. To program the EEPROM, first unlock the EEPROM by setting the EUN bit in the EEPROM unlock register. After the EEPROM is unlocked, any subsequent $I^2C$ writes to the register map locations program a corresponding non-volatile memory location in the EEPROM. Programming a single location typically takes 7 ms to complete and consumes 230 µA. Do not perform any $I^2C$ writes until programming is complete. During programming, the EEPROM_busy flag is set. Read this flag to monitor if the programming is complete. After programming the desired data, issue a general-call reset command to trigger a software reset. The programmed data from the EEPROM are then loaded to the corresponding register map locations as part of the reset sequence. This command also clears the EUN bit and automatically locks the EEPROM to prevent any further accidental programming. Avoid using the device to perform temperature conversions when the EEPROM is unlocked.

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## Programming (continued)

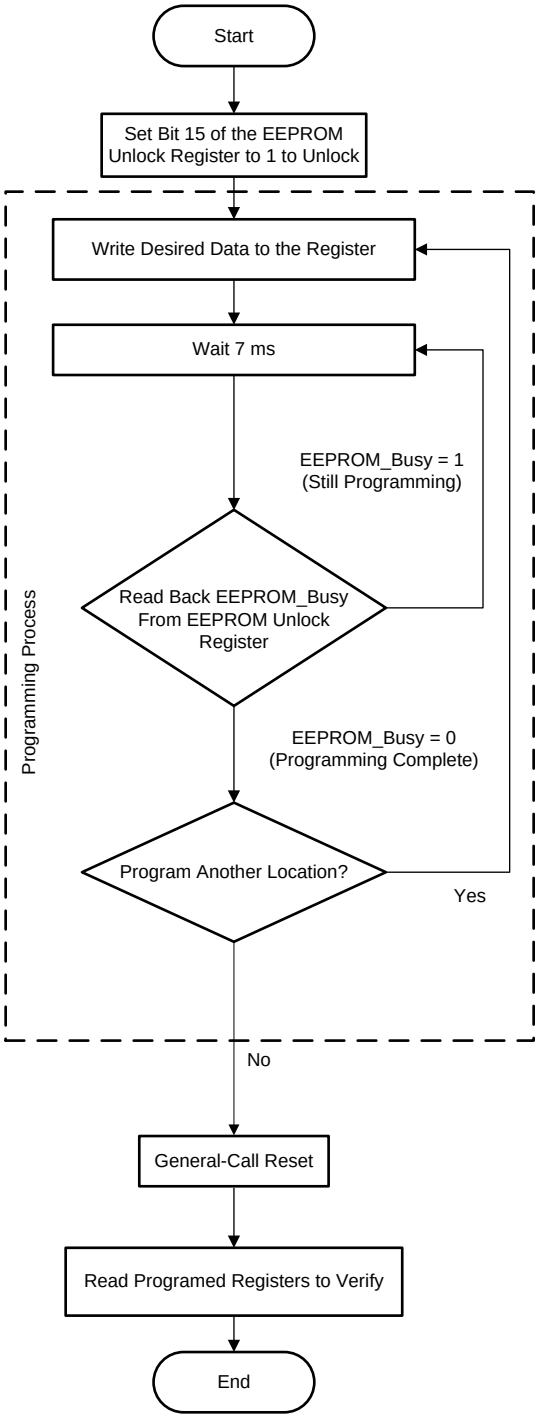


**Figure 19. EEPROM Programming Sequence**

## Programming (continued)

### 7.5.2 Pointer Register

Figure 20 shows the internal register structure of the TMP117. The 8-bit pointer register of the device is used to address a given data register. The power-up reset value is 00. By default, the TMP117 reads the temperature on power-up.

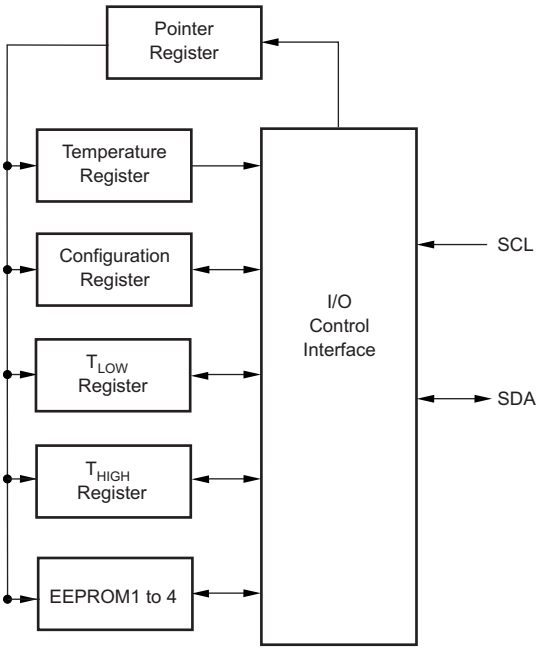


**Figure 20. Internal Register Structures**

### 7.5.3 I²C and SMBus Interface

#### *7.5.3.1 Serial Interface*

The TMP117 operates as a slave device only on the two-wire, SMBus and I²C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines and the SDA and SCL pins. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The device supports the transmission protocol for fast (1 kHz to 400 kHz) mode. Register bytes are sent with the most significant byte first, followed by the least significant byte.

##### 7.5.3.1.1 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a high- to low-logic level when the SCL pin is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, and the last bit indicates whether a read or write operation is intended. During the ninth clock pulse, the addressed slave generates an acknowledge and pulls the SDA pin low to respond to the master.

A data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During the data transfer, the SDA pin must remain stable when the SCL pin is high because any change in the SDA pin when the SCL pin is high is interpreted as a START or STOP signal.

When all data are transferred, the master generates a repeated START or STOP condition indicated by pulling the SDA pin from low to high when the SCL pin is high.

## Programming (continued)

#### 7.5.3.1.2 Serial Bus Address

To communicate with the TMP117, the master must first address slave devices through an address byte. The address byte has seven address bits and a read-write (R/W) bit that indicates the intent of executing a read or write operation.

The TMP117 features an address pin to allow up to four devices to be addressed on a single bus. Table 2 describes the pin logic levels used to properly connect up to four devices. *x* represents the read-write (R/$\overline{W}$) bit.

**Table 2. Address Pin and Slave Addresses**

| DEVICE TWO-WIRE ADDRESS | ADD0 PIN CONNECTION |
|---|---|
| 1001000x | Ground |
| 1001001x | V+ |
| 1001010x | SDA |
| 1001011x | SCL |

#### 7.5.3.1.3 Writing and Reading Operation

The user can write a register address to the pointer register to access a particular register on the TMP117. The value for the pointer register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP117 requires a value for the pointer register.

When reading from the TMP117, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. The user can issue an address byte with the R/$\overline{W}$ bit low, followed by the pointer register byte, to write a new value for the pointer register. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 23 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to send the pointer register bytes continuously because the TMP117 retains the pointer register value until the value is changed by the next write operation.

Register bytes are sent with the most significant byte first, followed by the least significant byte.

#### 7.5.3.1.4 Slave Mode Operations

The TMP117 can operate as a slave receiver or slave transmitter. As a slave device, the TMP117 never drives the SCL line.

##### *7.5.3.1.4.1 Slave Receiver Mode*

The first byte transmitted by the master is the slave address with the R/$\overline{W}$ bit low. The TMP117 then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP117 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP117 acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

##### *7.5.3.1.4.2 Slave Transmitter Mode*

The first byte transmitted by the master is the slave address with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a *not-acknowledge* on reception of any data byte or by generating a START or STOP condition.

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#### 7.5.3.1.5 SMBus Alert Function

The TMP117 supports the SMBus alert function. When the ALERT pin is connected to an SMBus alert signal and a master senses that an alert condition is present, the master can send out an SMBus ALERT command (0001 1001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus ALERT command and responds by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the alert condition is caused by the temperature exceeding $T_{(HIGH)}$ or falling below $T_{(LOW)}$. The LSB is high if the temperature is greater than $T_{(HIGH)}$, or low if the temperature is less than $T_{(LOW)}$. See Figure 24 for details of this sequence.

If multiple devices on the bus respond to the SMBus ALERT command, arbitration during the slave address portion of the SMBus ALERT command determines which device clears the alert status of that device. The device with the lowest two-wire address wins the arbitration. If the TMP117 wins the arbitration, the TMP117 ALERT pin becomes inactive at the completion of the SMBus ALERT command. If the TMP117 loses the arbitration, the TMP117 ALERT pin remains active.

#### 7.5.3.1.6 General-Call Reset Function

The TMP117 responds to a two-wire, general-call address (0000 000) if the eighth bit is 0. The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0000 0110, the TMP117 internal registers are reset to power-up values.

#### 7.5.3.1.7 Timeout Function

The TMP117 resets the serial interface if the SCL line is held low by the master or the SDA line is held low by the TMP117 for 35 ms (typical) between a START and STOP condition. The TMP117 releases the SDA line if the SCL pin is pulled low and waits for a START condition from the host controller. To avoid activating the timeout function, maintain a communication speed of at least 1 kHz for the SCL operating frequency.

#### 7.5.3.1.8 Timing Diagrams

The TMP117 is two-wire, SMBus, and $I^2C$ interface-compatible. Figure 21 to Figure 25 show the various operations on the TMP117. Parameters for Figure 21 are defined in *Two-Wire Interface Timing*. Bus definitions are:

**Bus Idle:** Both SDA and SCL lines remain high.

**Start Data Transfer:** A change in the state of the SDA line from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

**Stop Data Transfer:** A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

**Data Transfer:** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The TMP117 can also be used for single byte updates. To update only the MS byte, terminate the communication by issuing a START or STOP communication on the bus.

**Acknowledge:** Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. The user must take setup and hold times into account. On a master receive, the termination of the data transfer can be signaled by the master generating a *not-acknowledge* (1) on the last byte transmitted by the slave.

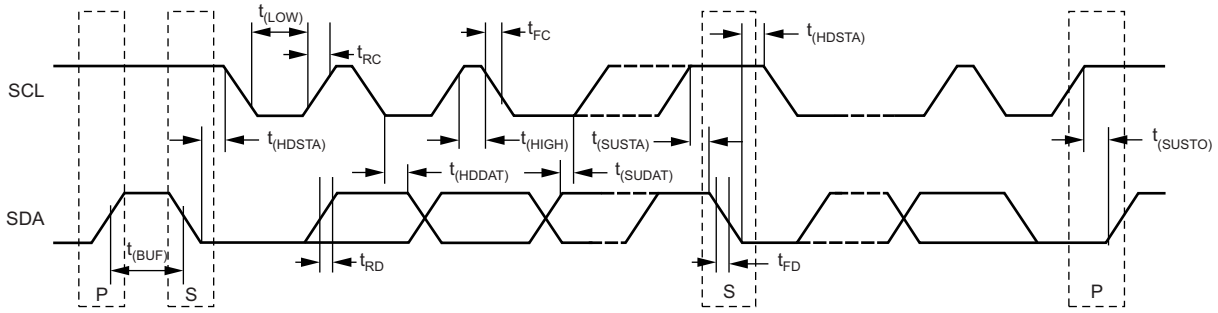


**Figure 21. Two-Wire Timing Diagram**

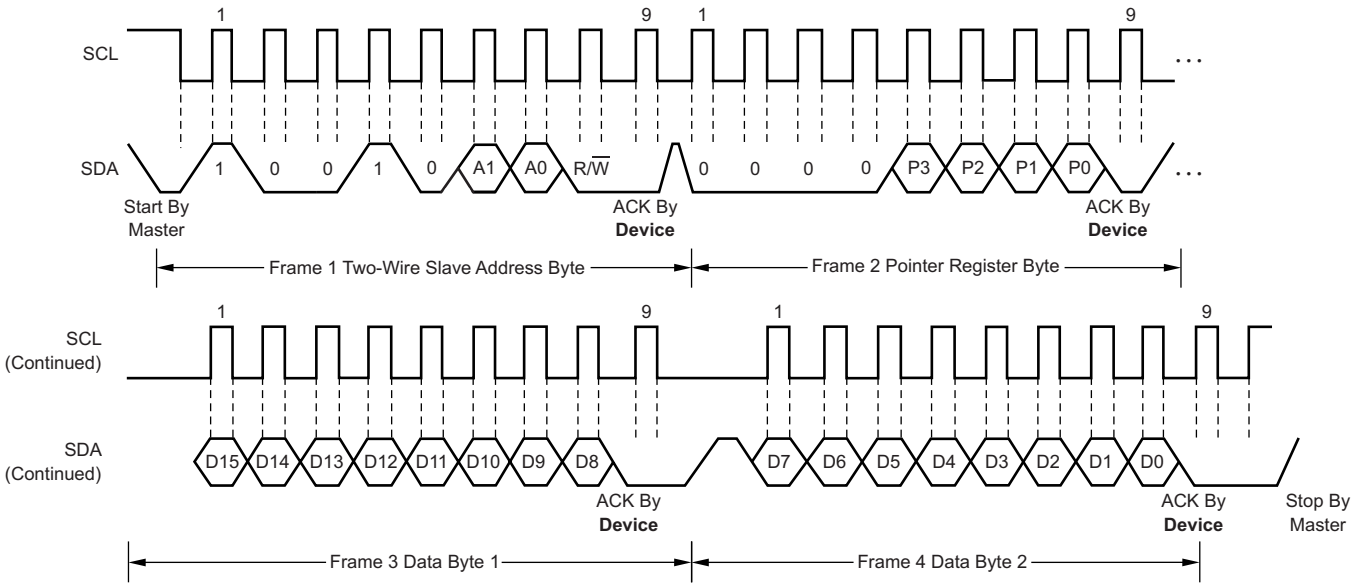


**Figure 22. Write Word Command Timing Diagram**

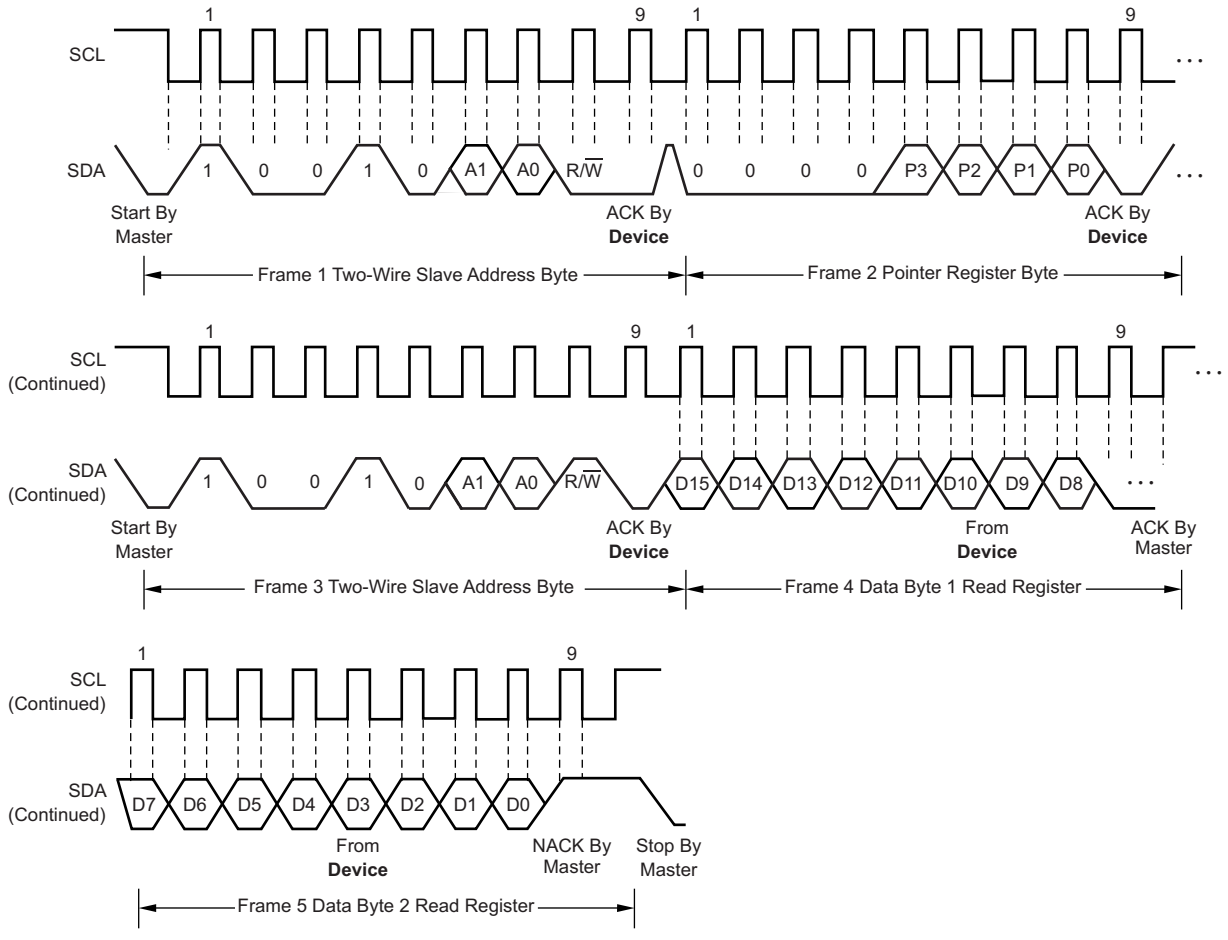


**Figure 23. Read Word Command Timing Diagram**

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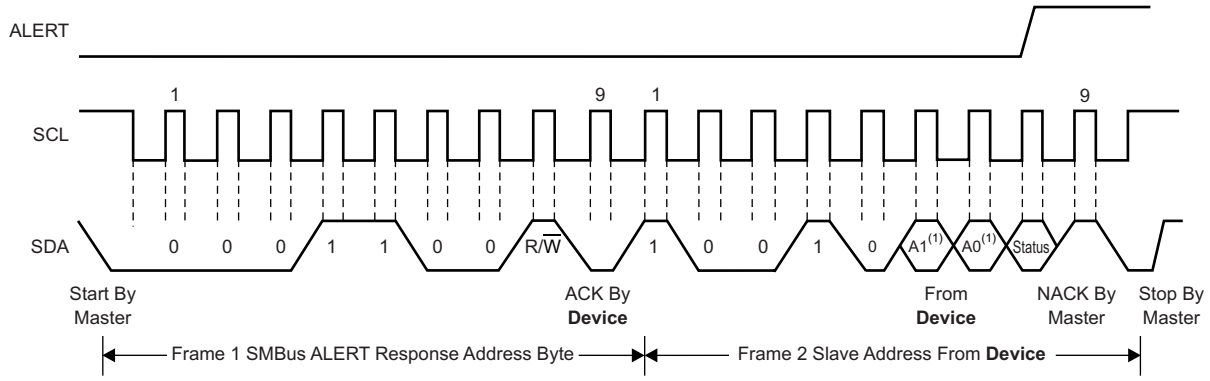


**Figure 24. SMBus ALERT Timing Diagram**

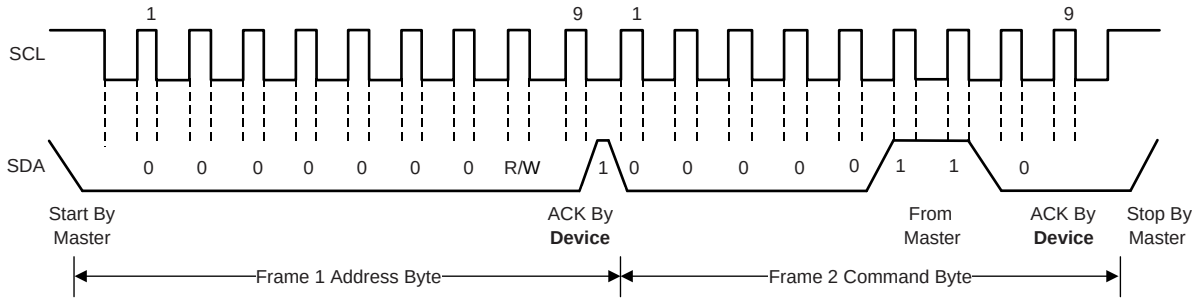


**Figure 25. General-Call Reset Command Timing Diagram**

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## 7.6 Registers Map

**Table 3. Register Map**

| ADDRESS (HEX) | DEFAULT VALUE (HEX) | REGISTER DATA | | | | | | | | | | | | | | | | REGISTER NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 00h | 8000 | T15 | T14 | T13 | T12 | T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 | Temperature |
| 01h | 0220(1) | HIGH_ Alert | LOW_ Alert | Data_ Ready | EEPROM _Busy | MOD1 | MOD0 | CONV2 | CONV1 | CONV0 | AVG1 | AVG0 | T/nA | POL | DR/nAlert _EN | Soft_Rest | — | Configuration |
| 02h | 6000(1) | H15 | H14 | H13 | H12 | H11 | H10 | H9 | H8 | H7 | H6 | H5 | H4 | H3 | H2 | H1 | H0 | High Limit |
| 03h | 8000(1) | L15 | L14 | L13 | L12 | L11 | L10 | L9 | L8 | L7 | L6 | L5 | L4 | L3 | L2 | L1 | L0 | Low Limit |
| 07h | 0000(1) | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Temperature Offset |
| 04h | 0000 | EUN | EEPROM _ Busy | — | — | — | — | — | — | — | — | — | — | — | — | — | — | EEPROM Unlock |
| 05h | xxxx(1) | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | EEPROM1 |
| 06h | xxxx(1) | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | EEPROM2 |
| | | | | | | | | | | | | | | | | | | |
| 08h | xxxx(1) | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | EEPROM3 |
| 0Fh | x116 | — | — | — | — | DID11 | DID10 | DID9 | DID8 | DID7 | DID6 | DID5 | DID4 | DID3 | DID2 | DID1 | DID0 | Device ID |

(1) This value is stored in electrically-erasable, programmable read-only memory (EEPROM) during device manufacturing. The device reset value can be changed by writing the relevant code in the EEPROM cells (see the *EEPROM Overview* section).

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### 7.6.1 Register Descriptions

**Table 4. TMP117 Access Type Codes**

| ACCESS TYPE | CODE | DESCRIPTION |
|---|---|---|
| R | R | Read |
| Read-write | R/W | Read, write, or both |
| W | W | Write |
| *-n* | | Value after reset or the default value |

#### *7.6.1.1 Temperature Register (address = 00h) [default reset = 8000h]*

This register is a 16-bit, read-only register that stores the output of the most recent conversion. One LSB equals 7.8125 m°C. Data are represented in binary two's complement format. Following power-up or a general-call reset, the temperature register reads –256°C until the first conversion is complete. See the *Power Up* section for more information.

**Figure 26. Temperature Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| T15 | T14 | T13 | T12 | T11 | T10 | T9 | T8 |
| R-1 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

**Table 5. Temperature Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15:0 | T[15:0] | R | 8000h | 16-bit, read-only register that stores the most recent temperature conversion results. |

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### 7.6.1.2 Configuration Register (address = 01h) [default reset = 0220h]

**Figure 27. Configuration Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| HIGH_Alert | LOW_Alert | Data_Ready | EEPROM_Busy | MOD1(1) | MOD0(2) | CONV2(2) | CONV1(2) |
| R-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CONV0(2) | AVG1(2) | AVG0(2) | T/nA(2) | POL(2) | DR/Alert(2) | — | — |
| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 |

(1) The MOD1 bit cannot be stored in EEPROM. The device can only be programmed to start up in shutdown mode or continuous conversion mode.
(2) These bits can be stored in EEPROM. The factory setting for this register is 0220.

**Table 6. Configuration Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15 | HIGH_Alert | R | 0 | Alert mode:<br>1: Set when the conversion result is higher than the high limit<br>0: Cleared on read of configuration register<br>Therm mode:<br>1: Set when the conversion result is higher than the therm limit<br>0: Cleared when the conversion result is lower than the hysteresis |
| 14 | LOW_Alert | R | 0 | Alert mode:<br>1: Set when the conversion result is lower than the low limit<br>0: Cleared when the configuration register is read<br>Therm mode: Always set to 0 |
| 13 | Data_Ready | R | 0 | Data ready flag.<br>This flag indicates that the conversion is complete and the temperature register can be read. Every time the temperature register or configuration register is read, this bit is cleared. This bit is set at the end of the next conversion when the temperature register is updated. Data ready can be monitored on the ALERT pin by using bit 2 of the configuration register. |
| 12 | EEPROM_Busy | R | 0 | EEPROM busy flag.<br>The value of the flag indicates that the EEPROM is busy during programming or power-up. |
| 11:10 | MOD[1:0] | R/W | 0 | Set conversion mode.<br>00: Continuous conversion (CC)<br>01: Shutdown (SD)<br>10: Continuous conversion (read back = 00)<br>11: One-shot conversion (OS) |
| 9:7 | CONV[2:0] | R/W | 100 | Conversion cycle bit.<br>See Table 7 for the standby time between conversions. |
| 6:5 | AVG[1:0] | R/W | 01 | Conversion averaging modes.<br>These bits determine the number of conversion results that are collected and averaged before updating the temperature register. The average is an accumulated average and not a running average. Table 8 lists the bit settings for AVG. |
| 4 | T/nA | R/W | 0 | Therm/alert mode select.<br>1: Therm mode<br>0: Alert mode |
| 3 | POL | R/W | 0 | ALERT pin polarity bit.<br>1: Active high<br>0: Active low |
| 2 | DR/Alert | R/W | 0 | Data ready, ALERT flag select bit.<br>1: ALERT pin reflects the status of the data ready flag<br>0: ALERT pin reflects the status of the alert flags |
| 1 | Soft_Reset | R/W | 0 | Software reset bit.<br>When set to 1 it triggers software reset with a duration of 2ms<br>This bit always read back 0 |
| 0 | — | R | 0 | Not used |

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**Table 7. Conversion Cycle Time in CC Mode**

| CONV[2:0] | AVG[1:0] = 00 | AVG[1:0] = 01 |
|---|---|---|
| 000 | 15.5 ms | 125 ms |
| 001 | 125 ms | 125 ms |
| 010 | 250 ms | 250 ms |
| 011 | 500 ms | 500 ms |
| 100 | 1 s | 1 s |
| 101 | 4 s | 4 s |
| 110 | 8 s | 8 s |
| 111 | 16 s | 16 s |

**Table 8. AVG Bit Settings**

| AVG1 | AVG0 | DESCRIPTION |
|---|---|---|
| 0 | 0 | No averaging,15.5-ms active conversion time |
| 0 | 1 | 8 averages, 125-ms active conversion time |

ADVANCE INFORMATION

### 7.6.1.3 High Limit Register (address = 02h) [reset = 6000h]

This register is a 16-bit, read/write register that stores the high limit for comparison with the temperature result. One LSB equals 7.8125 m°C. The range of the register is ±256°C. Negative numbers are represented in binary two's complement format. Following power-up or a general-call reset, the high-limit register is loaded with the stored value from the EEPROM that is set as factory default to 6000h.

**Figure 28. High Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| H15 | H14 | H13 | H12 | H11 | H10 | H9 | H8 |
| R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| H7 | H6 | H5 | H4 | H3 | H2 | H1 | H0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 9. High Limit Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15:0 | H[15:0] | R/W | 6000h | 16-bit, read/write register that stores the high limit for comparison with the temperature result. |

### 7.6.1.4 Low Limit Register (address = 03h) [reset = 8000h]

This register is configured as a 16-bit, read/write register that stores the low limit for comparison with the temperature result. One LSB equals 7.8125 m°C. The range of the register is ±256°C. Negative numbers are represented in binary two's complement format. Following power-up or reset, the low-limit register is loaded with the stored value from the EEPROM that is set in the factory to 8000h.

**Figure 29. Low Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| L15 | L14 | L13 | L12 | L11 | L10 | L9 | L8 |
| R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| L7 | L6 | L5 | L4 | L3 | L2 | L1 | L0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 10. Low Limit Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15:0 | L[15:0] | R/W | 8000h | 16-bit, read/write register that stores the low limit for comparison with the temperature result. |

### 7.6.1.5 Temperature Offset Register (address = 07h) [reset = 0000h]

This 16-bit register is to be used as a user-defined temperature offset register during system calibration. The offset will be added to the temperature result after linearization. It has a same resolution of 7.8125m°C and same range of ±256°C as the temperature result register. If added result is out of boundary, then the temperature result will show as the maximum or minimum value. This register read-write functionality is similar as the EEPROM1 register.

**Figure 30. Temperature Offset Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

ADVANCE INFORMATION

**Table 11. Temperature Offset Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15:0 | D[15:0] | R/W | 0 | This 16-bit register is to be used as a scratch pad by the customer. |

### 7.6.1.6 EEPROM Unlock Register (address = 04h) [reset = 0000h]

**Figure 31. EEPROM Unlock Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| EUN | EEPROM_Busy | — | — | — | — | — | — |
| R/W-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| — | — | — | — | — | — | — | — |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

**Table 12. EEPROM Unlock Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15 | EUN | R/W | 0 | EEPROM unlock.<br>0: EEPROM is locked for programming: writes to all EEPROM addresses (such as configuration, limits, and EEPROM locations 1-4) are written to registers in digital logic and are not programmed in the EEPROM<br>1: EEPROM unlocked for programming: any writes to writable registers program the respective location in the EEPROM |
| 14 | EEPROM_Busy | R | 0 | EEPROM busy. This flag is the mirror of the EEPROM busy flag (bit 12) in the configuration register.<br>0: Indicates that the EEPROM is ready, which means that the EEPROM has finished the last transaction and is ready to accept new commands<br>1: Indicates that the EEPROM is busy, which means that the EEPROM is currently completing a program or power-up on reset load |
| 13:0 | — | R | 0 | Not used |

### 7.6.1.7 EEPROM1 Register (address = 05h) [reset = 0000h]

The EEPROM1 register is a 16-bit register that be used as a scratch pad by the customer to store general-purpose data. This register has a corresponding EEPROM location. Writes to this address when the EEPROM is locked write data into the register and not to the EEPROM. Writes to this register when the EEPROM is unlocked causes the corresponding EEPROM location to be programmed. See the *Programming the EEPROM* section for more information. EEPROM[4:1] are preprogrammed during manufacturing with the unique ID that can be overwritten. To support NIST traceability, do not delete or reprogram EEPROM[4:1].

**Figure 32. EEPROM1 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |

**Table 13. EEPROM1 Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15:0 | D[15:0] | R/W | xxxxh | This 16-bit register is to be used as a scratch pad by the customer. |

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### 7.6.1.8 EEPROM2 Register (address = 06h) [reset = 0000h]

This register function the same as the EEPROM1 register.

**Figure 33. EEPROM2 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |

**Table 14. EEPROM2 Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15:0 | D[15:0] | R/W | xxxxh | This 16-bit register is to be used as a scratch pad by the customer. |

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### 7.6.1.9 EEPROM3 Register (address = 08h) [reset = xxxxh]

This register function is the same as the EEPROM1 register.

**Figure 34. EEPROM3 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |

**Table 15. EEPROM3 Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15:0 | D[15:0] | R/W | xxxxh | This 16-bit register is to be used as a scratch pad by the customer. |

### 7.6.1.10 Device ID Register (address = 0Fh) [reset = x116h]

This read-only register indicates the device ID.

**Figure 35. Device ID Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | DID11 | DID10 | DID9 | DID8 |
| R-x | R-x | R-x | R-x | R-0 | R-0 | R-0 | R-1 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DID7 | DID6 | DID5 | DID4 | DID3 | DID2 | DID1 | DID0 |
| R-0 | R-0 | R-0 | R-1 | R-0 | R-1 | R-1 | R-0 |

**Table 16. Device ID Register Field Descriptions**

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|---|---|---|---|---|
| 15:12 | — | R | x | Not used. |
| 11:0 | DID[11:0] | R | 116h | These bits indicate the device ID. |

ADVANCE INFORMATION

# 8 Application and Implementation

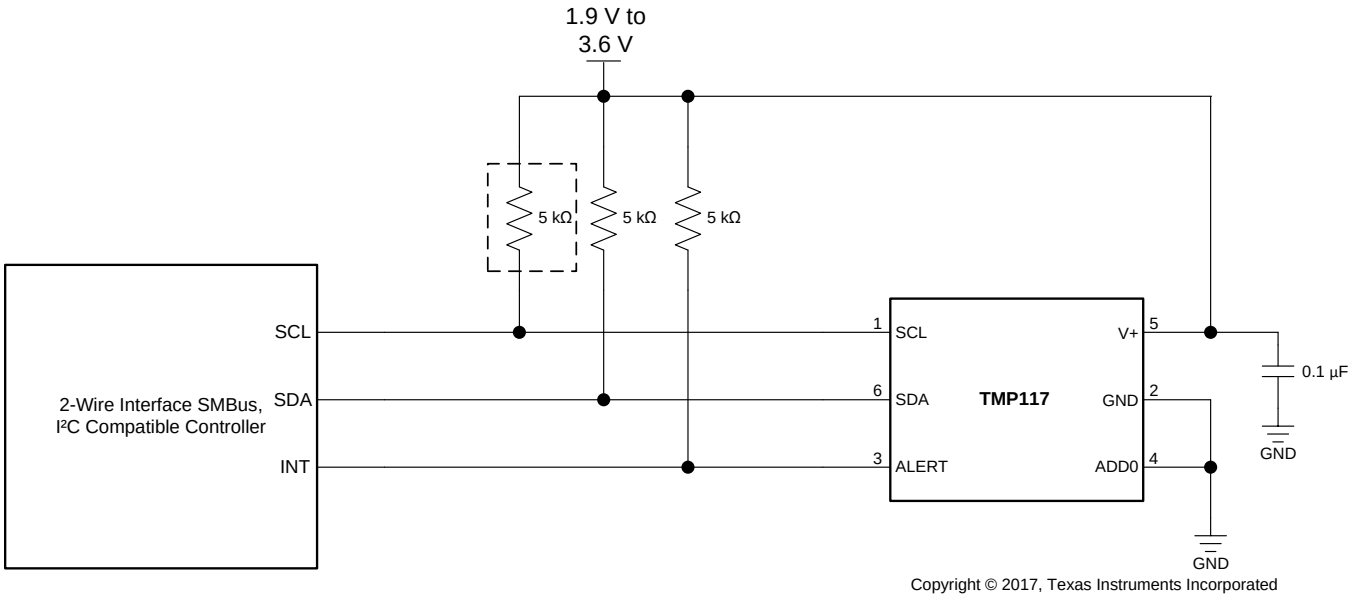
**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TMP117 is used to measure the temperature of the board location where the device is mounted. The programmable address options allow up to four locations on the board to be monitored on a single serial bus. For more information, refer to the related *TMP116 Ambient Air Temperature Measurement* (SNOA966), *Replacing Resistance Temperature Detectors with the TMP116 Temp Sensor* (SNOA969), and *Temperature Sensors: PCB Guidelines for Surface Mount Devices* (SNOA967) application reports on ti.com.

### 8.1.1 Typical Application




NOTE: The SDA and ALERT pins require pullup resistors.

**Figure 36. Typical Connections**

#### *8.1.1.1 Design Requirements*

The TMP117 operates only as a slave device and communicates with the host through the $I^2C$-compatible serial interface. SCL is the input pin, SDA is a bidirectional pin, and ALERT is the output. The TMP117 requires a pullup resistor on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistors is 5 kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ. A 0.1-µF bypass capacitor is recommended to be connected between V+ and GND. An SCL pullup resistor is required if the system microprocessor SCL pin is open-drain. Use a ceramic capacitor type with a temperature rating from –40°C to +125°C, placed as close as possible to the V+ pin of the TMP117. The decoupling capacitor reduces any noise induced by the system. When connected directly to GND, V+, SDA, and SCL, use the ADD0 pin for address selection for configuring four possible unique slave ID addresses. Table 1 explains the addressing scheme. The ALERT output pin can be connected to a microcontroller interrupt that triggers an event that occurred when the temperature limit exceeds the programmable value in registers 02h and 03h. The ALERT pin can be left floating if not in use or connected to ground.

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## Application Information (continued)

### *8.1.1.2 Detailed Design Procedure*

#### 8.1.1.2.1 TMP117 Design Procedure

The TMP117 is a local temperature sensor. Measuring a temperature point with a surface-mount device is very challenging because of the external influence of surrounding air and other components. The TMP117 mainly monitors the PCB temperature at the desired hotspot. To maintain accuracy in applications that requires surface temperature measurement, follow good layout techniques (such as understanding the dominant thermal path, isolating the island surround by the package, and keeping the distance as far as possible from the heat source).

For sensors in plastic packages (such as the TMP117 DFN device), Figure 37 shows that the die attach pad (DAP) provides the most dominant thermal path. With the DAP, a board-mounted sensor usually does an excellent job of measuring board temperature. The die sits on top of the metal plate leadframe with a non-conductive die adhesive in between, allowing for a fast thermal response.

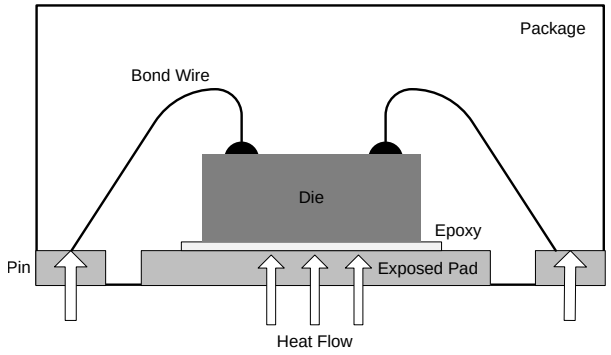


**Figure 37. WSON Package Cross Section**

Most power-hungry electronic components such as processor chips, field programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs), and voltage regulators heat up during operation. In order to accurately measure the ambient temperature of a sensor in a plastic package, isolate the sensor from the heat source using isolation island techniques and distance. TI recommends two vias per TMP117 dimension of the thermal pad. The DAP and two vias help improve thermal characteristics. Thus, in order to take advantage of this feature, mount the TMP117 on the board with the two copper planes on the top and bottom of the via of equal length as the exposed die attach dimension. The bottom plane contains the temperature sensing elements. In order to achieve the fast temperature response, the mini board dimension must be enough to accommodate the TMP117 and the bypass capacitor with the isolation air gap to prevent the heat source dissipated to the mini sub-board.

#### 8.1.1.2.2 Noise and Averaging

The device temperature sampling distribution (without internal averaging) covers an area of approximately six neighboring codes. The noise area of the six codes remains the same at full supply and full temperature range with a standard deviation of approximately 1 LSB. The device provides an averaging tool for 8, 32, and 64 samples. As illustrated in , even the 8-sample averaging reduces the internal noise distribution to a theoretical minimum of 2 LSB. This averaging means that if the system temperature slowly changes and the supply voltage is stable, then the 8-sample averaging can be enough to neutralize the device noise and provide stable temperature readings. However, if the system temperature is noisy (such as when measuring air flow temperatures), than higher averaging numbers are recommended to be used.

ADVANCE INFORMATION

## Application Information (continued)

#### 8.1.1.2.3 Self-Heating Effect (SHE)

During ADC conversion some power is dissipated that heats the device despite the small power consumption of the TMP117. Consider the self-heating effect (SHE) for certain precise measurements. Figure 38 shows the device SHE in still air at 25°C after the supply is switched on. The device package, including the thermal pad, is soldered to the 11-mm × 20-mm × 1.1-mm size coupon board. The board is located horizontally, with the device on top. The TMP117 is in continuous conversion mode with 64 sampling averaging and zero conversion cycle time. There is no digital bus activity aside from reading temperature data one time each second. As shown in Figure 38, the SHE stabilization time in still air is greater when the device dissipates more power.

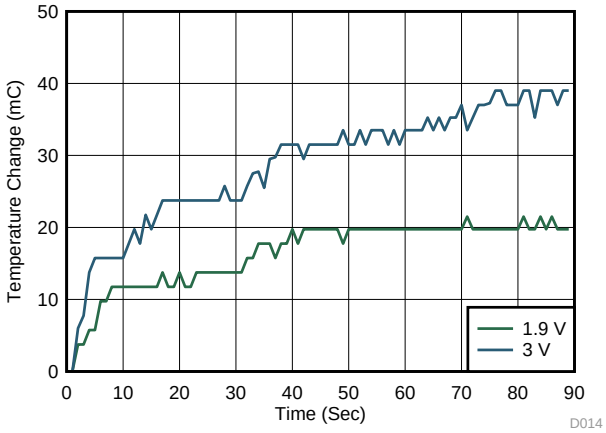


**Figure 38. Self-Heating in Still Air vs. Temperature and Dissipated Power**

The SHE drift is strongly proportional to the device dissipated power. The SHE drift is also proportional to the device temperature because the consumption current with the same supply voltage increases with temperature. Figure 39 shows the SHE drifts versus temperature and dissipated power at 25°C for the same coupon board and the same conditions described previously.

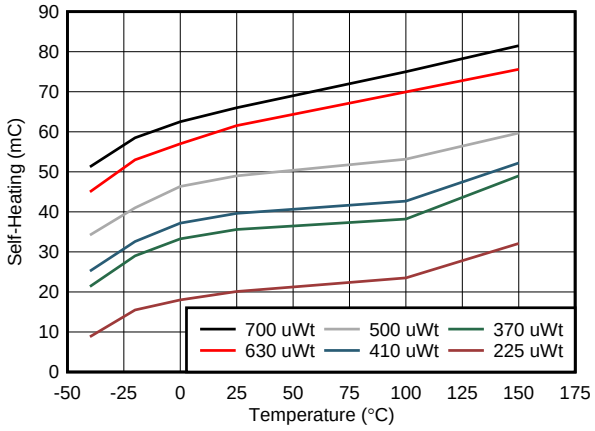


**Figure 39. Self-Heating in Still Air vs. Temperature and Dissipated Power at 25°C**

To estimate the SHE for similar size boards, calculate the device consumption power for 25°C and use the corresponding power line shown in Figure 39. For example, in CC mode without DC at a 3.3-V supply at 25°C, the device dissipates 410 µWt. So self-heating in still air is approximately 40 m°C for the described condition.

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## Application Information (continued)

The following methods can reduce the SHE:

- System calibration removes not only the self-heating error and power-supply rejection ratio (PSRR) effect but also compensates the temperature shift caused by the thermal resistance between the device and the measured object.
- If practical, use the device one-shot mode. If continuous conversion is needed, use the conversion cycle mode with significant standby time. For example, in most cases an 8-sample averaging (125 ms) with a 1-second conversion cycle provides enough time for the device to cool down to the environment temperature and removes the SHE.
- Use the minimal acceptable power supply voltage.
- Use a printed-circuit board (PCB) layout that provides minimal thermal resistance to the device.
- Avoid using small-value pullup resistors on the SDA and ALERT pins. Instead, use pullup resistors larger than 2 kΩ.
- Ensure that the SCL and SDA signal levels remain below 10% or above 90% of the device supply voltage.
- Avoid heavy bypass traffic on the data line. Communication to other devices on the same data line increases the supply current even if the device is in SD mode.
- Use the highest available communication speed.

#### 8.1.1.2.4 Synchronized Temperature Measurements

When four temperature measurements are needed in four different places simultaneously, triggering a reset is recommended. In this method, four devices are programed with control registers set to CC mode with a conversion cycle time of 16 s. All four devices are connected to same two-wire bus with four different bus addresses. The bus general-call reset command is issued by the master. This command triggers all devices to reset (which takes approximately 1.5 ms) and triggers a simultaneous temperature sampling according to configuration registers setting. The master has 16 seconds to read data from the devices.

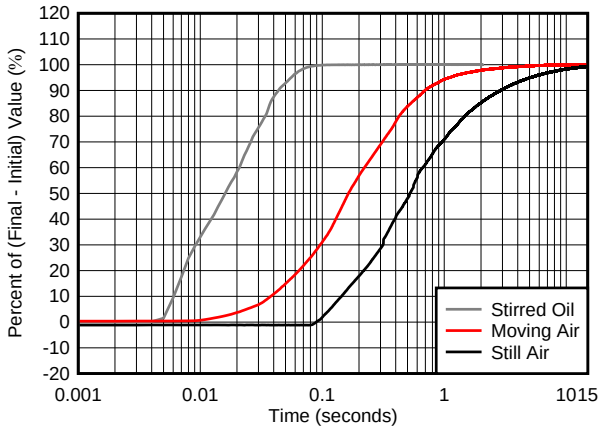
## Application Information (continued)

### 8.1.1.3 Application Curve

Figure 40 shows how fast the TMP117 reacts to changes in temperature. Two elements must be considered when conducting the thermal responses experiment: the thermal conductivity and thermal mass. Thermal conductivity is the measure of the capacity of a material (such as still air or stirred oil) to conduct heat. Thermal conductivity is mainly used to describe how heat is conducted through a material. Higher values reflect greater efficiency of transferring heat. A good layout technique is to keep the thermal mass as small as possible. Smaller thermal masses result in better thermal responses.

The purpose of these experiments is to investigate how much time is required for the TMP117 temperature to reach the set point temperature and stabilize. There are three types of tests for the thermal response: still air, moving air, and stirred oil, as shown in Figure 40. This figure shows the step response of the TMP117 enclosed in a chamber of still air, in a wind tunnel of moving air, and submerged in an oil bath (for the respective traces) in a temperature environment of 70°C from room temperature (23°C). The time-constant, or the time for the output to reach 63% of the input step is dependent on the type of test. The time-constant result depends on the PCB and the thickness of the board that the TMP117 is mounted to. For this test, the TMP117EVM is used to perform the thermal response. The TMP117EVM dimension is 7.6 mm × 17.8 mm with a 1-mm thickness.

Among all methods, still air has the slowest thermal response because of the enclosed box placed inside the oven chamber without any helping elements, whereas the stirred oil experiment yields the fastest thermal response time.




V+ = 3.3 V, $t_{INITIAL}$ = 23°C, $t_{FINAL}$ = 70°C

**Figure 40. Thermal Response**

ADVANCE INFORMATION

# 9 Power Supply Recommendations

The TMP117 operates on a power-supply range from 1.9 V to 5.5 V. The device is trimmed for operation at a 3.3-V supply, but can measure temperature accurately in the full supply range. A power-supply bypass capacitor is required, which must be placed as close to the supply and ground pins of the device as possible. A typical value for this supply bypass capacitor is 100 nF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

The TMP117 is a very low-power device that generates low noise on the supply bus. The user can apply an RC filter to the V+ pin of the device to further reduce noise that the TMP117 might propagate to other components. $R_F$ in Figure 41 must be less than 0.5 kΩ and $C_F$ must be at least 100 nF. The package thermal pad is not connected to the device ground and can be left floating for convenience or grounded for better thermal resistance.

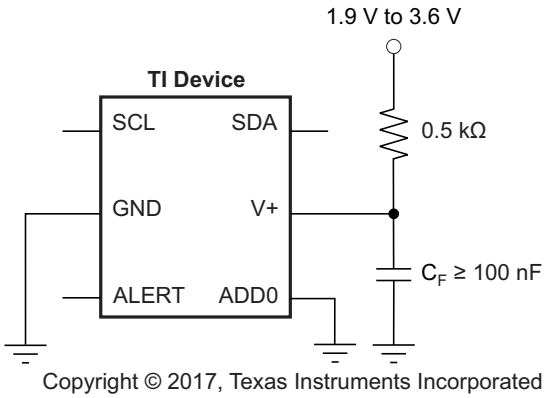



**Figure 41. Noise-Reduction Techniques**

# 10 Layout

## 10.1 Layout Guidelines

**NOTE**

To achieve a high-precision temperature reading for a rigid PCB, do not solder down the thermal pad. For a flexible PCB, the user can solder the thermal pad to increase board level reliability.

For more information on board layout, refer to the related *Precise Temperature Measurements With TMP116* (SNOA986) and *Wearable Temperature Sensing Layout Considerations Optimized for Thermal Response* (SNIA021) application reports on ti.com.

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 μF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. In some cases, the pullup resistor can be the heat source, therefore, maintain some distance between the resistor and the device. Mount the TMP117 on the PCB pad to provide the minimum thermal resistance to the measured object surface or to the surrounding air. The recommended PCB layout minimizes the device self-heating effect, reduces the time delay as temperature changes, and minimizes the temperature offset between the device and the object.

## 10.2 Layout Example

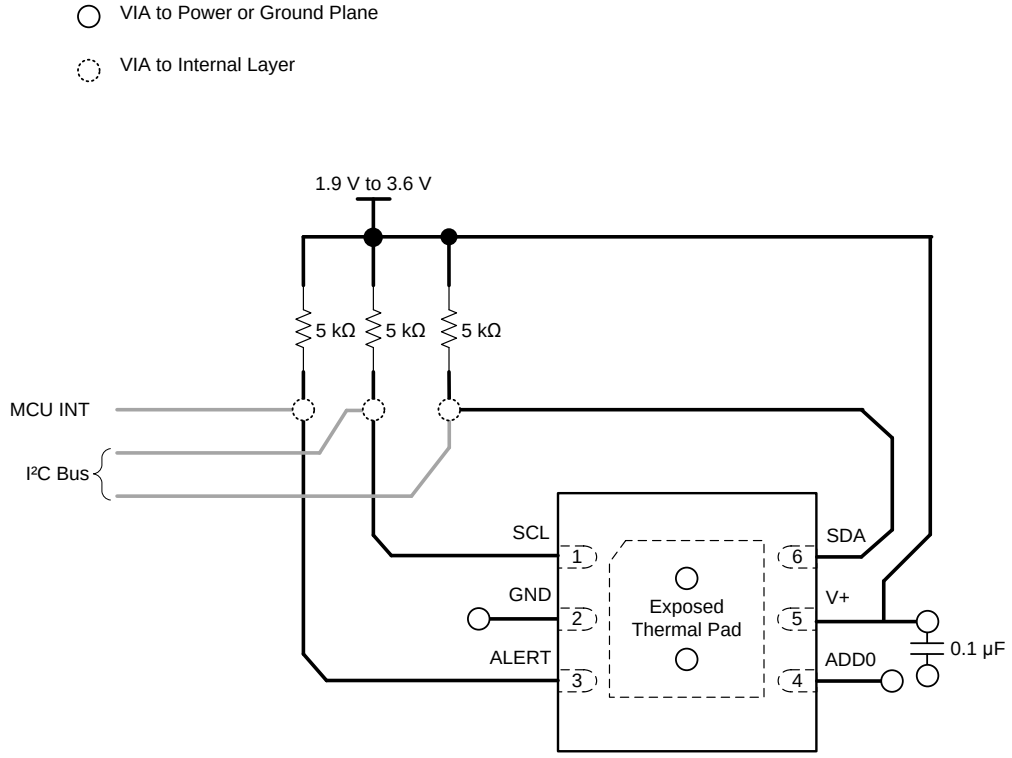



**Figure 42. Layout Recommendation**

ADVANCE INFORMATION

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

- *TMPx75 Temperature Sensor With I²C and SMBus Interface in Industry Standard LM75 Form Factor and Pinout* (SBOS288)
- *TMP275 ±0.5°C Temperature Sensor With I2C and SMBus Interface in Industry Standard LM75 Form Factor and Pinout* (SBOS363)
- *TMP116 Ambient Air Temperature Measurement* (SNOA966)
- *Replacing Resistance Temperature Detectors with the TMP116 Temp Sensor* (SNOA969)
- *Temperature Sensors: PCB Guidelines for Surface Mount Devices* (SNOA967)
- *Precise Temperature Measurements With TMP116* (SNOA986)
- *Wearable Temperature Sensing Layout Considerations Optimized for Thermal Response* (SNIA021)

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.
SMBus is a trademark of Intel Corporation.
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTMP117AIDRVR | ACTIVE | WSON | DRV | 6 | 3000 | TBD | Call TI | Call TI | -55 to 150 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

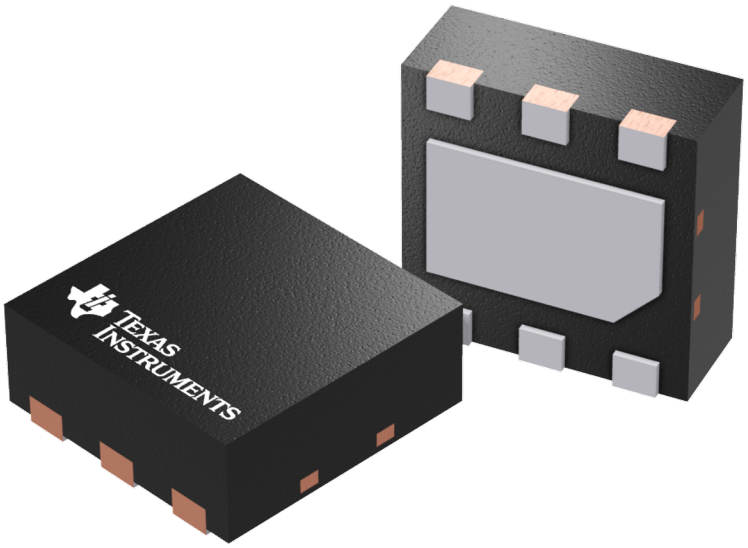
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

# DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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