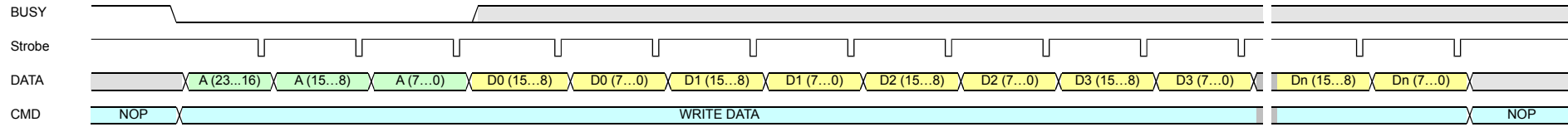
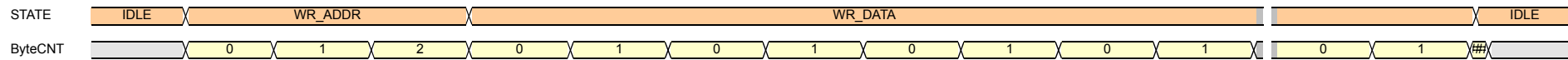


CPU INTERFACE

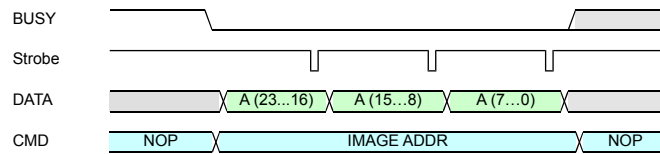
CPU Control Signals (Write new Image Data to SDRAM with Start Address)



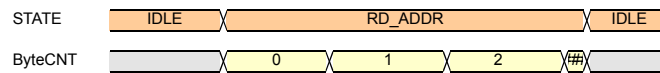
Interne States



CPU Control Signals (Write new Image Start Address)



Interne States



	CMD (1)	CMD (0)
NOP	0	0
WRITE DATA	0	1
IMAGE ADDR	1	0
<i>unused</i>	1	1