# Section 7. DDS as a Clock Generator

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Clock Generator Defined

A clock generator should produce a precisely timed logic pulse train with very low edge jitter and a fixed duty cycle. The logic output levels should be compatible with the device(s) that it will be "clocking". Precise timing implies a very high-Q oscillator; low edge jitter implies high noise immunity. While these attributes are relatively easy to accommodate for a single frequency, for example, a crystal clock oscillator; how can a designer accommodate the need for multiple clock frequencies that need to be changed frequently or rapidly and that have no integer relationship with each other? This is where the DDS shines! With a single precise pulse train that times the *assembly* of new sine wave *samples*, the DDS can output $2^{N-1}$ discrete frequencies (where N is the DDS resolution in bits). These frequencies range from dc to one-half the input clock frequency at intervals of $1/2^N$.

The DDS Clock Generator

The DDS output is a sampled sine wave containing <u>many</u> extraneous frequency components that will create jitter if used "as is". The amount of jitter resulting from an unfiltered sampled sine wave is equal to 1 input clock cycle. If a clock cycle is 5.7ns (175 MHz) then that much jitter will be observed from an accumulation of adjacent cycles of the DDS output signal. Figure 1 shows an unfiltered sampled sine wave from a DDS being clocked at 175 MHz. Only about 3 samples per cycle are being synthesized; however, the cycle-to-cycle samples are different as is evident by the change in voltage levels of the samples as they progress from left to right. This waveform represents about 56 MHz. When this signal is routed to a comparator with a fixed zero-crossing threshold, the 1 clock period jitter becomes visible with the scope in the infinite persistence mode. Incidentally, the jitter magnitude is the same if only the MSB of the 10-bit input code to the DAC were to be examined.
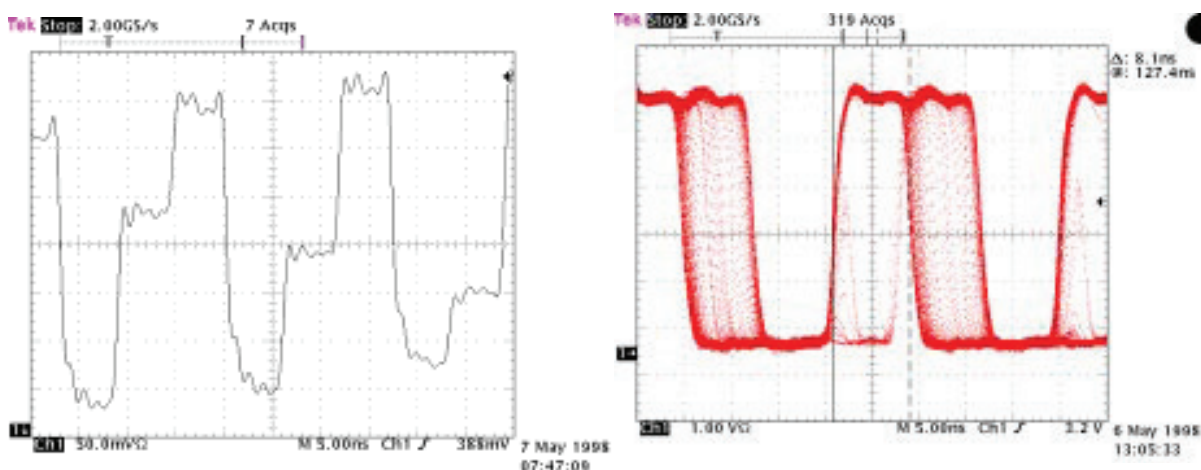
Figure 7-1. "Raw" DAC Output and Corresponding 1 Clock-period Jitter from a Comparator

Six nanoseconds of clock jitter are unsuitable for most clock applications. By low-pass or band-pass filtering the DDS output signal, many of the extraneous signals can be removed from the

DDS output and a nearly pure sine wave is extracted at the filter's output. When the filtered signal is presented to the comparator, edge jitter of the "squared-up" logic output signal reduces from 1 clock period to approximately 250 picoseconds peak-to-peak (including the jitter of the measurement instrument). Filtering can reduce the jitter to a certain level and thereafter, further filtering is ineffective due to the inherent jitter associated with the comparator being used. Effective filtering can be achieved inexpensively with a low pass filter that reduces spurious components to a level at least -50 dB (preferably more) relative to the fundamental signal. For the AD985X DDS products, the on-chip comparator has an inherent edge jitter of approximately 80 picoseconds peak-to-peak. This indicates that with better filtering the clock signal jitter can be reduced even further. Figure 7-2 shows the effect of filtering the sampled DAC output signal seen in Figure 7-1 with a $7^{th}$ order elliptic low pass filter with a cutoff (-3dB) frequency of approximately 65 MHz.
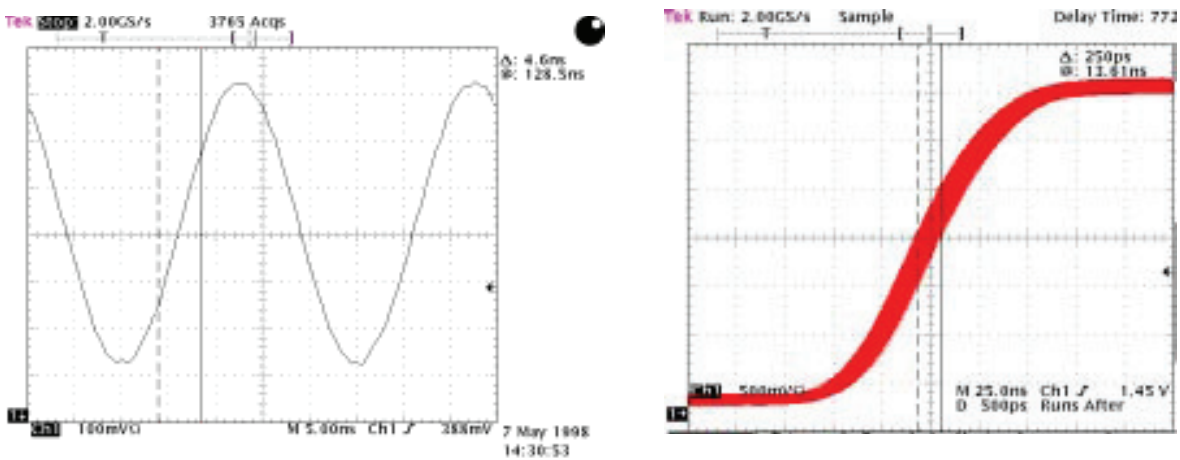


Figure 7-2. Filtered DAC Output and Corresponding Comparator Edge Jitter

Figure 7-3 below shows a frequency domain view of the DDS/DAC output before and after filtering with a simple 65 MHz $7^{th}$ order elliptic low pass filter. The low pass filter does nothing to remove *aliased* harmonics of the fundamental that fall within the legitimate passband of the DDS output. For this reason, band-pass filtering would be a better choice when only a narrow segment of the DDS passband is needed.
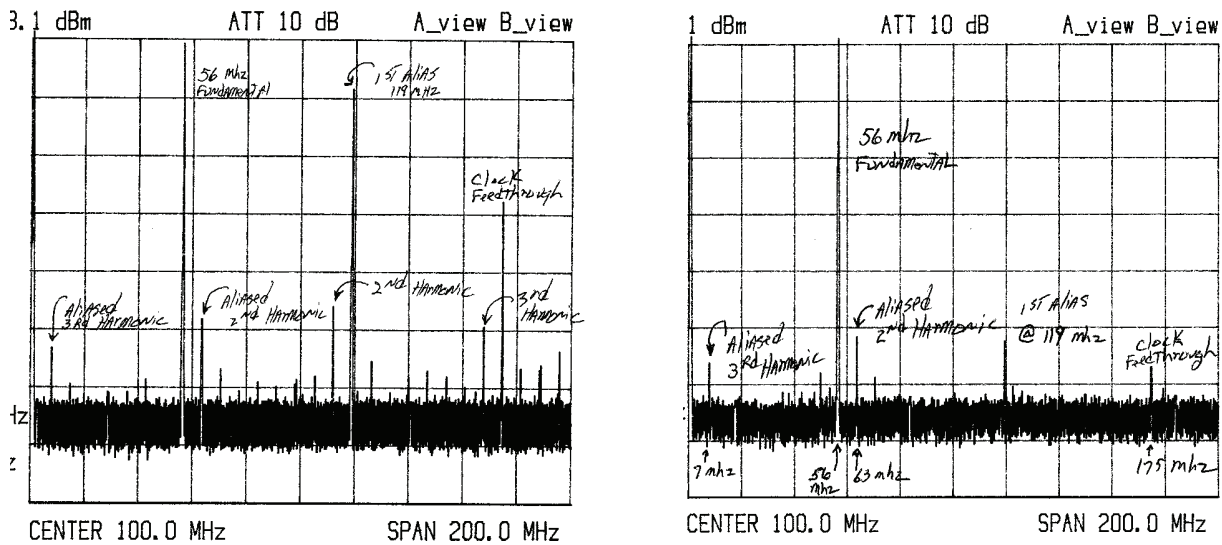
Figure 7-3: DDS/DAC Output Spectrum Before and After 65 MHz Elliptic LPF

Shown in Figure 7-4 below is the schematic diagram of the elliptic low pass filter used in a typical clock generator application. The input and output impedance of the filter has been designed for 200-Ohms to allow the 10 ma current output of the DDS/DAC to develop a 1-volt p-p signal at the output of the filter. The large output signal increases the signal slew rate and overdrive at the comparator switching threshold which reduces jitter caused by internal input noise. The 200-Ohm impedance also makes the filter more susceptible to component tolerance error, output impedance mismatch and complicates filter examination with customary 50-Ohm instruments. Figure 5 shows the swept frequency response of the filter using the tracking generator of a spectrum analyzer.

A 50% duty cycle at the comparator output is maintained by the averaging circuit composed of R4, R5 and C1. This circuit simply combines the unfiltered Iout and IoutB complementary DAC signals which should be of equal p-p amplitude and provides low pass filtering. The result is a dc voltage that equals the center point of the sampled sine wave. This voltage is used as the comparator threshold at the inverting input to the comparator. This circuit tracks amplitude variations and compensates the dc level at the comparator threshold input to maintain the 50% output duty cycle.
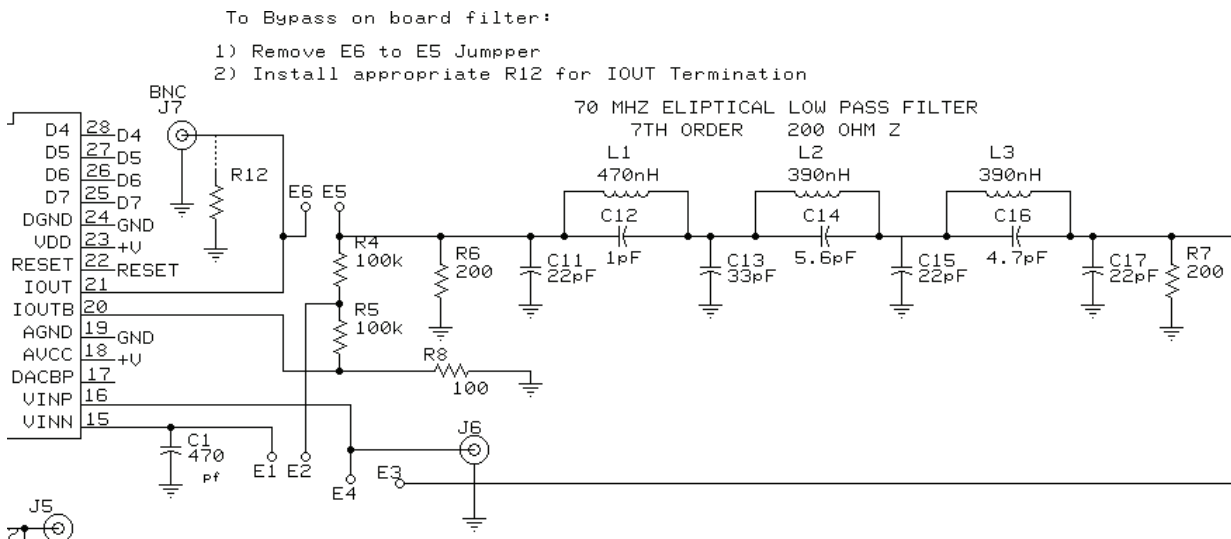
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Figure 7-4. Elliptical Filter Design for Clock Generator Application

The circuit shown in Figure 7-4 is the lowpass filter and threshold voltage averaging circuit for the DDS Clock Generator application.  Operation requires the following connections to be made. E5 to E6, E3 to E4, E1 to E2.
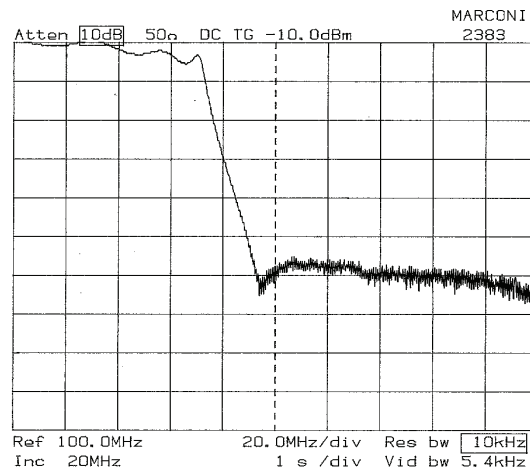


Figure 7-5. Frequency Sweep Plot of Lowpass Filter

The frequency sweep of the above filter shows the approximately –60dB stopband beginning only 25 MHz beyond the cutoff frequency approximately 70 MHz passband.  (Vertical scale = 10 dB per division).

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