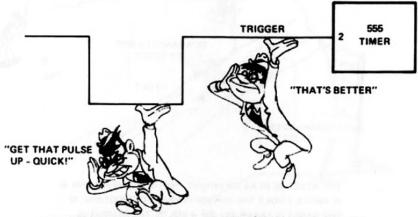
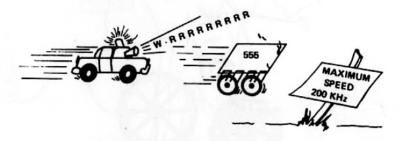
## TRIGGER MODE



THE DEVICE TRIGGERS ON THE NEGATIVE GOING EDGE OF A LOW GOING PULSE. THE TRIGGER PULSE MUST BE OF SHORTER DURATION THAN THE "RC" TIME INTERVAL. IF THE TRIGGER IS HELD LOW, THE OUTPUT WILL STAY HIGH UNTIL TRIGGER IS DRIVEN HIGH AGAIN.

## MAXIMUM OSCILLATION FREQUENCY



THE 555 TIMER IS CAPABLE OF OSCILLATING AT UP TO 300 KHz. HOWEVER, FOR TEMPERATURE STAB-ILITY THE LIMIT SHOULD BE AROUND 200 KHz.

# GUARANTEED NOT TO RESET VCC VCC GUARANTEED NOT TO RESET VCC GUARANTEED RESET

THE RESET ACTS AS AN INHIBIT. WHEN THE RESET (PIN 4) IS ABOVE 1 VOLT THE DEVICE IS FREE TO FUNCTION. IF THE RESET IS TAKEN BELOW .4 VOLTS, THE OUTPUT IS FORCED LOW. WHEN THE RESET IS RELEASED, THE OUTPUT WILL STILL REMAIN LOW UNTIL A TRIGGER PULSE IS APPLIED.



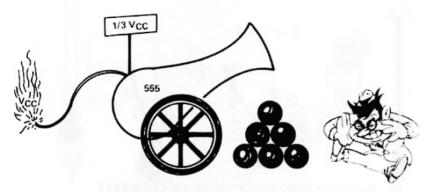
THE INITIAL ACCURACY IS THE TIMING REPEATABILITY FROM DEVICE TO DEVICE AND ALSO THE SAME DEVICE TODAY, TO-MORROW AND 3 YEARS FROM NOW, WITH THE SAME "RC" NETWORK AND SUPPLY VOLTAGE. TYPICALLY, THE NE555 HAS A 1% INITIAL ACCURACY.

## THRESHOLD VOLTAGE

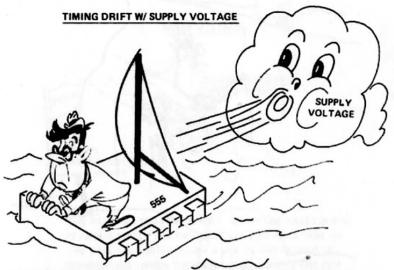


WHEN TRIGGERED, THE TIMER STARTS ITS TIMING CYCLE BY DRIVING THE OUTPUT, PIN 3, HIGH. SIMULTANEOUSLY, THE TIMING CAPACITOR STARTS CHARGING FROM ITS STEADY-STATE LEVEL AT GROUND. WHEN IT REACHES 2/3  $V_{CC}$ , AN INTERNAL COMPARATOR IS TRIPPED, CAUSING THE CAPACITOR TO DISCHARGE TO GROUND. THIS DRIVES THE OUTPUT LOW, ENDING THE TIMING CYCLE.

## TRIGGER VOLTAGE



THE TRIGGER PULSE MUST DROP BELOW 1/3 OF THE SUPPLY VOLTAGE BEFORE THE TIMER TRIGGERS.



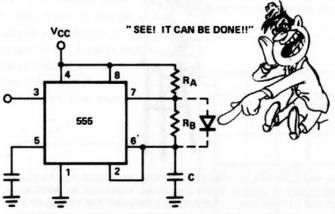
THE TIMING OF THE DEVICE WILL VARY SLIGHTLY WITH CHANGE IN SUPPLY VOLTAGE. THE TYPICAL TIMING DRIFT IS 0.1% PER VOLT.

#### TIMING DRIFT W/ TEMPERATURE



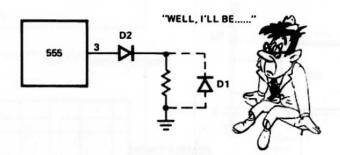
THE TIMER IN THE MONOSTABLE MODE HAS A TIMING DRIFT OF 50 PPM/°C TYPICAL. IN THE ASTABLE MODE, SINCE BOTH COMPARATORS OF THE DEVICE ARE USED, THE DRIFT IS SOMEWHAT GREATER. TYPICALLY 150 PPM/°C DRIFT.

# DUTY CYCLE



THE DUTY CYCLE IS "ON TIME" EXPRESS IN TERMS OF TOTAL CYCLE TIME. THE DUTY CYCLE IS LIMITED, UNDER NORMAL CIRCUMSTANCES, TO 50%. HOWEVER, BY ADDING A DIODE A DUTY CYCLE OF LESS THAN 50% CAN BE ACHIEVED.

#### LATCH UP WHEN DRIVING AN INDUCTIVE LOAD



A NEGATIVE VOLTAGE AT PIN 3 CAN CAUSE A LATCH UP. THE SOLUTION IS TO ADD TWO DIODES AS SHOWN. THIS CIRCUIT PROHIBITS A NEGATIVE VOLTAGE FROM REACHING PIN 3.

#### CONTROL VOLTAGE

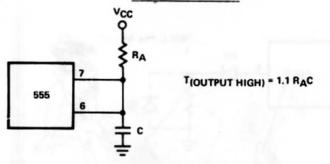


PIN 5, THE CONTROL VOLTAGE PIN, IS PRIMARILY USED FOR FILTERING WHEN DEVICE IS USED IN NOISY ENVIRONS. HOWEVER, BY IMPOSING A VOLTAGE AT THIS POINT, IT IS POSSIBLE TO VARY THE TIMING OF THE DEVICE INDEPENDENTLY OF THE "RC" NETWORK. THE CONTROL VOLTAGE MAY BE VARIED FROM 45% TO 90% OF  $V_{\rm CC}$  IN THE MONOSTABLE MODE, AND FROM 1.7 VOLTS TO  $V_{\rm CC}$  IN THE ASTABLE MODE.

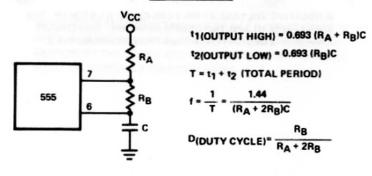
#### FORMULAS



# MONOSTABLE TIMING

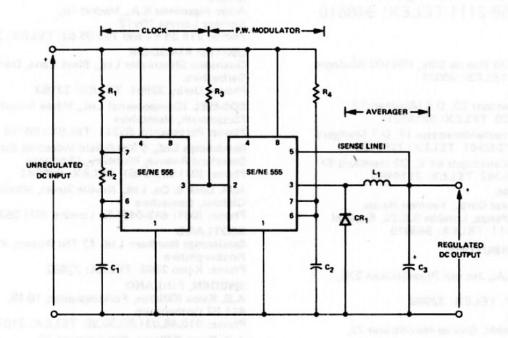


# ASTABLE TIMING



# APPLICATIONS (Cont'd)

## SWITCHING STEP-DOWN REGULATOR



# SCHEMATIC DIAGRAM OF DELAYED LIGHT TURN-OFF

