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SP8735

600MHz÷8 (BINARY OUTPUTS)

The SP8735 is a ÷8 ECL counter with binary outputs. In addition, carry outputs are provided in TTL and ECL. The AC coupled input requires a 600mV p-p signal and the outputs are open collectors. A TTL compatible reset is provided, making this device ideal for instrumentation applications.

FEATURES

- Binary Outputs to Open Collectors
- TTL Compatible Reset Input
- AC Coupled Input (Internal Bias)
- TTL and ECL Compatible Carry Outputs
- ECL Compatible Clock Inhibit Input

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 400mW
- Temperature Range: 0°C to +70°C

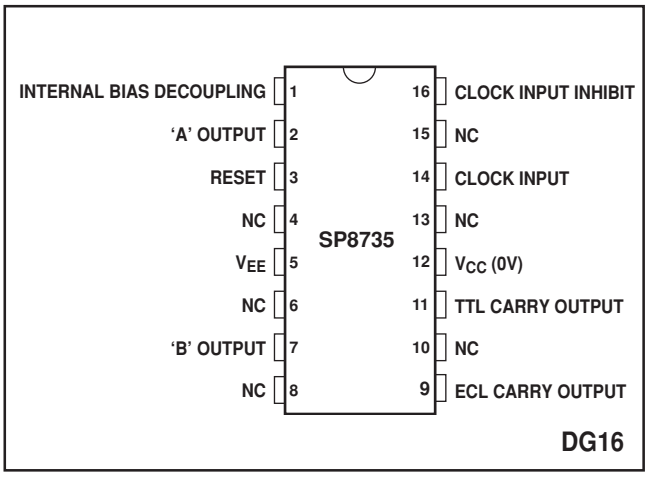


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−8V
Binary output voltage	V_{EE}+11V
Storage temperature range	−55°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8735 B DG

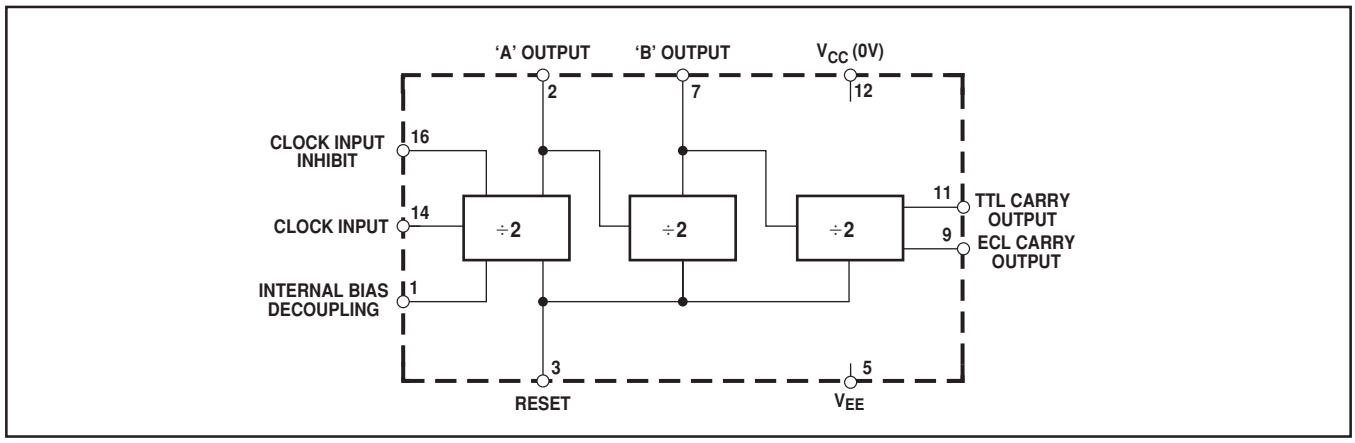


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V±0·25V
Temperature, T_{AMB} = 0°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	600		MHz	Input = 400-800mV p-p	4
Minimum toggle frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	6
Power supply current	I_{CC}		90	mA	V_{EE} = −5·2V	5
Clock inhibit high voltage	V_{INH}	−0·96		V	V_{EE} = −5·2V (25°C)	
Clock inhibit low voltage	V_{INL}		−1·65	V	V_{EE} = −5·2V (25°C)	
TTL output high voltage (pins 2, 7)	V_{OH}	2·4		V	10kΩ from TTL output to +5V	5
TTL output low voltage (pins 2, 7)	V_{OL}		0·4	V	10kΩ from TTL output to +5V	5
TTL carry output high voltage (pin 11)	V_{OH}	2·4		V	5kΩ from TTL output to +5V	5
TTL carry output low voltage (pin 11)	V_{OL}		0·4	V	5kΩ from TTL output to +5V	5
ECL output high voltage (pin 9)	V_{OH}	−0·9	−0·7	V	V_{EE} = −5·2V (25°C)	
ECL output low voltage (pin 9)	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
Edge speed for correct operation at maximum frequency	t_E		2·5	ns	10% to 90%	6
Reset ON time for correct operation	t_{ON}	100		ns		6
Reset input high voltage	V_{INH}	2·4		V		5
Reset input low voltage	V_{INL}		0·5	V		5

NOTES
1. The temperature coefficient of V_{OH} (ECL) = +3mV/°C and V_{OL} = +0·5mV/°C but these are not tested.
1. The temperature coefficient of inhibit threshold voltage = +0·24mV/°C but this is not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 0°C and +70°C only.
5. Tested at +25°C only.
6. Guaranteed but not tested.

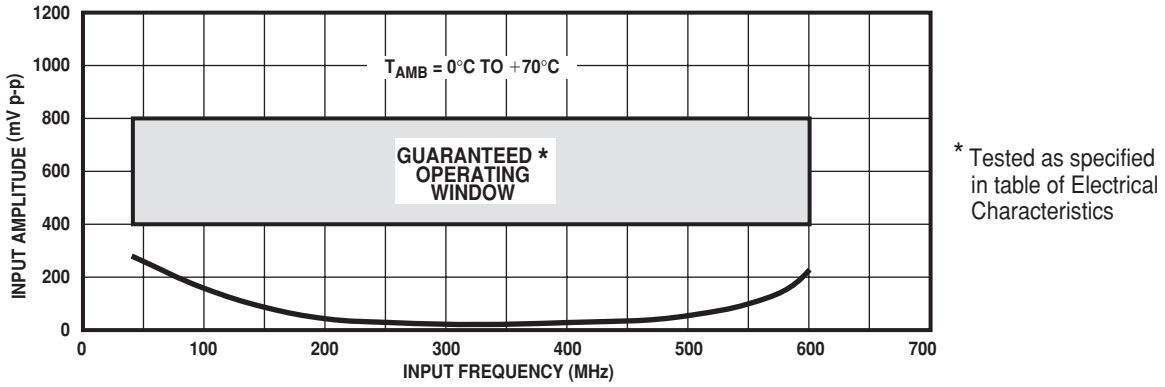


Fig. 3 Typical input characteristic

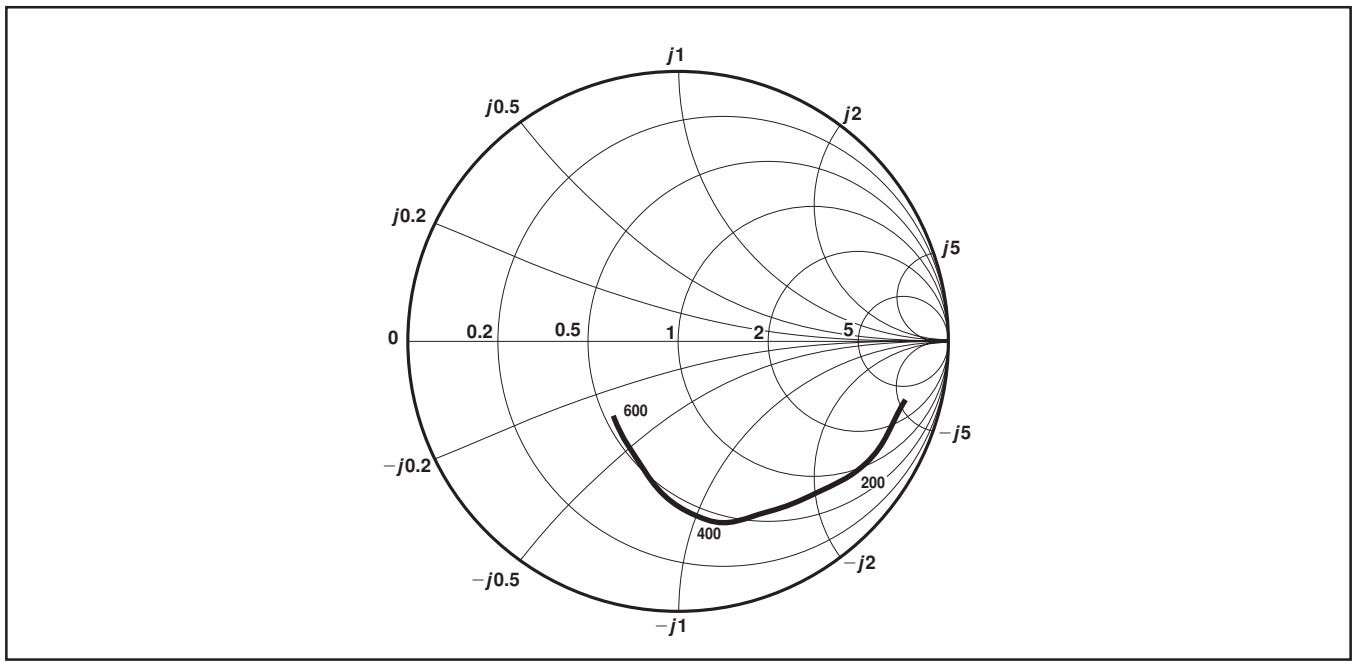


Fig. 4 Typical input impedance. Test conditions: supply voltage = −5·2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

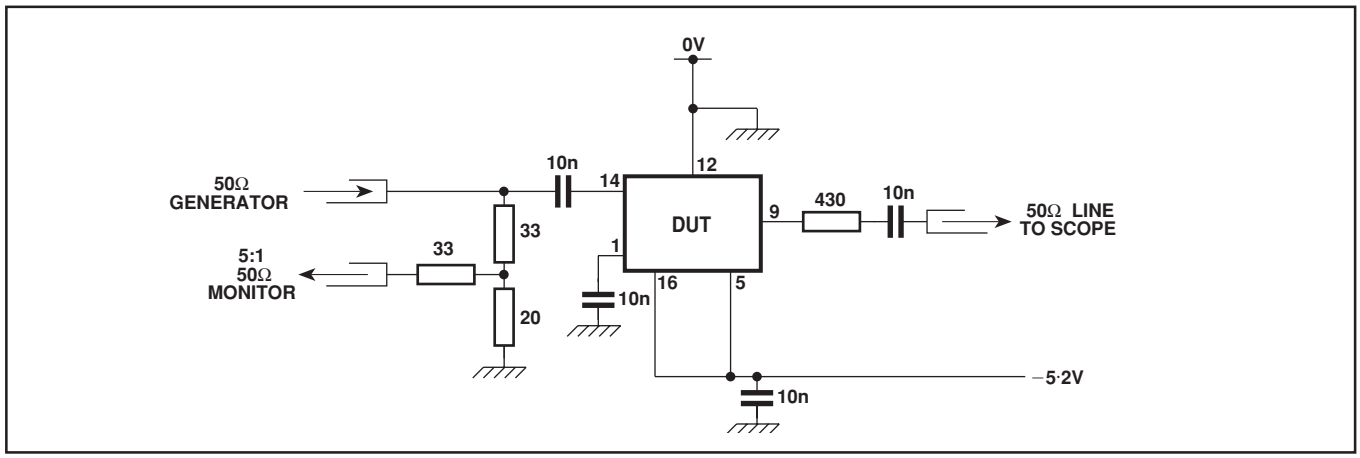


Fig. 5 SP8735 high frequency test circuit

OPERATING NOTES

1. The clock input (pin 14) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling (pin 1) to ground.
2. In the absence of a signal the device will self-oscillate. This can be prevented by connecting a 68kΩ resistor between the clock input (pin 14) and the negative supply (pin 5).
3. The device will operate down to DC but the input slew rate must be better than 100V/μs.
4. The ECL carry output (pin 9) is ECLII compatible but can be interfaced to ECLIII/10K by the addition of two resistors as shown in Fig. 7.
5. The clock inhibit is compatible with ECLIII/10K throughout the temperature range.
6. The 'A', 'B' and TTL carry outputs (pin 11) are current sources and require the addition of 10kΩ resistors (pins 2 and 7) and a 5kΩ resistor (pin 11) to +5V as shown in Fig. 6. This gives a fan-out of 1, which can be increased by buffering with a PNP transistor as shown in Fig. 6.
7. The circuits are clocked on the positive transitions of the clock input, provided that the clock inhibit input (pin 16) is in the low state.
8. Input impedance varies as a function of frequency; see Fig. 4

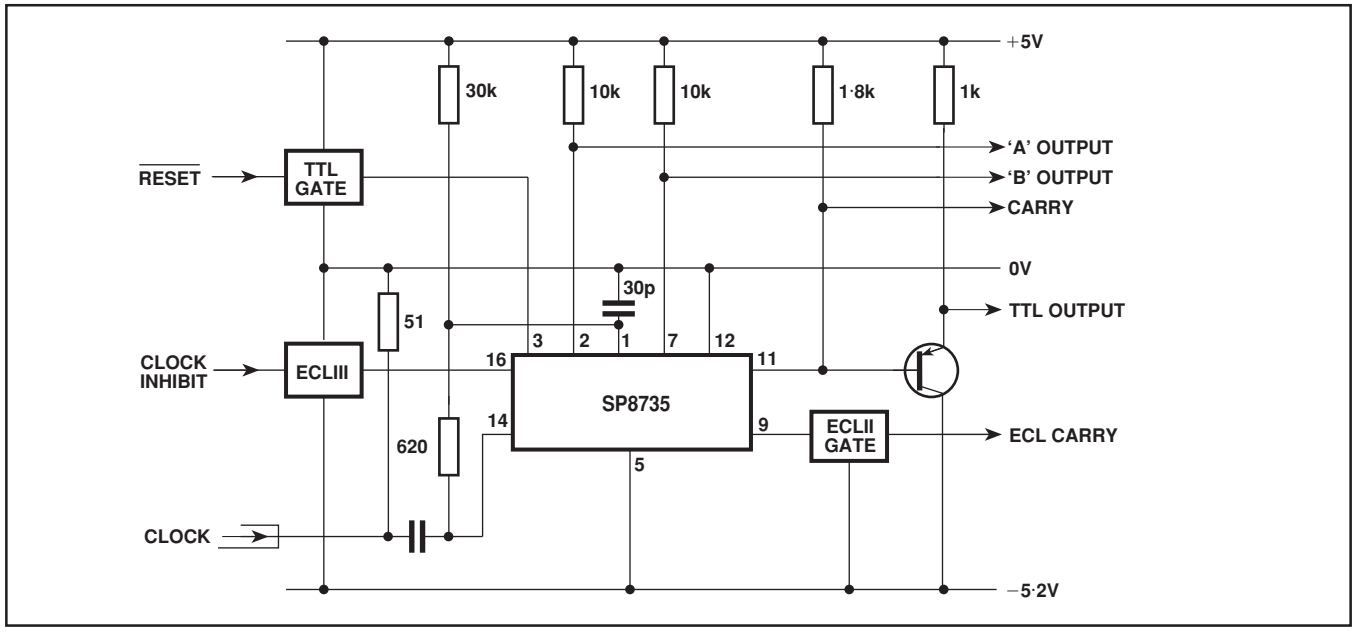


Fig. 6 Typical application configuration

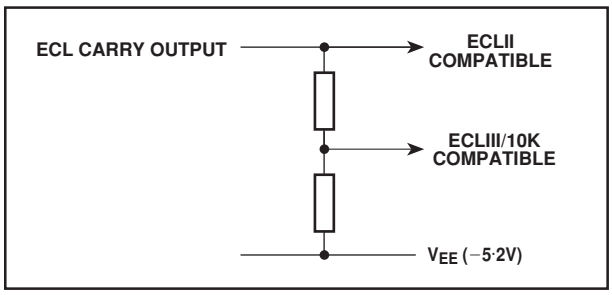


Fig. 7 ECLIII/10k interfacing

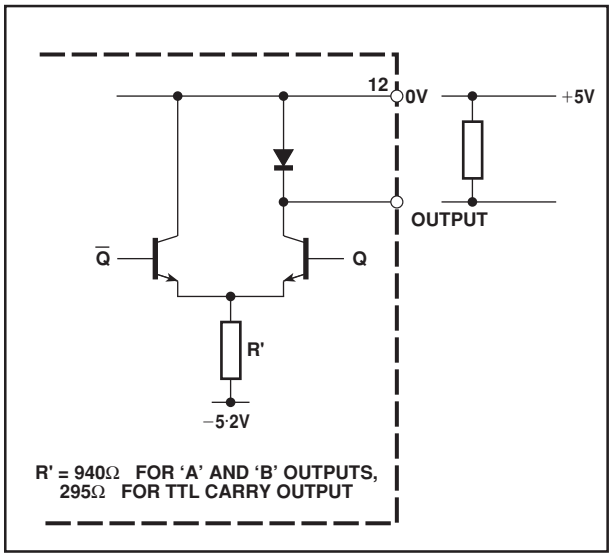


Fig. 8 TTL output circuit

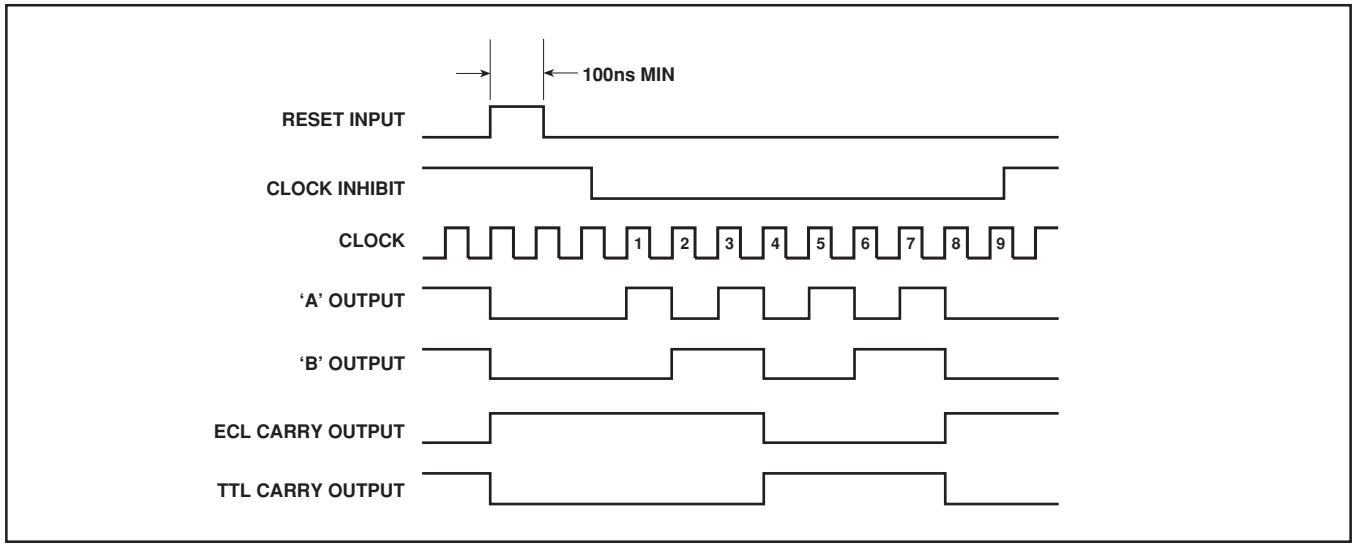
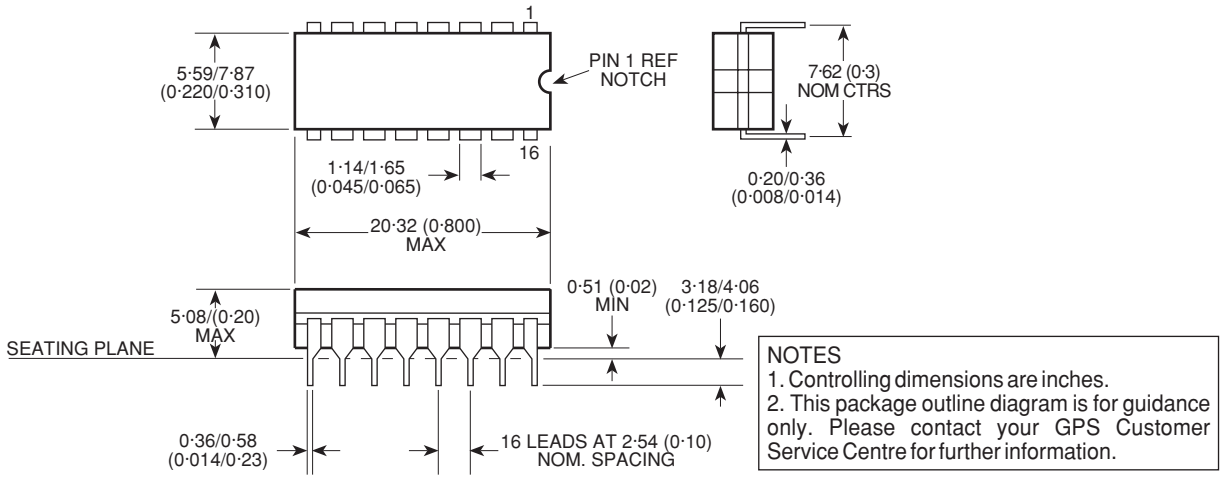


Fig.9 Timing diagram

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

16-LEAD CERAMIC DIL – DG16

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