11

Butler Crystal Oscillator Design

11.1 Introduction

This chapter introduces the Butler oscillator topology, which is named after its inventor. It is a topology that is popular with oscillator designers for frequencies above 50 MHz. The discrete topology shown in Figure 11.1 is Butler's emitter follower. The topology has no parasitics of any kind [1] and it is very repeatable in production. The topology has the advantage that it can oscillate at any crystal mode, that is, fundamental or overtone (third, fifth, seventh, and so forth) with only value changes. This makes a single PCB layout very useful for covering a wide range of frequencies.

The Butler emitter follower topology is a free-running oscillator circuit. By free running, we mean that the crystal can be replaced with a resistor and the circuit can oscillate close to the desired frequency. The free running is a useful feature that will be used to pretune the oscillator at the correct frequency before the introduction of the crystal into the circuit.

In this topology, the transistor emitter presents a low-impedance drive to match to the crystal. It is an emitter follower, which means no voltage gain ($V/V = 1$) but provides current amplification. The Butler emitter follower is a good performing circuit for a high-frequency overtone operation.

11.2 Butler's Emitter Follower Oscillator Operation

Understanding how the Butler emitter follower operates is actually straightforward. Let us break the circuit at the base junction and draw its ac equivalent circuit as shown in Figure 11.2. We start at the base in which the base-to-emitter

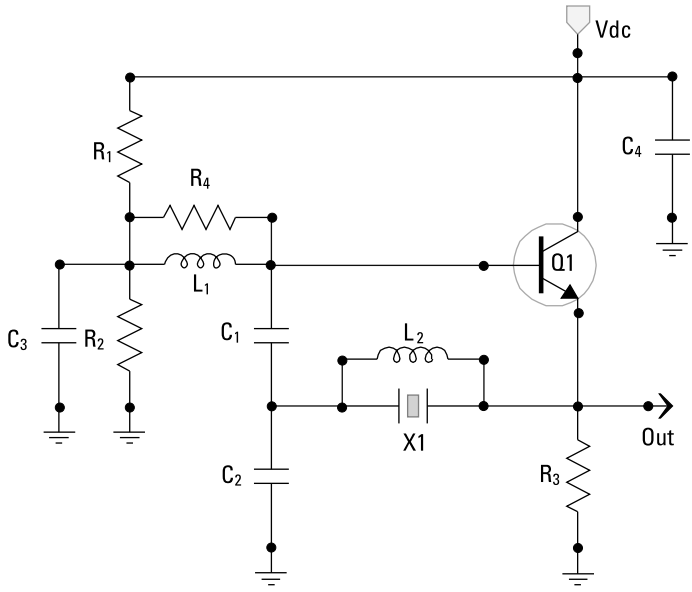

Figure 11.1 Butler's emitter follower crystal oscillator. It operates the crystal at series resonance: easy to tune, no parasitics.

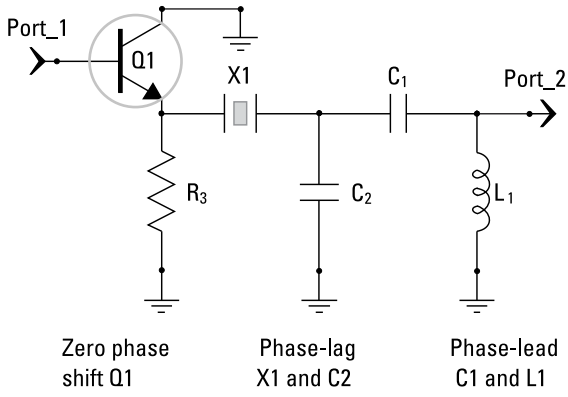

Figure 11.2 Butler emitter follower open-loop ac equivalent.

voltage gain is 1 and with a phase shift of 0 (or nearly 0). The crystal X1 in the steady state is at series resonance, so it looks resistive with a value equal to its motional resistance R_1. The capacitor C_2 acts as a capacitive load to the crystal and together with R_1 form a phase-lag network. The capacitor C_1 and inductor L_1 form a phase-lead network to advance the phase such that the Barkhausen criteria for phase shift around the loop are satisfied.

As C_1 and L_1 provide all the necessary phase lead necessary around the loop, their proper selection is critical. When the phase lead is set to a frequency other than the frequency of oscillation, the circuit can behave erratically.

The combination of C_1, C_2, and L_1 will also be selected to provide sufficient loop gain in the design procedure that will follow.

The resistor R_4 in Figure 11.1 is critical and its primary function is to de-Q the phase-lead inductor L_1. Without R_4, L_1 can take over the as the resonator in the circuit, creating a free-running condition.

The inductor L_2 is there to resonate out the shunt capacitance C_0 of the crystal if needed. Notice that L_1 is going to ac ground at the junction of R_1 and R_2 and, because of this, I prefer to use low values for R_1 and R_2 (less than 10 kilo-ohms).

11.3 Butler's Emitter Follower Design Procedure

The procedure that follows has some rule-of-thumb guidelines that I have tailored over the years based on personal design experience with the Butler emitter follower topology.

1. Choose the transistor. Select a transistor that has a transition frequency f_T that is ten times higher than the frequency of operation. With such a transistor, the phase shift from base to emitter will be negligible. For a high-performance oscillator (i.e., good short-term stability), select a transistor with a low $1/f$ noise. Unfortunately, this parameter is rarely specified by the transistor manufacturer. Try different transistors until one is found that meets the required phase noise/short-term stability.
2. With regard to transistor bias, for most +5-V supply operations, it will suffice to set the emitter current initially to ~5 mA and the base voltage to between +2.5V and +3V. Simulation after the initial values will confirm these assumptions.
3. The base resistors, R_1 and R_2, are typically chosen in the range of 2 to 10 kilo-ohms. The emitter resistor R_3 sets the emitter to ~5 mA in conjunction with the base resistors.
4. Select the value of the Butler inductor L_1 such that its reactance is equal to 100 ohms.
5. With the value of L_1 selected, C_1 can be derived by resonating it with L_1 at the frequency of operation.
6. Select C_2 to be between three to ten times larger than C_1. A higher ratio is even possible. Optimize C_2 by simulation to maximize the loaded Q of the oscillator.

7. The inductor L_2 must be used when the crystal's shunt capacitance C_0 starts to bypass the oscillator signal around the crystal. When this occurs, the oscillator will free-run and not be crystal controlled. Calculate the value of L_2 such that it resonates with the shunt capacitance C_0.
8. The resistor R_4 is critical and should not be omitted. I have found that a value between 1 and 3.3 kilo-ohms has worked well. This resistor will lower the open-loop gain; the smaller its value, the lower the open-loop gain. Performing start-up tests over temperature and power range will validate if the value chosen is correct. The oscillator should not jump away from crystal control under these or any conditions.
9. Select the crystal. This topology can be designed with a fundamental or any overtone crystal. The crystal will not need to provide any phase shift at the steady state and therefore it has to be series-resonant crystal. Because C_2 is a capacitive load to the crystal, the motional resistance of the crystal and C_2 not only form a lag network, but they will also affect the loop gain. This means going back and adjusting (if necessary) the value of C_2 depending of the motional resistance of the crystal. I optimize C_2 during the open-loop gain simulation once the crystal motional parameters are known. Simulate this initial design and make sure the open-loop gain (s21) is greater than 6 dB with all the components chosen.

11.4 Butler's Emitter Follower VCXO Design Example

Design a 155.52-MHz VCXO using Butler's emitter follower topology for a +5-V supply operation. Given are the crystal parameters:

- Frequency: 155.52 MHz;
- Load: Series;
- Mode of operation: Fundamental;
- Motional resistance: 35 ohms maximum;
- Motional capacitance: 7 fF typical;
- Shunt capacitance: 2.2 pF;
- Frequency stability: ±25 ppm over −10°C to +70°C;

Design the VCXO with a minimum pull range of ±50 ppm with a control voltage of +0.5V to +4.5V and centered at +2.5V.

Solution:

Because we need to design a VCXO, we will add at least one varactor to Figure 11.1. The best place to add a varactor in this topology is in series with the crystal. We will add the varactor between the emitter and crystal and not between the junction of C_1, C_2, and the crystal. The advantage of this location is that any noise on the control line will be filtered by the crystal. The VCXO schematic is shown in Figure 11.3.

We have added five additional components to the schematic of Figure 11.1 to convert into a VCXO. Resistors R_5 and R_6 will be high values (>10 kilo-ohms) to isolate the oscillator loop. Resistor R_6 isolates the oscillator from the control voltage line while R_5 is the dc return for the reversed bias varactor DV1. The capacitor C_5 is now needed to dc block the control voltage on the varactor. The inductor L_3 will bring back the oscillator to series resonance that has been shifted by the capacitive reactance of the varactor. Hence, L_3 will be chosen to compensate (series resonate) the varactor capacitance value at the center control voltage.

The first task is to select a transistor with an f_T of 1.5 GHz or higher. Let us assume that we have selected such a transistor. Using the guidelines for the bias, we have selected 2.2 kilo-ohms for the two base resistors and 360 ohms for the emitter resistor.

The Butler inductor L_1 is selected to have a reactance of 100 ohms. That is,

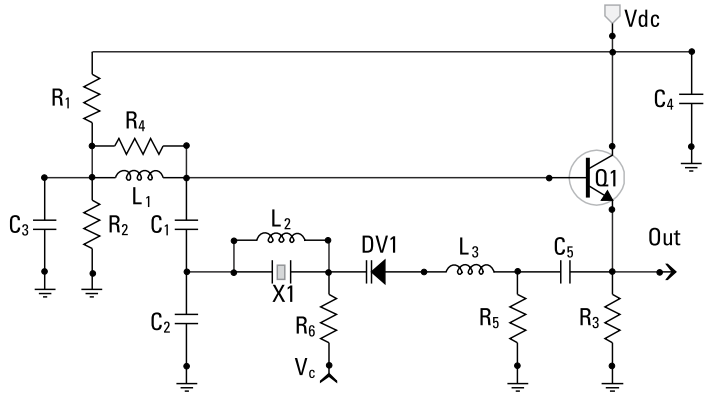

Figure 11.3 Butler's emitter follower VCXO schematic.

$$L_1 = \frac{100}{2\pi(155.52\ \text{MHz})} = 102.3\ \text{nH}$$

We therefore select 100 nH for L_1 which is a standard value. Next we calculate the value of C_1 by resonating it with L_1. Therefore,

$$C_1 = \frac{\left(\frac{1}{2\pi(155.52\ \text{MHz})}\right)^2}{100\ \text{nH}} = 10.47\ \text{pF}$$

The value of L_2 is calculated by resonating it with the shunt capacitance of the crystal. Therefore,

$$L_2 = \frac{\left(\frac{1}{2\pi(1.55.25\ \text{MHz})}\right)^2}{2.2\ \text{pF}} = 476\ \text{nH}$$

We now have enough information to perform an open-loop analysis. The open-loop analysis is where I select a value for C_2. A value of 82 pF has been selected and for C_2 and 3,300 ohms for R_4, which were optimized during the open-loop analysis. Figure 11.4 is our open-loop schematic and Figure 11.5 shows the gain and phase response [2].

The results in Figure 11.5 show that we have an open-loop gain of 11.35 dB at 155.5 MHz, which is a good result. The peak open-loop gain aligns well with the 0° phase shift point. Note the 35-ohm resistor added to simulate the motional resistance of the crystal. The oscillator will free-run with this 35-ohm resistor at 155.5 MHz in place of the crystal. Once built, the free-run frequency will be lower than 155.5 MHz, which we desire so that the circuit will not lock to one of the crystal spurs which exist above its series frequency. This circuit should oscillate reliably under all conditions.

We have so far designed a CLOCK and not a VCXO. We need our VCXO to pull the crystal frequency by ±50 ppm minimum. A crystal resonator is a reactance meter with the motional parameter at hand. This means that the crystal frequency can be calculated exactly knowing its reactive load or vice versa. That reactance load can also be calculated exactly knowing the crystal frequency in circuit.

Selecting the correct varactor that will achieve the ±50-ppm pullability will be instructive to understand exactly how the frequency is being varied by

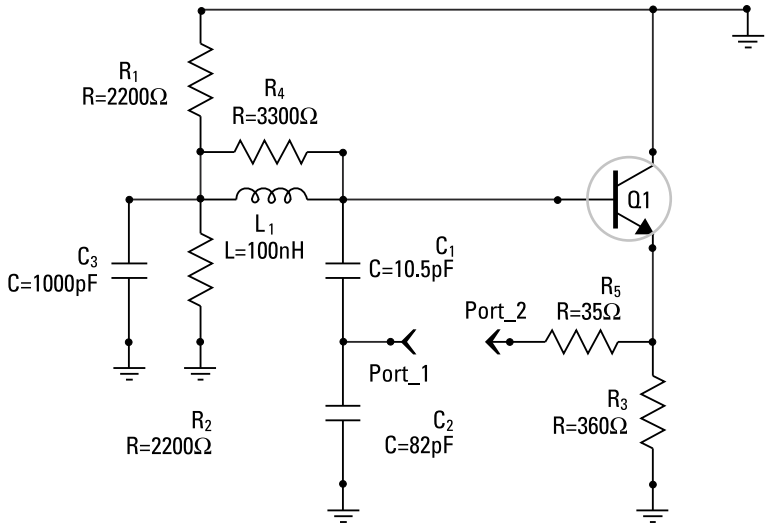

Figure 11.4 Open-loop schematic of VCXO design problem.

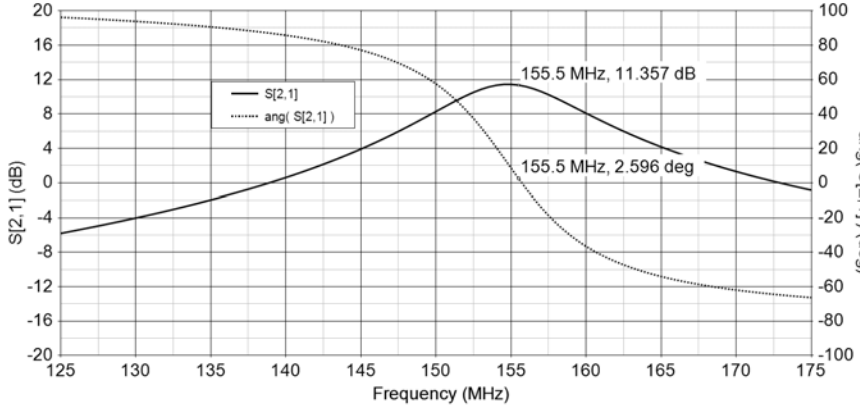

Figure 11.5 Gain-phase response of Figure 11.4.

the varactor. Recall from above that the crystal has to be series-resonant, which is the same as saying there is no reactive component at the oscillating frequency. Hence, the oscillator frequency will be at the point that the series combination of the crystal X1, the varactor DV1, and the inductor L_3 look resistive. This series branch is resistive when the imaginary part of its impedance is zero. In other words, the varactor is varying the frequency by moving the point at which the imaginary branch is equal to zero in direct proportion to the control voltage.

A VCXO designer is limited with the availability varactor choices. This forces us to go through an iterative exercise in the selection of the varactor. I

have written a MathCad file to aid in selecting an appropriate varactor. The file works by entering the motional parameters of the crystal, the pull required, and the center capacitance value of the varactor. The file will then calculate the inductor (L_3) value necessary to resonate out the varactor and the inductor (L_2) necessary to compensate the shunt capacitance. Most importantly, the file solves numerically the varactor capacitance range necessary to meet the required pull.

In the following MathCad [3] file, we have entered our VCXO requirements. A varactor with a capacitance value of 20 pF when the control voltage is +2.5V has been chosen. From this, MathCad calculated L_3 to be 52.36 nH and L_2 to be 476 nH. The file also calculated that the varactor maximum low value has to be 15.55 pF and the minimum varactor high value has to be 28 pF. Under these conditions, the VCXO will pull our required ±50 ppm minimum.

To calculate the varactor capacitance range required to meet the above pull, set the imaginary part of above impedance equation to zero under the unknown high and low varactor capacitance conditions.

This MathCad file calculates the capacitance range needed by a varactor in a series-resonant VCXO.

Enter the crystal motional parameters below

$$C1 := 7 \cdot 10^{-15} \quad R1 := 35 \quad L1 := 149.613137 \cdot 10^{-6} \quad C0 := 2.2 \cdot 10^{-12}$$

The crystal series frequency is:

$$Fs := \frac{1}{2 \cdot \pi \cdot \sqrt{L1 \cdot C1}} \quad Fs = 155.51999983 \times 10^{6}$$

$Cv := 20 \cdot 10^{-12}$ ⇐ Enter chosen/proposed varactor center capacitance; that is, varactor capacitance at mid control voltage.

The inductor necessary to compensate the varactor center capacitance is:

$$L3 := \frac{\left(\frac{1}{2 \cdot \pi \cdot Fs}\right)^2}{Cv} \quad L3 = 5.23646 \times 10^{-8}$$

Enter below the minimum required pull range

$$\text{Plus\_pull} := 50C \quad \text{Minus\_pull} := 50$$

Calculating the required pull in Hertz becomes:

$$\text{FL\_low} := \text{Fs} - \frac{\text{Fs} \cdot \text{Minus\_pull}}{10^6} \quad \text{FL\_low} = 1.555122 \times 10^8$$

$$\text{FL\_high} := \text{Fs} - \frac{\text{Fs} \cdot \text{Plus\_pull}}{10^6} \quad \text{FL\_high} = 1.555278 \times 10^8$$

With the shunt capacitance compensated with an inductor value of:

$$L2 := \frac{\left(\frac{1}{2 \cdot \pi \cdot Fs}\right)^2}{C0} \quad L2 = 4.760418 \times 10^{-7}$$

The impedance of the series combination of Cv, L_3, R_1, C_1, and L_1 is:

In order to calculate the varactor capacitance range required to meet the above pull, set the imaginary part of the above impedance equation to zero under the unknown high and low varactor capactinace conditions.

Guesses

$$\text{Cv\_low} := 10 \cdot 10^{-12} \quad \text{Cv\_high} := 30 \cdot 10^{-12}$$

Given

$$\text{Im}\left(Z\left(\text{FL\_low}, \text{Cv\_high}\right)\right) = 0$$

$$\text{Im}\left(Z\left(\text{FL\_high}, \text{Cv\_low}\right)\right) = 0$$

$$\begin{pmatrix} \text{Var\_cap\_low} \\ \text{Var\_cap\_high} \end{pmatrix} := \text{Find}\left(\text{Cv\_low}, \text{Cv\_high}\right)$$

$$\text{Var\_cap\_low} = 1.555426 \times 10^{-11} \Leftarrow \text{Maximum varactor low value}$$

$$\text{Var\_cap\_low} = 2.800364 \times 10^{-11} \Leftarrow \text{Minimum high value}$$

In this example, the varactor is centered at 20 pF, and at minimum control voltage, the varactor capacitance must be 28 pF or greater. With the control voltage set maximum, the varactor capacitance must be 15.5 pF or smaller.

Let us check with GENESYS [2] our varactor branch MathCad calculations. We have set up the varactor series branch as shown in Figure 11.6.

Let us check if our series branch calculations are correct, we will sweep C_1 in Figure 11.6 from 15 pF to 28 pF. The simulation results are shown in Figure 11.7.

Figure 11.7 shows that the imaginary part of the varactor series branch is zero at 155.512 MHz (−51.44 ppm) when C_1 = 28 pF. When C_1 = 15 pF, the frequency is 155.529 MHz (+57.87 ppm). These results match with our MathCad calculations and our VCXO design will meet the pullability specification requirement.

Our VCXO is now complete as shown in Figure 11.8 using standard values for the components. If a standard value inductor does not exist close to the calculated value, then add an additional capacitor such that the series combination equals the calculated value of the single inductor. There are more standard values for capacitors than for inductors.

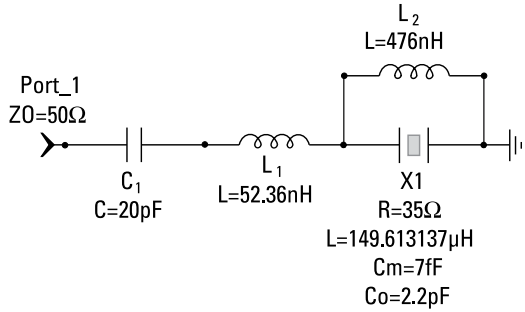

Figure 11.6 Varactor series branch from Figure 11.3. The capacitor C_1 represents the varactor at center capacitance.

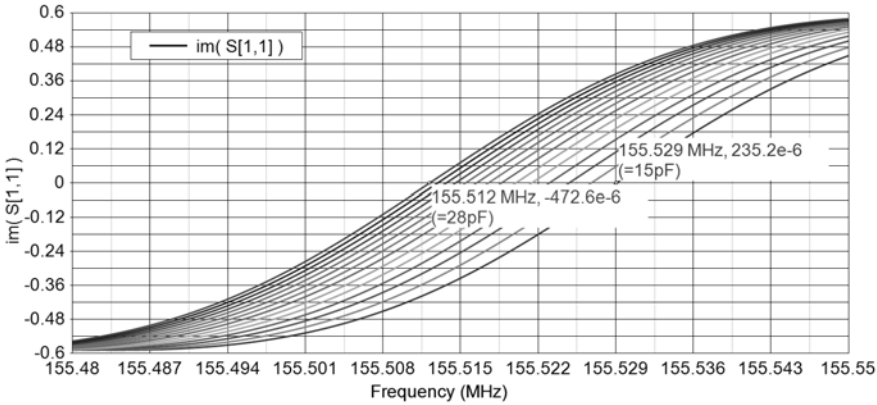

Figure 11.7 Simulation result of sweeping equivalent varactor capacitance (C_1) of Figure 11.6 from 15 pF to 28 pF in 1-pF steps.

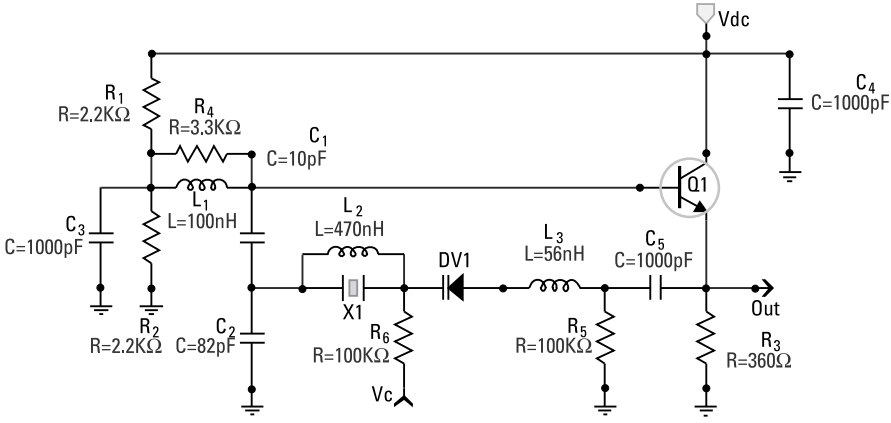

Figure 11.8 Completed 155.520-MHz VCXO problem using standard component values.

11.5 Butler Gate Oscillator

The Butler emitter follower can also be designed with digital gates instead of a discrete transistor. A very popular configuration is shown in Figure 11.9 using PECL gates.

This gate version of the Butler oscillator works exactly as the discrete transistor, that is, the function of L_1, C_1, C_2, and R_1 are all the same as in Figure 11.1. The capacitor C_3 is simply a bypass capacitor. The pull-down resistors R_2 and R_3 on the output of the first gate are needed because the PECL gates being utilized are open emitters.

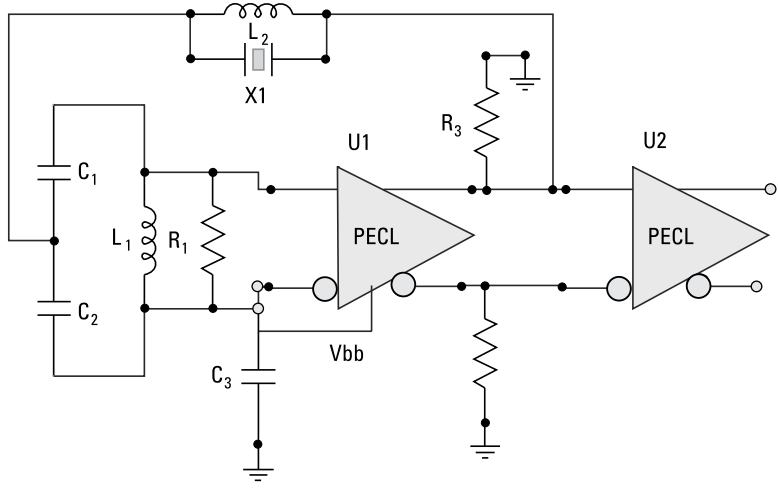

Figure 11.9 Butler crystal oscillator using PECL gates.