

6502 MICROPROCESSOR

INSTRUCTION SET SUMMARY

INSTRUCTIONS		IMMEDIATE	ABSOLUTE	ZERO PAGE	ACCUM.	IMPLIED	(IND),X	(IND),Y	Z,PAGE,X	ABS,X	ABS,Y	RELATIVE	INDIRECT	Z,PAGE,Y	CONDITION CODES					
MNEMONIC	OPERATION	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	N	Z	C	I	D	V
A D C	A + M + C → A (4)(1)	69 2 2	6D 4 3	65 3 2			61 6 2	71 5 2	75 4 2	7D 4 3	79 4 3				✓	✓	✓	-	-	✓
A N D	A ^ M → A (1)	29 2 2	2D 4 3	25 3 2			21 6 2	31 5 2	35 4 2	3D 4 3	39 4 3				✓	✓	✓	-	-	-
A S L	C ← 7.....0 ← 0		0E 6 3	06 5 2	0A 2 1				16 6 2	1E 7 3					✓	✓	✓	-	-	-
B C C	BRANCH ON C=0 (2)											90 2 2			-	-	-	-	-	-
B C S	BRANCH ON C=1 (2)											B0 2 2			-	-	-	-	-	-
B E Q	BRANCH ON Z=1 (2)											F0 2 2			-	-	-	-	-	-
B I T	A ^ M		2C 4 3	24 3 2											M ₇	✓	-	-	-	M ₆
B M I	BRANCH ON N=1 (2)											30 2 2			-	-	-	-	-	-
B N E	BRANCH ON Z=0 (2)											D0 2 2			-	-	-	-	-	-
B P L	BRANCH ON N=0 (2)											10 2 2			-	-	-	-	-	-
B R K	(See Fig 1)					00 7 1									-	-	-	✓	-	-
B V C	BRANCH ON V=0 (2)											50 2 2			-	-	-	-	-	-
B V S	BRANCH ON V=1 (2)											70 2 2			-	-	-	-	-	-
C L C	0 → C					18 2 1									-	-	0	-	-	-
C L D	0 → D					D8 2 1									-	-	-	0	-	-
C L I	0 → I					58 2 1									-	-	-	0	-	-
C L V	0 → V					B8 2 1									-	-	-	-	0	-
C M P	A - M (1)	C9 2 2	CD 4 3	C5 3 2			C1 6 2	D1 5 2	D5 4 2	DD 4 3	D9 4 3				✓	✓	✓	-	-	-
C P X	X - M	E0 2 2	EC 4 3	E4 3 2											✓	✓	✓	-	-	-
C P Y	Y - M	C0 2 2	CC 4 3	C4 3 2											✓	✓	✓	-	-	-
D E C	M - 1 → M		CE 6 3	C6 5 2					D6 6 2	DE 7 3					✓	✓	-	-	-	-
D E X	X - 1 → X					CA 2 1									✓	✓	-	-	-	-
D E Y	Y - 1 → Y					88 2 1									✓	✓	-	-	-	-
E O R	A ◊ M → A (1)	49 2 2	4D 4 3	45 3 2			41 6 2	51 5 2	55 4 2	5D 4 3	59 4 3				✓	✓	-	-	-	-
I N C	M + 1 → M		EE 6 3	E6 5 2					F6 6 2	FE 7 3					✓	✓	-	-	-	-
I N X	X + 1 → X					E8 2 1									✓	✓	-	-	-	-
I N Y	Y + 1 → Y					C8 2 1									✓	✓	-	-	-	-
J M P	JUMP TO NEW LOCATION		4C 3 3										6C 5 3		-	-	-	-	-	-
J S R	JUMP INTO SUBROUTINE		20 6 3												-	-	-	-	-	-
L D A	M → A (1)	A9 2 2	AD 4 3	A5 3 2			A1 6 2	B1 5 2	B5 4 2	BD 4 3	B9 4 3				✓	✓	-	-	-	-

INSTRUCTIONS		IMMEDIATE	ABSOLUTE	ZERO PAGE	ACCUM.	IMPLIED	(IND),X	(IND),Y	Z,PAGE,X	ABS,X	ABS,Y	RELATIVE	INDIRECT	Z,PAGE,Y	CONDITION CODES					
MNEMONIC	OPERATION	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	OP N #	N	Z	C	I	D	V
L D X	M → X (1)	A2 2 2	AE 4 3	A6 3 2							BE 4 3				✓	✓	-	-	-	-
L D Y	M → Y (1)	A0 2 2	AC 4 3	A4 3 2					B4 4 2	BC 4 3					✓	✓	-	-	-	-
L S R	0 → 7.....0 → C		4E 6 3	46 5 2	4A 2 1				56 6 2	5E 7 3					0	✓	✓	-	-	-
N O P	NO OPERATION					EA 2 1									-	-	-	-	-	-
O R A	A v M → A	09 2 2	0D 4 3	05 3 2			01 6 2	11 5 2	15 4 2	1D 4 3	19 4 3				✓	✓	-	-	-	-
P H A	A → Ms, S - 1 → S					48 3 1									-	-	-	-	-	-
P H P	P → Ms, S - 1 → S					08 3 1									-	-	-	-	-	-
P L A	S + 1 → S, Ms → A					68 4 1									✓	✓	-	-	-	-
P L P	S + 1 → S, Ms → P					28 4 1									RESTORED					
R O L	C ← 7.....0 ← C		2E 6 3	26 5 2	2A 2 1				36 6 2	3E 7 3					✓	✓	✓	-	-	-
R O R	C → 7.....0 → C		6E 6 3	66 5 2	6A 2 1				76 6 2	7E 7 3					✓	✓	✓	-	-	-
R T I	RETURN FROM INTERRUPT					40 6 1									RESTORED					
R T S	RETURN FROM SUBROUTINE					60 6 1									-	-	-	-	-	-
S B C	A - M - C → A (1)(3)	E9 2 2	ED 4 3	E5 3 2			E1 6 2	F1 5 2	F5 4 2	FD 4 3					✓	✓	(3)	-	-	✓
S E C	1 → C					38 2 1									-	-	1	-	-	-
S E D	1 → D					F8 2 1									-	-	-	1	-	-
S E I	1 → I														-	-	-	1	-	-
S T A	A → M		8D 4 3	85 3 2			81 6 2	91 6 2	95 4 2	9D 5 3	99 5 3				-	-	-	-	-	-
S T X	X → M		8E 4 3	86 3 2											-	-	-	-	-	-
S T Y	Y → M		8C 4 3	84 3 2					94 4 2						-	-	-	-	-	-
T A X	A → X					AA 2 1									✓	✓	-	-	-	-
T A Y	A → Y					AB 2 1									✓	✓	-	-	-	-
T S X	S → X					BA 2 1									✓	✓	-	-	-	-
T X A	X → A					8A 2 1									✓	✓	-	-	-	-
T X S	X → S					9A 2 1									-	-	-	-	-	-
T Y A	Y → A					98 2 1									✓	✓	-	-	-	-

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|-------------------------------------------------|----------------------------------|----------------|-----------------------------|
| (1) ADD 1 TO "N" IF PAGE BOUNDARY IS CORSSSED | X = X REGISTER | + ADD | - NOT MODIFIED |
| (2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE | Y = Y REGISTER | - SUBTRACT | M ₇ MEMORY BIT 7 |
| ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE | A = ACCUMULATOR | ^ AND | M ₆ MEMORY BIT 6 |
| (3) C = CARRY NOT = BORROW | S = STACK POINTER | v OR | N NUMBER OF CYCLES |
| (4) IF IN DECIMAL MODE, Z FLAG IS INVALID | M = MEMORY PER EFFECTIVE ADDRESS | ◊ EXCLUSIVE OR | # NUMBER OF BYTES |
| ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT | Ms = MEMORY PER STACK POINTER | ✓ MODIFIED | |

6502 MICROPROCESSOR

INSTRUCTION SET OP CODE MATRIX

MSD	LSD															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5		PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6		CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	1
2	JSR ABS 2 3	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5		PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	2
3	BMI Relative 2 2**	AND (IND), Y 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6		SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5		PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6		CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	5
6	RTS Implied 1 6	ADC (IND, X) 2 6\$				ADC ZP 2 3\$	ROR ZP 2 5		PLA Implied 1 4	ADC IMM 2 2\$	ROR Accum 1 2		JMP (ABS) 3 6	ADC ABS 3 4\$	ROR ABS 3 6	6
7	BVS Relative 2 2**	ADC (IND), Y 2 5*\$				ADC ZP, X 2 4\$	ROR ZP, X 2 6		SEI Implied 1 2	ADC ABS, Y 3 4*\$				ADC ABS, X 3 4*\$	ROR ABS, X 3 7	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3		DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	8
9	BCC Relative 2 2**	STA (IND), Y 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4		TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3		TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4		CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 3		INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6		CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	D
E	CPX IMM 2 2	SBC (IND, X) 2 6\$			CPX ZP 2 3	SBC ZP 2 3\$	INC ZP 2 5		INX Implied 1 2	SBC IMM 2 2\$	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4\$	INC ABS 3 6	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*\$				SBC ZP, X 2 4\$	INC ZP, X 2 6		SED Implied 1 2	SBC ABS, Y 3 4*\$				SBC ABS, X 3 4*\$	INC ABS, X 3 7	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

BRK	-> OP Code
Implied	-> Addressing Mode
1 7	-> Instruction Bytes, N = Machine Cycles

- \$ Add 1 to N if in decimal mode
- * Add 1 to N if page boundary is crossed
- ** Add 1 to N if branch occurs to different page
- Add 2 to N if branch occurs to same page