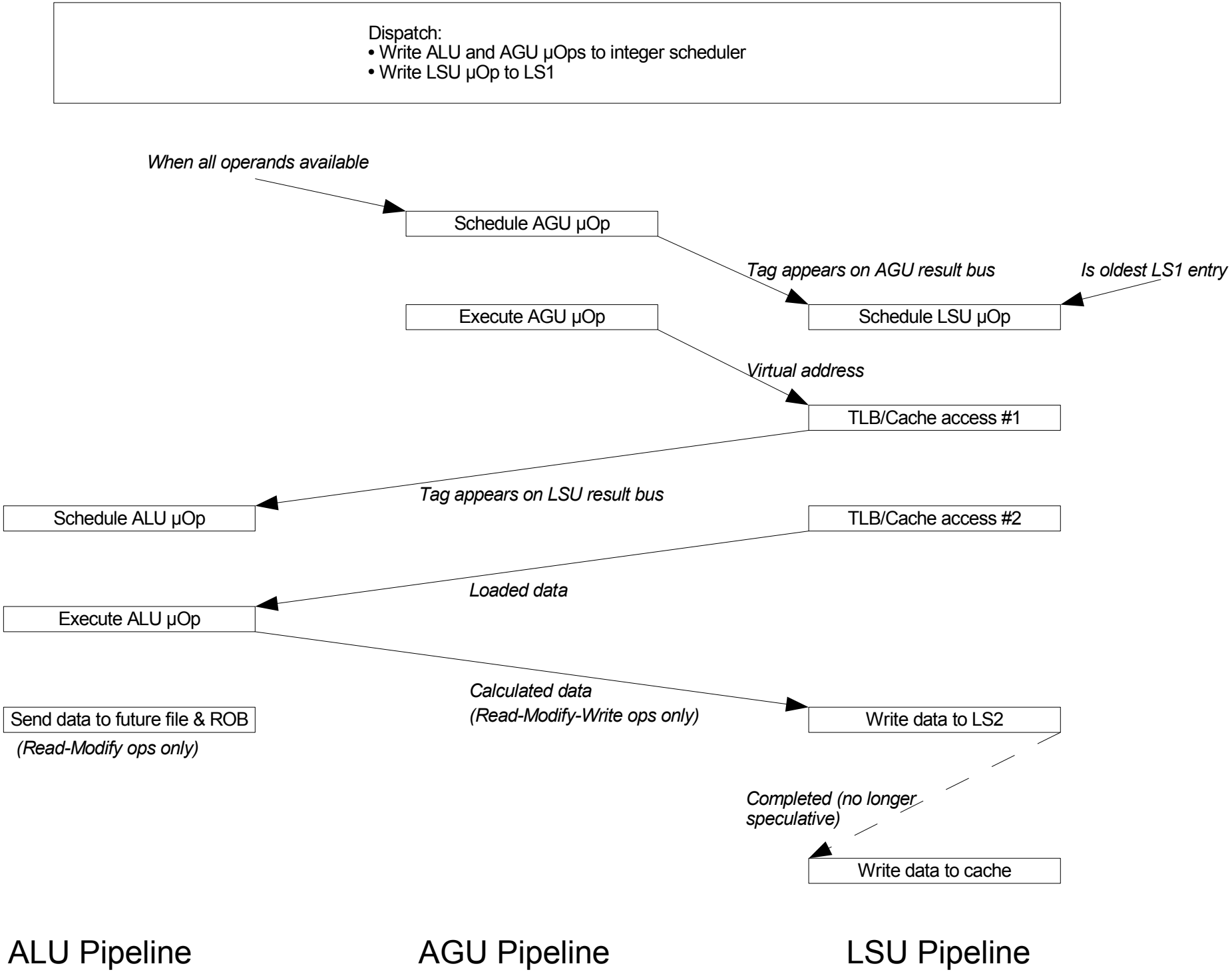
Dispatch:
• Write ALU and AGU µOps to integer scheduler
• Write LSU µOp to LS1
When all operands available
Schedule AGU µOp
Tag appears on AGU result bus
Is oldest LS1 entry
Execute AGU µOp
Schedule LSU µOp
Virtual address
TLB/Cache access #1
Tag appears on LSU result bus
Schedule ALU µOp
TLB/Cache access #2
Loaded data
Execute ALU µOp
Calculated data
(Read-Modify-Write ops only)
Send data to future file & ROB
(Read-Modify ops only)
Write data to LS2
Completed (no longer speculative)
Write data to cache
ALU Pipeline
AGU Pipeline
LSU Pipeline