Raystar Display

IC SPECIFICATION

Model No:

RS0012

MODLE NO：

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2013-10-11		First issue

DESCRIPTION

RS0012 is an OLED Driver/Controller IC utilizing CMOS Technology specially designed to display alphanumeric and Japanese kana characters as well as symbols and graphics. It can interface with either 4-bit, 8-bit, SPI and I2C Microprocessor and display up to one 8-character line or two 8-character lines.

Display RAM, Character Generator, OLED Driver as well as a wide range of instruction functions such as Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Display Character Blink, Cursor Shift, Display Shift are all incorporated into a single chip having the highest performance and reliability. Pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.

FEATURES

CMOS technology
Low power consumption
Microprocessor Interface
-- High-speed 8-bit parallel bi-directional interface with 6800-series or 8080-series
-- Serial interface available
-- I2C interface available
4-bit or 8-Bit MPU interface
High speed MPU interface: 2MHz
128 x 8-bit display RAM (128 characters max.)
Auto power on reset function
5 x 8 and 5 x 10 dot matrix
Built-in oscillator
Programmable duty cycle:
                --Graphic mode--1/1.1/2.1/3.1/4.1/5.1/6.1/7.1/8 and 1/16
1/1 : all com output low in the same time
1/2 : COM1~8 switch together and COM9~16 switch together
1/3 : COM1~5, COM6~10 and COM11~16
1/4 : COM1~4, COM5~8, COM9~12 and COM13~16
1/5 : COM1~3, COM4~6, COM7~9, COM10~12 and COM13~16
1/6 : COM1~2, COM3~4, COM5~6, COM7~8, COM9~10, COM11~16
1/7 : COM1~2, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12 and COM13~16
1/8 : COM1~2, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12 COM13~14 and COM15~16
1/16: COM1,COM2,COM3 ….. COM14,COM15,COM16
--Character mode--1/8.1/11 and 1/16
Build-in selectable four sets of character generator ROM (CGROM)
- English Japanese Character
- Western European Character-I
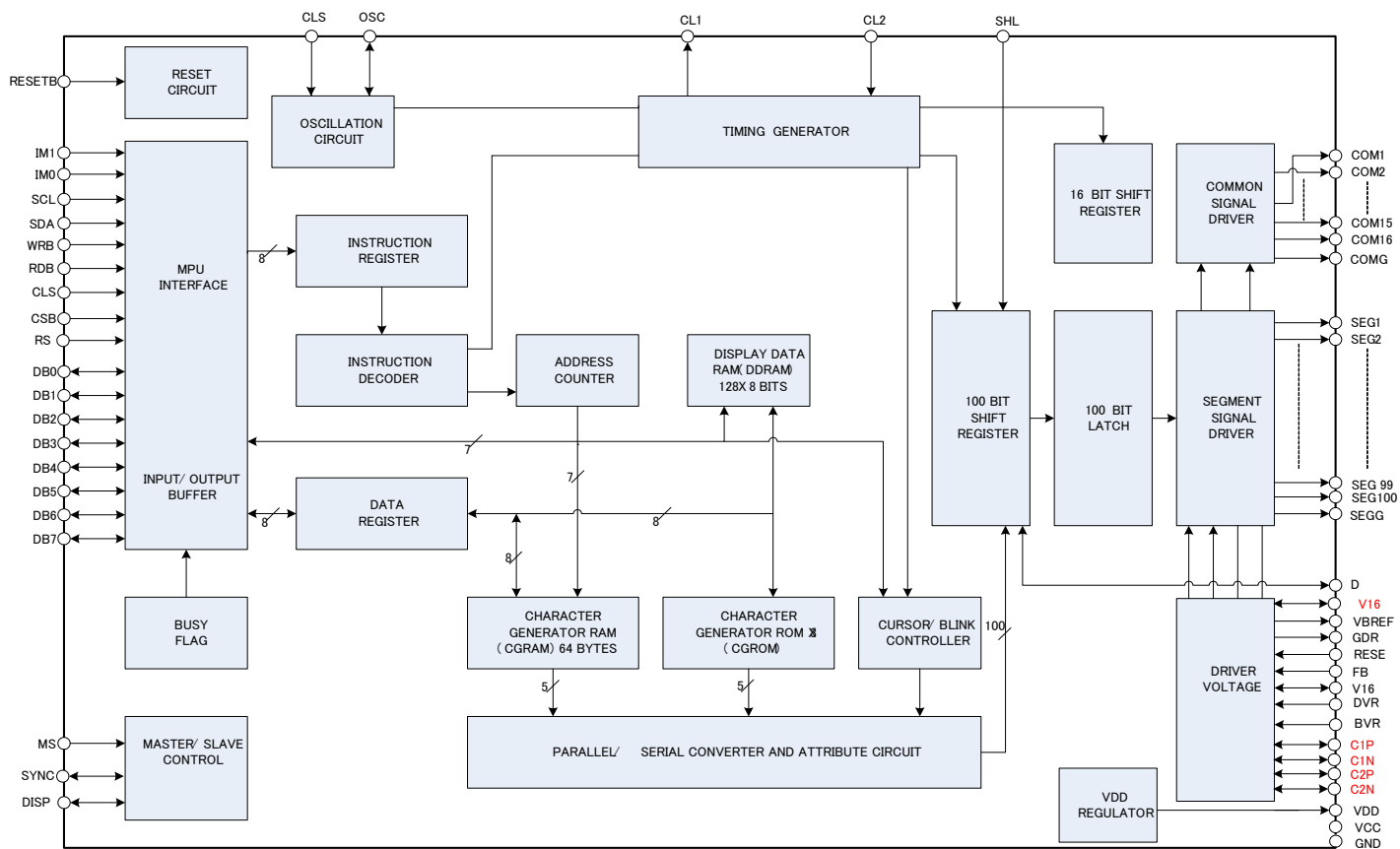
- English Russian Character

- Western European Character-II

64 x 8-bits character generator RAM (CGRAM)
- Either 8 character fonts (5 x 8 dot matrix)
- or 4 character fonts (5 x 10 dot matrix)
16 common x 100 segment OLED drivers
Support graphic mod
Cascade application
Embedded DC-DC voltage converter
--DCDC with operation frequency selection
Embedded DC-DC2 with external 2 capacitors
Adjustable DVR with 2 bits selection or external resistor (200k,100k,50k,0)
Adjustable BVR with 4 bits selection or external resistor
Vertical scrolling in graphic mode
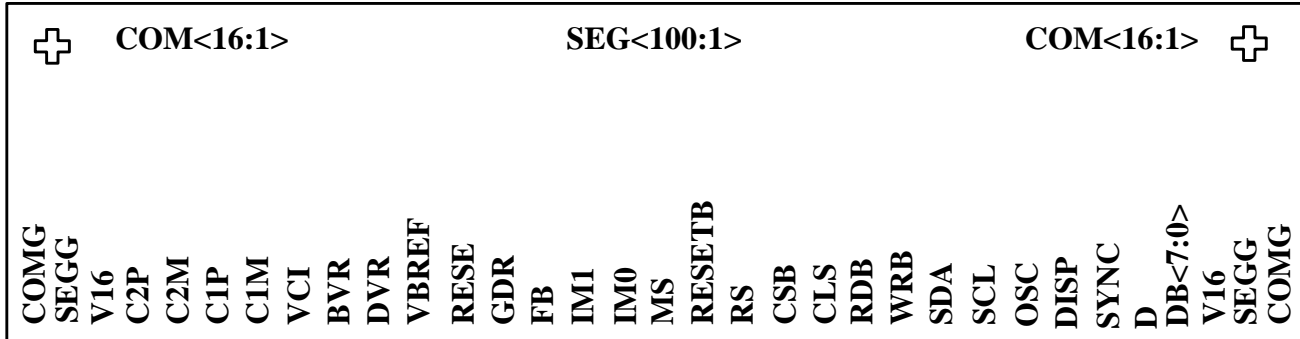Smart pre-charge selection (initial on)
Package : COG (NO TCP)

APPLICATIONS

Data bank/Organizer
Information appliance
P.D.A.
P.O.S.
Car audio
Electronic equipment with OLED display

Block Diagram

CLS OSC   CL1   CL2   SHL

RESETB — RESET CIRCUIT

IM1
IM0
SCL
SDA
WRB
RDB
CLS
CSB
RS

MPU INTERFACE

OSCILLATION CIRCUIT

TIMING GENERATOR

16 BIT SHIFT REGISTER

COMMON SIGNAL DRIVER

COM1
COM2
COM15
COM16
COMG

INSTRUCTION REGISTER

8

INSTRUCTION DECODER

ADDRESS COUNTER

DISPLAY DATA RAM（DDRAM） 128X 8 BITS

DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7

INPUT/ OUTPUT BUFFER

DATA REGISTER

100 BIT SHIFT REGISTER

100 BIT LATCH

SEGMENT SIGNAL DRIVER

SEG1
SEG2

SEG 99
SEG100
SEGG

7

8

8

BUSY FLAG

CHARACTER GENERATOR RAM （CGRAM）64 BYTES

CHARACTER GENERATOR ROM Ⅺ （CGROM）

CURSOR/ BLINK CONTROLLER   100

5   5

D
V16
VBREF
GDR
RESE
FB
V16
DVR
BVR
C1P
C1N
C2P
C2N

DRIVER VOLTAGE

MS
SYNC
DISP

MASTER/ SLAVE CONTROL

PARALLEL/   SERIAL CONVERTER AND ATTRIBUTE CIRCUIT

VDD REGULATOR

VDD
VCC
GND

PAD LOCATION

COM<16:1>　　　　　　　SEG<100:1>　　　　　　　COM<16:1>

COMG SEGG V16 C2P C2M C1P C1M VCI BVR DVR VBREF RESE GDR FB IM1 IM0 MS RESETB RS CSB CLS RDB WRB SDA SCL OSC DISP SYNC D DB<7:0> V16 SEGG COMG

CHIP SIZE : 7754 X 805 um^2

TOP Output PAD	Bump	Min. Pitch
COM&Dummy(2)	63 * 80	78
SEG&Dummy(2)	25 * 119	47.5
BOTTOM	Bump	Min. Pitch
COMG/SEGG/V16/VCI	106 * 50	212
VCC/VDD/GND	106 * 50	197
CXP/CXN/VDD	106 * 50	136
IM2,1,0/MS/TEST/RESETB/RS/ CSB/CLS/RDB/WRB/SDA/SCL	106 * 50	136.1
BVR/DVR/VBREF/RESE/GDR/FB	92.4 * 50	122.4
DB0 ~ DB7	99 * 50	130.1
OSC/DISP/SYNC/D	93 * 50	136.1

Alignment mark	X	Y
Left side	-3817	357.5
Right side	3817	357.5
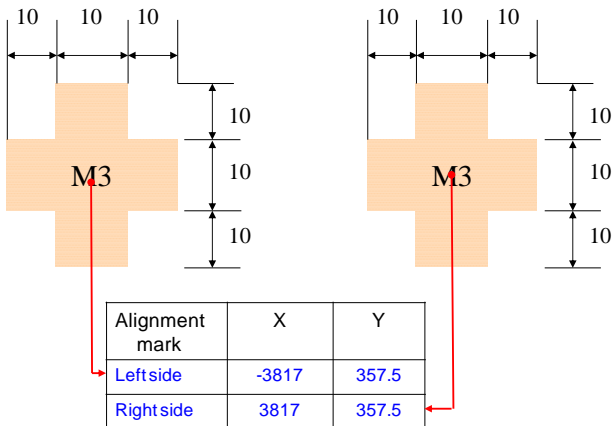
PAD CONFIGURATION

PAD NO.	PAD Name	X-axis	Y-axis	PAD NO.	PAD Name	X-axis	Y-axis
1	COMG	-3645.7	-337.5	36	D	1703.7	-337.5
2	SEGG	-3433.7	-337.5	37	VCC	1863.7	-337.5
3	V16	-3221.7	-337.5	38	DB<7>	2079.1	-337.5
4	C2P	-3047.7	-337.5	39	DB<6>	2209.2	-337.5
5	C2M	-2911.7	-337.5	40	DB<5>	2338.2	-337.5
6	C1P	-2775.7	-337.5	41	DB<4>	2468.3	-337.5
7	C1M	-2639.7	-337.5	42	DB<3>	2597.3	-337.5
8	VCI	-2401	-337.5	43	DB<2>	2727.4	-337.5
9	GND	-2196.7	-337.5	44	DB<1>	2856.4	-337.5
10	VCC	-1999.7	-337.5	45	DB<0>	2986.5	-337.5
11	BVR	-1840	-337.5	46	V16	3221.7	-337.5
12	DVR	-1717.6	-337.5	47	SEGG	3433.7	-337.5
13	VBREF	-1595.2	-337.5	48	COMG	3645.7	-337.5
14	RESE	-1472.8	-337.5	49	DUMMY_PAD	3708.75	300
15	GDR	-1350.4	-337.5	50	COMR<1>	3630.75	300
16	FB	-1228	-337.5	51	COMR<2>	3552.75	300
17	VDD	-1054.7	-337.5	52	COMR<3>	3474.75	300
18	IM2	-879.2	-337.5	53	COMR<4>	3396.75	300
19	IM1	-743.2	-337.5	54	COMR<5>	3318.75	300
20	IM0	-607.1	-337.5	55	COMR<6>	3240.75	300
21	VCC	-440.5	-337.5	56	COMR<7>	3162.75	300
22	GND	-243.5	-337.5	57	COMR<8>	3084.75	300
23	MS	-77	-337.5	58	COMR<9>	3006.75	300
24	TEST	60.7	-337.5	59	COMR<10>	2928.75	300
25	RESETB	196.8	-337.5	60	COMR<11>	2850.75	300
26	RS	332.9	-337.5	61	COMR<12>	2772.75	300
27	CSB	469	-337.5	62	COMR<13>	2694.75	300
28	CLS	605.1	-337.5	63	COMR<14>	2616.75	300
29	RDB	741.2	-337.5	64	COMR<15>	2538.75	300
30	WRB	877.3	-337.5	65	COMR<16>	2460.75	300
31	SDA	1015	-337.5	66	DUMMY_PAD	2398.75	300
32	SCL	1151.1	-337.5	67	SEG<100>	2351.25	300
33	OSC	1308.5	-337.5	68	SEG<99>	2303.75	300
34	DISP	1444.6	-337.5	69	SEG<98>	2256.25	300
35	SYNC	1567.6	-337.5	70	SEG<97>	2208.75	300

PAD NO.	PAD Name	X-axis	Y-axis	PAD NO.	PAD Name	X-axis	Y-axis
71	SEG<96>	2161.25	300	106	SEG<61>	498.75	300
72	SEG<95>	2113.75	300	107	SEG<60>	451.25	300
73	SEG<94>	2066.25	300	108	SEG<59>	403.75	300
74	SEG<93>	2018.75	300	109	SEG<58>	356.25	300
75	SEG<92>	1971.25	300	110	SEG<57>	308.75	300
76	SEG<91>	1923.75	300	111	SEG<56>	261.25	300
77	SEG<90>	1876.25	300	112	SEG<55>	213.75	300
78	SEG<89>	1828.75	300	113	SEG<54>	166.25	300
79	SEG<88>	1781.25	300	114	SEG<53>	118.75	300
80	SEG<87>	1733.75	300	115	SEG<52>	71.25	300
81	SEG<86>	1686.25	300	116	SEG<51>	23.75	300
82	SEG<85>	1638.75	300	117	SEG<50>	-23.75	300
83	SEG<84>	1591.25	300	118	SEG<49>	-71.25	300
84	SEG<83>	1543.75	300	119	SEG<48>	-118.75	300
85	SEG<82>	1496.25	300	120	SEG<47>	-166.25	300
86	SEG<81>	1448.75	300	121	SEG<46>	-213.75	300
87	SEG<80>	1401.25	300	122	SEG<45>	-261.25	300
88	SEG<79>	1353.75	300	123	SEG<44>	-308.75	300
89	SEG<78>	1306.25	300	124	SEG<43>	-356.25	300
90	SEG<77>	1258.75	300	125	SEG<42>	-403.75	300
91	SEG<76>	1211.25	300	126	SEG<41>	-451.25	300
92	SEG<75>	1163.75	300	127	SEG<40>	-498.75	300
93	SEG<74>	1116.25	300	128	SEG<39>	-546.25	300
94	SEG<73>	1068.75	300	129	SEG<38>	-593.75	300
95	SEG<72>	1021.25	300	130	SEG<37>	-641.25	300
96	SEG<71>	973.75	300	131	SEG<36>	-688.75	300
97	SEG<70>	926.25	300	132	SEG<35>	-736.25	300
98	SEG<69>	878.75	300	133	SEG<34>	-783.75	300
99	SEG<68>	831.25	300	134	SEG<33>	-831.25	300
100	SEG<67>	783.75	300	135	SEG<32>	-878.75	300
101	SEG<66>	736.25	300	136	SEG<31>	-926.25	300
102	SEG<65>	688.75	300	137	SEG<30>	-973.75	300
103	SEG<64>	641.25	300	138	SEG<29>	-1021.25	300
104	SEG<63>	593.75	300	139	SEG<28>	-1068.75	300
105	SEG<62>	546.25	300	140	SEG<27>	-1116.25	300

PAD NO.	PAD Name	X-axis	Y-axis	PAD NO.	PAD Name	X-axis	Y-axis
141	SEG<26>	-1163.75	300	176	COML<8>	-3084.75	300
142	SEG<25>	-1211.25	300	177	COML<7>	-3162.75	300
143	SEG<24>	-1258.75	300	178	COML<6>	-3240.75	300
144	SEG<23>	-1306.25	300	179	COML<5>	-3318.75	300
145	SEG<22>	-1353.75	300	180	COML<4>	-3396.75	300
146	SEG<21>	-1401.25	300	181	COML<3>	-3474.75	300
147	SEG<20>	-1448.75	300	182	COML<2>	-3552.75	300
148	SEG<19>	-1496.25	300	183	COML<1>	-3630.75	300
149	SEG<18>	-1543.75	300	184	DUMMY_PAD	-3708.75	300
150	SEG<17>	-1591.25	300				
151	SEG<16>	-1638.75	300				
152	SEG<15>	-1686.25	300				
153	SEG<14>	-1733.75	300				
154	SEG<13>	-1781.25	300				
155	SEG<12>	-1828.75	300				
156	SEG<11>	-1876.25	300				
157	SEG<10>	-1923.75	300				
158	SEG<9>	-1971.25	300				
159	SEG<8>	-2018.75	300				
160	SEG<7>	-2066.25	300				
161	SEG<6>	-2113.75	300				
162	SEG<5>	-2161.25	300				
163	SEG<4>	-2208.75	300				
164	SEG<3>	-2256.25	300				
165	SEG<2>	-2303.75	300				
166	SEG<1>	-2351.25	300				
167	DUMMY_PAD	-2398.75	300				
168	COML<16>	-2460.75	300				
169	COML<15>	-2538.75	300				
170	COML<14>	-2616.75	300				
171	COML<13>	-2694.75	300				
172	COML<12>	-2772.75	300				
173	COML<11>	-2850.75	300				
174	COML<10>	-2928.75	300				
175	COML<9>	-3006.75	300				

PIN/PAD DESCRIPTION

Pin Name	I/O	Description	Pad/Pin No.
SEG100 ~ SEG1	O	Segment Driver Output Pins	
COM1 ~ COM16	O	Common Driver Output Pins	
SEGG	Pwr	OLED Drive Power Supply (0V)	
COMG	Pwr	OLED Drive Power Supply (0V)	
VCC	Pwr	Power pin (2.6V~5.5V)	
GND	Pwr	Ground Pin (0V)	
VDD	Pwr	Power Pin (connect to stabilization capacitor)	
VCI	Pwr	DCDC buffer Power Supply (2.6 to 5.5V):	
OSC	I/O	Oscillator Pin	
MS	I	Master/Slave select pin	
SYNC	I/O	Master/Slave connect for synchronism When "master" mode, SYNC is output When "slave" mode, SYNC is input	
D	I/O	Character Pattern Data Pin When "master" mode, D is output When "slave" mode, D is input	
CSB	I	Chip select input pins Data / instruction I/O is enabled only when CSB is "L".	
DB0 ~ DB3	I/O	Low Order Bidirectional Data I/O Pins These pins are used for data transfer and reception between the MPU and RS0012. These pins are not used during a 4-bit operation.	
DB4 ~ DB7	I/O	High Order Bidirectional Data I/O Pins These pins are used for data transfer and reception between the MPU and RS0012.	
RESETB	I	Reset pin	
IM ~ IM0	I	Interface selection <table><tr><td>IM1</td><td>IM0</td><td>Interface</td></tr><tr><td>L</td><td>L</td><td>68</td></tr><tr><td>L</td><td>H</td><td>80</td></tr><tr><td>H</td><td>L</td><td>SPI</td></tr><tr><td>H</td><td>H</td><td>I2C</td></tr></table>	
DISP	I/O	Display on/off synchronize pin, only used in cascade application When "Master" mode, DISP is output When "slave" mode, DISP is input	

CLS	I	In Master mode : When CLS is "1", the clock is from embedded OSC When CLS is "0", the clock is form external OSC pin	
RS	I	Register Select Input Pin When this pin is set to "0", it is used as an Instruction Register. When this pin is set to "1", it is used for as the Data Register.	
RW_WRB	I	Read / Write execution control pin | MPU Type	RW_WRB	Description
---	---	---
6800-series	RW	Read / Write control input pin RW = "H" : read RW = "L" : write
8080-series	WRB	Write enable clock input pin The data on DB0 to DB7 are latched at the rising edge of the /WRB signal.		
E_RDB	I	Read / Write execution control pin | MPU Type	E_RDB	Description
---	---	---
6800-series	E	Read / Write control input pin - RW = "H" : When E is "H", DB0 to DB7 are in an output status. - RW = "L" : The data on DB0 to DB7 are latched at the falling edge the E signal.
8080-series	RDB	Read enable clock input pin When / RDB is "L", DB0 to DB7 are in an output status.		
V16	I	This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC-DC voltage converter.	
VBREF	O	This pin is the internal voltage reference of DCDC1 circuit. A stabilization capacitor should be connected between this pin and GND	
RESE	I	NMOS source input pin: This pin connects to the source current pin of the external NMOS of the booster circuit.	
GDR	O	Gate drive pulse output pin:	
FB	I	Feedback voltage input pin: This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level.	
DVR	I	Pre charge time control	
BVR	I	Brightness control pin	

C1M~C2M,C1P~C2P	O	Internal DCDC2 capacitor pins	

FUNCTION DESCRIPTION

REGISTERS

RS0012 provides two types of 8-bit registers, namely: Instruction Register (IR) and Data Register (DR). The register is selected using the RS Pin. When the RS pin is set to "0", the Instruction Register Type
is selected. When RS pin is set to "1", the Data Register Type is selected. Please refer to the table below.

RS	RW_WRB	Operat
0	0	Instruction register write as an internal operation.
1	0	Data register write as an internal operation (DR to DDRAM or CGRAM)
1	1	Data register read as an internal operation (DDRAM or CGRAM to DR)

INSTRUCTION REGISTER (IR)

The Instruction Register is used to store the instruction code (i.e. Display Clear, Cursor Home and others), Display Data RAM (DDRAM) Address, and the Character Generator RAM (CGRAM) Address. Instruction register can only be written from the MPU.

DATA REGISTER (DR)

The Data Register is used as a temporary storage for data that are going to be written into the DDRAM or CGRAM as well as those data that are going to be read from the DDRAM or CGRAM.

ADDRESS COUNTER (AC)

The address counter is used to assign the Display Data RAM (DDRAM) Address and the Character Generator RAM (CGRAM) Address. When Address information is written into the Instruction Register (IR), this Address information is sent from the Instruction Register to the Address Counter. At the same time, the nature of the Address (either CGRAM or DDRAM) is determined by the instruction.
After writing into or reading from the DDRAM or CGRAM, the Address Counter is automatically increased or decreased by 1 (for Write or Read Function). It must be noted that when the RS pin is set to "0" and R/WB is set to "1", the contents of the Address Counter are outputted to the pins -- DB0 to DB6.

DISPLAY DATA RAM (DDRAM)

The Display Data RAM (DDRAM) is used to store the Display Data which is represented as 8-bit character code.
The Display Data RAM supports an extended capacity of 128 x 8-bits or 128 characters.
The Display Data RAM Address (ADD) is set in the Address Counter as a hexadecimal.

	High Order Bits			Low Order Bits		
Address Counter (hex)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

An example of a DDRAM Address=39 is given below.

DDRAM Address: 39						
AC6	AC5	AC4	AC3	AC2	AC1	AC0
0	1	1	1	0	0	1

1-LINE DISPLAY (N=0)

When the number of characters displayed is less than 128, the first character is displayed at the head position. The relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position (digit)	1	2	3	4	………….	126	127	128
DDRAM address (hexadecimal)	00	01	02	03	………….	7D	7E	7F

For example, when only 8 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position	1	2	3	4	5	6	7	8
DDRAM address	00	01	02	03	04	05	06	07
Shift left	01	02	03	04	05	06	07	08
Shift right	7F	00	01	02	03	04	05	06

2-LINE DISPLAY (N=1)

Case 1: The Number of Characters displayed is less than 64 x 2 lines

When the number of characters displayed is less than 64 x 2 lines, then the first character of the first and second lines are displayed starting from the head. It is important to note that every line reserve 64 x8bits DDRAM space. 1st line is 00 to 3F,second line is 40 to 7F.Please refer the figure below.

Display Position	1	2	3	4	……….	61	62	63	64
DDRAM Address (hexadecimal)	00	01	02	03	……….	3C	3D	3E	3F
	40	41	42	43	……….	7C	7D	7E	7F

To illustrate, for 2-line x 20 characters display, the relationship between the DDRAM address and position of the OLED panel is shown below.

Display Position	1	2	3	4	……….	18	19	20
DDRAM address (hexadecimal)	00	01	02	03	……….	11	12	13
	40	41	42	43	……….	51	52	53
Shift left	01	02	03	04	……….	12	13	14
	41	42	43	44	……….	52	53	54
Shift right	3F	00	01	02	……….	10	11	12
	7F	40	41	42	……….	50	51	52

Case 2: 40-Character x 2 Lines Display

RS0012(Master) can be extended to display 40 characters x 2 lines by cascade the other RS0012(Slave). When there is a Display Shift operation, the DDRAM Address is also shifted.   Please refer to the example below.

Display Position	1	2	3	….	….	18	19	20	21	22	23	….	….	38	39	40
DDRAM address (Hexadecimal)	00	01	02	….	….	11	12	13	14	15	16	….	….	25	26	27
	40	41	42	….	….	51	52	53	54	55	56	….	….	65	66	67
	RS0012 display (Master)								Cascade 2nd RS0012(Slave)							
Shift left	01	02	03	….	….	12	13	14	15	16	17	….	….	26	27	28
	41	42	43	….	….	52	53	54	55	56	57	….	….	66	67	68
Shift right	3F	00	01	….	….	10	11	12	13	14	15	….	….	24	25	26
	7F	40	41	….	….	50	51	52	53	54	55	….	….	64	65	66

SLAVE MODE DATA INPUT

When RS0012 is under slave mode, display data is send from the other RS0012(master).The input data "D" is shifted at the falling edge of CL
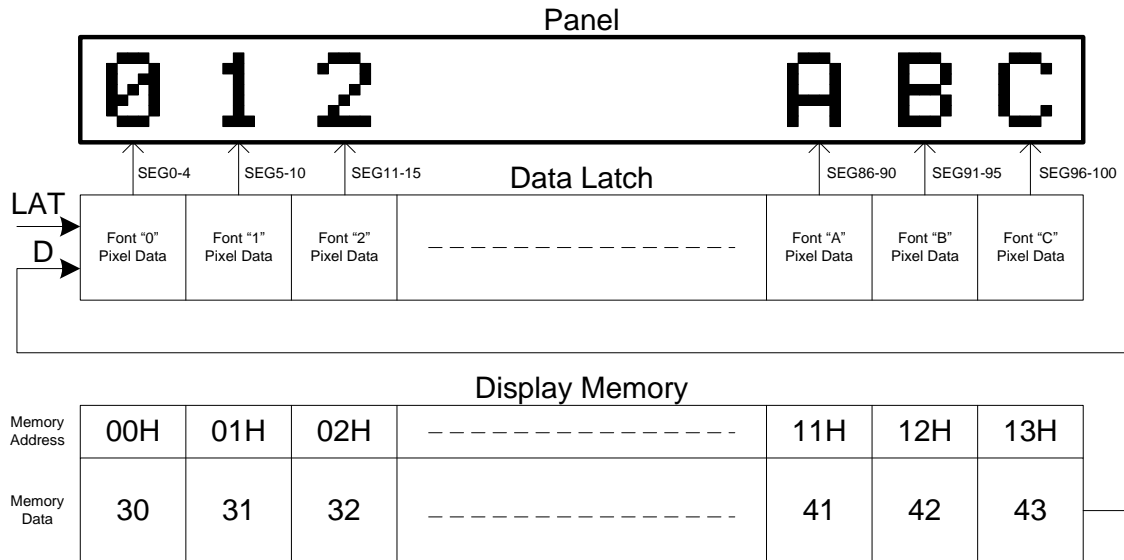
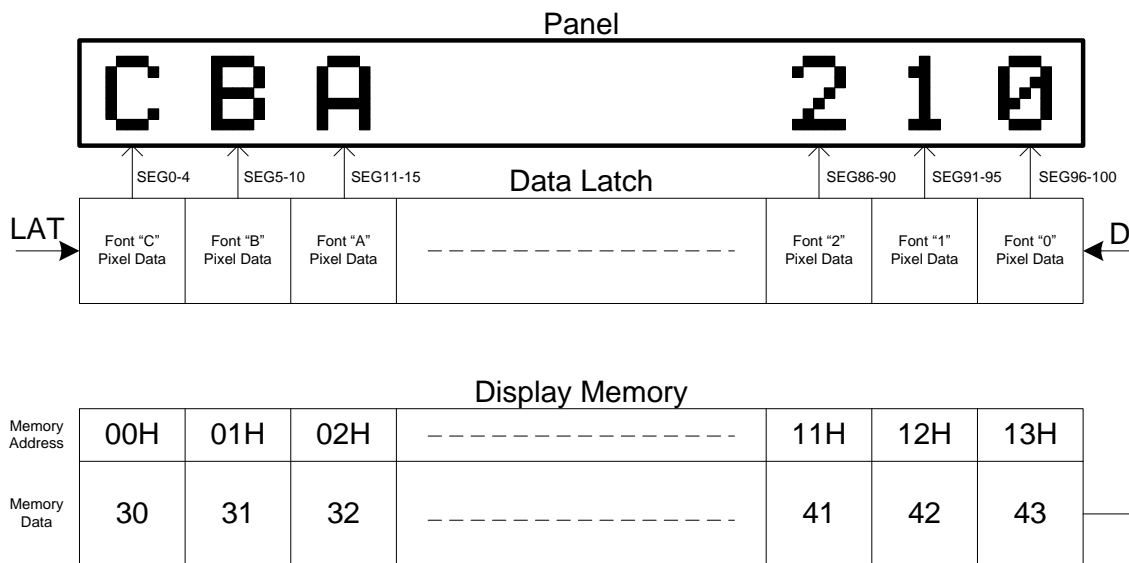| M/S	Mode	DISP	SYNC	D	OSC
H	Master	Output	Output	Output	Output
L	Slave	Input	Input	Input	Input
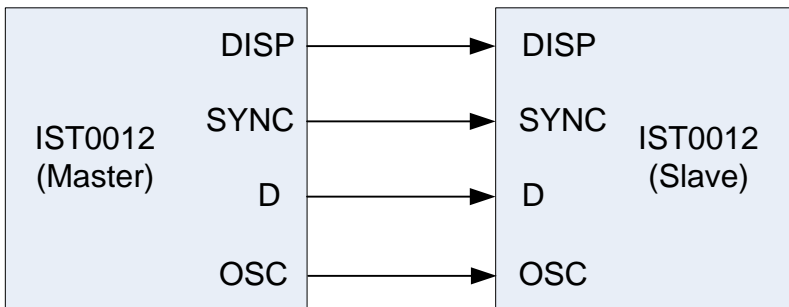
BIDIRECTIONAL SHIFT REGISTER BLOCK

This block shifts the serial data at the falling edge of CL. When SHL is set "H", the data input from D is shifted from bit100 to bit1 (When RS0012 is "master" mode, D is output; When RS0012 is "slave" mode, D is input). When SHL is set "L", the data input is shifted from bit1 to bit100.

Condition 1 : SHL="H"

Panel

| SEG0-4 | SEG5-10 | SEG11-15 | | SEG86-90 | SEG91-95 | SEG96-100 |

Data Latch

LAT

D

| Font "0" Pixel Data | Font "1" Pixel Data | Font "2" Pixel Data | — — — — — — — | Font "A" Pixel Data | Font "B" Pixel Data | Font "C" Pixel Data |

Display Memory

Memory Address	00H	01H	02H	— — — — — —	11H	12H	13H
Memory Data	30	31	32	— — — — — —	41	42	43

Condition 2 : SHL="L

Panel

| SEG0-4 | SEG5-10 | SEG11-15 | | SEG86-90 | SEG91-95 | SEG96-100 |

Data Latch

LAT

| Font "C" Pixel Data | Font "B" Pixel Data | Font "A" Pixel Data | — — — — — — — | Font "2" Pixel Data | Font "1" Pixel Data | Font "0" Pixel Data | D |

Display Memory

Memory Address	00H	01H	02H	— — — — — —	11H	12H	13H
Memory Data	30	31	32	— — — — — —	41	42	43

CHARACTER GENERATOR ROM (CGROM)

The Character Generator ROM (CGROM) is used to generate either 5 x 8 dots or 5 x 10 dots character patterns from 8-bit character codes.RS0012 build in four set of font tables as "Western European-I", "English Japanese", "English Russian" and "Western European-II" . User can use software to select suitable font table **(Default "English Japanese")**.

DC-DC1 VOLTAGE CONVERTER

It is a switching voltage generator circuit, designed for handheld applications. In RS0012, internal DC- DC voltage converter accompanying with an external application circuit (shown in below) can generate a high voltage supply V16   from a low voltage supply input VCC. V16   is the voltage supply to the OLED driver block.
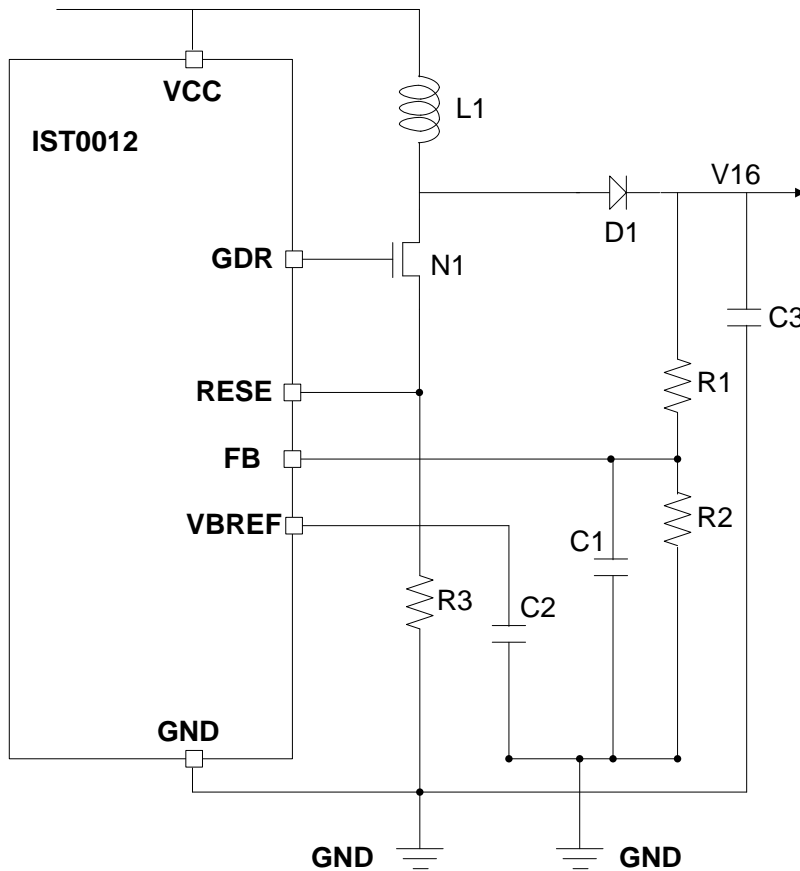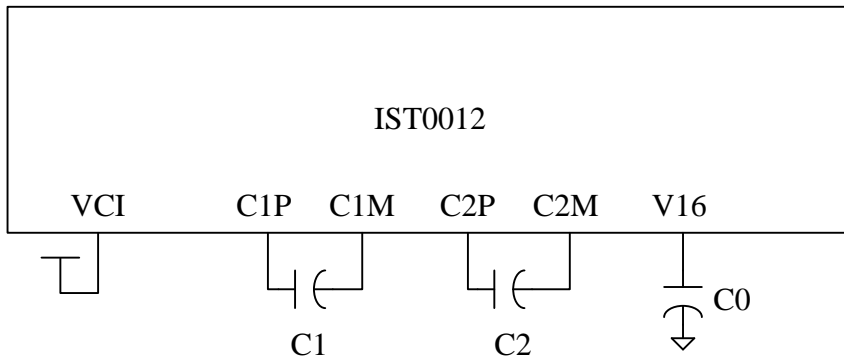

Passive component selection:

Components	Typical Value	Remark
L1	Inductor	● Select proper device according to system's requirement. (*1)
D1	Schottky diode	● Select proper device according to system's requirement. (*1)
N1	MOSFET	
R1, R2, R3	Resistor	● R1=510Kohm, R2=100Kohm, R3=1ohm
C1	Capacitor, 10nF	
C2	Capacitor, 1µF	
C3	Capacitor, 22uF/25V	

(*1)   L1=10uH, D1=1N5819 is one kind of possible solution, Please choose proper devices according to real system's requirements.

DC-DC2VOLTAGE CONVERTER

It is a charge pump voltage generator circuit with two capacitors. The DCDC2 designed for stable V16 output.
The V16 ideal voltage is 7.2V

Passive component selection:

Components	Typical Value	Remark
C1	1uf	
C2	1uf	
C0	1~10uf	

ENGLISH_JAPANESE CHARACTER FONT TABLE(default FT[1:0]= 00)

WESTERN EUROPEAN CHARACTER FONT TABLE I (FT[1:0]=01)

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	CG RAM (2)															
LLHL	CG RAM (3)															
LLHH	CG RAM (4)															
LHLL	CG RAM (5)															
LHLH	CG RAM (6)															
LHHL	CG RAM (7)															
LHHH	CG RAM (8)															
HLLL	CG RAM (1)															
HLLH	CG RAM (2)															
HLHL	CG RAM (3)															
HLHH	CG RAM (4)															
HHLL	CG RAM (5)															
HHLH	CG RAM (6)															
HHHL	CG RAM (7)															
HHHH	CG RAM (8)															

ENGLISH_RUSSIAN CHARACTER FONT TABLE(FT[1:0]=10)

Upper 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	CG RAM (2)															
LLHL	CG RAM (3)															
LLHH	CG RAM (4)															
LHLL	CG RAM (5)															
LHLH	CG RAM (6)															
LHHL	CG RAM (7)															
LHHH	CG RAM (8)															
HLLL	CG RAM (1)															
HLLH	CG RAM (2)															
HLHL	CG RAM (3)															
HLHH	CG RAM (4)															
HHLL	CG RAM (5)															
HHLH	CG RAM (6)															
HHHL	CG RAM (7)															
HHHH	CG RAM (8)															

WESTERN EUROPEAN CHARACTER FONT TABLE II (FT[1:0]=11)

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	CG RAM (2)															
LLHL	CG RAM (3)															
LLHH	CG RAM (4)															
LHLL	CG RAM (5)															
LHLH	CG RAM (6)															
LHHL	CG RAM (7)															
LHHH	CG RAM (8)															
HLLL	CG RAM (1)															
HLLH	CG RAM (2)															
HLHL	CG RAM (3)															
HLHH	CG RAM (4)															
HHLL	CG RAM (5)															
HHLH	CG RAM (6)															
HHHL	CG RAM (7)															
HHHH	CG RAM (8)															

CHARACTER GENERATOR RAM (CGRAM)

The Character Generator RAM (CGRAM) is used to generate either 5 x 8 dot or 5 x 10 dot character patterns. It can generate eight 5 x 8 dot character patterns or four 5 x 10 dot character patterns. The character patterns generated by the CGRAM can be rewritten. User-defined character patterns for the CGRAM are supported.

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR 5 X 8 DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)								CGRAM Address						Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
High							Low	High					Low	High							Low	
											0	0	0	*	*	*	1	1	1	1	0	Character pattern 1
											0	0	1	*	*	*	1	0	0	0	1	
											0	1	0	*	*	*	1	0	0	0	1	
0	0	0	0	*	0	0	0	0	0	0	0	1	1	*	*	*	1	1	1	1	0	
											1	0	0	*	*	*	1	0	1	0	0	
											1	0	1	*	*	*	1	0	0	1	0	
											1	1	0	*	*	*	1	0	0	0	1	
											1	1	1	*	*	*	0	0	0	0	0	Cursor Position
											0	0	0	*	*	*	1	0	0	0	1	Character pattern 2
											0	0	1	*	*	*	0	1	0	1	0	
											0	1	0	*	*	*	1	1	1	1	1	
0	0	0	0	*	0	0	1	0	0	1	0	1	1	*	*	*	0	0	1	0	0	
											1	0	0	*	*	*	1	1	1	1	1	
											1	0	1	*	*	*	0	0	1	0	0	
											1	1	0	*	*	*	0	0	1	0	0	
											1	1	1	*	*	*	0	0	0	0	0	Cursor position
0	0	0	0	*	.	.	.	.	.	.	.	.	.				.	.	.	.	.	Character pattern 3~7
					.	.	.	.	.	.	.	.	.	*	*	*	.	.	.	.	.	
					.	.	.	.	.	.	.	.	.				.	.	.	.	.	
					.	.	.	.	.	.	.	.	.				.	.	.	.	.	
											0	0	0	*	*	*	0	0	0	0	0	Character pattern 8
											0	0	1	*	*	*	0	1	0	1	0	
											0	1	0	*	*	*	0	0	0	0	0	
0	0	0	0	*	1	1	1	1	1	1	0	1	1	*	*	*	0	0	0	0	0	
											1	0	0	*	*	*	1	0	0	0	1	
											1	0	1	*	*	*	0	1	1	1	0	
											1	1	0	*	*	*	0	0	1	0	0	
											1	1	1	*	*	*	0	0	0	0	0	Cursor position

Notes:

1. * = Not Relevant

2. The character pattern row positions correspond to the CGRAM data bits -- 0 to 4, where bit 4 is in the left position.

3. Character Code Bits 0 to 2 correspond to the CGRAM Address Bits 3 to 5 (3 bits: 8 types)

4. If the CGRAM Data is set to "1", then the selection is displayed. If the CGRAM is set to "0", there no selection is made.

5. The CGRAM Address Bits 0 to 2 are used to define the character pattern line position. The 8th line is the cursor position and its display is formed by the logical OR with the cursor. The 8th line CGRAM data bits 0 to 4 must be set to "0". If any of the 8th line CGRAM data bits 0 to 4 is set to "1", the corresponding display location will light up regardless of the cursor position.

6. When the Character Code Bits 4 to 7 are set to "0", then the CGRAM Character Pattern is selected.

It must be noted that Character Code Bit 3 is not relevant and will not have any effect on the character display. Because of this, the first Character Pattern shown above (R) can be displayed when the Character Code is 00H or 08H.

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR 5 X 10 DOT CHARACTER PATTERN)

7	6	5	4	3	2	1	0		5	4	3	2	1	0		7	6	5	4	3	2	1	0	
High							Low		High					Low		High							Low	
0	0	0	0	*	0	0	*		0	0	0	0	0	0		*	*	*	0	0	1	0	0	Character pattern 1
											0	0	0	1		*	*	*	0	1	1	1	0	
											0	0	1	0		*	*	*	1	0	1	0	1	
											0	0	1	1		*	*	*	1	0	1	0	0	
											0	1	0	0		*	*	*	0	1	1	0	0	
											0	1	0	1		*	*	*	0	0	1	1	0	
											0	1	1	0		*	*	*	0	0	1	0	1	
											0	1	1	1		*	*	*	1	0	1	0	1	
											1	0	0	0		*	*	*	0	1	1	1	0	
											1	0	0	1		*	*	*	0	0	1	0	0	
											1	0	1	0		*	*	*	*	*	*	*	*	Cursor Position
											1	0	1	1		*	*	*	*	*	*	*	*	
											1	1	0	0		*	*	*	*	*	*	*	*	
											1	1	0	1		*	*	*	*	*	*	*	*	
											1	1	1	0		*	*	*	*	*	*	*	*	
											1	1	1	1		*	*	*	*	*	*	*	*	
0	0	0	0	*	.	.	*		.	.	.	.	.	.		*	*	*	.	.	.	.	.	Character pattern 2~3
0	0	0	0	*	1	1	*		1	1	0	0	0	0		*	*	*	1	0	1	0	1	Character pattern 4
											0	0	0	1		*	*	*	1	1	1	1	1	
											0	0	1	0		*	*	*	1	1	1	1	1	
											0	0	1	1		*	*	*	1	1	1	1	1	
											0	1	0	0		*	*	*	0	1	1	1	0	
											0	1	0	1		*	*	*	0	0	1	0	0	
											0	1	1	0		*	*	*	0	0	1	0	0	
											0	1	1	1		*	*	*	1	0	1	0	1	
											1	0	0	0		*	*	*	0	1	1	1	0	
											1	0	0	1		*	*	*	0	0	1	0	0	
											1	0	1	0		*	*	*	*	*	*	*	*	Cursor Position
											1	0	1	1		*	*	*	*	*	*	*	*	
											1	1	0	0		*	*	*	*	*	*	*	*	
											1	1	0	1		*	*	*	*	*	*	*	*	
											1	1	1	0		*	*	*	*	*	*	*	*	
											1	1	1	1		*	*	*	*	*	*	*	*	

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Notes:

1. * = Not Relevant

2. The character pattern row positions correspond to the CGRAM data bits -- 0 to 4, where bit 4 is in the left position.

3. Character Code Bits 1 and 2 correspond to the CGRAM Address Bits -- 4 and 5 respectively (2 bits : 4 types)

4. If the CGRAM Data is set to "1", then the selection is displayed. If the CGRAM is set to "0", there no selection is made.

5. The CGRAM Address Bits 0 to 3 are used to define the character pattern line position. The 11th line is the cursor position and its display is formed by the logical OR with the cursor. The 11th line CGRAM data bits 0 to 4 must be set to "0". If any of the 11th line CGRAM data bits 0 to 4 is set to "1", the corresponding display location will light up regardless of the cursor position.

6. When the Character Code Bits 4 to 7 are set to "0", then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit -- 0 and 3 are not relevant and will not have any effect on the character display. Because of this, the Character Pattern shown above ($) can be displayed when the Character Code is 00H, 01H, 08H or 09H.

TIMING GENERATION CIRCUIT

The timing signals for the internal circuit operations (i.e. DDRAM, CGRAM, and CGROM) are generated by the Timing Generation Circuit. The timing signals for the MPU internal operation and the RAM Read for Display are generated separately in order to prevent one from interfering with the other. This means that, for example, when the data is being written into the DDRAM, there will be no unwanted interference such as flickering in areas other than the display area.

OLED DRIVER CIRCUIT

RS0012 provides 16 Common Drivers and 100 Segment Driver Outputs. When a character font and the number of lines to be displayed have been selected, the corresponding Common Drivers output the waveform automatically. A non-selection waveform will be outputted by the rest of the Common outputs.

CURSOR/BLINK CONTROL CIRCUIT

The cursor or character blinking is generated by the Cursor / Blink Control Circuit. The cursor or the blinking will appear with the digit located at the Display Data RAM (DDRAM) Address Set in the Address Counter (AC).

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Address counter	0	0	0	0	1	1	1

CASE 1: FOR 1-LINE DISPLAY

Example: When the Address Counter (AC) is set to 0EH, the cursor position is displayed at DDRAM Address 0EH.

Display position	1	2	3	4	5	......	14	15	......	19	20
DDRAM address (hexadecimal)	00	01	02	03	04	......	0D	**0E**	......	12	13

Cursor Position

Note: The cursor or blinking appears when the Address Counter (AC) selects the Character Generator RAM (CGRAM). When the AC selects CGRAM Address, then the cursor or the blinking is displayed in a irrelevant and meaningless position.

CASE 2: FOR 2-LINE DISPLAY

Example: When the Address Counter (AC) is set to 46H, the cursor position is displayed at DDRAM Address 46H.

Display position	1	2	3	4	5	6	7	8	......	19	20
DDRAM address	00	01	02	03	04	05	06	07	......	09	13
(hexadecimal)	40	41	42	43	44	45	**46**	47	......	49	53

Cursor Position

Note:
The cursor or blinking appears when the Address Counter (AC) selects the Character Generator RAM (CGRAM). When the AC selects CGRAM Address, then the cursor or the blinking is displayed in an irrelevant and meaningless position.

INTERNAL RESET CIRCUIT INITIALIZATION

When power is turned ON, RS0012 is initialized automatically by an internal reset circuit . The following items are set (default) during the initialization.

1. Display clear
2. Function set:
   NL="1": 8-bit interface data
   N="0": 1-line display
   F="0": 5 x 8 dot character font

3. Power turn off
   PWR="0"
4. Display on/off control:
   D="0": Display off
   C="0": Cursor off
   B="0": Blinking off
5. Entry mode set
   I/D="0": decrement by 1
   S="0": No shift

6. Cursor/Display shift/Mode / Pwr
   S/C="0", R/L="1": Shifts cursor position to the right
   G/C="0": Character mode
   Pwr="1": Internal DCDC power on

CHARACTER MODE ADDRESSING

RS0012 provides two kind of character mode. User can fill in 128 characters data (N=0, one line) or 64 characters data per line (N=1, two line) in embedded RAM to display graphic. Character mode address can be controlled by DDRAM address instruction.

Address Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CA (Character Address)	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

(1)1-Line condition (N=0)

1	2	3	4	……	……	125	126	127	128
CA=10000000	CA=10000001	CA=10000010	CA=10000011	……	……	CA=11111100	CA=11111101	CA=11111110	CA=11111111

(2)2-Line condition (N=1)

1	2	3	4	……	……	61	62	63	64
CA=10000000	CA=10000001	CA=10000010	CA=10000011	……	……	CA=10111100	CA=10111101	CA=10111110	CA=10111111
CA=11000000	CA=11000001	CA=11000010	CA=11000011	……	……	CA=11111100	CA=11111101	CA=11111110	CA=11111111

GRAPHIC MODE ADDRESSING

RS0012 provides not only character mode but also graphic mode. User can fill in 100x16 data in embedded RAM to display graphic. Graphic mode addressing is different from character mode.

Use DDRAM address instruction to set X-axis address of Graphic mode and CGRAM address instruction to set Y-axis of Graphic mode.

Address Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
GXA (Graphic X-axis Address)	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
GYA (Graphic Y-axis Address)	0	1	0	0	0	0	0	ACG0

	1	2	3	4	……	……	97	98	99	100
ACG0=0	GXA=10000000 GYA=01000000	GXA=10000001 GYA=01000000	GXA=10000010 GYA=01000000	GXA=10000011 GYA=01000000	D0 D1 D2 D3 D4 D5 D6 D7	……	GXA=11100000 GYA=01000000	GXA=11100001 GYA=01000000	GXA=11100010 GYA=01000000	GXA=11100011 GYA=01000000
ACG0=1	GXA=10000000 GYA=01000001	GXA=10000001 GYA=01000001	GXA=10000010 GYA=01000001	GXA=10000011 GYA=01000001	D0 D1 D2 D3 D4 D5 D6 D7	……	GXA=11100000 GYA=01000001	GXA=11100001 GYA=01000001	GXA=11100010 GYA=01000001	GXA=11100011 GYA=01000001

INITIALIZATION BY INSTRUCTION

The basic initialization flow is illustrated as below, and it should be re-optimized according to the application requirements of individual system.

(1) 8-bit mode

Step	Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Power on	--	--	--	--	--	--	--	--	--	--
2	Wait 500ms for power stabilization	--	--	--	--	--	--	--	--	--	--
3	Function Set	0	0	0	0	1	1	N	F	FT1	FT0
4	Display On/Off Control	0	0	0	0	0	0	1	D	C	B
5	Clear Display	0	0	0	0	0	0	0	0	0	1
6	Wait 1.5ms	--	--	--	--	--	--	--	--	--	--
7	Return Home	0	0	0	0	0	0	0	0	1	0
8	Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S
9	Command Table 2 Entry	0	0	0	0	0	0	0	0	1	1
10	Power On/Off	0	0	0	0	1	0	BVR	DVR	DC2	DC1
11	RAM Access Control	0	0	0	0	0	0	1	1	0	0
		0	0	0	0	0	0	0	0	0	0
12	Command Table 2 Exit	0	0	0	0	0	0	0	0	0	0

<Note>
Once executing the "Clear Display" command, the minimum wait time is 1.5ms.

(2) 4-bit mode

Step	Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	Power on	--	--	--	--	--	--	X	X	X	X
2	Wait 500ms for power stabilization	--	--	--	--	--	--	X	X	X	X
3	Function Set	0	0	0	0	1	0	X	X	X	X
		0	0	0	0	1	0	X	X	X	X
		0	0	NF	F	FT1	FT0	X	X	X	X
4	Display On/Off Control	0	0	0	0	0	0	X	X	X	X
		0	0	1	D	C	B	X	X	X	X
5	Clear Display	0	0	0	0	0	0	X	X	X	X
		0	0	0	0	0	1	X	X	X	X
6	Wait 1.5ms	--	--	--	--	--	--	X	X	X	X
7	Return Home	0	0	0	0	0	0	X	X	X	X
		0	0	0	0	1	0	X	X	X	X
8	Entry Mode Set	0	0	0	0	0	0	X	X	X	X
		0	0	0	1	I/D	S	X	X	X	X
9	Command Table 2 Entry	0	0	0	0	0	0	X	X	X	X
		0	0	0	0	1	1	X	X	X	X
10	Power On/Off	0	0	0	0	1	0	X	X	X	X
		0	0	BVR	DVR	DC2	DC1	X	X	X	X
11	RAM Access Control	0	0	0	0	0	0	X	X	X	X
		0	0	0	0	1	1	X	X	X	X
		0	0	0	0	0	0	X	X	X	X
		0	0	0	0	0	0	X	X	X	X
12	Command Table 2 Exit	0	0	0	0	0	0	X	X	X	X
		0	0	0	0	0	0	X	X	X	X

<Note>
Once executing the "Clear Display" command, the minimum wait time is 1.5ms..

INSTRUCTIONS

RS0012's Instruction Register (IR) and Data Register (DR) are the only registers that can be controlled by the MPU. Prior to the commencement of it internal operation, RS0012 temporarily stores the control information to its Instruction Register (IR) and Data Register (DR) in order to easily facilitate interface with various types of MPU. The internal operations of the RS0012 are determined by the signals (RS, R/WB, DB0 to DB7) that are sent from the MPU. These signals are categorized into 4 instructions types, namely:

1. Function Setting Instructions (i.e. Display, Format, Data Length etc.)
2. Internal RAM Address Setting Instructions
3. Data Transfer with Internal RAM Instructions
4. Miscellaneous Function Instructions

The generally used instructions are those that execute data transfers with the internal RAM. However, when the internal RAM addresses are auto incremented/decremented by 1 after each Data Write, the program load of the MPU is lightened. The Display Shift Instruction can be executed at the same time as the Display Data Write, thereby minimizing system development time with maximum programming efficiency.

Command Table 1

Instruction	Cod										Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display.
Return Home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM Address 0 into the Address Counter. Returns shifted display to original position. DDRAM contents remain unchanged.
Entry Mode Se	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. (These operations are performed during data write and read.)
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Sets entire Display (D) ON/OFF. Sets Cursor (C) ON/OFF. Sets Blinking (B) of Cursor Position Character.
Cursor/ Display Shift	0	0	0	0	0	1	S/C	R/L	0	0	Moves cursor & shifts display without changing DDRAM contents. Sets Graphic/Character Mode Sets internal power on/off
C/G Mode			0	0	0	1	GC	0	1	1	
OSC on/off	0	0	0	0	0	1	0	OSC ON	0	1	
Display direction control	0	0	0	0	0	1	CMS	SHL	1	0	Sets COM shift direction(CMS) Sets SEG shift direction (SHL)
Function Set	0	0	0	0	1	NL	N	F	FT1	FT0	Sets 4bit I/F (NL). Sets number of display lines (N). Sets Character Font (F).
Set CGRAM Address	0	0	0	1	ACG5	ACG4	ACG3	ACG2	ACG1	ACG0	Sets CGRAM Address. CGRAM data is sent and received after this setting. **(ACG0 is also served as DDRAM Address)**
Set DDRAM	0	0	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	Sets DDRAM Address. The DDRAM data Is sent and received after this setting.
Write data into the CGRAM	1	0	Write Data								Write data to the CGRAM or DDRAM
Read Data from the CGRAM	1	1	Read Data								Read data from the CGRAM or DDRAM
Command Table 2 entry	0	0	0	0	0	0	0	0	1	1	Command table 2 entry
Command Table 2 exit	0	0	0	0	0	0	0	0	0	0	Command table 2 exit

Command Table 2

Instruction	RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Power clock control (DCDC1	0	0	0	0	0	0	1	0	0	0	Double byte command PCK = OSC/(DC+1) PCK = OSC, when DC = 0 (default=10)
	0	0	0	DC6	DC5	DC4	DC3	DC2	DC1	DC0	
Power clock control (DCDC2	0	0	0	0	0	0	1	0	0	1	Double byte command KA/KB = OSC/(PCYC+1) (default=23)
	0	0	PCYC7	PCYC6	PCYC5	PCYC4	PCYC3	PCYC2	PCYC1	PCYC0	
Power on/off	0	0	0	0	1	0	BVR	DVR	DC2	DC1	**DC1&DC2 can't enable together**
Vertical scrolling	0	0	0	0	1	1	LAD3	LAD2	LAD1	LAD0	For graphic mode only
Graphic duty select	0	0	0	1	0	0	GT3	GT2	GT1	GT0	For graphic mode only
Frequency adjust	0	0	0	1	0	1	RTN3	RTN2	RTN1	RTN0	
BVR adjust	0	0	0	1	1	0	BVR3	BVR2	BVR1	BVR0	
DVR adjust	0	0	0	1	1	1	0	0	DVR1	DVR0	
Smart pre-charge	0	0	0	1	1	1	0	1	1	SPB	
Frame rate control	0	0	1	FROFT							FR=1.2M/((320+FROFT*8)*16)
Engineering Mode	0	0	0	0	0	1	1	1	1	ENG	ENG=0 Normal mode (default) ENG=1 Engineering mode
RAM access Control	0	0	0	0	0	0	1	1	0	0	Double byte command Default (FTD1, FTD0) = (0,1), MUST set to (0,0) during initialization.
	0	0	0	0	0	0	0	0	FTD1	FTD0	

Notes:
1. After the CGRAM/DDRAM Read or Write Instruction has been executed, the RAM Address
   Counter is incremented or decremented by 1.

2. I/D=Increment/Decrement Bit
   - I/D="1": Increment
   - I/D="0": Decrement

3. S=Shift Entire Display Control Bit. When S="0", shift function disable.

4. R/L=Shift Right/Left
   - R/L="1": Shift to the Right
   - R/L="0": Shift to the Left

5. S/C=Display Shift/Cursor Move
   - S/C="1": Display Shift
   - S/C="0": Cursor Move

6. G/C=Graphic/Character mode selection. G/C="0", Character mode is selected. G/C="1", Graphic   mode is
   selected.

7. DDRAM=Display Data RAM

8. CGRAM=Character Generator RAM

9. ACG=CGRAM Address

10. ADD=Address Counter Address (corresponds to cursor address)

11. AC=Address Counter (used for DDRAM and CGRAM Addresses)

12. F=Character Pattern Mode
    - F="1": 5 x 10 dots
    - F="0": 5 x 8 dots

13. N=Number of Lines Displayed
    - N="1": 2 -Line Display
    - N="0": 1-Line Display

INSTRUCTION DESCRIPTION
CLEAR DISPLAY INSTRUCTION

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This instruction is used to clear the Display Write Space 20H in all DDRAM Addresses. That is, the character pattern for the Character Code 20H must be a BLANK pattern.

Once executing the "CLEAR DISPLAY" command, the minimum wait time is 1.5ms waiting for the whole process to be completed.

RETURN HOME INSTRUCTION

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0

Note: * = Not Relevant

This instruction is used to set the DDRAM Address 0 into the Address Counter and revert the display to its original status (if the display has been shifted). The DDRAM contents do not change.
The cursor or blinking will go to the left edge of the display. If there are 2 lines displayed, the cursor or blinking will go to the first line's left edge of the display.

ENTRY MODE SET INSTRUCTION

The Entry Mode Set Instruction has two controlling bits: I/D and S. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

I/D IS THE INCREMENT/DECREMENT BIT.

When I/D is set to "1", the DDRAM Address is incremented by "1" when a character code is written into or read from the DDRAM. An increment of 1 will move the cursor or blinking one step to the right.

When I/D is set to "0", the DDRAM is decremented by 1 when a character code is written into or read from the DDRAM. A decrement of 1 will move the cursor or blinking one step to the left.

S: SHIFT ENTIRE DISPLAY CONTROL BIT

This bit is used to shift the entire display. When S is set to "1", the entire display is shifted to the right (when I/D ="0") or left (when I/D ="1"). When S is set to "0", the display is not shifted.

Ex1 : I/D=1, S=1

Ex2 : I/D=0, S=1

DISPLAY ON/OFF CONTROL INSTRUCTION

The Display On / OFF Instruction is used to turn the display ON or OFF. The controlling bits are D, C and B.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

D: DISPLAY ON/OFF BIT

When D is set to "1", the display is turned ON. When D is set to "0", the display is turned OFF and the display data is stored in the DDRAM. The display data can be instantly displayed by setting D to "1".

C: CURSOR DISPLAY CONTROL BIT

When C is set to "1", the cursor is displayed. In a 5 x 8 dot character font, the cursor is displayed via the 5 dots in the 8th line. In a 5 x 10 dot character font, it is displayed via 5 dots in the 11th line.

When C is set to "0", the cursor display is disabled.
During a Display Data Write, the function of the I/D and others will not be altered even if the cursor is not present. Please refer to the figure below.

5 x 8 Dot
Character
Font

5 x 10 Dot
Character
Font
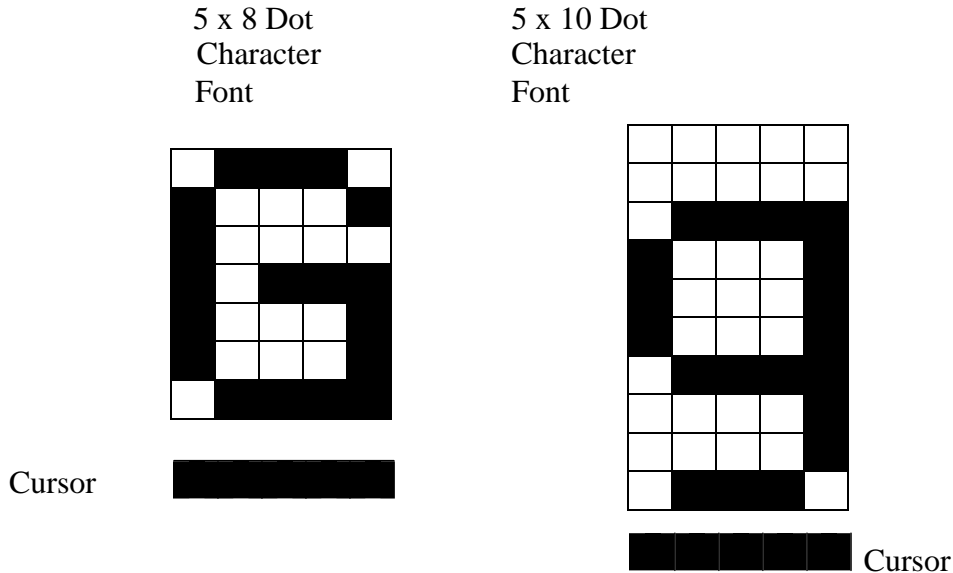
Cursor

Cursor

B: BLINKING CONTROL BIT

When B is set to '1", the character specified by the cursor blinks. The blinking feature is displayed by switching between the blank dots and the displayed character at a speed of 409.6ms intervals when the fcp or fosc is 250kHz. Please refer to the figure below.
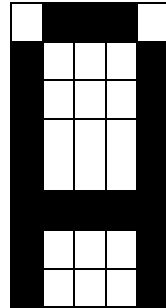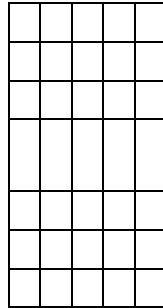
Figure 1   Figure 2

Note: Figures 1 and 2 are alternately displayed

The cursor and the blinking can be set to display at the same time. The blinking frequency depends on the fosc or the reciprocal of fcp.

To illustrate, when fosc=250K Hz, then, the blinking frequency=409.6 x 250/270=379.2ms

CURSOR/DISPLAY SHIFT INSTRUCTION

This instruction is used to shift the cursor or display position to the left or right without writing or reading the Display Data. This function is used to correct or search the display. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	0	0

S/C	R/L	Shift Function
0	0	Shifts the cursor position to the left. (AC is decremented by 1).
0	1	Shifts cursor position to the right. (AC incremented by 1).
1	0	Shifts entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

In a 2-line Display, the cursor moves to the second line when it passes the 40th digit of the first line. The first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly, each line moves only horizontally. The second line display does not shift into the first line position.

The Address Counter (AC) contents will not change if the only action performed is a Display Shift. When SHL=0, the direction will reverse.

G/C: GRAPHIC MODE / CHARACTER MODE SELECTION

This bit is used to select the display mode for further process.
When G/C = 1, the *GRAPHIC MODE* will be selected.
When G/C = 0, the *CHARACTER MODE* will be selected.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	G/C	0	1	1

OSC on/off INSTRUCTION

This instruction is used to set OSC on/off and external clock in.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	OSC ON	0	1

When OSCON = 1, the OSC will start oscillating.
When OSCON = 0, the OSC will shut down.

DISPLAY DIRECTION CONTROL INSTRUCTION

The Display direction control is set the segment data direction.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	CMS	SHL	1	0

When SHL = 0 the data direction is SEG100 -> SEG1
When SHL = 1 the data direction is SEG1 -> SEG100
When CMS = 0 the scan direction is COM1 -> COM16
When CMS = 1 the scan direction is COM16 -> COM1

FUNCTION SET INSTRUCTION

The Function Set Instruction has three controlling 3 bits, namely: NL, N and F. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	NL	N	F	FT1	FT0

NL: INTERFACE DATA LENGTH CONTROL BIT

This is used to set the interface data length. When NL is set to "1", the data is sent or received in 8-bit length via the DB0 to DB7 (for an 8-Bit Data Transfer). When NL is set to "0", the data is sent or received in 4-bit length via DB4 to DB7 (for a 4-Bit Data Transfer). When the 4-bit data length is selected, the data must be sent or received twice.

N: NUMBER OF DISPLAY LINE

This is used to set the number of display lines. When N="1", the 2-line display is selected. When N is set to "0", the 1-line display is selected.

F: CHARACTER FONT SET

This is used to set the character font set. When F is set to "0", the 5 x 8 dot character font is selected. When F is set to "1", the 5 x 10 dot character font is selected.

It must be noted that the character font setting must be performed at the head of the program before executing any instructions. Otherwise, the Function Set Instruction cannot be executed unless the interface data length is changed.

FT1, FT0: FONT TABLE SELECTION

These two bits are used to select one font table out of the three for further process.

When (FT1, FT0) = (0, 0), the *ENGLISH_JAPANESE CHARACTER FONT TABLE* will be selected.

     (FT1, FT0) = (0, 1), the *WESTERN EUROPEAN CHARACTER FONT TABLE-I* will be selected.

     (FT1, FT0) = (1, 0), the *ENGLISH_RUSSIAN CHARACTER FONT TABLE* will be selected.

     (FT1, FT0) = (1, 1), the *WESTERN EUROPEAN CHARACTER FONT TABLE-II* will be selected.

Note: The default setting for FT1 and FT0 is 0 and 0 respectively which means the default Font Table

     is *ENGLISH_JAPANESE CHARACTER FONT TABLE.*

SET CGRAM ADDRESS INSTRUCTION

This instruction is used to set the CGRAM Address binary AAAAAA into the Address Counter. Data is then written to or read from the MPU for CGRAM.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	ACG	ACG	ACG	ACG	ACG	ACG

Note: ACG is the CGRAM Address

SET DDRAM ADDRESS INSTRUCTION

This instruction is used to set the DDRAM Address binary AAAAAAA into the Address Counter. The data is written to or read from the MPU for the DDRAM. If 1-line display is selected (N="0"), then AAAAAAA can be 00H to 4FH. When the 2-line display is selected, then AAAAAAA can be 00H to 27H for the first line and 40H to 67H for the second line.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD

Note: ADD = DDRAM Address

WRITE DATA TO CGRAM / DDRAM INSTRUCTION

This instruction writes 8-bit binary data -- DDDDDDD to the CGRAM or the DDRAM. The previous CGRAM or DDRAM Address setting determines whether a data is to be written into the CGRAM or the DDRAM. After the write process is completed, the address is automatically incremented or decremented by 1 in accordance with the Entry Mode instruction. It must be noted that the Entry Mode instruction also determines the Display Shift.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D	D	D	D	D	D	D	D

READ DATA FROM THE CGRAM OR DDRAM INSTRUCTION

This instruction reads the 8-bit binary data -- DDDDDDD from the CGRAM or the DDRAM. The Set CGRAM Address or Set DDRAM Address Set Instruction must be executed before this instruction can be performed, otherwise, the first Read Data will not be valid.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D	D	D	D	D	D	D	D

When the Read Instruction is executed in series, the next address data is normally read from the Second Read. There is no need for the Address Set Instruction to be performed before this Read instruction when using the Cursor Shift Instruction to shift the cursor (Reading the DDRAM). The Cursor Shift Instruction has the same operation as that of the Set the DDRAM Address Instruction.

After a Read instruction has been executed, the Entry Mode is automatically incremented or decremented by 1. It must be noted that regardless of the Entry Mode, the Display Shift is not executed.

After the Write instruction to either the CGRAM or DDRAM has been performed, the Address Counter is automatically increased or decreased by 1. The RAM data selected by the Address Counter cannot be read out at this time even if the Read Instructions are executed. Therefore, in order to correctly read the data, the following procedure has suggested:

1. Execute the Address Set or Cursor Shift (only with DDRAM) Instruction
2. Just before reading the desired data, execute the Read Instruction from the second time the Read Instruction has been sent.

COMMAND TABLE2 ENTRY INSTRUCTION

This instruction control the command table to command table2

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	1

COMMAND TABLE2 EXIT INSTRUCTION

This instruction control the command table back to command table1

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0

POWER CLOCK1 CONTROL INSTRUCTION

This instruction control the DCDC1 clock frequency (double byte command)

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	0	0	0

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	DC6	DC5	DC4	DC3	DC2	DC1	DC0

PCK = OSC / (DC<6:0>+1) ,default DC<6:0> = 10

POWER CLOCK2 CONTROL INSTRUCTION

This instruction control the DCDC2 clock frequency (double byte command)

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	0	0	1

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	PCYC7	PCYC6	PCYC5	PCYC4	PCYC3	PCYC2	PCYC1	PCYC0

PCK2 = OSC / (PCYC<7:0>+1) ,default PCYC<7:0> = 23

POWER ON/OFF CONTROL INSTRUCTION

This instruction control the power blocks on/off

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	BVR	DVR	DC2	DC1

BVR：Control the BVR block on/off
DVR：Control the DVR block on/off
DC2：Control the DCDC2 block on/off
DC1：Control the DCDC1 block on/off

The DCDC1 & DCDC2 must independent enable,
If the DC1 is "H" the DC2 must be "L"
If the DC2 is "H" the DC1 must be "L"

VERTICAL SCROLLING CONTROL INSTRUCTION (GRAPHIC MODE ONLY)

This instruction setting the COM start point for the virtual scrolling function

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	LAD3	LAD2	LAD1	LAD0

Sets the line address of display RAM to determine the starting Line. The RAM display data is displayed at the top row of LCD panel.

LAD3	LAD2	LAD1	LAD0	Line address
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

GRAPHIC DUTY SELECT INSTRUCTION (GRAPHIC MODE ONLY)

This instruction control the com duty selection.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	GT3	GT2	GT1	GT0

RS0012 support 9 duty types in graphic mode. Each of these mode will control the number of multi com drive. Please refer the table as blew.

GT<3:0>	Function
8~F	all com always on
7	The grouping is COM1~8 and COM9~16
6	The grouping is COM1~5, COM6~10 and COM11~16
5	The grouping is COM1~4, COM5~8, COM9~12 and COM13~16
4	The grouping is COM1~3, COM4~6, COM7~9, COM10~12 and COM13~16
3	The grouping is COM1~2, COM3~4, COM5~6, COM7~8, COM9~10 and COM11~16
2	The grouping is COM1~2, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12 and COM13~16
1	The grouping is COM1~2, COM3~4, COM5~6, COM7~8, COM9~10, COM11~12 COM13~14 and COM15~16
0	Normal display

FREQUENCY ADJUST INSTRUCTION

This instruction control the OSC adjustment

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	RTN3	RTN2	RTN1	RTN0

RTN<3:0> initial is "1000"
If RTN<3:0> smaller than "1000", the OSC frequency will faster.
If RTN<3:0> bigger than "1000", the OSC frequency will slower.

BVR BRIGHTNESS INSTRUCTION

This instruction setting the BVR resistor for the brightness adjustment.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	BVR3	BVR2	BVR1	BVR0

BVR<3:0>	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Resistor (K ohm)	0	4	5	6	8	10	12	16	18	20	24	30	40	50	75	100

The BVR pin can connect external resistor for larger usage.

DVR Brightness INSTRUCTION
This instruction setting the DVR resistor for the pre-charge range adjustment.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	0	DVR1	DVR0

The DVR1~0 = 00 , the resistor of DVR is "0"
The DVR1~0 = 01 , the resistor of DVR is "50K"
The DVR1~0 = 10 , the resistor of DVR is "100K"
The DVR1~0 = 11 , the resistor of DVR is "200K"
The DVR pin can connect the external resistor for larger resistance usage

Smart Pre-charge INSTRUCTION
This instruction setting the SEG driver using smart pre-charge.
When the smart pre-charge on, the SEG driver will only pre-charge at the data is from "0" to "1"

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	1	SPB

The SPB=0 Smart pre-charge on
The SPB=1 Smart pre-charge off

FRAME RATE CONTROL INSTRUCTION
This instruction setting the display frame rate.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	FROFT6	FROFT5	FROFT4	FROFT3	FROFT2	FROFT1	FROFT0

Frame Rate = 1.2MHz / ((320+8*FROFT<6:0>)*16)

Example:
FROFT<6:0>=0011011
Frame Rate = 1200000/((320+8*27)*16)=140Hz

Engineering Mode (Don't use)

This command is reserved for engineering test and please don't use it.
The default setting of ENG=0 (Normal mode).

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	1	1	ENG

RAM ACCESS CONTROL (Double-Byte Command)

The Internal RAM access speed can be adjusted by FTD1 & FTD0.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	0	0
0	0	0	0	0	0	0	0	FTD1	FTD0

FTD1	FTD0	RAM Access Speed	Description
0	0	Medium	● The FTD1 and FTD0 should both be set to 0 during initialization.
0	1	Fast (default, but don't use)	● The FTD1 and FTD0 should both be set to 0 during initialization.
1	0	X (don't use)	
1	1	X (don't use)	

The internal RAM access speed can be adjusted by FTD1 and FTD0. The faster the speed, the more peak current will be consumed, but the internal operation will also be susceptible to system noise interference. In order to enhance the noise immunity, the FTD1 and FTD0 have to be set to "0" during initialization.

MPU INTERFACE

RS0012 provides high-speed parallel 4bit/8bit 6800/8080-series bi-directional interface, serial interface and IIC interface. It can be configured by hardware pins "IM1" and "IM0".

When it is configured as parallel interface, it is required to send "Function Set" instruction first to specify the NL register to decide which belongs to 4bit (NL=0) or 8bit (NL=1) interface.

For parallel 4bit interface, only DB7~DB4 pins are used (DB3~DB0 should be connected to VCC or GND level, those pins cannot be floating), and the 8 bit data is divided into two 4 bit data for transmission; First transmits the high nibble (Bit7(DB7) ~ Bit4(DB4)) and then the low nibble (Bit3(DB7) ~ Bit0(DB4)).

IM1	IM0	Interface
L	L	6800-series
L	H	8080-series
H	L	SPI
H	H	I2C

6800-series interface
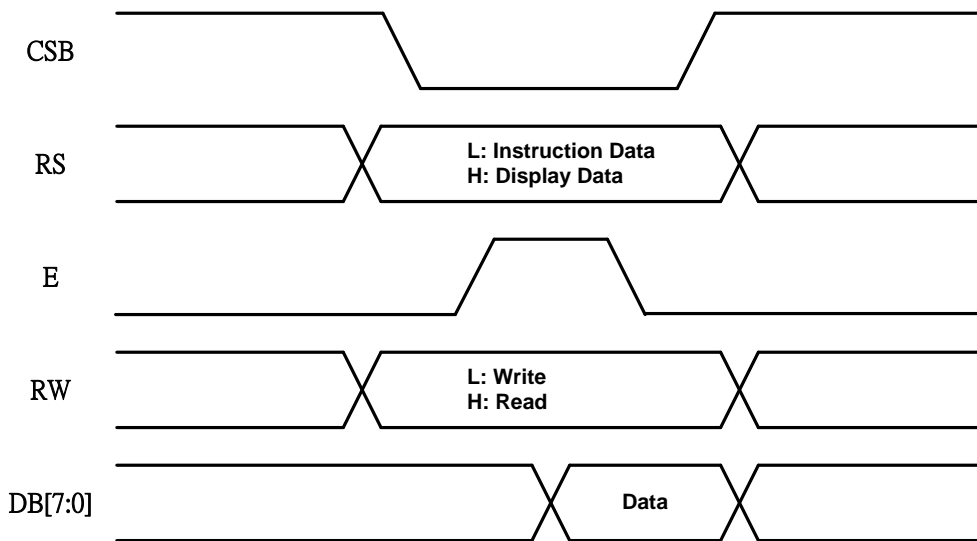
(a) 8-bit mode

When reading back the display data, the dummy read is required. The first readout byte is a dummy byte, and the subsequent bytes are the valid ones.
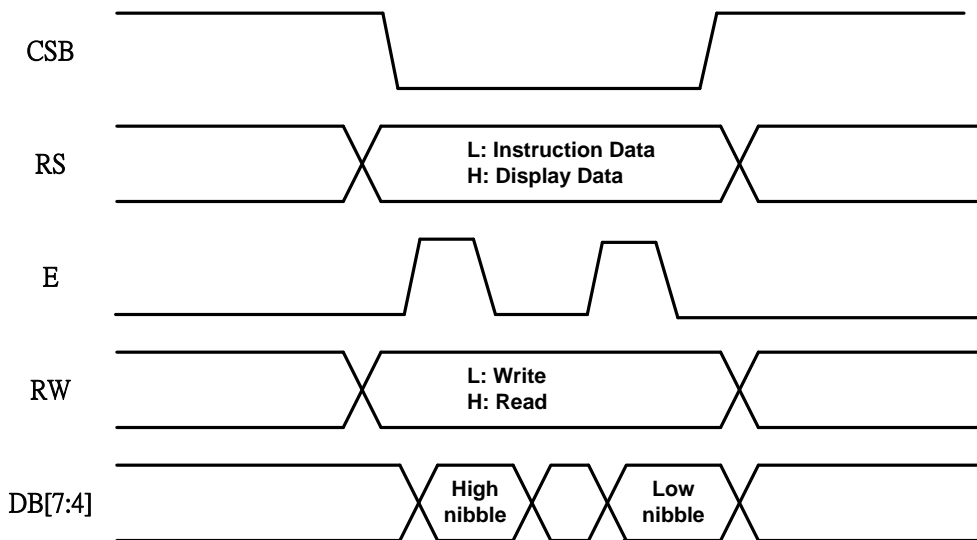
(b) 4-bit mode

When reading back the display data, the dummy read is required. The first two readout nibbles are dummy bytes, and the subsequent nibbles are the valid ones. (high-nibble first, low-nibble next)
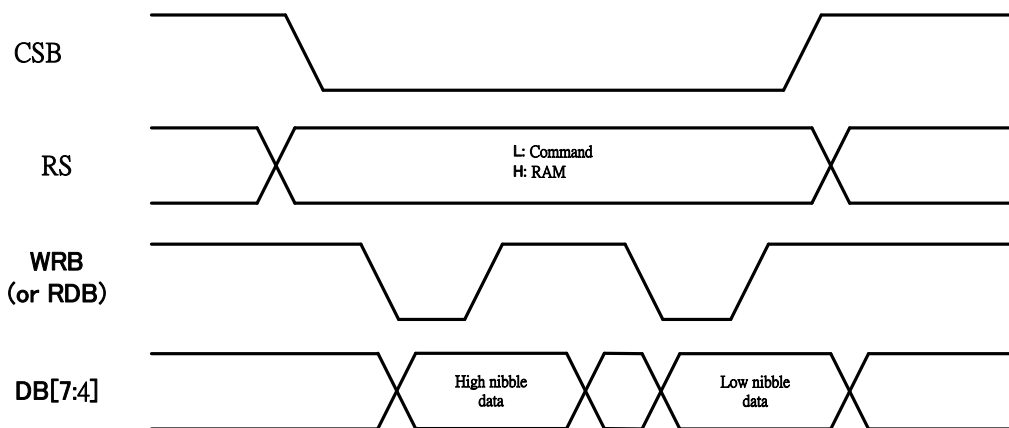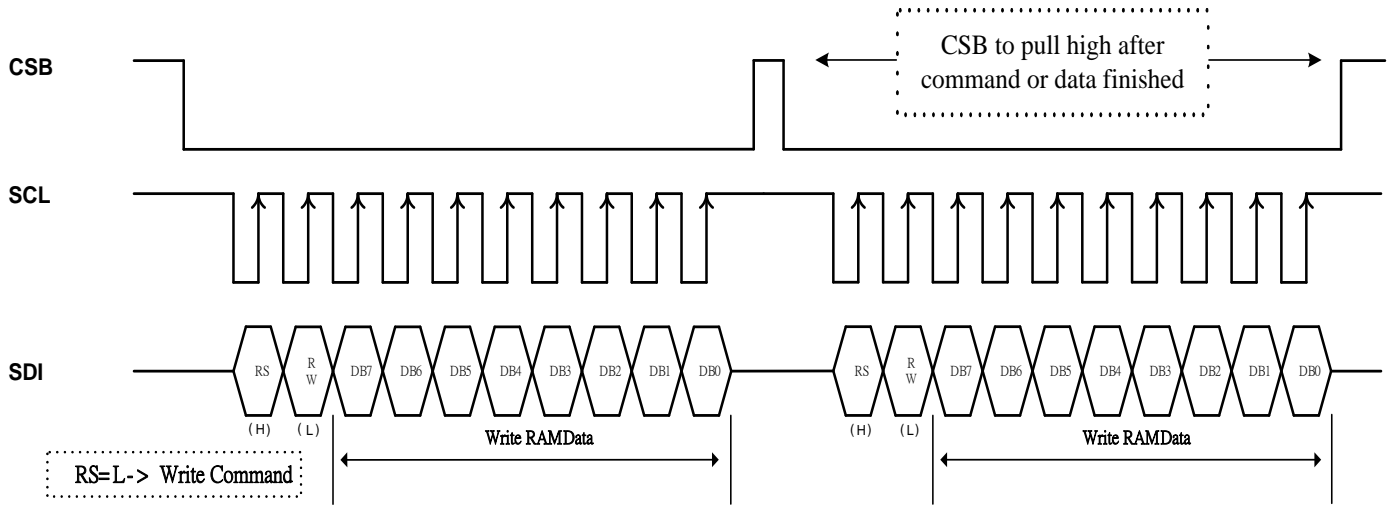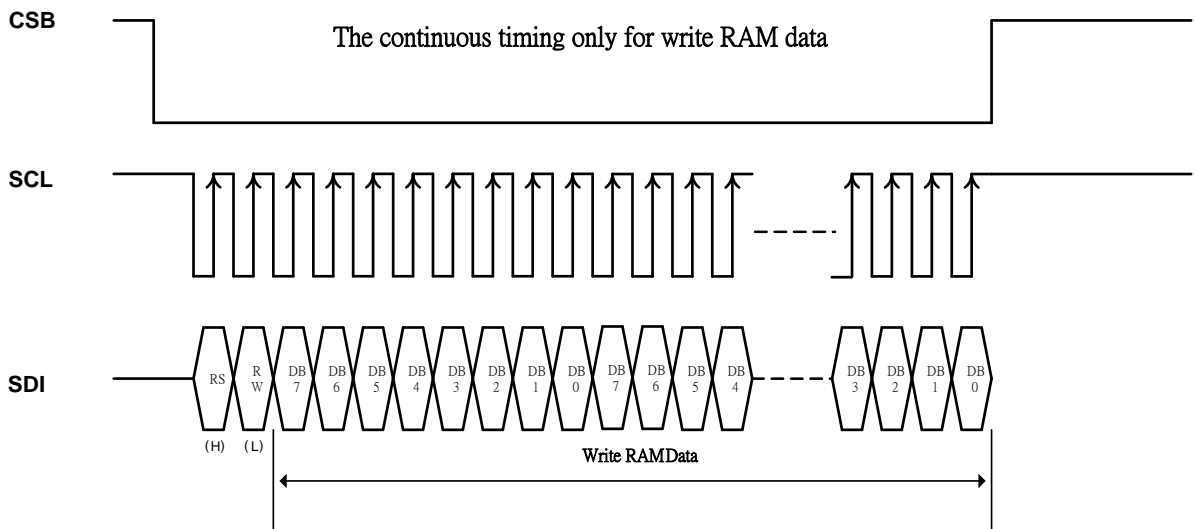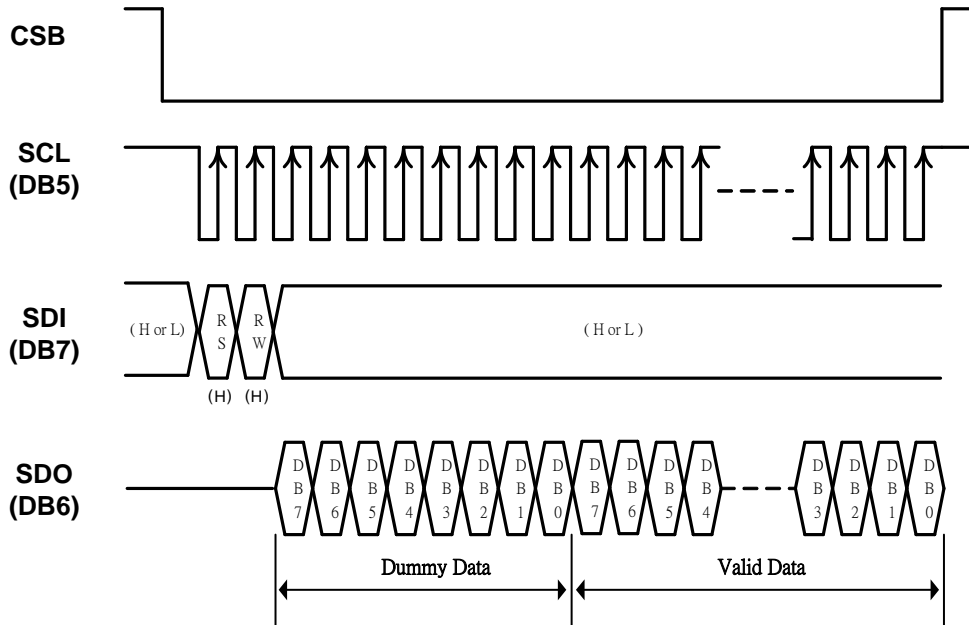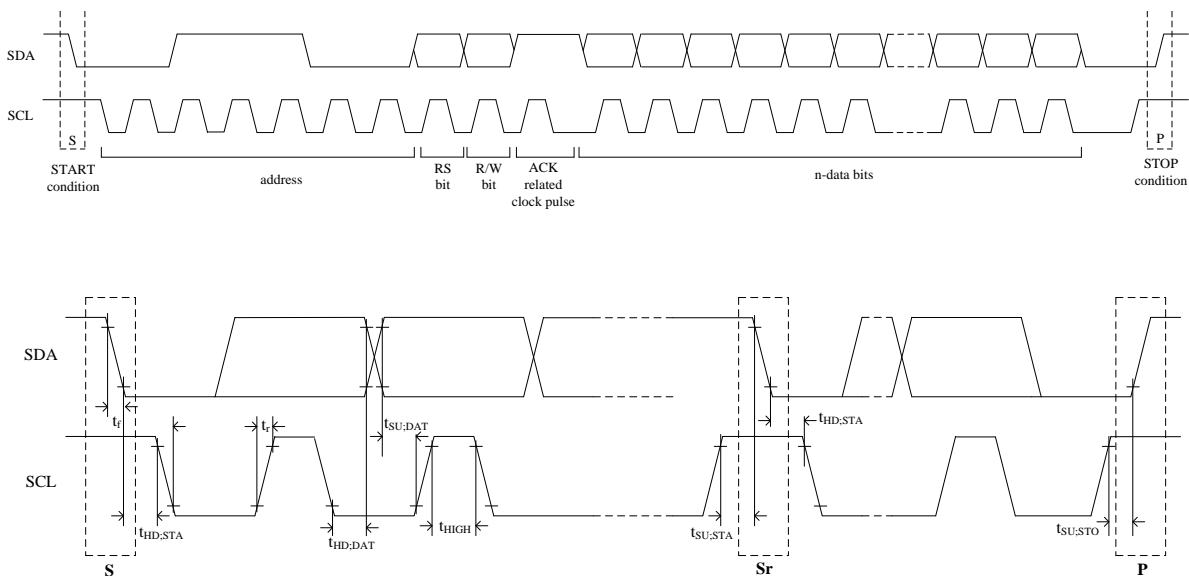
8800-series interface
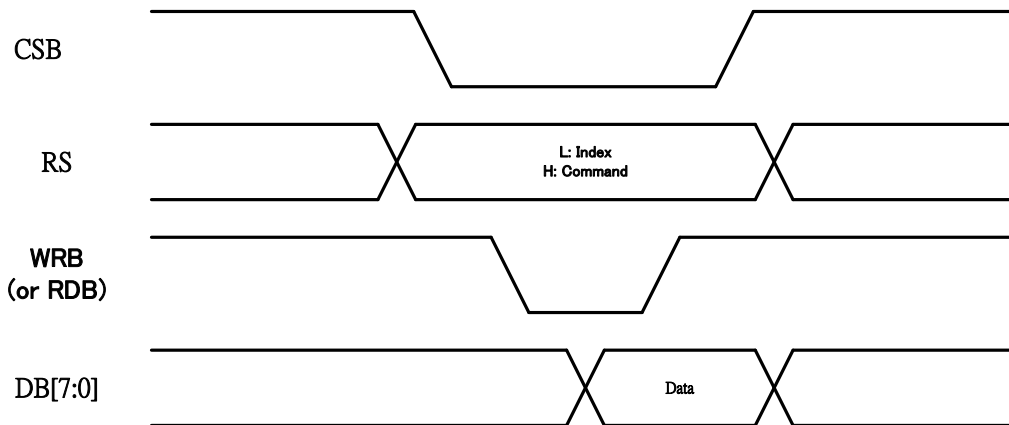
(a) 8-bit mode

When reading back the display data, the dummy read is required. The first readout byte is a dummy byte, and the subsequent bytes are the valid ones.

(b) 4-bit mode

When reading back the display data, the dummy read is required. The first two readout nibbles are dummy bytes, and the subsequent nibbles are the valid ones. (high-nibble first, low-nibble next)

RS0012

Serial interface

3- Line Series Write
(a) Command / RAM Data(Single)

CSB

CSB to pull high after command or data finished

SCL

SDI

(H) (L)

RS=L-> Write Command

Write RAMData

(b) RAM Data Continuous Write

CSB

The continuous timing only for write RAM data

SCL

SDI

(H) (L)

Write RAMData

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3- Line Series Read (Display data read only)

When reading back the display data, the dummy read is required. The first readout byte is a dummy byte, and the subsequent bytes are the valid ones.

IIC interface Timing Characteristics

When reading back the display data, the dummy read is required. The first readout byte is a dummy byte, and the subsequent bytes are the valid ones.

(V**CC** = 2.7 to 5.5V, Ta = -30 to +80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
SCL clock frequency		fSCL	0	-	400	kHz	
Set-up time for START condition		tSU;STA	600	-	-	ns	
Hold time for START condition		tHD;STA	600	-	-	ns	
Low period of the SCL clock		tLow	1300	-	-	ns	
High period of the SCL clock		tHIGH	600	-	-	ns	
Data set-up time		tSU;DAT	100	-	-	ns	
Data hold time		tHD;DAT	-	-	900	ns	
Rise time of both SDA and SCL signals		tr	T.B.D	-	300	ns	
Fall time of both SDA and SCL signals		tf	T.B.D	-	300	ns	
Set-up time for STOP condition		tSU;STO	600	-	-	ns	

OLED INTERFACE

RS0012 supports two display types in characteristic mode, namely: 5 x 8 dots and 5 x 10 dots character fonts. Each of these types includes a cursor display. Up to 2 lines may be displayed in a 5x 8 dot character font type and 1
line for a 5 x 10 dots character font type. The number of lines that can be displayed as well as the type of font can be selected by using the software program. Please refer to the table below

Number of Display Line	Character Font Type	Number of Common Signals	Duty Factor
1	5 x 8 dots + cursor	8	1/8
1	5 x 10 dots + cursor	11	1/11
2	5 x 8 dots + cursor	16	1/16

As shown in the table above, three types of common signals are available. An example of each configuration is shown in the examples below. It should be noted that every 5 segment signal lines can display one digit, therefore, RS0012 can display up to 8 digits in a 1-line display and 16 digits in a 2-line display.
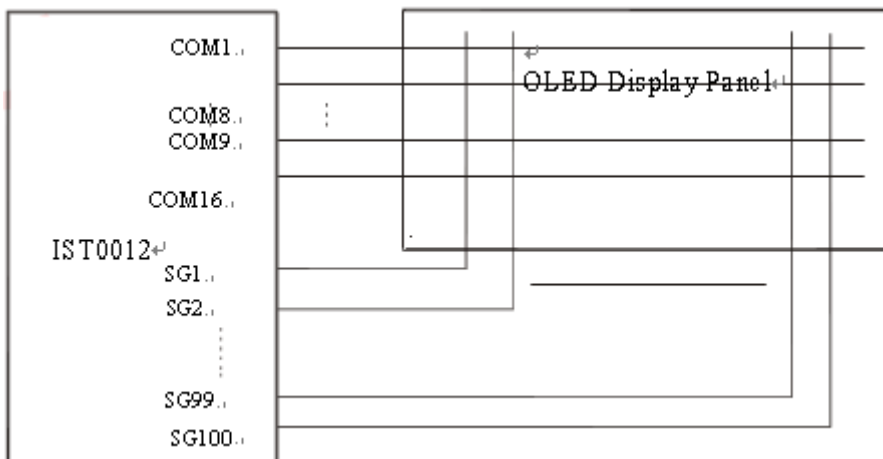
Example 1: An OLED and RS0012 interface with a 5 x 10 dot, 8-character x 1-line display at 1/11 duty cycle is given below.
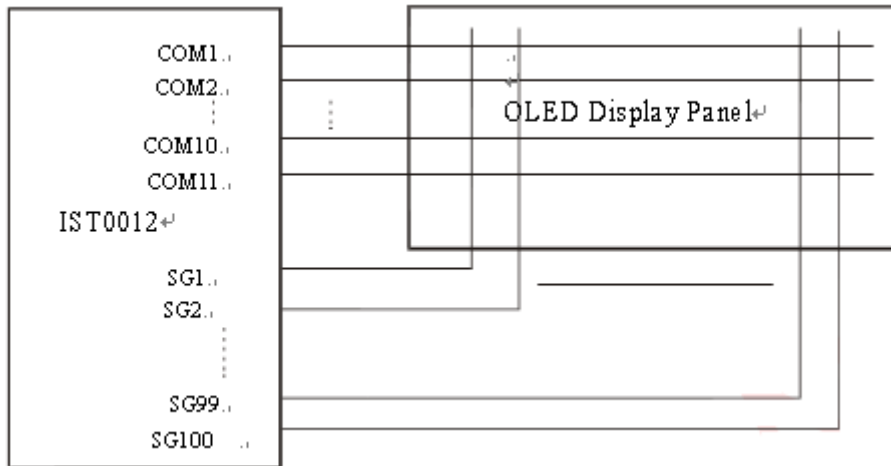
Example 1: An OLED and RS0012 interface with a 5 x 10 dot, 8-character x 1-line display at 1/11 duty cycle is given below.
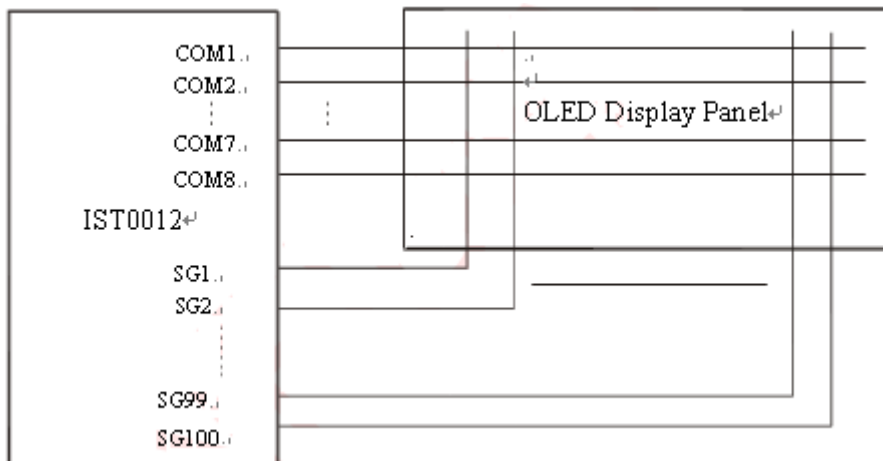
Example 3: OLED and RS0012 Connection when 5 x 8 dots, 8-character x 2-line display at 1/16 duty cycle.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Supply voltage range	VCC/VCI	- 0.3 to +6.5	V
	V16	-0.3 to +19.0	V
Input voltage range	V_{IN}	-0.3 to VCC + 0.3	V
Operating temperature range	T_{OPR}	-30 to +80	℃
Storage temperature range	T_{STR}	-55 to +125	℃

NOTES:
1. VCC/VCI and V16 are based on GND = 0V
2. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

(GND = 0V, VCC = 2.6 to 5.5V, Ta = -30 to +80℃)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating Voltage		VCC		2.6	-	5.5	V	VCC
Operating Voltage		V16		-	-	16	V	V16
Input voltage	High	V_{IH}		0.9 VCC	-	VCC	V	*1
	Low	V_{IL}		GND	-	0.1 VCC		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8 VCC	-	VCC	V	*2
	Low	V_{OL}	I_{OL} = 0.5mA	GND	-	0.2 VCC		
Input leakage current		IIL\IIH	V_{IN} = VCC or GND	-1	-	1	µA	*1
Oscillator frequency		fosc			1200		KHz	OSC(for external)
High level segment output current		ISEGOH	VSEGOH=14V	-30	-	-300	µA	SEG1~100
High level segment output current tolerance		ITOL	VSEGOH=14V	-	-	±6	%	SEG1~100
Low level common sink current		ICOMOL	VCOMOL=0.4V	15	-	-	mA	COM1~16
DC-DC1 converter output voltage		V16	-	-	-	16	V	V16
DC-DC2 converter output voltage		V16			7.2			
Standby current		Istd	(*3)	-	-	10	uA	VCC
Operating current		IVcc	VCC=3.3V, 25℃ fosc= 1.2MHz No loading External V16	-	-	500	uA	VCC

[Notes]

*1: MS,D,SHL,CSB,DB7~DB0,RESETB,RS,RDB,WRB,OSC,IM1,IM0,DISP,SYNC

*2: D, DB7~DB0, OSC, DISP, SYNC

*3: VCC=3.3V ,25℃ ,OSC = OFF ,All power = OFF

AC CHARACTERISTICS
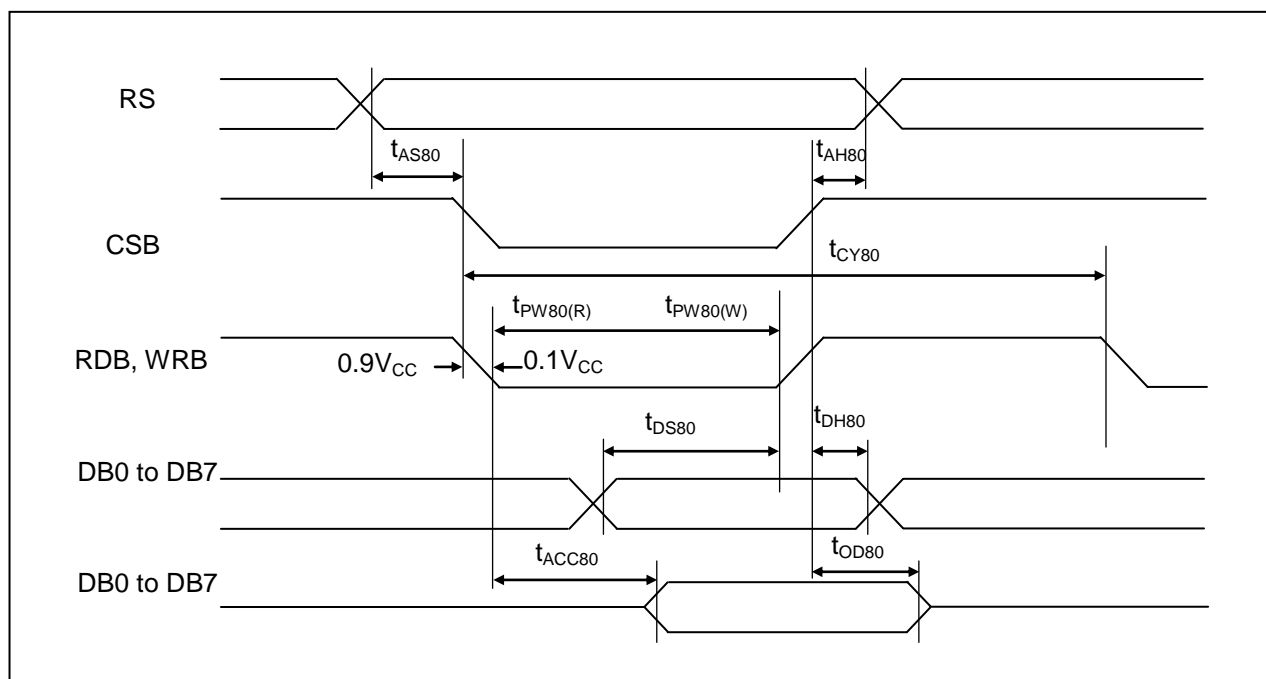
Read / Write Characteristics (8080-series MPU)

Figure 1. Read / Write Characteristics (8080-series MPU)

V_{CC} = 2.6 to 5.5V, Ta = -30 to +80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t$_{AS}$80 t$_{AH}$80	20 0	- -	- -	ns	
System cycle time (Write)	---	t$_{CY}$80(W)	500	-	-	Ns	● 4-bit MCU interface
			850	-	-	ns	● 8-bit MCU interface
System cycle time (Read)	---	t$_{CY}$80(R)	1000	-	-	ns	● 4-bit MCU interface
			1200	-	-	ns	● 8-bit MCU interface
Pulse width (WRB)	RW_WRB	t$_{PW}$80(W)	250	-	-	ns	
Pulse width (RDB)	E_RDB	t$_{PW}$80(R)	500	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t$_{DS}$80 t$_{DH}$80	40 20	- -	- -	ns	
Read access time Output disable time		t$_{ACC}$80 t$_{OD}$80	- 10	- -	180 -	ns	C_L = 100pF

Read / Write Characteristics (6800-series Microprocessor)
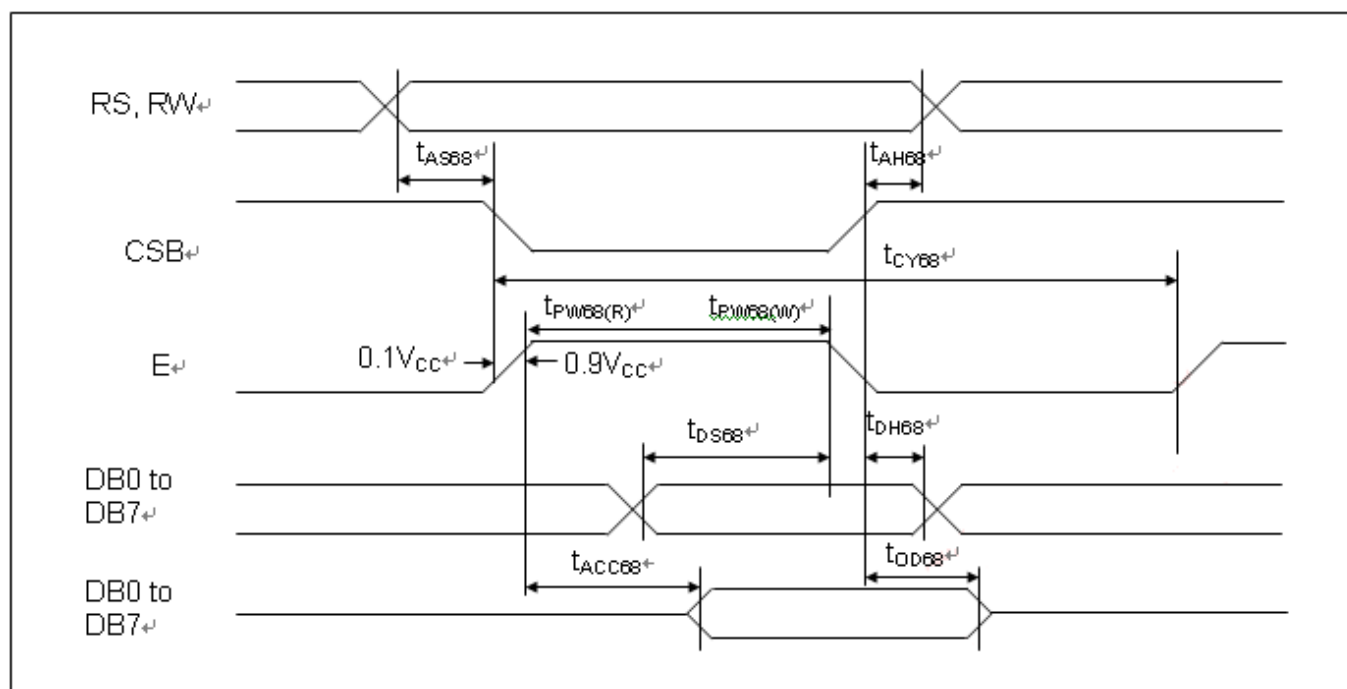
Figure 3. Serial Interface Characteristics

(V**CC** = 2.6 to 5.5V, Ta = -30 to +80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	DB5 (SCL)	t**CYS** t**WHS** t**WLS**	300 100 100	- - -	- - -	ns	
CSB setup time CSB hold time	CSB	t**CSS** t**CHS**	150 150	- -	- -	ns	
Data setup time Data hold time	DB7 (SDI)	t**DSS** t**DHS**	100 100	- -	- -	ns	
Read access time	DB6 (SDO)	t**ACCS**	-	-	80	ns	
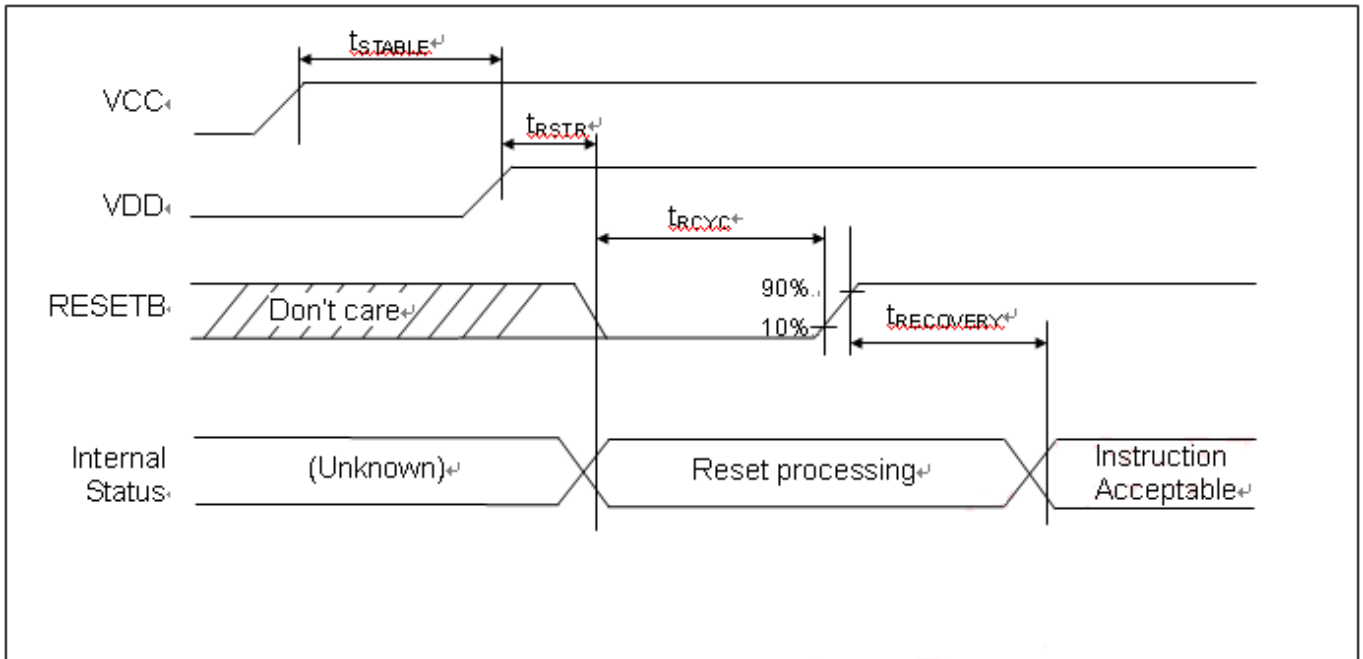
Reset Input Timing

Figure 4. Reset Input Timing

(V_{CC} = 2.6 to 5.5V, Ta = -30 to +80℃)

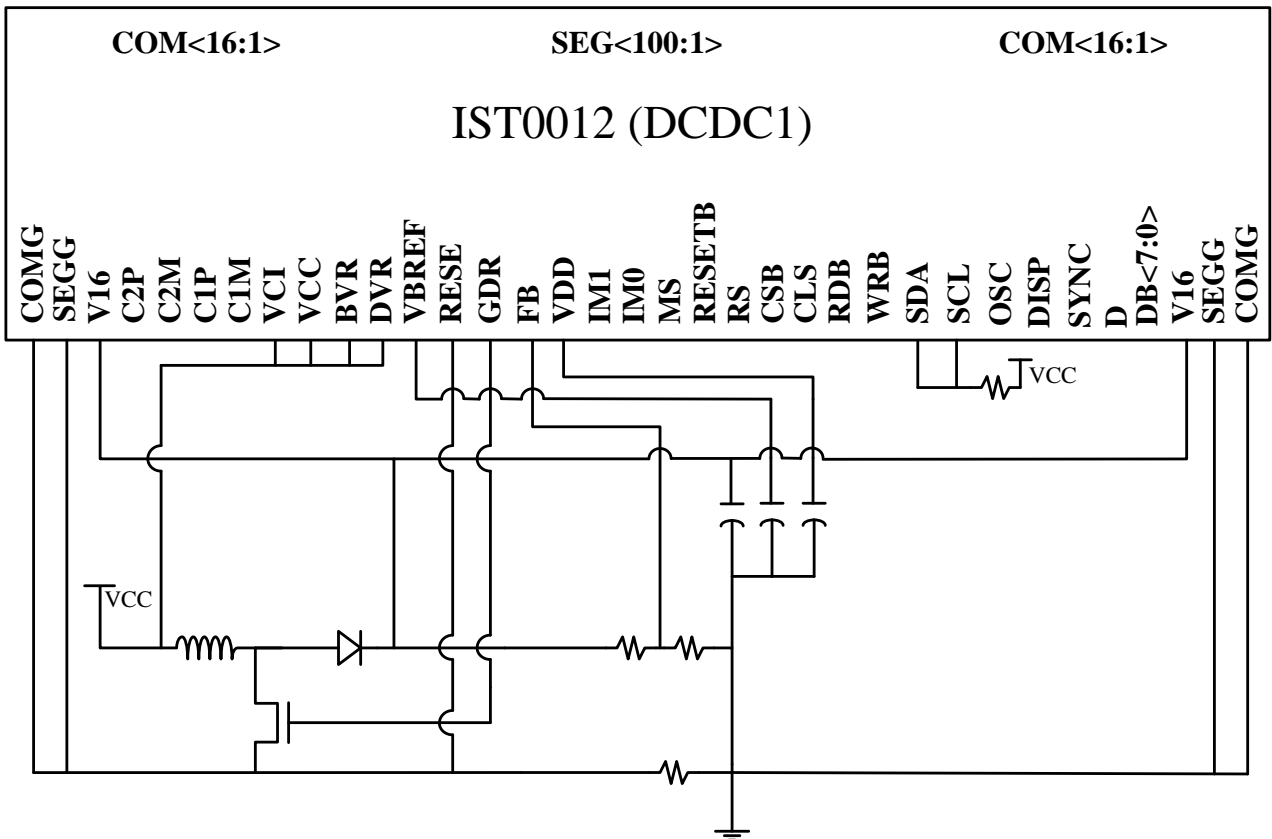| Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
VDD stable time	VDD	t_{STABLE}	500	-	-	ms	C1=1uF (*1)
Reset start time	RESETB	t_{RSTR}	0	-	-	us	
Reset cycle time	RESETB	t_{RCYC}	2.5	-	-	us	
Reset recovery time	RESETB	$t_{RECOVERY}$	2.0	-	-	us	(*2)

NOTE

*1. t_{STABLE} varies depending on different capacitance of C1 (stabilizing capacitor), and It should be re-adjusted for different C1.

*2. The first instruction should only be issued after the internal reset processing has been completed.
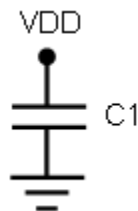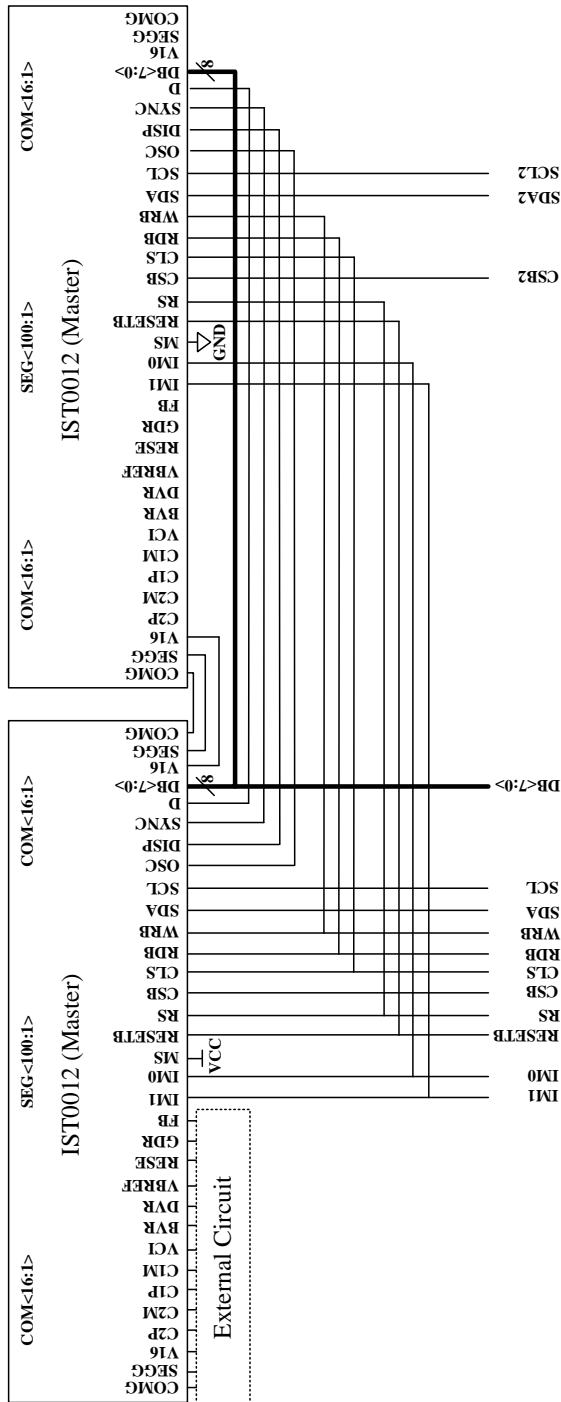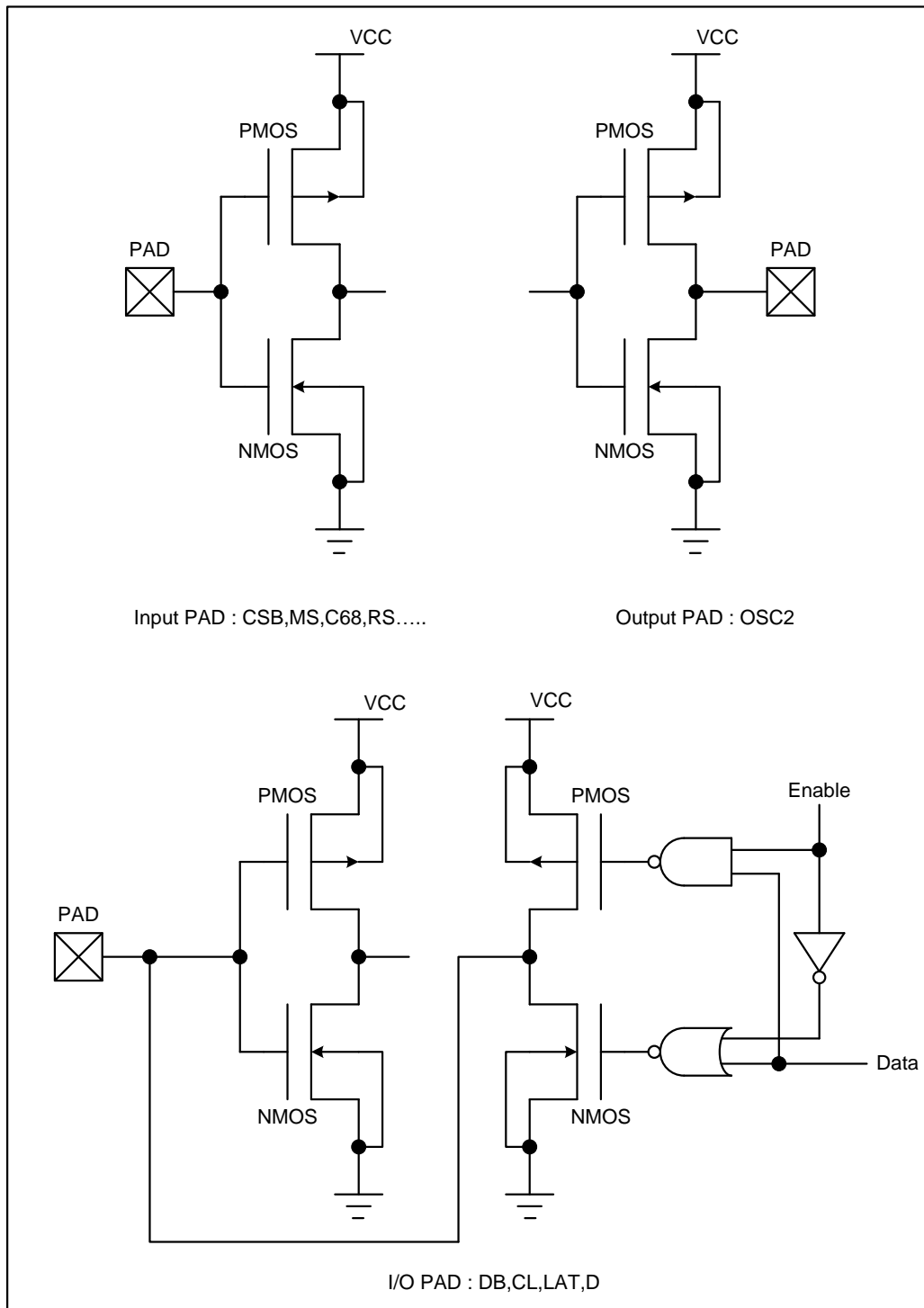
APPLICATION CIRCUIT

DCDC1&2 APPLICATION

COM<16:1>   SEG<100:1>   COM<16:1>

IST0012 (DCDC1)

COMG SEGG V16 C2P C2M C1P C1M VCI VCC BVR DVR VBREF RESE GDR FB VDD IM1 IM0 MS RESETB RS CSB CLS RDB WRB SDA SCL OSC DISP SYNC D DB<7:0> V16 SEGG COMG

COM<16:1>   SEG<100:1>   COM<16:1>

IST0012 External V16

COMG SEGG V16 C2P C2M C1P C1M VCI VCC BVR DVR VBREF RESE GDR FB VDD IM1 IM0 MS RESETB RS CSB CLS RDB WRB SDA SCL OSC DISP SYNC D DB<7:0> V16 SEGG COMG

External V16 Power Supply
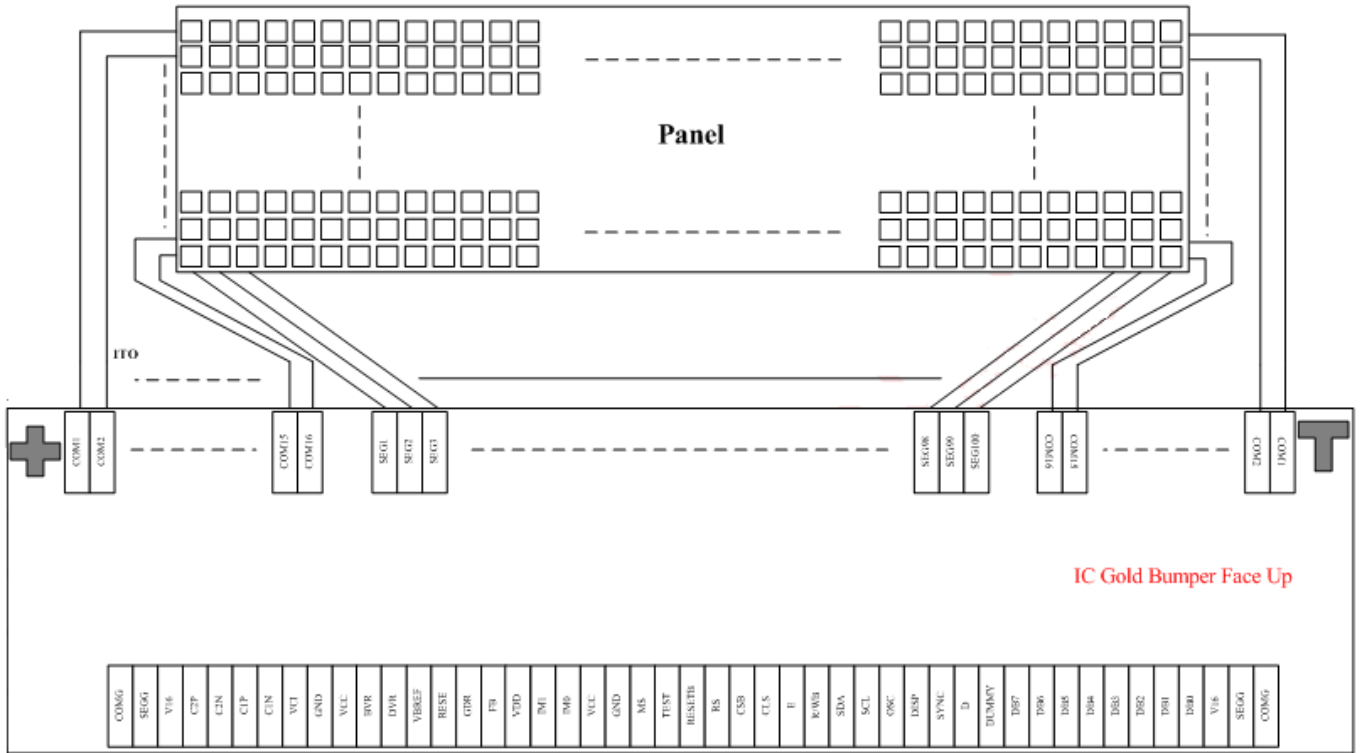
MASTER/SLAVE APPLICATION

I/O PAD CONFIGURATION

Input PAD : CSB,MS,C68,RS…..

Output PAD : OSC2

I/O PAD : DB,CL,LAT,D

CAUTIONS:

  1.This Specification will be subjected to modify without notice.

  2.Precutions on Light:

   Characteristics of semiconductor devices can be changed when exposed to light as described in the
      operational principles of solar batteries. Exposing this IC to light ,therefore ,can potentially lead to its
      malfunctioning.

  2.1Care must be exercised in designing the operation system and mounting the IC so that it may   not
      be exposed light during operation .

  2.2Care must be exercised in designing the inspection process and handling the IC so that it may not be
      exposed to light during the process.

  2.3The IC must be shielded from light in the front , back and side faces.

3.ESD control and prevention:

    3.1Humidity Control:30~70% relative humidity is recommended.

    3.2To reduce the risk of ESD, all equipment at the wok surface should be properly grounded and all
      sources of static fields removed.(Example: Station ionizers).

    3.3Grounding all personnel who come in contact with parts will eliminate a possible source of ESD.
      (Example: Wrist straps remove charge from the body and constitute a central part of ESD control).

4.Storage Conditions:

Before open package	After open package
Temp.=25±5℃ Humidity:50~70% Less than 1 Years	Temp.=25±5℃ Humidity:50~70% Less than 3 Months