Anlogic Technology EAGLE Series FPGA Data Sheet

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Table of Contents

1 Introduction

1.1 EAGLE Device family features

■ Flexible logical structure

- 4 devices ranging in size from 4,320 to 49,000 LUTs and user IOs ranging from 93 to 456.

■ Low-power device

- Advanced 55nm low-power process
- Static power consumption as low as 5mA

■ Support for distributed and embedded memory

- 392K bits distributed memory (maximum)
- 2M bits embedded block memory (maximum)
- Embedded block memory capacity 9K bits, configurable as true dual-port, 8Kx1 to 512x18 mode
- Dedicated FIFO control logic
- Embedded block memory capacity 32K bits, configurable as true dual-port, can be set to 2K*16 or 4K*8

■ Configurable logic modules (PLBs)

- Optimized LUT4/LUT5 combination design
- Dual-port distributed memory
- Support for arithmetic logic operations
- Fast carry chain logic
- Single slice supports 2M 18x18 or 4M 9x9

■ Source-synchronous input/output interface

- Input/output unit contains DDR register
- Generic DDRx1
- Generic DDRx2

■ High performance, flexible input/output buffer

- Configurable to support the following single-ended standards:
- LVTTL
- LVCMOS (3.3/2.5/1.8V/1.5/1.2V)
- PCI
- SSTL 3.3V (Class I and II)
- SSTL 1.8V and 1.5V (Class I and II)
- HSTL 1.8V and 1.5V (Class I and II)
- Support for the following differential standards through configuration
- LVDS，Bus-LVDS， MLVDS， RSDS， LVPECL
- Support hot swap
- Configurable pull-up/pull-down mode
- On-chip 100 ohm differential resistor
- Configurable Schmitt trigger with a maximum 0.5V hysteresis

■ Clock resource

- Optimize the global clock's 2-way fast clock
- 2 IOCLKs designed for high speed I/O interfaces
- 16-channel global clock
- Supports up to 4 PLLs for frequency synthesis
- 5 clock outputs
- Dividing factor 1 to 128
- Supports 5 channels of clock output cascade
- Dynamic phase selection

Configuration mode

- Main mode serial SPI (MSPI)
- Slave mode serial (SS)
- Main mode parallel x8 (MP)
- Slave mode parallel x8 (SP)
- JTAG mode (IEEE-1532)

Each chip has a unique 64-bit DNA

BSCAN

- Compatible with IEEE-1149.1

Embedded hard core IP

- ADC
  - 12-bit successive approximation register type (SAR)
  - 8 analog inputs
  - 1MHz sampling rate (MSPS)
- Integrated voltage monitoring module
- Built-in ring oscillator

Package

- TQFP/BGA/QFN

Table 1-1-1 Members of the EAGLE FPGA family

General feature	EAGLE_4	EAGLE_10	EAGLE_20	EAGLE_50
Number of LUTs	4,480	8,640	19,600	49,000
Number of FFs	4,480	8,640	19,600	49,000
Equivalent Number of LUTS	4,928	10,368	23,520	58,800
Number of Dis-Ram bits	35,840	69,120	156,800	392,000
Number of BRAM9K	12	48	64	96
Number of BRAM32K	2	2	16	32
Total BRAM bits	176,128	507,904	1,114,112	1,933,312
Number of DSP	11	21	29	144
PLL	4	2	4	4
Low-skew gclock in chip	16	16	16	16
User IO Banks	0	8	8	8
Maximum user Ios	270	184	270	456

Table 1-1-2 EAGLE FPGA Package

Packages	EAGLE_4	EAGLE_10	EAGLE_20	EAGLE_50
100 TQFP (14x14, 0.5mm pitch)	76/15			
144 TQFP (20x20, 0.5mm pitch)	93/21	95/23		
256 fpBGA (17x17, 1.0mm pitch)		184/92	193/90	187/90
780 fpBGA (29x29, 1.0mm pitch)				456/190

193/90 indicates user availability IO/user available differential output (LVDS) pair

1.2 EAGLE device introduction

Anlogic's latest EAGLE family of FPGAs has four devices that target the low-cost, low-power programmable market. Designed for high-volume, cost-sensitive applications, EAGLE devices enable system designers to reduce costs while meeting ever-increasing bandwidth requirements.

The EAGLE device family is built on an optimized low-power process and achieves high functionality at the lowest cost. EAGLE devices are the ideal choice for low-cost, small-scale applications in the wireless, wireline, broadcast, industrial, and communications industries.

Anlogic Information provides a wealth of design tools to help users effectively use the EAGLE platform to achieve complex designs. Industry-leading integrated and place-and-route tools provide a powerful guarantee for users to design high quality products.

2 EAGLE Architecture introduction

The EAGLE family of devices consists of a look-up table logic block (PLB) array that forms the core resources, with input and output buffers distributed on four sides. An embedded block memory unit (BRAM9K) and a data signal processing module (DSP) are embedded in the middle of the PLB.

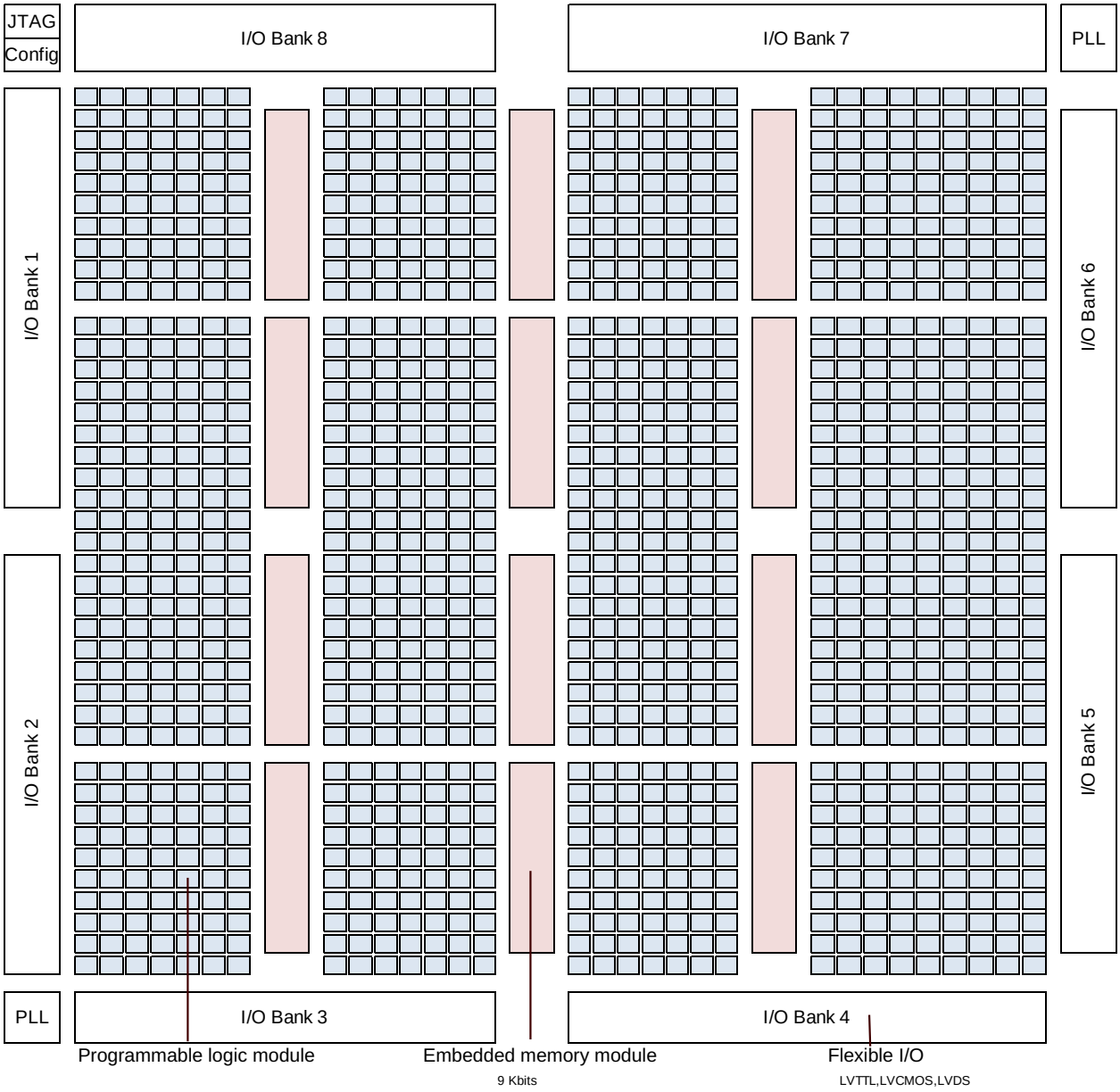


Figure 2-1 Simplified block diagram of the EAGLE-10k device

There are two types of lookup table logic modules, the logic programmable module (LSLICE) and the storage logic programmable module (MSLICE). Both modules support logic and arithmetic functions, except that MSLICE supports distributed RAM and ROM functions. Both the Logic Programmable Module (LSLICE) and the Storage Logic Programmable Module (MSLICE) are optimized for easy and efficient implementation of complex designs.

The EAGLE family of devices includes multi-row embedded memory blocks (BRAM) with a 9K memory module for fast data access. Each memory module can be independently configured as a 1-18 bit wide single or dual-port application.

EAGLE's I/O Buffers are divided into 8 groups and support multiple levels of single-ended and dual-ended levels.

The left and right I/Os can be configured as LVDS transmit/receive pairs.

The EAGLE series has two or four multi-function PLL blocks embedded in the four corners of the device. A dedicated clock line is connected to the two PLL inputs. The PLL has a divide-by-clock/multiplier/shift equal function.

2.1 PFB Module

Programmable logic blocks (PLBs) are arranged in a two-dimensional array according to row/column rules. Each PLB includes a programmable interconnect (Routing) and a Programmable Functional Block (PFB). The PFB is the core of the programmable function of the FPGA. The PFB inside the EAGLE device implements: logic, arithmetic, distributed RAM, ROM functions, and signal latching. The PFB contains 4 SLICEs, numbered 0~3. SLICE 0,1 is of type MSLICE and SLICE 2,3 is of type LSLICE.

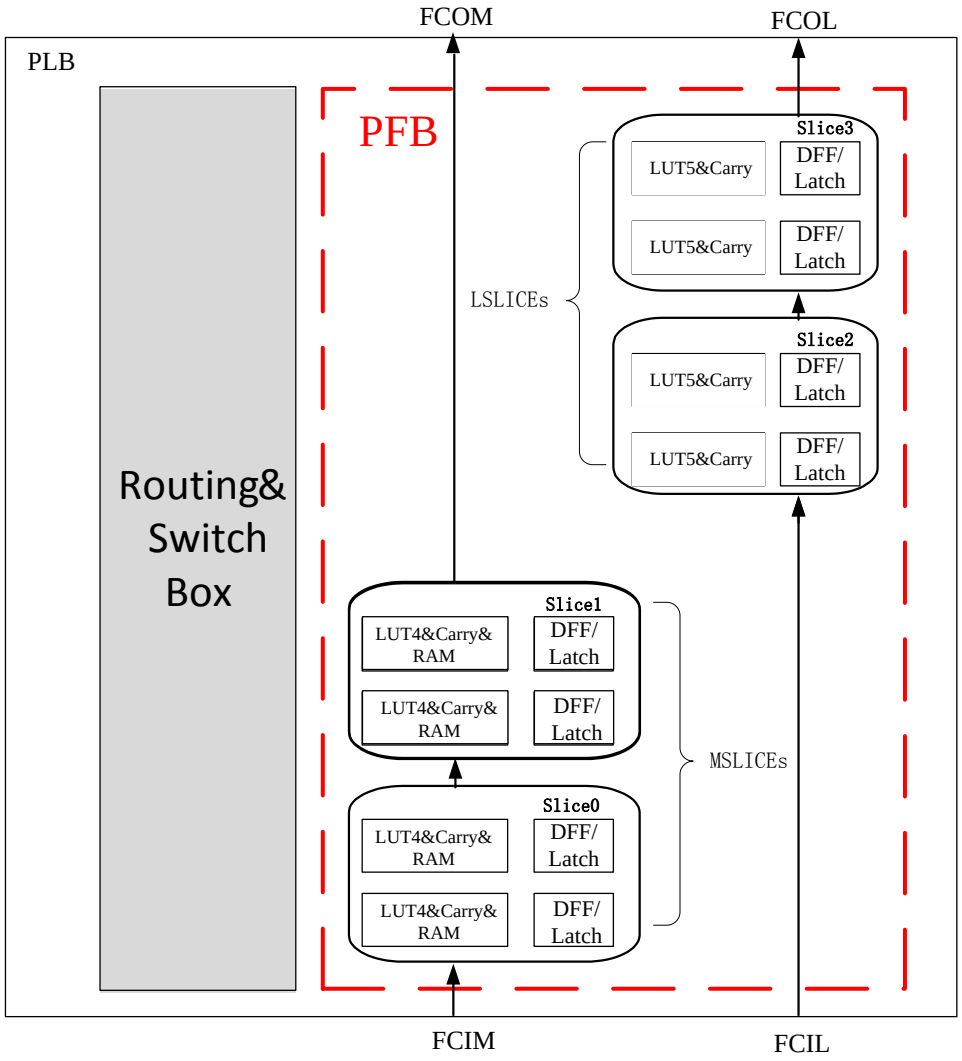


Figure 2-1-1 Programmable Function Block (PFB) Structure

2.1.1 SLICE

There are two SLICEs in the EAGLE PFB: MSLICE and LSLICE.

a) MSLICE

MSLICE includes 2 LUT4s and two registers and a 2-level carry chain. MSLICE can be additionally configured as a LUT-based distributed RAM function. The SLICE 0,1 in the PFB is of the MSLICE type and can be configured to be 16x4 RAM. The MSLICE internal logic implements a connection between LUT4s and can implement functions with more than 4 inputs, such as LUT5. Two MSLICEs combined enable a LUT6

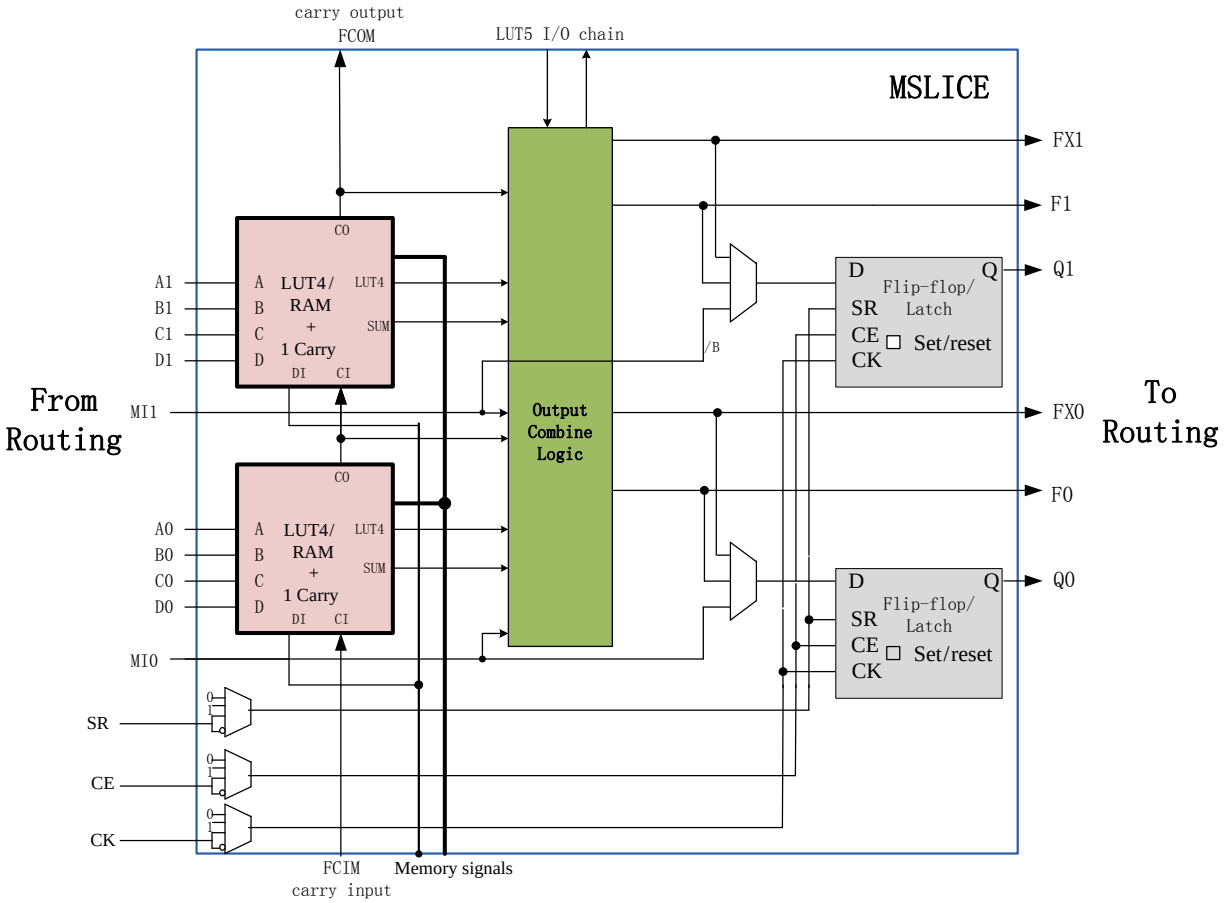


Figure 2-1-2 MSLICE structure diagram

The internal logic of MSLICE is shown in Figure 2-1- 2. There are two 4-input lookup tables (LUT4) with RAM write decoder combined with distributed RAM control logic inside the PFB. Each LUT4 can implement 16x1 bits of RAM memory, and two MSLICEs with one RAM controller. A 16x4 dual-port RAM is implemented. Each LUT4 in MSLICE can be combined with internal carry logic and carry input (FCIM) to implement a 1-bit full adder. An MSLICE implements 2-bit add/subtract and implements fast forward/borrow output (FCOM).

MSLICE and LSLICE have the same internal registers and can be configured as DFF or LATCH.

b) LSLICE

LSLICE includes 2 enhanced LUT5s and two registers and a 4-level carry chain. SLICE 2,3 in the PFB is of the LSLICE type. LSLICE internal logic can be implemented: split a LUT5s into 2 LUT4s; implement more input functions such as LUT5, LUT6. Two LSLICEs combined enable a LUT7.

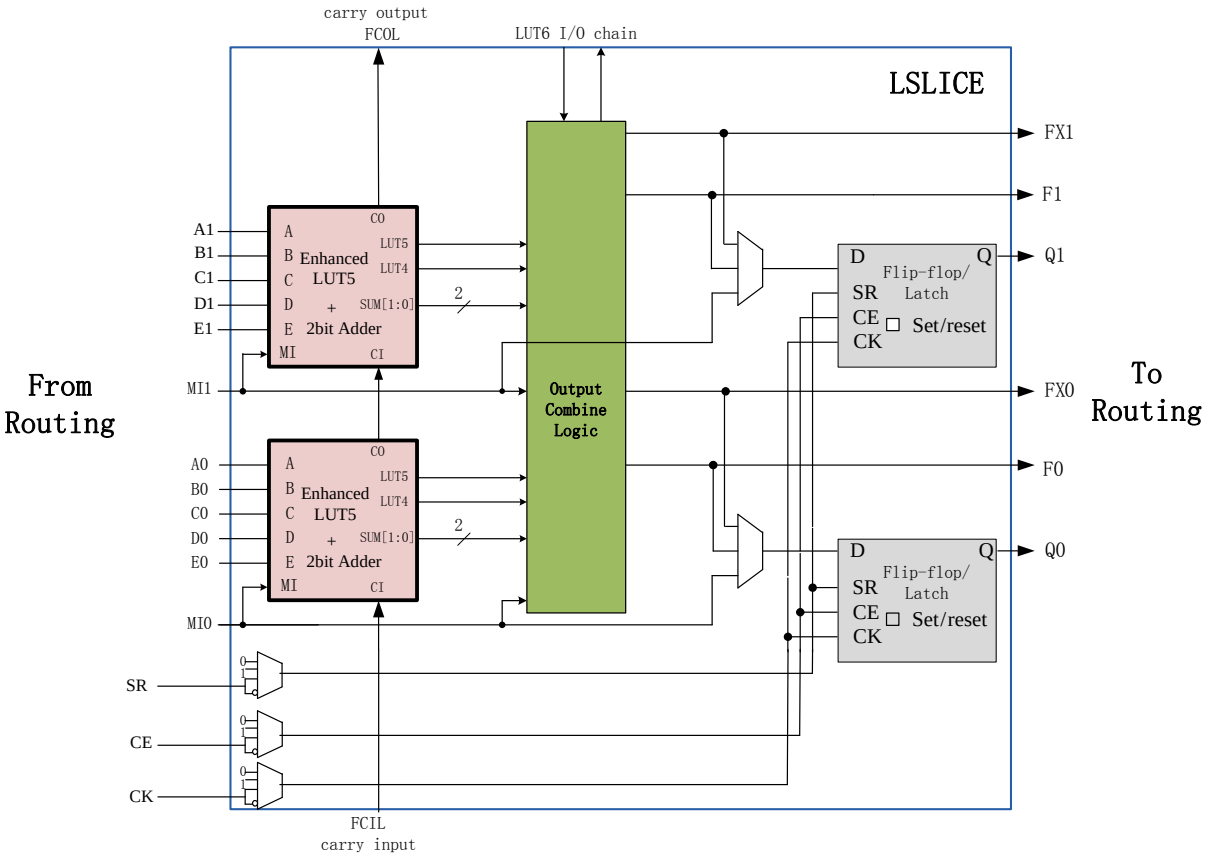


Figure 2-1-3 LSLICE structure diagram

The internal logic of LSLICE is shown in Figure 2-1- 3. There are four 4-input lookup tables (LUT4) and selection logic that can be combined to implement multiple logic functions: 4 LUT4s; 2 LUT4 + 1 LUT5; 2 LUT5s; 1 LUT6, etc. Each enhanced LUT5 combines internal carry logic with a carry input to implement a 2-bit full adder. An LSLICE implements 4-bit add/subtract and implements fast forward/borrow output (FCOL).

2.1.2 PFB Operating mode

MSLICE has four modes of operation: logic, arithmetic, distributed RAM and ROM.

LSLICE has three modes of operation: logic, arithmetic and ROM.

a) Logical mode

In logic mode, LUT4 in MSLICE is configured as a 4-input combinatorial logic lookup table, and any 4-input function can be implemented with this lookup table. The enhanced LUT5 in LSLICE can be configured into a variety of combined logical lookup tables. The LUTs within SLICE can also be cascaded into larger lookup tables via internal output combining circuits.

Table 2-1-1 Common Logic Implementation

LUT5	1 MSLICE	1/2 LSLICE
MUX4	1 MSLICE	1/2 LSLICE
LUT6	2 MSLICE	1 LSLICE
LUT7		2 LSLICE

b) Arithmetic mode

Arithmetic mode utilizes SLICE's internal fast carry chain for fast and efficient arithmetic, and both MSLICE and LSLICE support arithmetic mode. The arithmetic logic that can be supported is: addition, subtraction, add/subtractor with control selection, counter, multiplier, and comparator.

There are two carry chains inside the PFB, which are connected to the vertical MSLICE and the vertical LSLICE. The wide-bit arithmetic logic can be implemented by cascading vertically adjacent PFBs.

c) Distributed RAM mode

MSLICE can be configured in this mode. Two MSLICE: SLICE0 and SLICE1 can be combined to configure 16x4 simple dual-port RAM (one-stop/one-stop).

d) ROM mode

All SLICEs can be used as ROM mode under LUT logic, and the user can set the ROM initial value through software.

2.1.3 Register

Each SLICE in the PFB contains 2 configurable registers. The output of the LUT can be latched or the MI input from the interconnect. Register Configuration Options:

- Edge-triggered latch (DFF) or level-enable latch (LATCH)
- Reset synchronously or asynchronously 0 or set 1
- Whether with ClockEnable enable
- CLK/CE/SR with rising edge/falling edge /0/1 select

2.1.4 Interconnection (Routing)

Programmable interconnects enable signal transfer between individual functional blocks within the FPGA. The EAGLE family of devices has a wide range of interconnect resources, including line-to-line gating switches, line buffers, and signal traces. EAGLE series interconnects are all equipped with buffers for high speed signal transmission and reliable signal integrity.

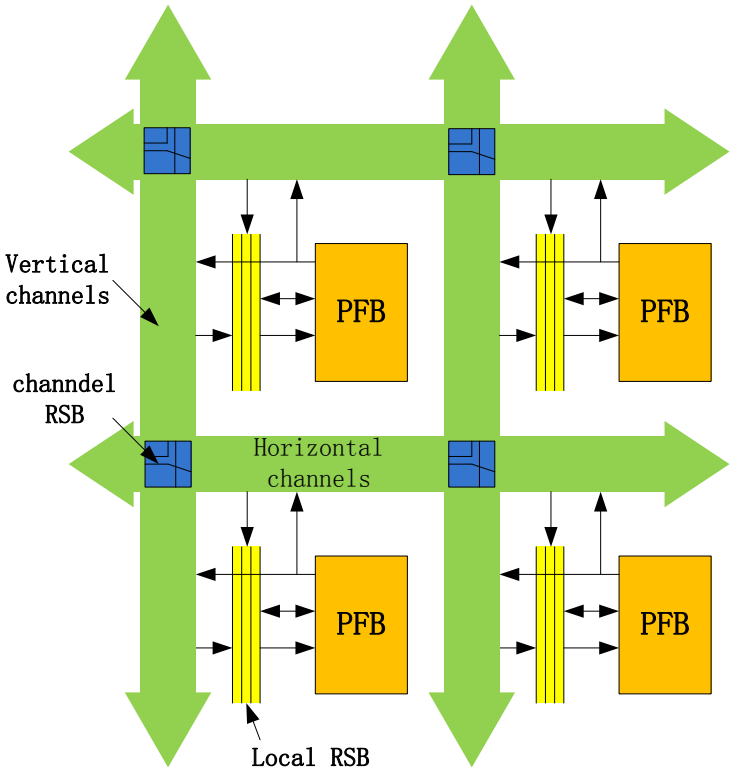


Figure 2-1-4 EAGLE Interconnect Architecture

Signals between PFBs are transmitted through horizontal and vertical channels. The PFB can directly drive horizontal/vertical channels. The channels are switched between channels RSB (routing switch box).
The signal transmitted on the channel enters the PFB via local RSB.

2.2 Embedded memory module (BRAM)

2.2.1 Introduction

The EAGLE family of devices supports embedded memory modules (BRAM). Two types of BRAM are included in EAGLE: BRAM9K and BRAM32K.

The BRAM9K has a capacity of 9Kbits per block, and multiple BRAM9K modules are arranged in a row and distributed in columns in the PFB array. The height of each BRAM9K is equivalent to 2.25 PFBs. 4 BRAM9K is equal to the height of 9 PFBs.

The BRAM32K has a capacity of 32Kbits per block and is distributed in the IO gap.

BRAM9K can achieve:

- Single port RAM/ROM
- Dual-port RAM
- Simple dual-port RAM (also known as pseudo dual-port)
- FIFO (embedded with hardware FIFO controller in EMB9K)

Features supported by the BRAM9K module are:

- 9216 （9K）bits / per block
- A/B port clock independent
- A/B port data width can be separately configured, true dual-port from x1 to x9, support x18 simple dual-port (write one read)
- 9 or 18-bit write operation with Byte Enable control
- Output latch selectable (supports 1-stage pipeline)
- Supports data initialization in RAM/ROM mode (initialize BRAM9K data during configuration via initialization file)
- Supports multiple write modes. You can choose to write only (Normal), Read before Write (Write before Write), Write through (Write through) three modes.

Table 2-2-1 BRAM9K Features

Category	Characteristic
capacity	9K
Configuration (depth x bit width)	8192 x 1　4096 x 2　2048 x 4 1024 x 8 or 9　512 x 16 or 18
Parity bits	8+1　16+2
Byte enable	Selectable
Input address/data register	Yes
Single-port mode	Supported
Simple dual-port mode	Supported
True dual-port mode	Supported
ROM mode	Supported
FIFO mode	Supported
Data output register	Selectable
Independent data output register enable	Yes
Read-during-write	Output old data (read before write) Output write (write through)
Pre-work RAM initialization	Supported

Byte Enable

The BRAM9K supports a byte enable function that masks the write data in bytes during a write operation and the masked bytes are not written to RAM. The byte enable (Byte Enable[1:0]) signals correspond to the datain[15:8] and datain[7:0] of the write data, respectively.

Read-during-Write

The ERAMLE family of BRAM9K supports read-during-write on the same port. Read-during-write means that in the single-port RAM or true dual-port RAM mode, the user reads the data of the same address to the output port while writing data. The default is not rdw selection, the output data remains unchanged (No change).

In RDW mode, the user has two choices: read the previous data (Read Before Write); read the new data, which is the data to be written (Write Through).

2.2.2 RAM Memory mode

The BRAM9K is divided into RAM memory mode (including ROM) and FIFO mode according to the operating mode. The BRAM9K user port names and settings are slightly different in both modes.

BRAM9K is a separate A/B port dual RAM in RAM mode, supporting multiple modes of synchronous RAM and ROM operation.

2.2.3 RAM Port signal in memory mode

The control signal and clock input signal of BRAM9K are completely independent. The input control signals are:

Chip select signal (ChipSelect)

Clock enable (Clock Enable)

Input/output register reset control signal (RST)

Write/read operation (WE)

Data output register latch enable (OCE)

Byte enable (Byte Enable[1:0]).

Table 2-2-2 is the control signal logic

Operating	CLK	CS	ClockEnable	RST	WE
Write operation	Rising edge	1	1	0	1
Read operation	Rising edge	1	1	0	0
IDLE	x	1	0	0	x
Save power	x	0	0	0	x

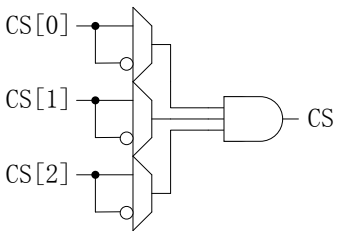
The ports of BRAM9K are as follows:

Table 2-2-3 Port Signals in RAM Mode

A port name	Direction	Description
dia[8:0]	Input	A port data input, simple dual-port 18-bit input port mode as low 9-bit data input
addra[12:0]	Input	The A port address is input, [12:4] is always valid as the word address, and [3:0] depends on the bit mode. In 18-bit mode, addra[1:0] is multiplexed into the byte enable signal Byte Enable[1:0].
Doa[8:0]	Output	A port data output, simple dual-port 18-bit output port mode as low 9-bit data output
clka	Input	A port clock input, valid for the rising edge (reverse), simple dual-port 18-bit mode as input address / data port clock
rsta	Input	A port reset signal, default high active (reversible), configurable synchronous/asynchronous reset
cea	Input	A port clock active control signal, default high active (reversible).
Wea	Input	A port write/read operation control, 1 is a write operation, 0 is a read operation, and is fixed to 1 in 18-bit write mode.
Csa[2:0]	Input	A port 3-bit chip select signal (reversible), csa[2:0]=3'b111 BRAM is selected for operation. The 3-bit signals can be independently set to reverse.
Ocea	Input	The A port data register clock is enabled and the default is high active (reversible). Only valid when the output register is used (REGMODE_A="OUTREG").
B port name	**Direction**	**Description**
dib[8:0]	Input	B port data input, high 9-bit data input in 18-bit input port mode
addrb[12:0]	Input	B port address input, [12:4] is always valid as word address, [3:0] depends on bit mode
dob[8:0]	Output	B port data output, high 9-bit data input in 18-bit output port mode
clkb	Input	B port clock input, default rising edge active (reversible), simple dual-port 18-bit mode as output address / data port clock
rstb	Input	B port reset signal, default high active (reversible), configurable synchronous/asynchronous reset
ceb	Input	B port clock active control signal, default high active (reversible).
Web	Input	B port write/read operation control, 1 is a write operation, 0 is a read operation, and is fixed to 0 in the 18-bit read mode.
Csb[2:0]	Input	B port 3-bit chip select signal (reversible), csb[2:0]=3'b111 BRAM is selected for operation. The 3-bit signals can be independently set to reverse.
Oceb	Input	The B port data register clock is enabled and the default is high active (reversible). Only valid when the output register is used (REGMODE_B="OUTREG").

■ Multi-bit chip select signal logic description:

BRAM9K CS in RAM and FIFO mode is generated by a reversible 3-bit chip select input. The logic is shown below (CSA, CSB in RAM mode / CSW, CSR in FIFO mode):



Configuration properties of CS: "SIG" means that the corresponding CS[x] input signal is straight through, and "INV" means that the signal is reversed.

The 3-bit CS input reverse configuration enables address decoding without additional logic, making it easy to scale up to 2~8 blocks of RAM.

- **Byte enable in 18-bit mode (Byte Enable) :**

  The BRAM9K supports a byte enable function that masks the write data in bytes during a write operation and the masked bytes are not written to RAM. The byte enable (Byte Enable[1:0]) signals correspond to the datain[16:9] and datain[8:0] of the write data, respectively. For example, Byte Enable[1:0]==00, neither byte will be written; Byte Enable[1:0]==01, low byte write (dia). In 18-bit mode, the Byte Enable Byte Enable[1:0] signal is multiplexed with the port addra[1:0].

- **Read-during-Write**

  The ERAMLE family of BRAM9K supports read-during-write on the same port. Read-during-write means that when the data is written in single-port RAM or true dual-port RAM mode, the user reads the data of the same address and outputs it to the output port. The default write mode (Normal) is selected, and the output data remains unchanged.

  In RDW mode, the user has two choices: read the previous data (Read Before Write); read out the new data (Write Through).

2.2.4 Common configuration in RAM memory mode

a) Single-Port Mode

Single-port mode supports read or write operations to the same address that are not simultaneous. There are two sets of read/write control logic inside the BRAM9K to manage port A and port B respectively, so BRAM9K can support two single-port mode RAM or ROM. Usually the ROM also works in this mode.

BRAM9K bit width supported in single port mode

- 8192 x 1 (independent port A or port B)
- 4096 x 2 (independent port A or port B)
- 2048 x 4 (independent port A or port B)
- 1024 x 8, 1024 x 9 (independent A or B port implementation)
- 512 x 16,512 x 18 (A port B joint implementation)

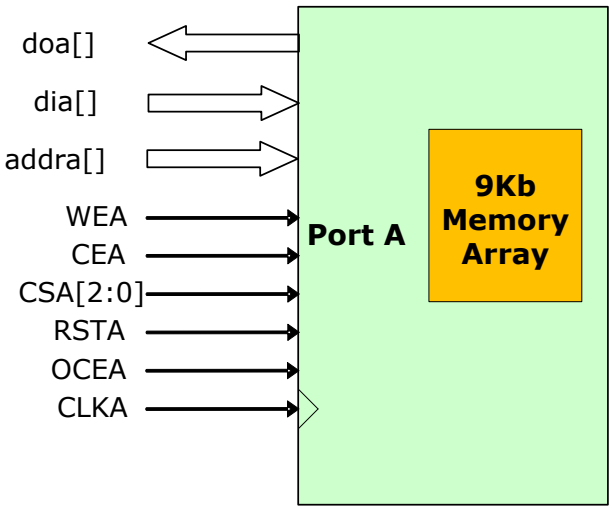


Figure 2-2-1 9-bit wide (and below) single-port RAM realized by port A

b) Simple Dual-Port Mode

When configured with a BRAM9K for 18-bit write or 18-bit readout, it does not support true dual-port mode and supports both single-port and simple dual-port modes. The configuration of the simple dual-port mode is as follows. In the 18-bit mode, the A port control signal is used as the write control signal and the B port control signal is used as the read control signal. In 18-bit write, DIB[8:0] is used as the upper 9-bit data input, DIA[8:0] is the lower 9-bit data input; when 18-bit read, DOB[8:0] is output as the upper 9-bit data. , DOA[8:0] is output as the lower 9 bits of data.

When the user uses 8/16 bit width, it is forbidden to use DIA[9], DIB[9], DOA[9], DOB[9] to prevent internal data mapping mismatch caused by different read/write bit widths.

Table 2-2-4 Data port connection relationship in 9/18-bit simple dual-port mode

Mode	BRAM9K RAM port	User port
W=18 digits R=18 digits	DIA[8:0]	wdata[8:0]
	DIB[8:0]	wdata[17:9]
	DOA[8:0]	Rdata[8:0]
	DOB[8:0]	Rdata[17:9]
W<=9 digits R=18 digits	DIA[]	Wdata[]
	DOA[8:0]	Rdata[8:0]
	DOB[8:0]	Rdata[17:9]
W=18 digits R<=9 digits	DIA[8:0]	wdata[8:0]
	DIB[8:0]	wdata[17:9]
	DOB[]	Rdata[]

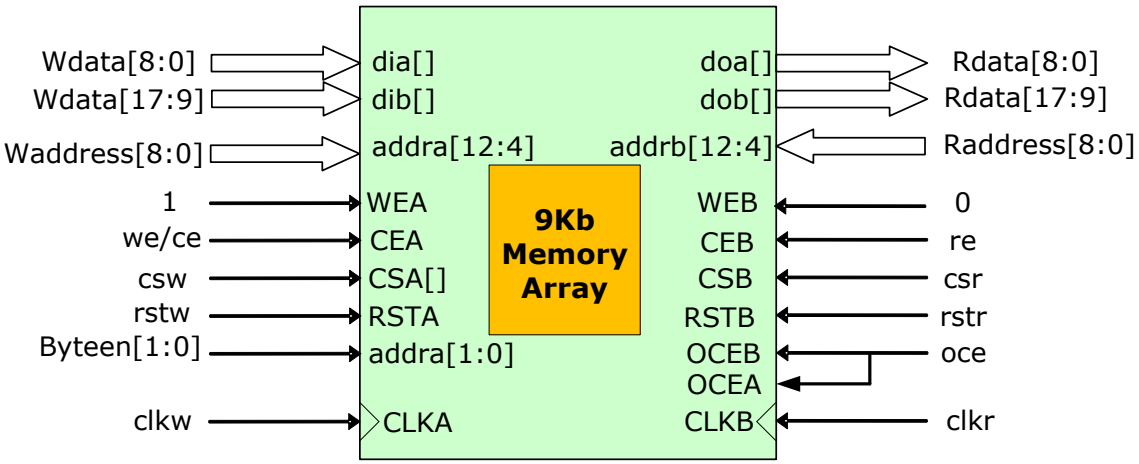


Figure 2-2-2 Simple Dual-Port 18-Bit Write/18-Bit Read Port Connection

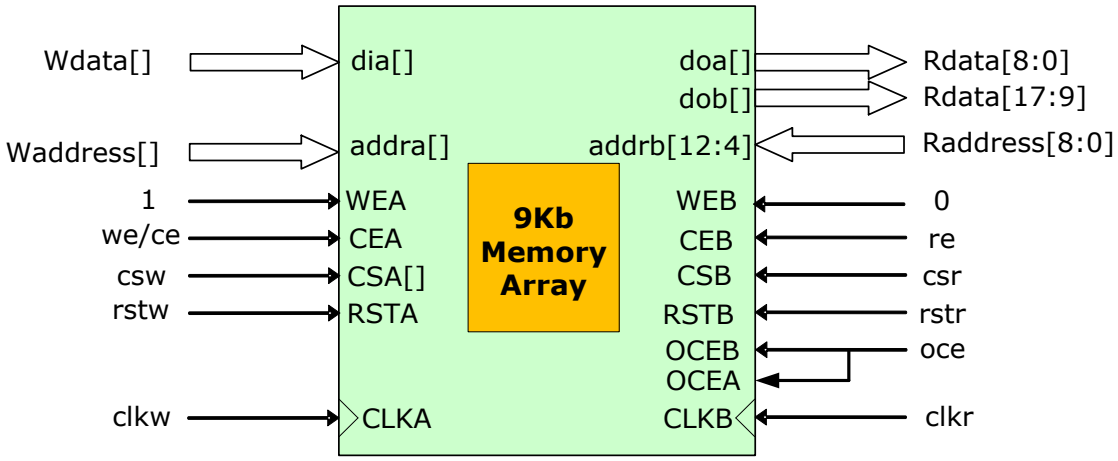


Figure 2-2-3 Simple Dual-Port Mode <=9 Bit Write/18 Bit Read Port Connection

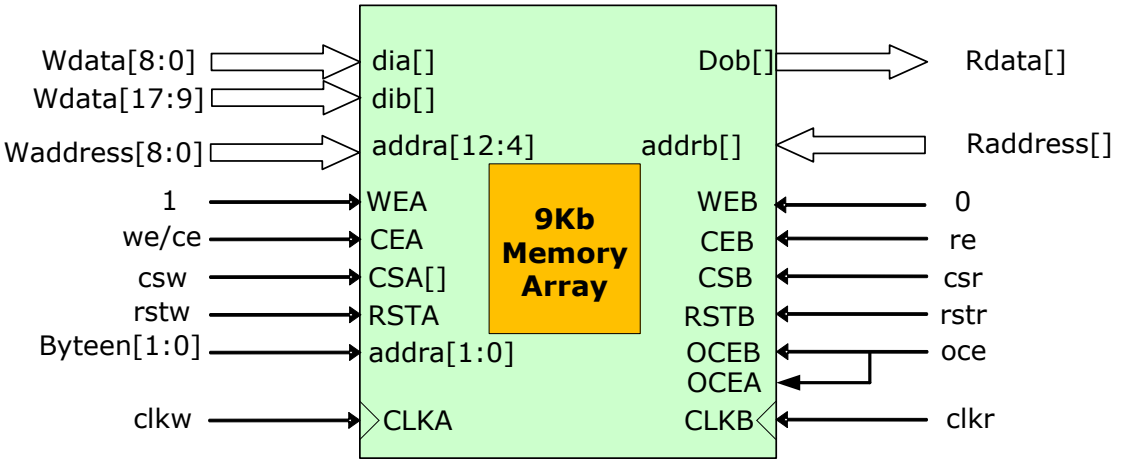


Figure 2-2-4 Simple Dual-Port Mode 18-Bit Write/<=9-Bit Read Port Connection

BRAM9K supports dual port/B port mixed port width selection in simple dual-port mode.

Table 2-2-5 Hybrid Port Width Configuration Supported in Simple Dual-Port Mode

Read Port	**Write Port**						
	8Kx1	4Kx2	2Kx4	1Kx8	512x16	1Kx9	512x18
8Kx1	√	√	√	√	√		
4Kx2	√	√	√	√	√		
2Kx4	√	√	√	√	√		
1Kx8	√	√	√	√	√		
512x16	√	√	√	√	√		
1Kx9						√	√
512x18						√	√

Table 2-2-6 WORD (16/18) and low-order address mapping when mixing width

	Port width	Address bit width	DOB[8]	DOA[8]	WORD internal data bit corresponding to the lowest 4-bit address addr[3:0] value													
	18	9	0		0													
	9	10	1	0	1								0					
	4	11	X	X	3				2				1				0	
	2	12	X	X	7		6		5		4		3		2		1	0
	1	13	X	X	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
18/16-bit WORD internal data bit			17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

c) True Dual-Port Mode

True dual-port mode supports all independent read and write operation combinations of port A/B: two reads, two writes, one read and one write.

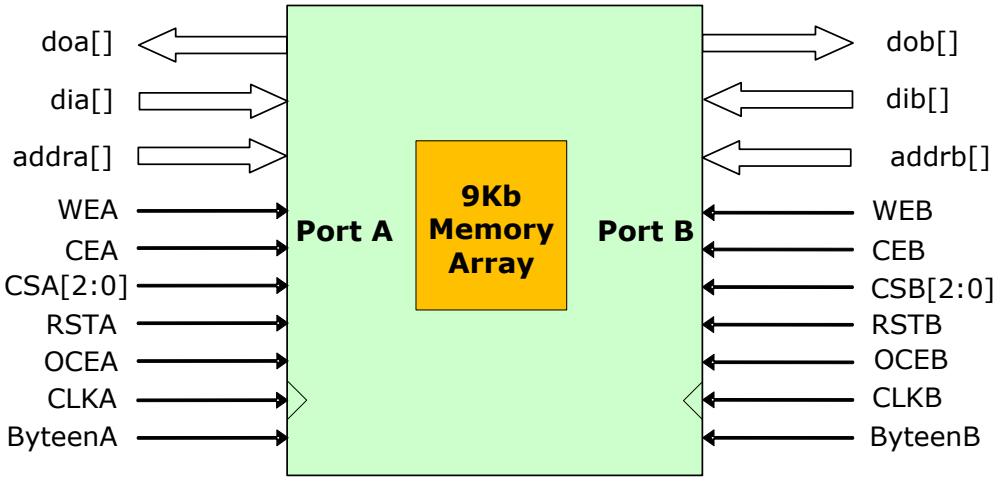


Figure 2-2-5 bit width <=9 bit A/B dual-port RAM

Table 2-2-7 shows the mixed port bit width configuration supported in true dual-port mode

Read Port	Write Port				
	8Kx1	4Kx2	2Kx4	1Kx8	1Kx9
8Kx1	√	√	√	√	
4Kx2	√	√	√	√	
2Kx4	√	√	√	√	
1Kx8	√	√	√	√	
1Kx9					√

d) ROM Mode

The BRAM9K supports ROM mode. The ROM contents are saved in the initialization file and written to BRAM9K during chip programming download. The initialization value can be set with the MIF file when the IP is generated. The ROM output can be selected with or without a register latch. The read operation of the ROM is the same as the read operation of the single-port RAM.

2.2.5 FIFO Mode

The BRAM9K has an integrated FIFO controller and hardware supports synchronous/asynchronous FIFO mode. The BRAM9K bit-width setting in FIFO mode is the same as the simple dual-port RAM setting, supporting up to 18-bit inputs and outputs.

Table 2-2-8 Port Signals in FIFO Mode

Input port name	Direction	Description
dia[8:0]	Input	FIFO data input, as low 9-bit data input in 16/18-bit input port mode
dib[8:0]	Input	It is used as a high 9-bit data input only in the 16/18-bit input port mode, and other bit widths are not used.
Clkw	Input	FIFO write port clock input, valid for the rising edge (reverse)
rst	Input	FIFO internal write pointer / read pointer reset signal (reverse)
we	Input	FIFO write enable, 1 for write operation, 0 no operation.
Csw[2:0]	Input	FIFO write port 3-bit chip select signal (reversible), similar to RAM mode.
Ocea	Input	The A port data register clock is enabled and the default is high active (reversible). Only valid when the output register is used (REGMODE_A="OUTREG").
Output port name	**Direction**	**Description**
doa[8:0]	Output	It is output as the lower 9-bit data only in the 18-bit output port mode, and is not used in other bit widths.
Dob[8:0]	Output	<= 9 bits are used as data output, and 18-bit output port mode is output as high 9-bit data.
Clkr	Input	Read port clock input, default rising edge is valid (reverse)
rprst	Input	FIFO read pointer reset signal
re	Input	FIFO read enable, 1 is read, 0 is no operation.
Csr[2:0]	Input	FIFO read port 3-bit chip select signal (reversible), similar to RAM mode.
Ocea	Input	The doa port data register clock is enabled and the default is high active (reversible). There is only an 18-bit output port mode and is valid when the output register is used (REGMODE_A="OUTREG").
Oceb	Input	The dob port data register clock is enabled and the default is high active (reversible). Only valid when the output register is used (REGMODE_B="OUTREG").

FIFO flag name	Direction	Description
empty_flag	Output	The FIFO read flag is synchronized with clkr.
Aempty_flag	Output	The FIFO reads the almost empty flag and is synchronized with clkr The relative readout advance is determined by the AE_POINT parameter.
Full_flag	Output	The FIFO is full and is synchronized with clkw. The FIFO full capacity is determined by the FULL_POINTER parameter.
Afull_flag	Output	The FIFO is almost full and is synchronized with clkw. The almost full capacity of the FIFO is determined by the AF_POINTER parameter.

Table 2-2-9 Mixed Port Bit Width Configuration Supported by FIFO Mode

Read Port	Write Port						
	8Kx1	4Kx2	2Kx4	1Kx8	512x16	1Kx9	512x18
8Kx1	√	√	√	√	√		
4Kx2	√	√	√	√	√		
2Kx4	√	√	√	√	√		
1Kx8	√	√	√	√	√		
512x16	√	√	√	√	√		
1Kx9						√	√
512x18						√	√

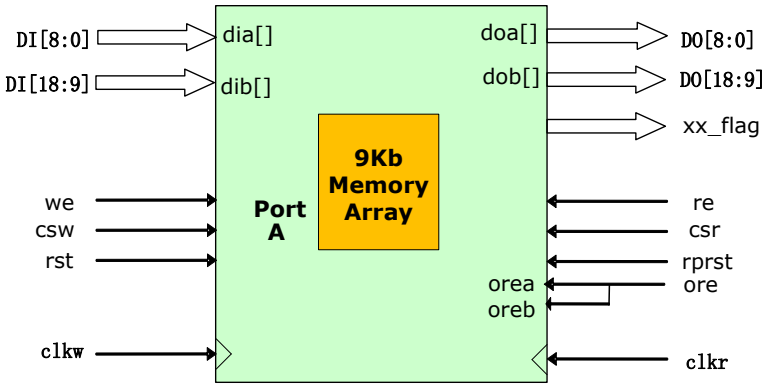


Figure 2-2-6 18-bit/18-bit out FIFO mode

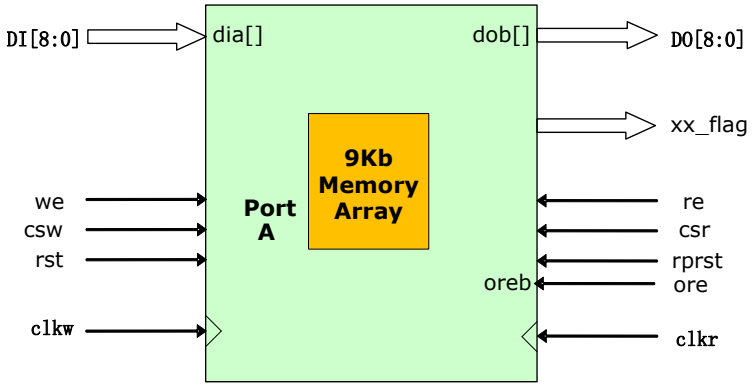


Figure 2-2-7 <=9 Bit In /<=9 Bit Out FIFO Mode

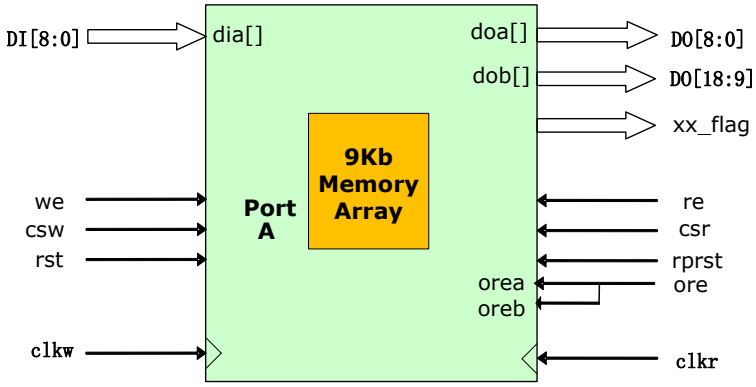


Figure 2-2-8 9-bit/18-bit out FIFO mode

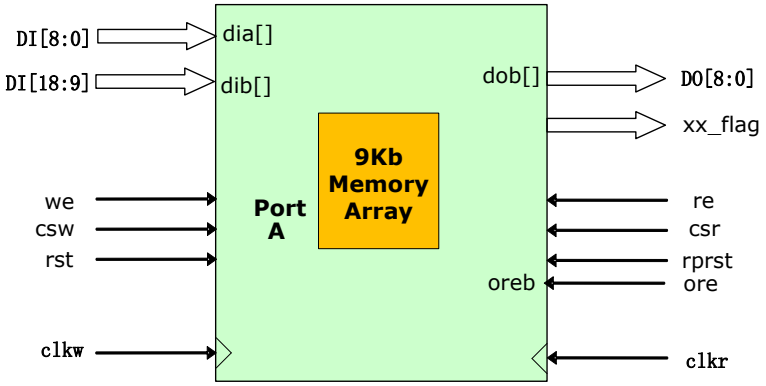


Figure 2-2-9 18-bit/9-bit out FIFO mode

■ Empty full flag attribute setting

In FIFO mode, the user can set the FIFO Empty Flag property via software. Empty flag (empty_flag), almost empty flag (almost_empty), full flag (full_flag), almost full flag (almost_full). When the internal counter counts to the flag value, it outputs a high level on the corresponding port of FF/AF/EF/AE.

Table 2-2-10 FF/AF/EF/AE Property Settings

FIFO attribute name	Description	Setting range
FF	Full flag	1 to Max
AF	Almost full	1 to Full-1
AE	Almost empty	1 to Full-1
EF	Empty setting	0

■ **Common configuration in FIFO mode**

The CSW/CSR in FIFO mode is similar to the CSA/CSB interface logic in RAM mode. To avoid pointer overflow when the FIFO is full or read, the full signal can be inverted by the interconnect resource and then connected to the csw terminal. After the full signal is inverted, it can be connected to the csr terminal. Reverse logic can be implemented using the inverse and logic inside csw/csr.

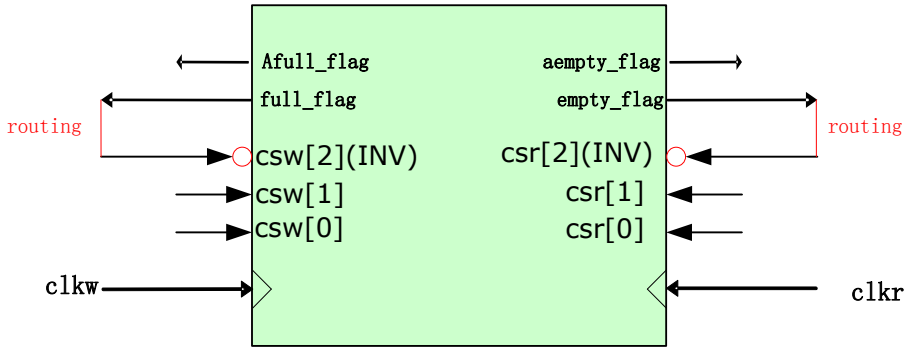


Figure 2-2-10 Single EMB9K FIFO Mode Connection

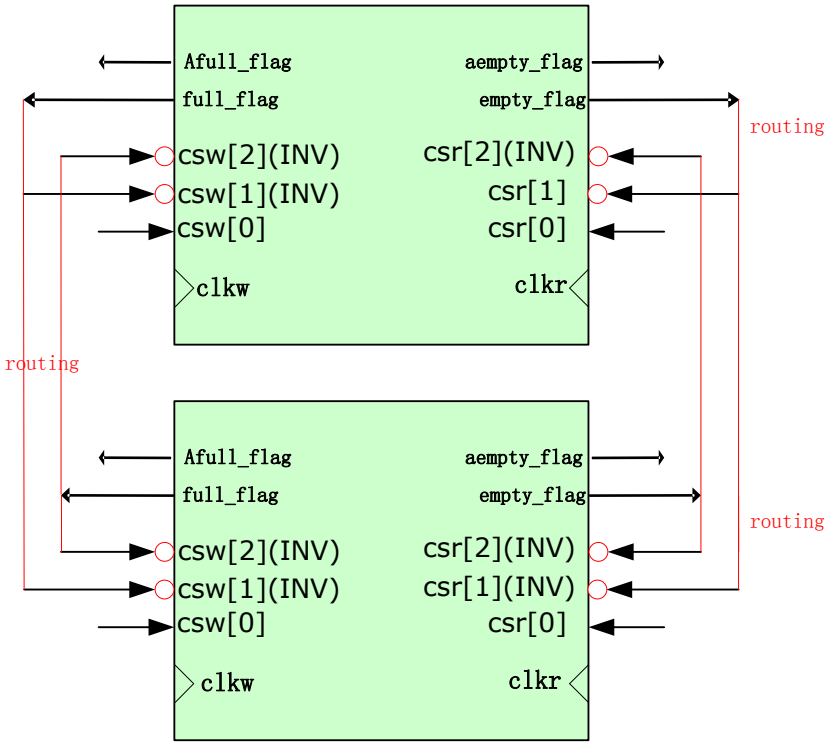


Figure 2-2-11 Two EMB9K FIFO cascade mode connections

2.2.6 BRAM32K

In order to achieve higher storage capacity, the EAGLE series devices are designed with an embedded true dual-port memory module BRAM32K with a memory capacity of 32K bits.

BRAM32K can achieve:

- Single port RAM
- Dual-port RAM

Features supported by the BRAM32K module are:

- 32K bits / per block, can be set to 2K*16 or 4K*8
- The A/B port clock is independent.
- A/B port data bit width can be configured separately, supporting 8 bits/16 bits width
- Output latch selectable (supports 1-stage pipeline)
- Support multiple write modes. You can choose to write only (Normal), write through (Write through) two modes

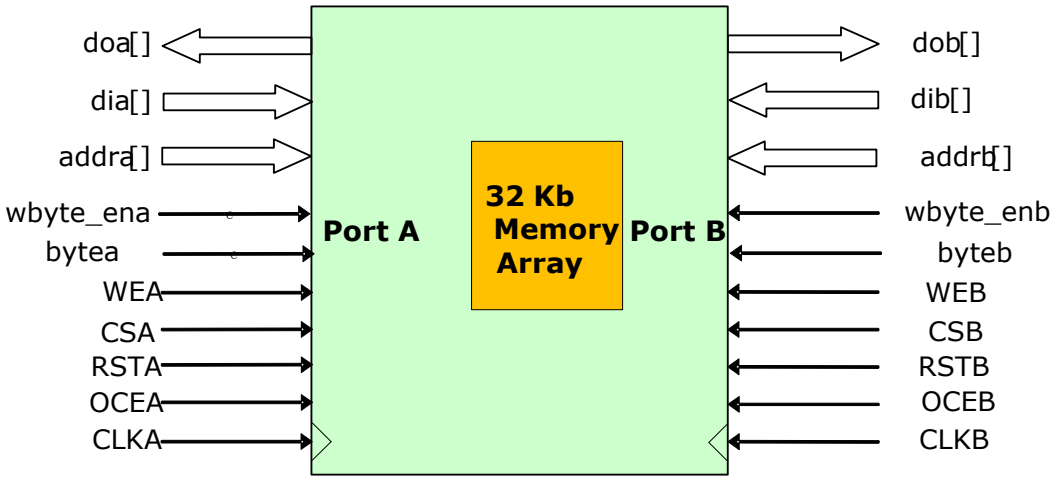


Figure 2-2-12 BRAM32K Dual-Port RAM

Table 2-2-11 BRAM32K Port Signal

A port name	Direction	Description
dia[15:0]	Input	A port data input, dia[7:0] is valid in 8-bit input port mode.
Addra[10:0]	Input	A port address input, 2K depth.
Wbyte_ena	Input	In port 16 mode, the 8-bit write mode is enabled and is active high. Connect to 0 in 8-bit mode.
Bytea	Input	In 8-bit mode, it is input as the least significant address; in 16-bit mode wbyte_ena=1, bytea=1 selects the upper 8 bits of writing, and the bytea=0 selects the lower 8 bits of writing.
doa[15:0]	Output	A port data output, only doa[7:0] is valid in 8-bit output port mode
clka	Input	A port clock input, valid for the rising edge (reverse)

rsta	Input	A port data output register synchronous reset signal, default high active (reversible)
csa	Input	A port chip selection, the default high effective (reversible).
Wea	Input	A port write/read operation control, 1 is a write operation and 0 is a read operation;
ocea	Input	The A port data register clock is enabled and the default is high active (reversible). Only valid when the output register is used (REGMODE_A="OUTREG").
B port name	**Direction**	**Description**
dib[15:0]	Input	B port data input, 8-bit input port mode dib[7:0] is valid
addrb[10:0]	Input	B port address input, 2K depth
wbyte_enb	Input	In port 16 mode, the 8-bit write mode is enabled and is active high. Connect to 0 in 8-bit mode.
Byteb	Input	In 8-bit mode, it is input as the least significant address; in 16-bit mode wbyte_enb=1, byteb=1 selects high 8-bit write, and byteb=0 selects lower 8-bit write.
dob[15:0]	Output	B port data output, 8-bit output port mode when dob[7:0] is valid
clkb	Input	B port clock input, the default rising edge is active (reversible).
Rstb	Input	B port data output register synchronous reset signal, default high active (reversible)
csb	Input	B port clock valid control signal, default low active (reversible).
Web	Input	B port write/read operation control, 0 is the write operation and 1 is the read operation.
Oceb	Input	The B port data register clock is enabled and the default is high active (reversible). Only valid when the output register is used (REGMODE_B="OUTREG").

2.3 Clock resource

The EAGLE family of FPGAs contains three clock resources, the first being the global clock (GCLK) for core logic, embedded memory, IOLs, and DSPs, and the second is the input and output clocks that support high-speed input/output interface strings and conversions (IOCLK), the third is a fast clock that supports clock fast input to IOCLK and PLL input.

2.3.1 Global clock

The EAGLE family of global clock resources includes dedicated clock inputs, buffers, and routing networks. The clock resource provides 16 low-latency, low-skew, interconnected global clock networks. The global clock network provides a uniform, high-performance, low-jitter, low-skew clock source for each FPGA block. At the same time, the global clock can also be used for high fanout signals.

There are two levels of multiplexers on the global clock transmission path, the first stage is 8:1, which is used to select one of the PLL output, clock pin, internal frequency divider, and internal logic feedback as the global clock driver; The output of the 8:1 multiplexer is inserted with the first-level dynamic clock enable logic, which enables dynamic operation of the glitch-free clock. A total of 32 clock resources are sent from the four sides, and the delay is on the transmission path. The time balance is sent to the second stage 36:1 multiplexer in the middle of the chip, and then sent to the four quadrant drive user logic DFF.

The entire chip has four quadrants in the horizontal and vertical middle lines, and each quadrant has 16 independent global clock resources.

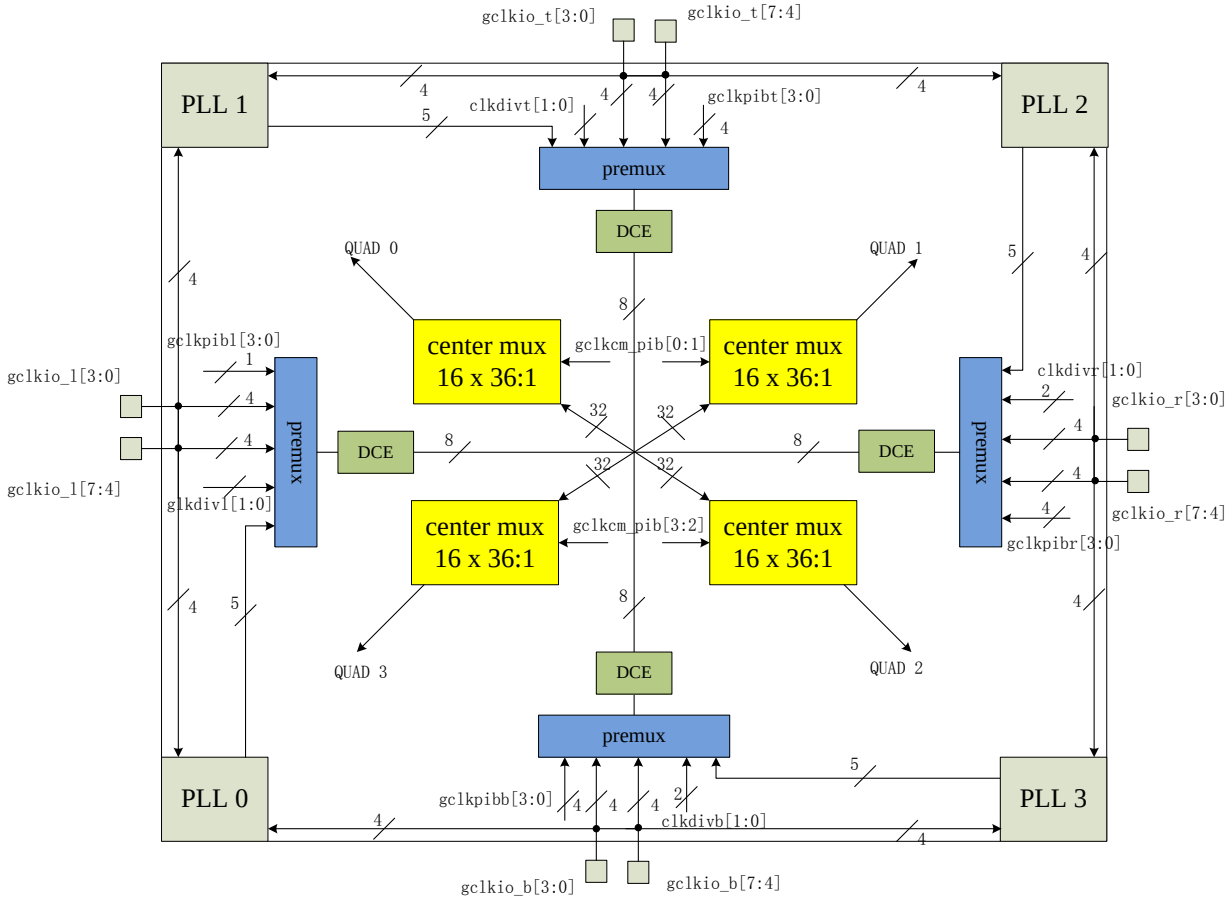


Figure 2-3-1 Global Clock Distribution Network

Note: EAGLE_4 only has PLL0

EAGLE_10 only PLL0 and PLL2

2.3.1.1 Dynamic clock enable (DCE)

The Dynamic Clock Enable (DCE) module allows the user to dynamically control the clock network through a logical description. When the selected clock is disabled, all logic modules driven by that clock will be at a standstill, reducing power consumption.

2.3.1.2 Clock switching module (CSB)

Each EAGLE device has 2 global clock dynamic clock switching modules. The clock switching module takes the output of all 32 global clock first stage multiplexers as inputs. The dynamic clock switch is designed to be configured as a synchronous or asynchronous glitchless 2:1 multiplexer with two clock inputs.

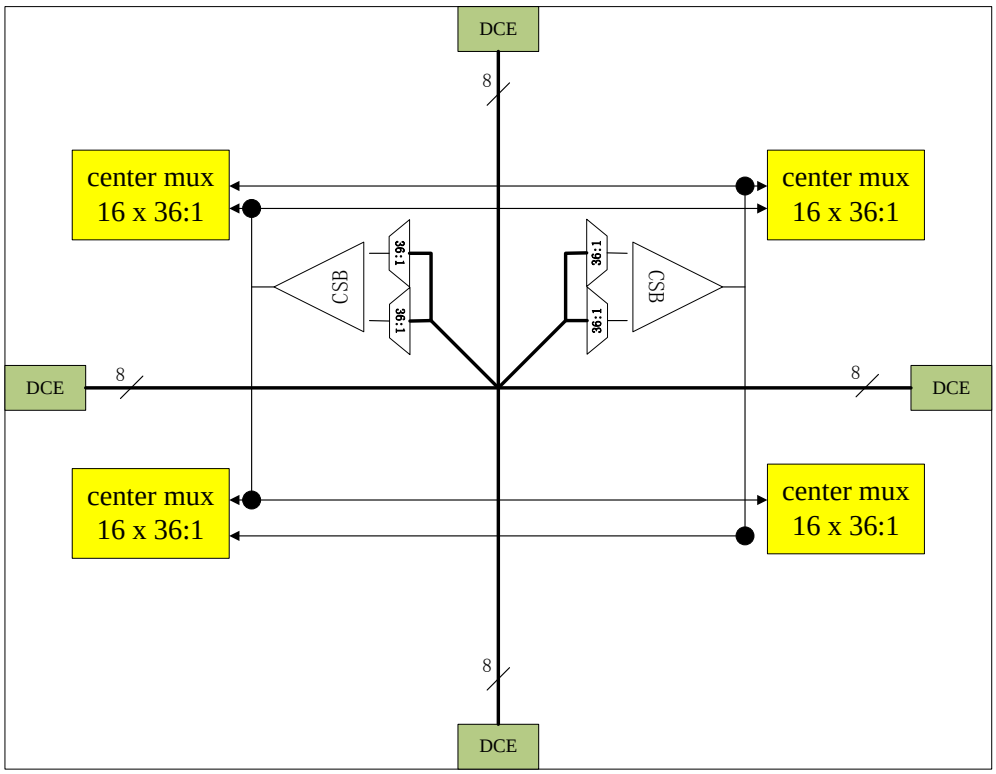


Figure 2-3-2 CSB block diagram

Figure 2-3- 3 shows the timing diagram of the CSB module operation.

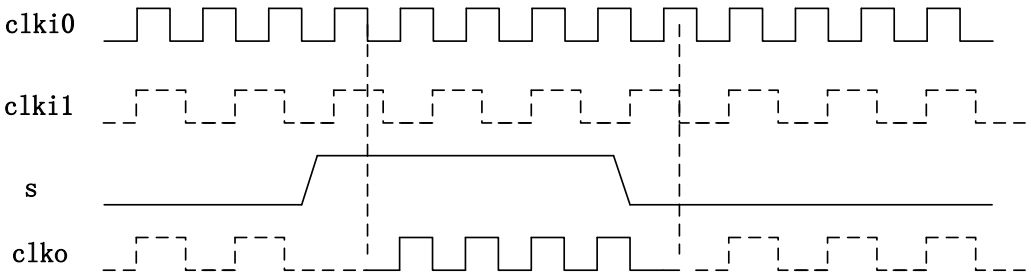


Figure 2-3-3 CSB Timing Chart

Table 2-3-1 DCS Operation Mode Table

Mode	S		Description
	1	0	
CSB	clki0	clki1	Falling edge trigger, latched state is low
CSB_1	clki0	clki1	Trigger on rising edge, latched state is high
BUFGCE	0	clki1	Enable high efficiency, low enable status output low
BUFGCE_1	0	clki1	Enable high efficiency, non-enabled state output high
BUFGCEB	clki0	0	Enable low active, non-enabled state output low
BUFGCEB_1	clki0	0	Enable low active, non-enabled state output high
BUFG0	clki0	clki0	Clock buffer
BUFG1	clki1	clki1	Clock buffer
BUFGMUX	clki0	clki1	Glitch clock switch

2.3.2 Input and output clock

The input and output clock (IOCLK) is a type of clock buffer used in EAGLE devices. IOCLK drives a dedicated clock network independent of global clock resources within the I/O column. In this way, BUFIO is ideally suited for source-synchronous data acquisition (transmit/receiver clock distribution). IOCLK can be driven by clock capable I/O in the same clock region or by PLL output. There are two IOCLKs in a typical I/O group. Each IOCLK drives an I/O clock network in the same zone/group. IOCLK cannot drive logic resources (PLB, BRAM, etc.) because the IOCLK clock network can only cover I/O columns in the same group or clock region.

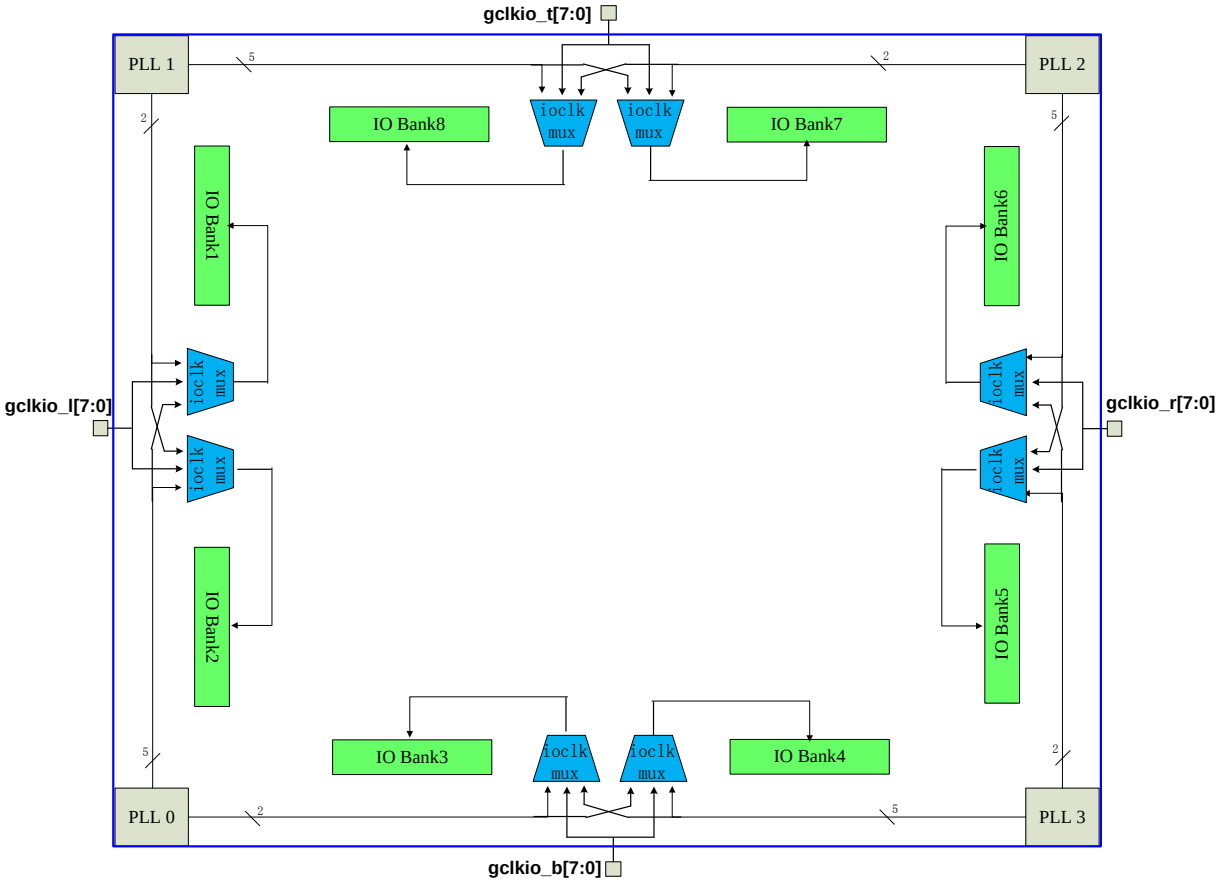


Figure 2-3-4 IOCLK architecture diagram

Note: EAGLEA05/10K only has PLL0 and PLL2

■ Clock divider

The EAGLE device has two clock dividers in each I/O group. The clock divider divides the input clock and its input is derived from the input and output clocks of the same I/O group. The output division factor can be either 1/2/4.

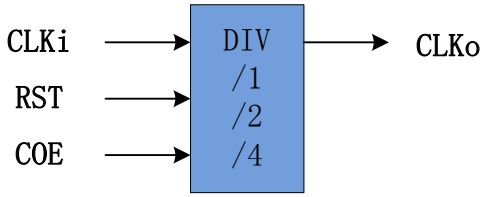


Figure 2-3-5 Clock Divider

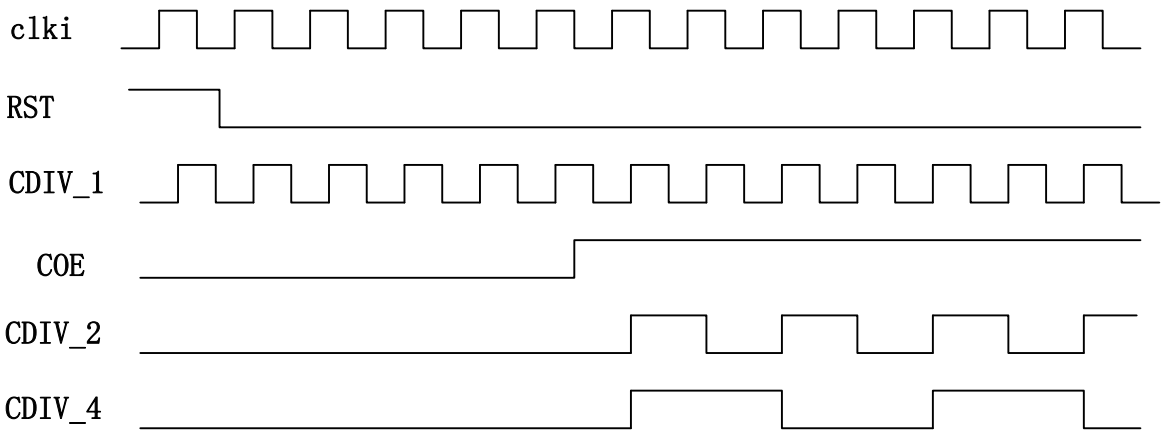


Figure 2-3-6 Clock Divider Timing

2.3.3 Fast clock

The fast clock is used to implement a single clock input for fast routing to multiple IOCLK and PLL inputs, which allows customers to be more flexible when implementing clock sharing input applications.

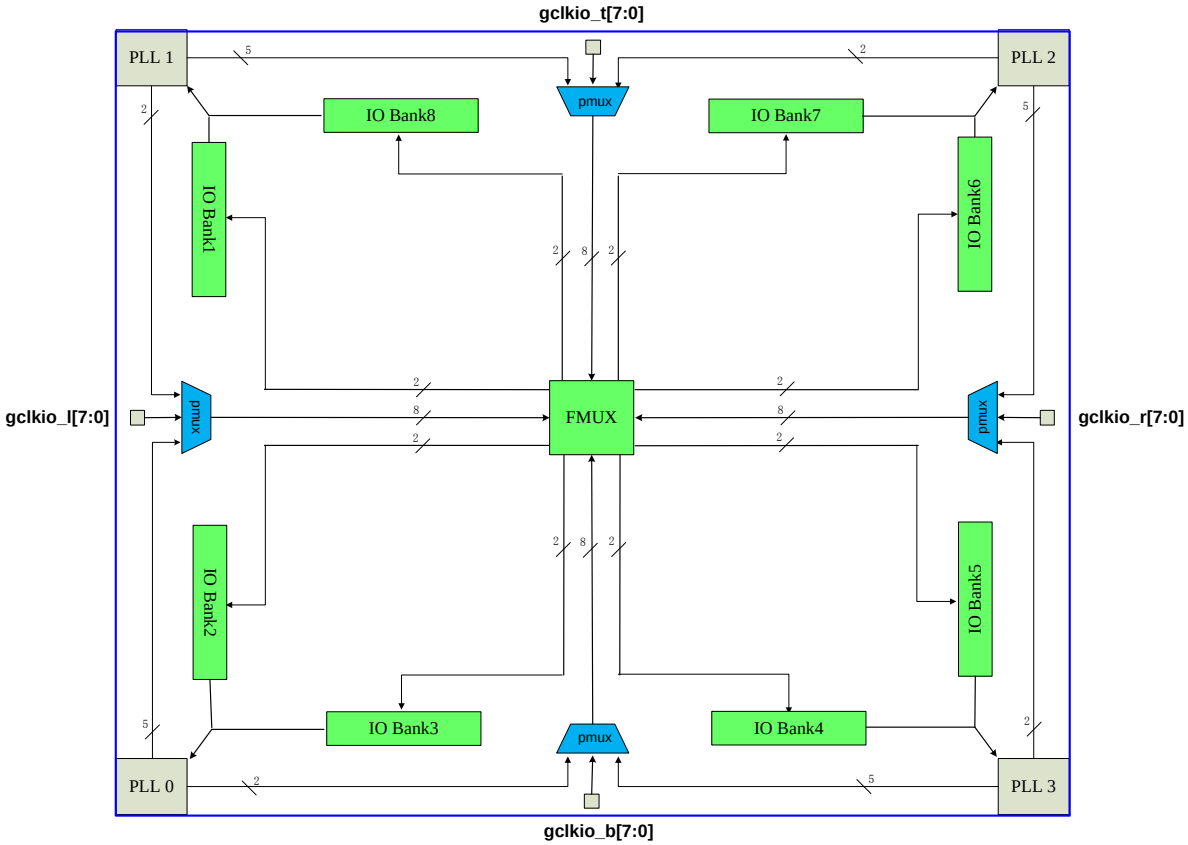


Figure 2-3-7 Fast Clock Architecture

2.4 Phase-locked loop (PLL)

2.4.1 Introduction

EAGLE series FPGAs have up to four multi-function phase-locked loops (PLL0~PLL3) for high-performance clock management. Each PLL implements clock division/multiplier/input and feedback clock alignment/multiphase clock output.

The user should pay attention to whether the PLL lock signal is high during use. It is recommended that the user wait for the input signal to stabilize before resetting the phase-locked loop to ensure the frequency and phase of the phase-locked loop output clock signal.

The PLL reference clock inputs are: clock network output, interconnect output, and internal oscillator output.

The PLL feedback clock inputs are: clock network output, internal register clock node, interconnect output, PLL internal feedback clock, and phase shift clock C0~C4.

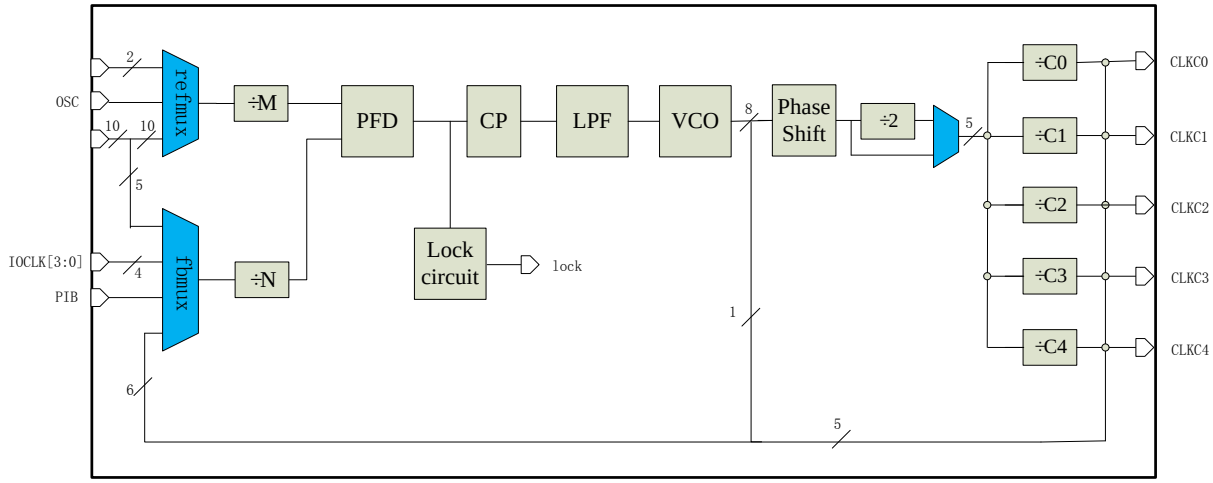


Figure 2-4-1 EAGLE PLL architecture diagram

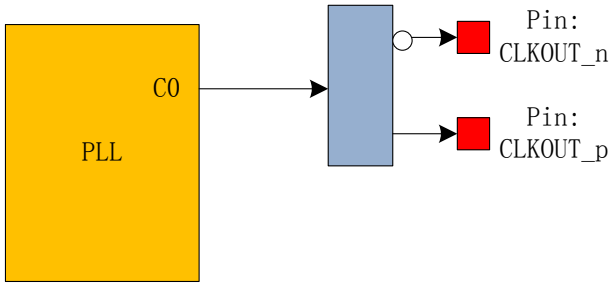


Figure 2-4-2 EAGLE C0 Direct Output to Clock Output IO Pin (Differential Mode)

Table 2-4-1 EAGLE PLL Characteristics Table

Feature	AL3 PLL
Input clock frequency range	10-400 Mhz
Output clock frequency range	4-400 Mhz
VCO frequency range	300-1200 Mhz
Number of output ports	5 (each port is independently independent)
Reference clock division factor (M)	1 to 128
Feedback clock division factor (N)	1 to 128
Output clock division factor (C0-4)	1 to 128
Phase shift resolution	45 (relative to VCO)
Output port selectable phase offset(°)	0，45，90，135，180，225，270，315
User dynamic phase shift control	Support (+/- 45 degree phase shift per unit, relative VCO)
Locked state output	Lock
Dedicated clock output pin	Support

2.4.2 Dynamic phase shift

The EAGLE Series PLL supports dynamic phase shifting. The EAGLE series of PLL control properties are divided into static and dynamic configurations. The static configuration is generated by the user through software settings, and cannot be changed after power-on download.

Static configuration parameters include:

- Reference/Feedback Clock Input/Output Selection
- Reference clock division factor (M)
- Feedback clock division factor (N)
- Output clock division factor (C0-4)

Dynamic phase shifting means that the user can change the phase output of the PLL's five clock outputs C0-C4 by sending a signal to the PLL control input interface. EAGLE dynamic phase shift control adjusts the phase by adding/decreasing. The progress is extended to 45 degrees of the output clock divided by the output division number. The user selects a phase shift of an output through the PSCLKSEL[2:0] signal. Each pulse of PSSTEP is incremented or decremented by one phase, and a low to high transition of PSDONE indicates that a phase shift is completed.

The dynamic phase shift can be used in all four feedback modes. It is worth noting that the PSCLK must be at least one-third smaller than the VCO, and the width of the PSSTEP requires at least two PSCLK cycles.

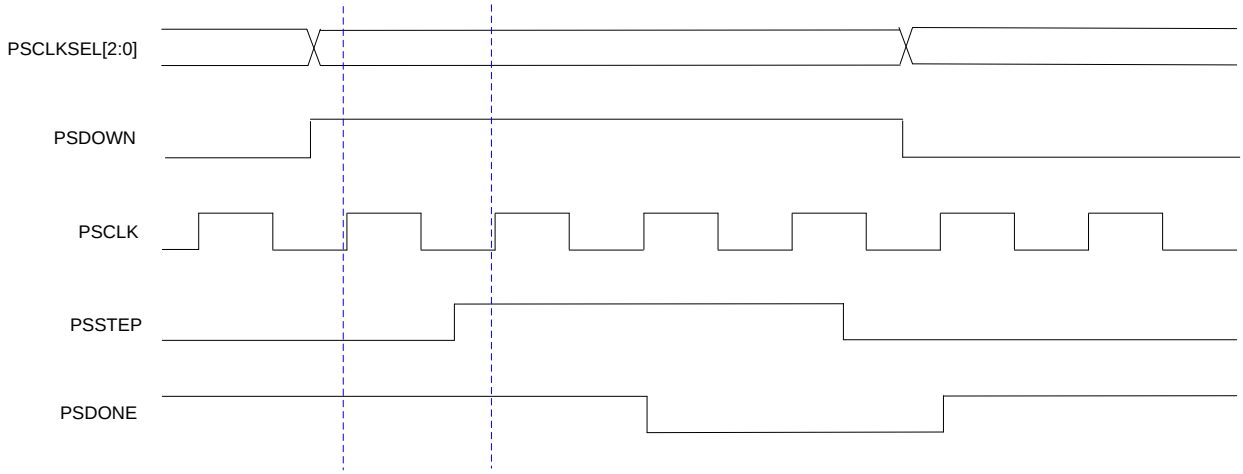


Figure 2-4-3 PLL Dynamic Phase Shift Control Timing

2.4.3 Dynamic configuration

Dynamic configuration allows the user to directly control the configuration parameters of the phase-locked loop through a dedicated I/O interface during PLL operation, including:

- Reference clock division factor (M)
- Feedback clock division factor (N)
- Output clock division factor (C0-4)
- Output phase P

Each parameter of the PLL is stored in 32*8 of RAM space. The dynamic configuration function is implemented by an 8-bit dynamic interface similar to MEMORY access in EG_PHY_PLL.

User dynamic configuration port list:

Table 2-4-2 User Dynamic Configuration Port

EG_PHY_PLLIF port	Direction	Description
DCLK	Input	Clock input, valid rising edge
DCS	Input	Chip select input, high active, clk rising edge latch
DADDR<5:0>	Input	Read and write address, latched edge of clk is latched
DWE	Input	Write enable, high active, clk rising edge latch
DWDATA<7:0>	Input	data input
DRDATA<7:0>	Output	Data no delay output, PLL configuration data read port

PLL internal 32BYTE control bit list:

Table 2-4-3 PLL Internal 32BYTE Control Table

Address	Bit<7:0>	Description
5'h01	0, Refclk_div<6:0>	Bit<7>=0, bit<6:0> is the reference clock division factor
5'h02	0, fdbkclk_div<6:0>	Bit<7>=0, bit<6:0> is the feedback clock division factor
5'h03	0, channel0_del<6:0>	Bit<7>=0, bit<6:0> is the channel 0 delay coefficient
5'h04	0, channel0_div<6:0>	Bit<7>=0, bit<6:0> is the channel 0 division factor
5'h05	0, channel1_del<6:0>	Bit<7>=0, bit<6:0> is channel 1 delay coefficient
5'h06	0, channel1_div<6:0>	Bit<7>=0, bit<6:0> is the channel 1 division factor
5'h07	0, channel2_del<6:0>	Bit<7>=0, bit<6:0> is channel 2 delay coefficient
5'h08	0, channel2_div<6:0>	Bit<7>=0, bit<6:0> is the channel 2 division factor
5'h09	0, channel3_del<6:0>	Bit<7>=0, bit<6:0> is channel 3 delay coefficient
5'h0A	0, channel3_div<6:0>	Bit<7>=0, bit<6:0> is the channel 3 division factor
5'h0B	0, channel4_del<6:0>	Bit<7>=0, bit<6:0> is channel 4 delay coefficient
5'h0C	0, channel4_div<6:0>	Bit<7>=0, bit<6:0> is the channel 4 division factor
5'h0D	Reserved	
5'h12	C2<1:0>,C1<2:0>,C0<2:0>	Bit<2:0> is channel 0 phase, Bit<5:3> is channel 1 phase, Bit<7:6> is channel 2 phase bit1,0
5'h13	0,C4<2:0>,C3<2:0>,C2<2>	Bit<0> is channel 2 phase bit2, Bit<3:1> is channel 3 phase, Bit<6:4> is channel 4 phase, Bit<7>=0

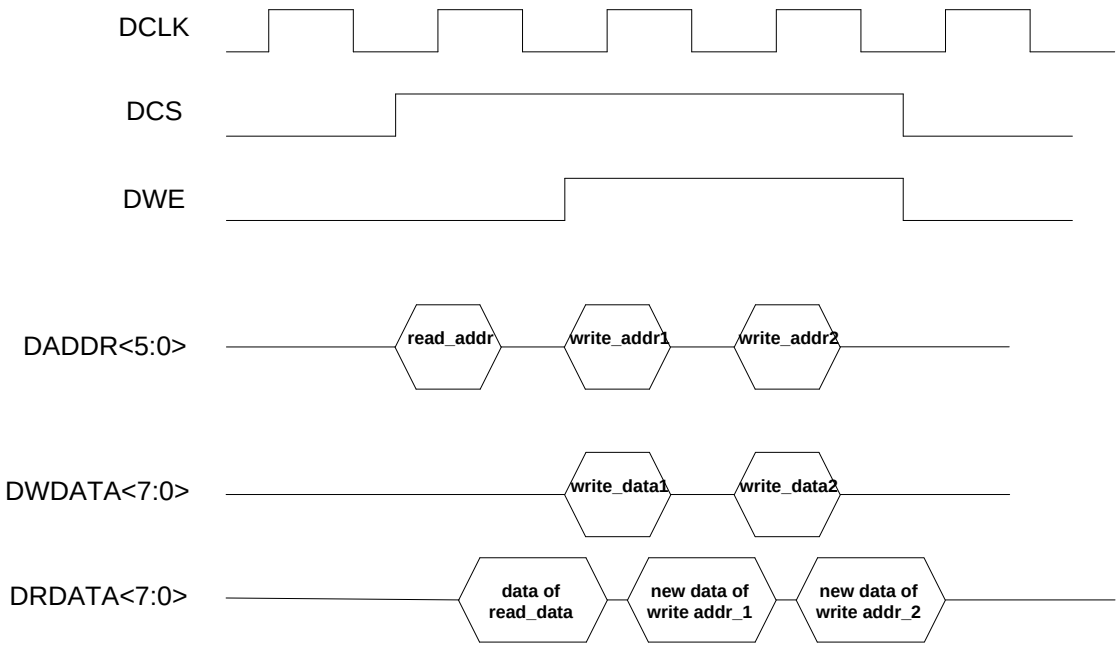


Figure 2-4-4 PLL Dynamic Configuration Control Timing

2.4.4 Clock feedback mode

The EAGLE Series PLL supports four feedback modes. Each mode supports clock division/multiplication and phase shift.

a) Source-Synchronous Mode

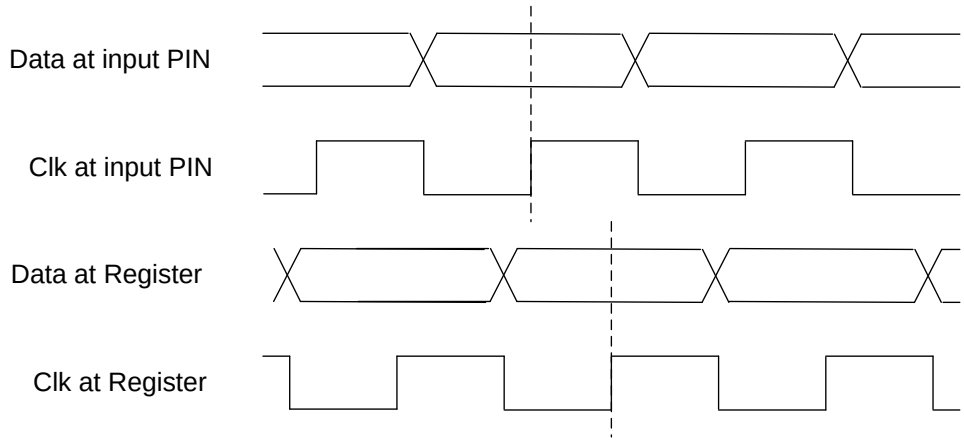


Figure 2-4-5 Source Synchronization Mode

Figure 2-4- 5 Source-Synchronous Mode The dynamic phase shift function adjusts the clock phase to ensure that the delay from the data port to the IOB input register is equal to the delay from the clock input port to the IOB register (in the same data and clock input port mode).

b) No Compensation Mode

In uncompensated mode, the PLL does not compensate for clock network delay, and the PLL uses internal self-feedback, which improves the jitter characteristics of the PLL.

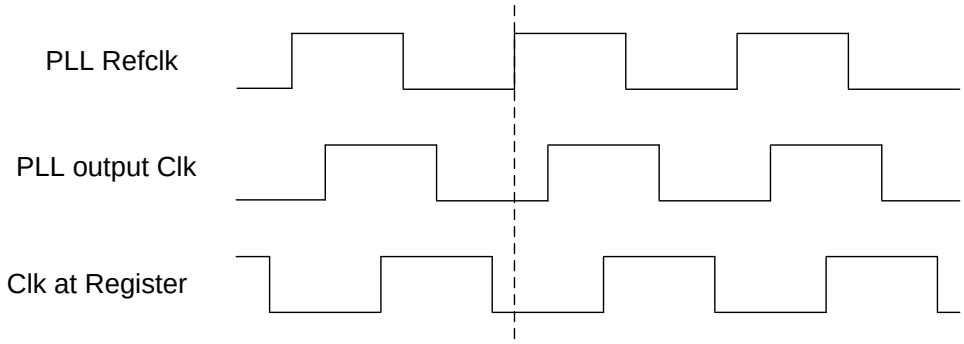


Figure 2-4-6 No compensation mode (phase misalignment)

c) Normal mode

In normal mode, the PLL compensates for the GCLK network delay, ensuring that the internal register input clock phase and clock pin phase are the same.

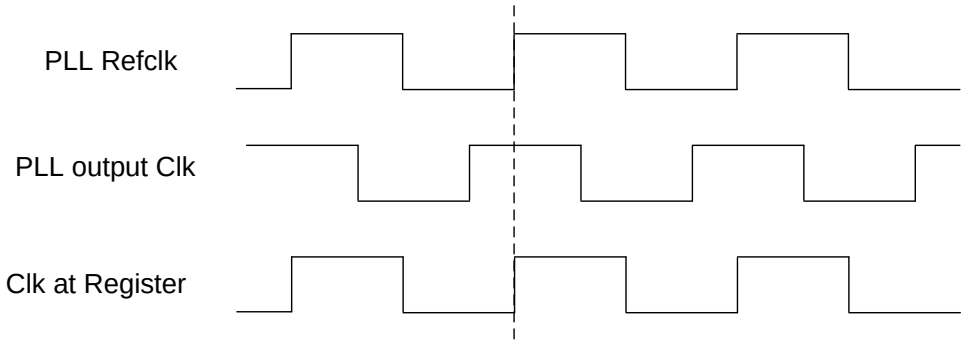


Figure 2-4-7 Normal mode (1/2 clock phase alignment)

d) Zero delay buffer mode

Zero delay buffer mode, clock output pin phase and PLL reference clock input pin phase alignment.

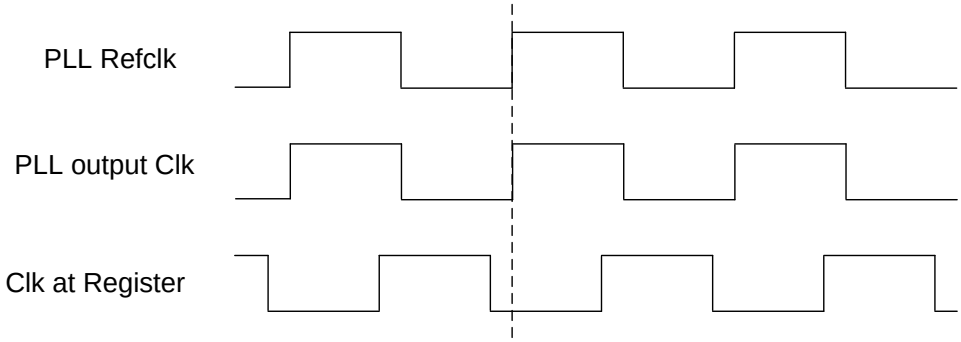


Figure 2-4-8 Zero Delay Buffer Mode (1/3 signal phase alignment)

2.5 Digital signal processing (DSP)

EAGLE devices combine on-chip resources with external interfaces to help improve performance, reduce system cost, and reduce power consumption in digital signal processing (DSP) systems. The EAGLE device itself or as a coprocessor for DSP devices can be used to increase the price/performance ratio of DSP systems.

2.5.1 Architecture

Figure 2-5-1 shows the height correspondence of an embedded multiplier column and adjacent logic array modules. The embedded multiplier can be configured as an 18 × 18 multiplier or as two 9 × 9 multipliers. Each embedded multiplier consists of the following units:

- Multiplier level
- Input and output registers
- Input and output interface

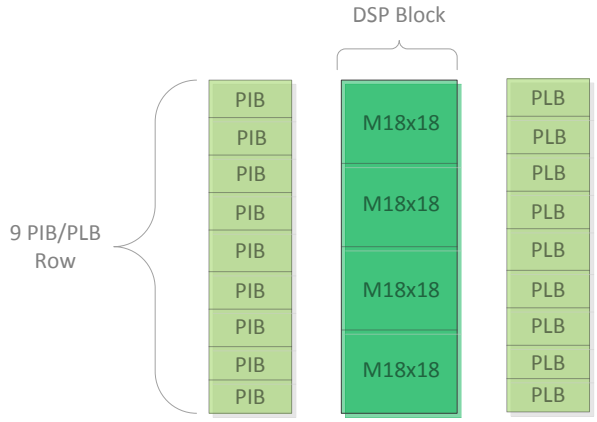


Figure 2-5-1 Embedded multiplier arranged in columns adjacent to PLB

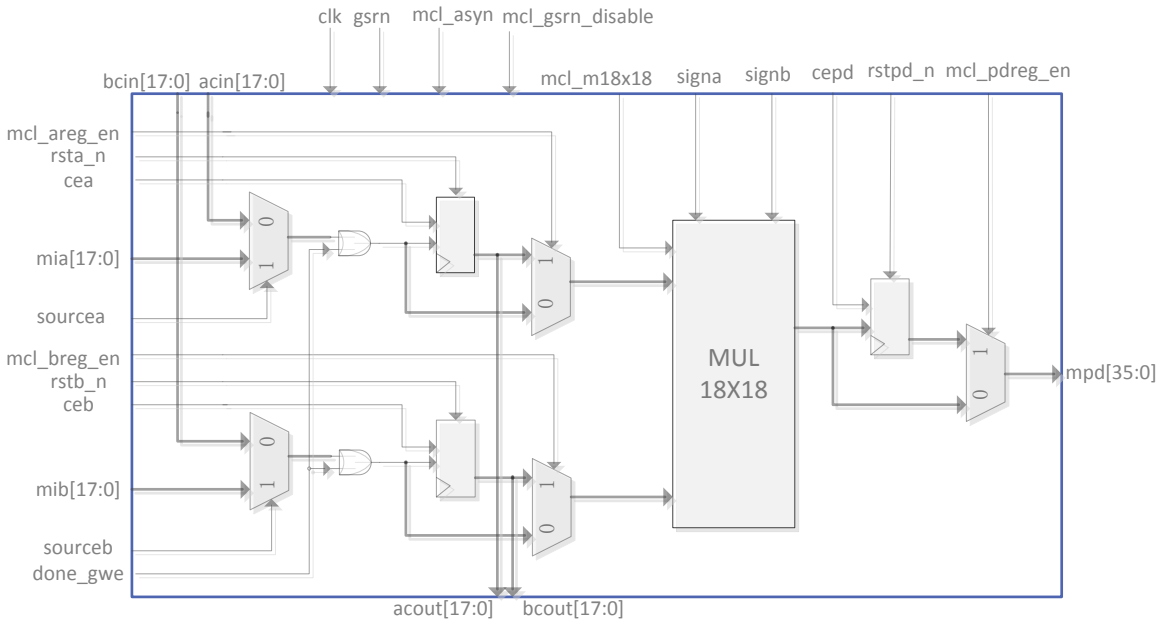


Figure 2-5-2 Architecture of the Multiplier Module

a) Input register

Depending on the mode of operation of the multiplier, each multiplier input signal can be connected to the input register or directly to the internal multiplier in 9bit or 18 bit form. You can set whether each input of the multiplier uses an input register separately. For example, connect the multiplier mia signal to the input register and the mib signal directly to the internal multiplier.

The following control signals are available for each input register in the embedded multiplier:

- Clock
- Clock enable
- Synchronous/asynchronous clear

All input and output registers in the same embedded multiplier are driven by the same clock signal, and the clock enable signal and the asynchronous clear signal driver can be independently configured.

b) Multiplier level

The multiplier stage of the embedded multiplier module supports 9x9 or 18x18 multipliers and supports other multipliers between these configurations. A single embedded multiplier can perform one or two multiplication operations simultaneously, depending on the data width or mode of operation of the multiplier.

Each operand of a multiplier is a unique signed or unsigned number. The Signa and signb signals control the input of the multiplier and determine whether the value is signed or unsigned. If the signa signal is high, the mia operand is a signed value. Conversely, the mia operand is an unsigned value.

Table 2-5- 1 shows the symbol types corresponding to the product of the operands of different symbol types. If any of the operands is a signed number, the result of the product is a signed number.

Table 2-5-1 Multiplier symbol representation

mia		mib		Product
Signa	Logical value	Signb	Logical value	
Unsigned	0	Unsigned	0	Unsigned
Unsigned	0	Signed	1	Signed
Signed	1	Unsigned	0	Signed
Signed	1	Signed	1	Signed

Each embedded multiplier module has only one signa signal and one signb signal that is used to control the symbolic representation of the module's input data. If the embedded multiplier has two 9 x9 multipliers, the mia input and the mib input of the two multipliers will share the same signa signal and the same signb signal, respectively. The signa and signb signals can be dynamically changed at runtime to modify the symbolic representation of the input operand. Signa and signb can be sent via a dedicated input register. The multiplier supports full precision regardless of the symbol representation.

c) Output register

Depending on the mode of operation of the multiplier, the output of the embedded multiplier can be registered using an output register in either 18 bit or 36 bit form. The following control signals are available for each of the output registers in the embedded multiplier:

- Clock
- Clock enable
- Synchronous/asynchronous clear

All input and output registers in the same embedded multiplier are driven by the same clock signal, and the clock enable signal and the asynchronous clear signal driver can be independently configured.

The port descriptions for DSP are shown in the following table:

Table 2-5-2 Multiplier Port Description Table

Name	Direction	Bit width	Description
mia	Input	18	Dsp operand input from PID. Has a register input mode.
Acin	Input	18	Cascading data input from the acout port of the previous stage dsp. Has a register input mode.
Acout	Output	18	Connect to the cascading data output on the acin port of the next level dsp.
Mib	Input	18	Another operand input from the dsp of the PIB. Has a register input mode.
Bcin	Input	18	Cascading data input from bcout of the previous level dsp. Has a register input mode.
Bcout	Output	18	Connect to the cascading data output on the bcin port of the next level dsp.
Cea	Input	1	The clock enable signal for the input register. When cea is high, the output of amux is passed to the register.
Ceb	Input	1	The clock enable signal for the input register. When ceb is high, the output of bmux is passed to the register.
Cepd	Input	1	The clock enable signal of the output register. When cepd is high, the data output of dsp is transferred to the register.
Clk	Input	1	Clk is the input clock to dsp and acts on all internal registers.
Rsta_n	Input	1	Input register reset signal. When the rsta_n input is low, the output of the register is "0".
Rstb_n	Input	1	Input register reset signal. When the rstb_n input is low, the output of the register is "0".
Rstpd_n	Input	1	The reset signal of the output register. When the rstpd_n input is low, the output of the register is "0".
Sourcea	Input	1	The control end of the first level data selector. When sourcea is high, the output of MUX is a. When sourcea is low, the output of MUX is acin.
Sourceb	Input	1	The control end of the first level data selector. When sourceb is high, the output of MUX is b. When sourceb is low, the output of MUX is bcin.
Mpd	Output	36	The product data output of dsp.

2.5.2 Operating mode

According to different application needs, you can choose one of the following two multiplier working modes:

- An 18 × 18 multiplier
- Up to two 9 × 9 independent multipliers

The multiplier adder and the multiply accumulator function can be implemented by using the embedded multiplier of the EAGLE device. The multiplier part of the function is implemented by the embedded multiplier, and the adder or accumulator function is implemented in the logic unit.

a) 18-bit multiplier

A single 18x18 multiplier supporting 10 to 18 bit input bit widths by configuring each embedded multiplier. Figure 2-5-3 shows the configured embedded multiplier to support an 18-bit multiplier.

All 18-bit multiplier input data and results are sent independently to the registers. The multiplier input data can be a signed integer, an unsigned integer, or a combination of both. Alternatively, the signa and signb signals can be dynamically modified and sent via a dedicated input register.

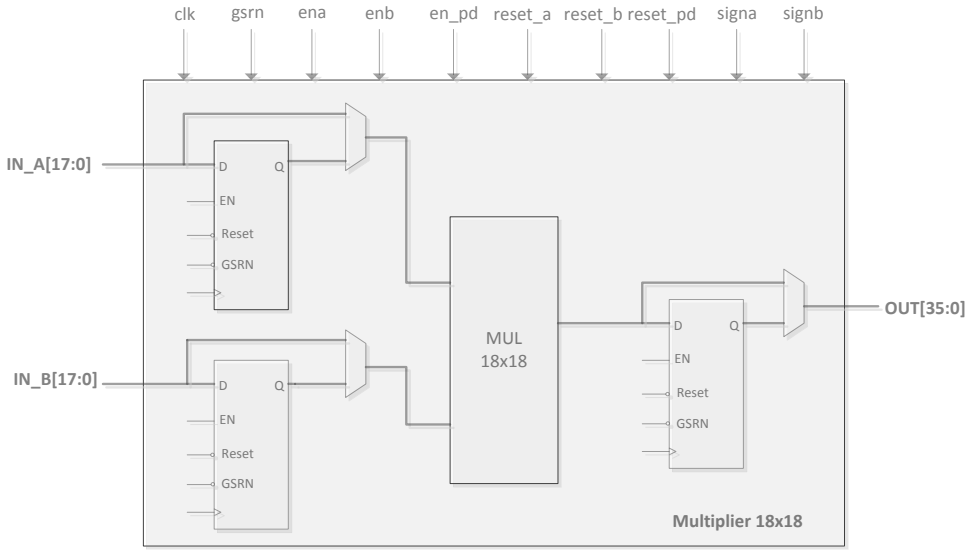


Figure 2-5-3 18-bit multiplier mode

b) 9-bit multiplier

Each of the embedded multipliers is configured to support two 9x9 multipliers with a maximum of 9 bits of input width. Figure 2-5–4 shows the configured embedded multiplier to support two 9-bit multipliers.

All 9-bit multiplier input data and results are sent independently to the registers. The multiplier input data can be a signed integer, an unsigned integer, or a combination of both. Two 9 × 9 multipliers in the same embedded multiplier block share the same signa and signb signals. Therefore, all mia input data used to drive the same embedded multiplier must have the same symbolic representation. Similarly, all mib input data used to drive the same embedded multiplier must also have the same symbolic representation.

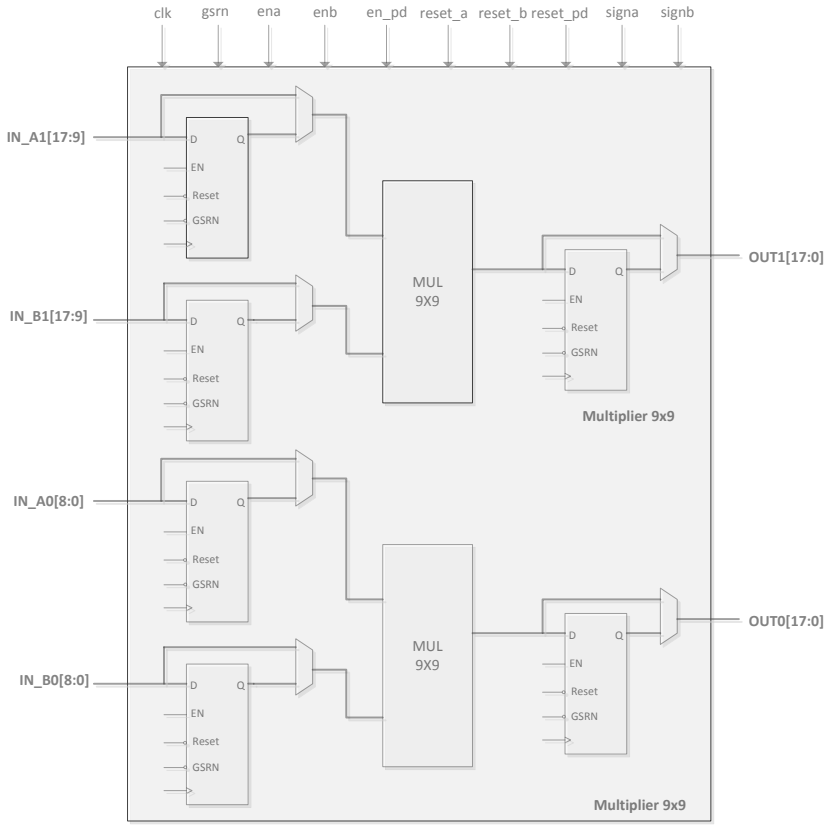


Figure 2-5-4 9-bit multiplier mode

2.6 Input and output logic (IOL)

The IOL logic of the EAGLE device supports multiple operating modes. This chapter focuses on how to configure IOL resources to support multiple modes of operation.

2.6.1 Input register

The input registers in the Input Output Logic (IOL) are used to process the high speed interface and reduce it to the frequency that the internal core logic can handle. The input registers contain configurable delay units as data sampling processing aids. Support for general dual edge data (GDDR) is enhanced based on this basic functionality.

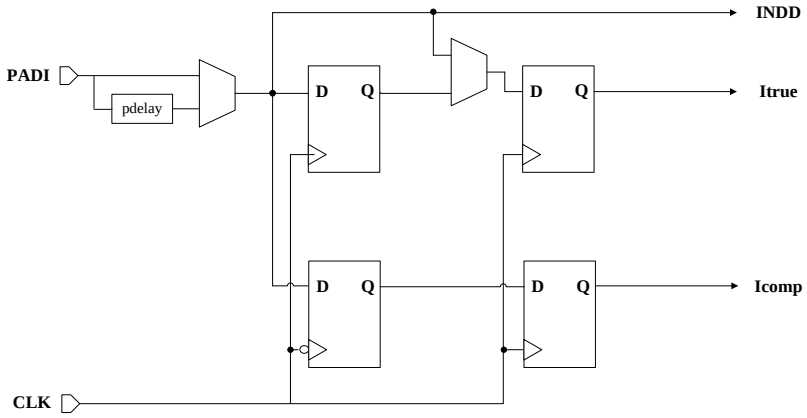


Figure 2-6-1 Input Register Block Diagram

a) Normal input mode

The IO logic in normal mode is shown in Figure 2-6-2. In this mode, the signal goes directly to the FPGA internal logic.

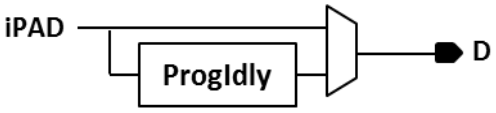


Figure 2-6-2 Common input mode block diagram

b) SDR input mode

Compared to the normal mode, as shown in Figure 2-6-3, the SDR mode uses the IOL register, which can effectively improve the timing performance of IO.

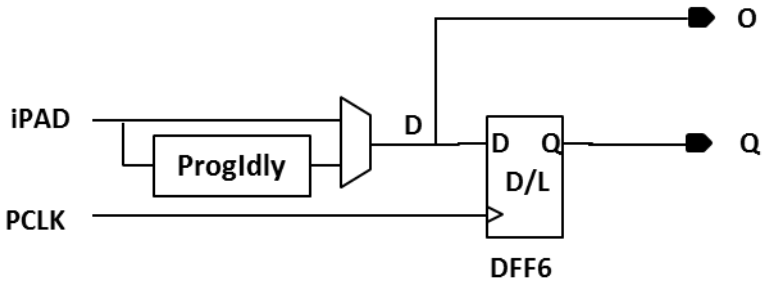


Figure 2-6-3 SDR Input Mode Block Diagram

c) DDR input mode

EAGLE devices have dedicated registers in the IOL to support the iDDRx1 and iDDRx2 modes.

■ **iDDRx1 same edge input mode**

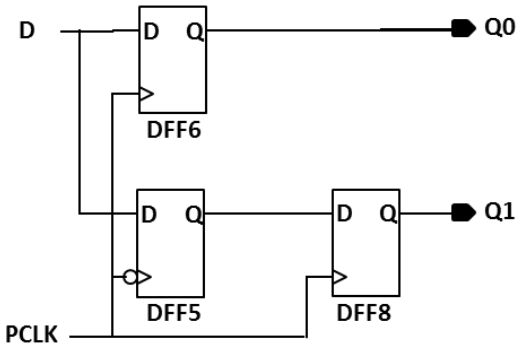


Figure 2-6-4 Igddr Same Edge Input Mode Block Diagram

In iDDRx1 in-edge mode, DFF5 and DFF6 sample the input data on the falling and rising edges, respectively, and DFF8 synchronizes the Q1 data to the rising edge of the clock. Due to the introduction of DFF8, Q1 data is one clock later than Q0, and the timing is shown in Figure 2-6-5.

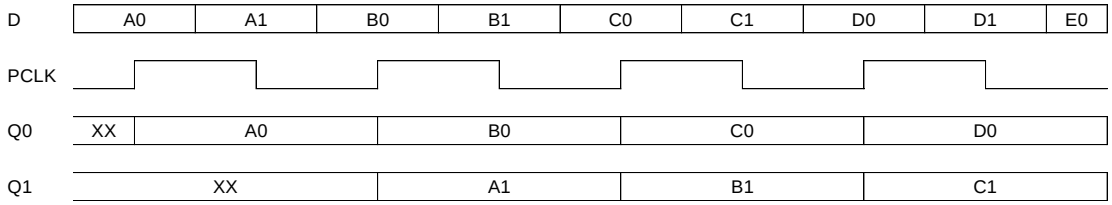


Figure 2-6-5 Igddr Same Edge Input Mode

■ **iDDRx1 along with Pipelined input mode**

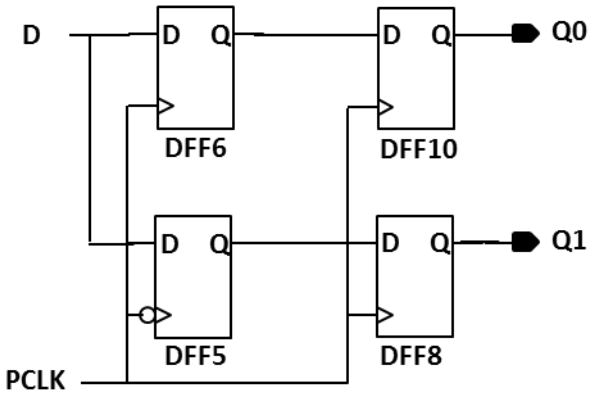


Figure 2-6-6 Igddr Same Edge Pipelined Input Mode Block Diagram

In the iDDRx1 edge mode, Q1 is one clock later than Q0. To compensate for this delay, DFF10 is introduced, as shown in Figure 2-6-6. The timing is shown in Figure 2-6-7.

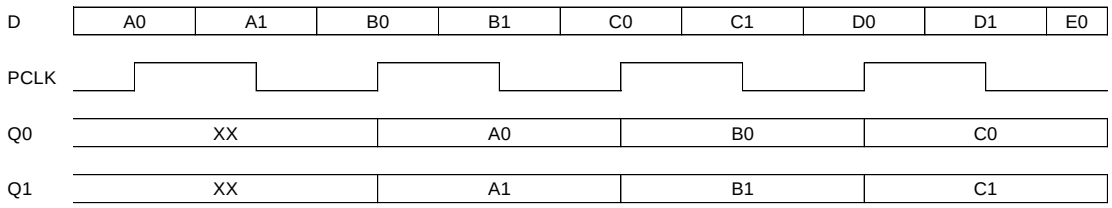


Figure 2-6-7 Igddr Same Edge Pipelined Input Mode

■ **iDDRx2 input mode**

In iDDRx2 mode, higher IO speeds can be supported. The ratio of PAD to FPGA internal logic is 4:1. In this mode, the first-stage sampling DFF is triggered by SCLK, which enables high-speed data sampling and 1:2 separation. The second stage of separation, DFF, is triggered by the FPGA system clock, PCLK, to achieve the same frequency as the core logic. PCLK is half the speed of SCLK.

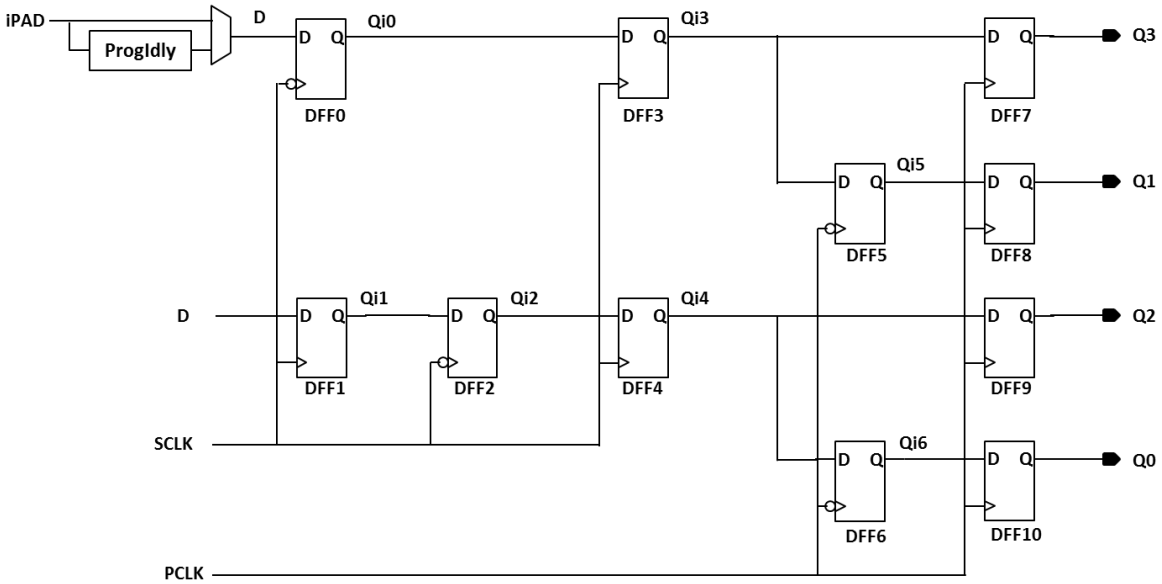


Figure 2-6-8 iDDRx2 Input Mode

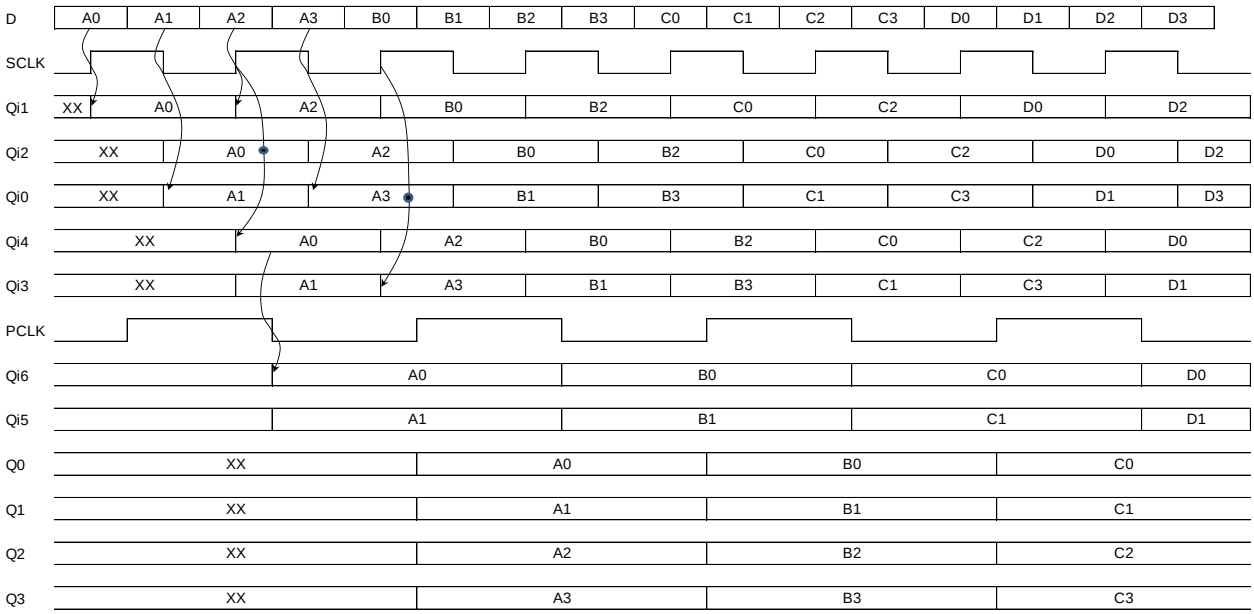


Figure 2-6-9 iDDRx2 Input Mode Timing

d) Input delay unit

Each IOL logic unit contains a programmable input delay unit that supports 32 levels of regulation with a maximum delay of 3.8ns. Support for static control of latency.

2.6.2 Output register

The output registers in the input and output logic (IOL) are used to handle the timing of the internal core logic to the high speed I/O interface. Figure 2-6-10 shows the output register block diagram.

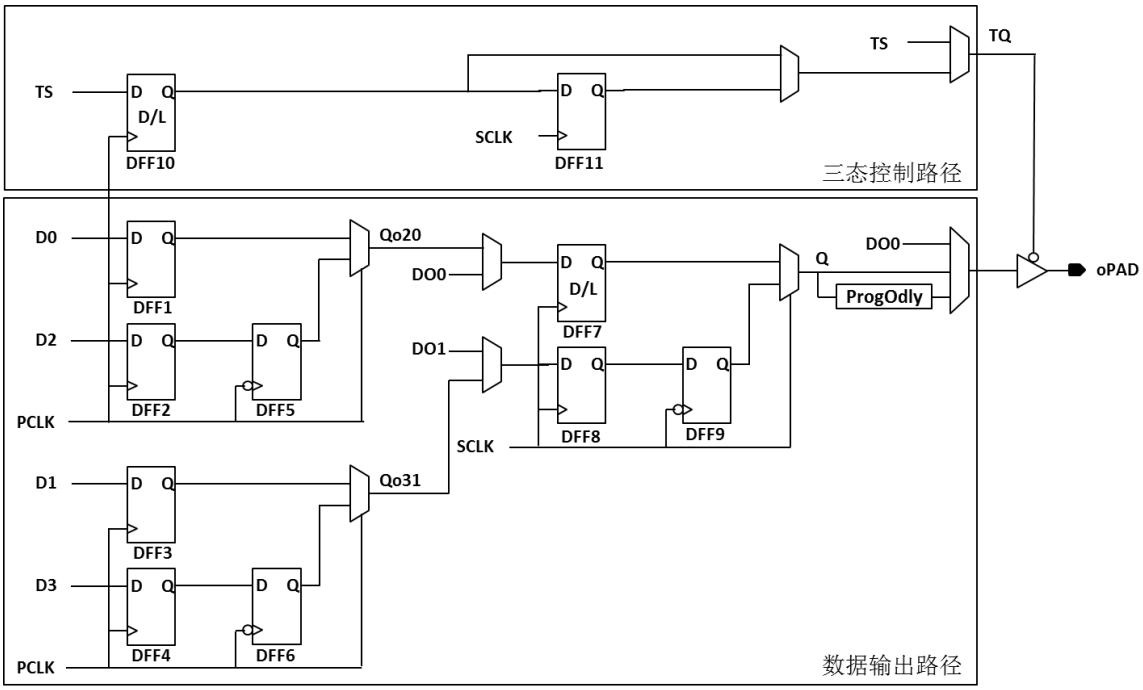


Figure 2-6-10 Output Register Block Diagram

a) Normal output mode

The IO logic in normal output mode is shown in Figure 2-6-11. In this mode, the signal is output directly from the FGPA internal logic to the PAD.

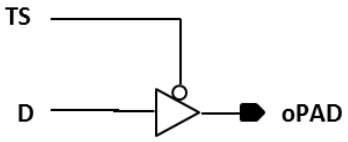


Figure 2-6-11 Common output mode block diagram

b) SDR output mode

Compared to the normal mode, as shown in Figure 2-6-12, the SDR mode uses the IOL register to effectively improve the timing performance of the IO.

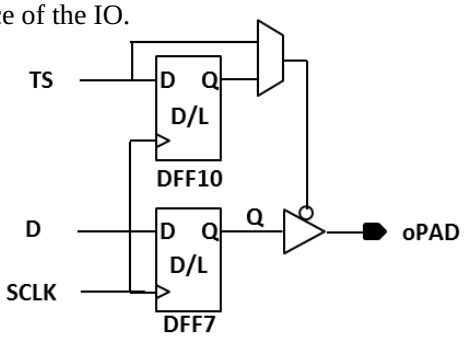


Figure 2-6-12 SDR output mode block diagram

c) DDR output mode

EAGLE devices have dedicated registers in the IOL to support oDDRx1 and oDDRx2 modes.

■ **oDDRx1 output mode**

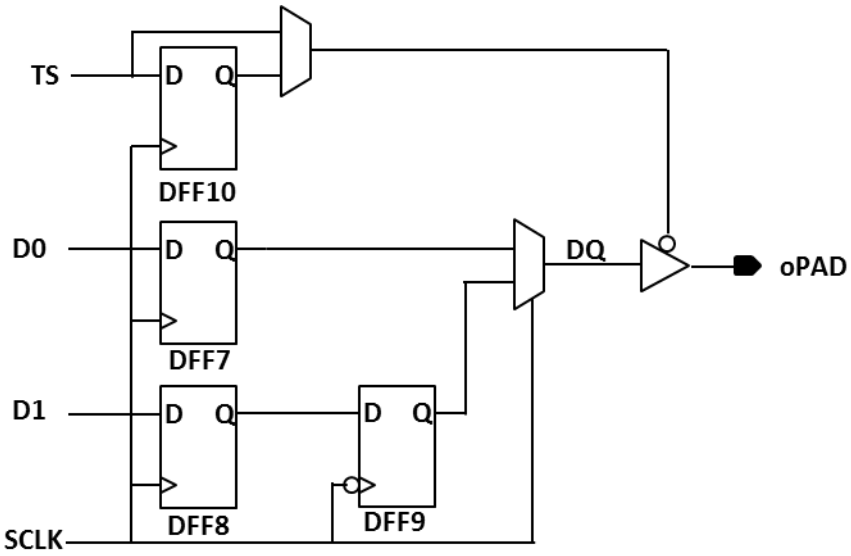


Figure 2-6-13 oDDRx1 output mode block diagram

In oDDRx1 mode, data DO0 and DO1 are sampled into the DFF7 and DFF8 by the same edge of SCLK and output to the Opad on the rising and falling edges, respectively, as shown in Figure 2-6-14.

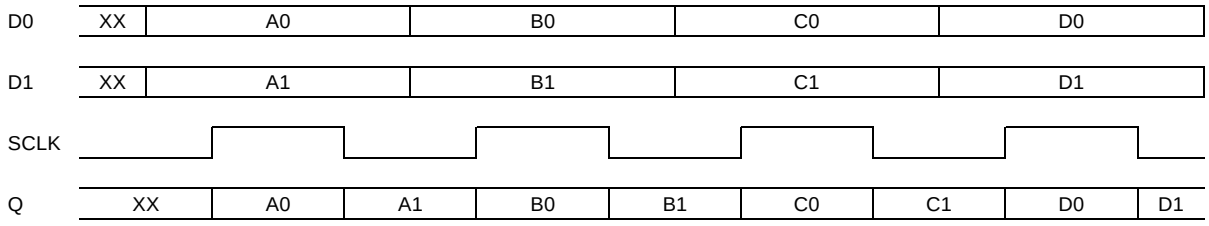


Figure 2-6-14 Ogddr output mode

■ **oDDRx2 output mode**

In DDRx2 mode, higher IO speeds can be supported. The ratio of PAD to FPGA internal logic is 4:1. In this mode, the first part of the DFF is triggered by the FPGA system clock PCLK, which enables data sampling and 2:1 parallel-to-serial conversion. The second part, DFF, is triggered by high-speed SCLK for high-speed serial output of data. PCLK is half the speed of SCLK.

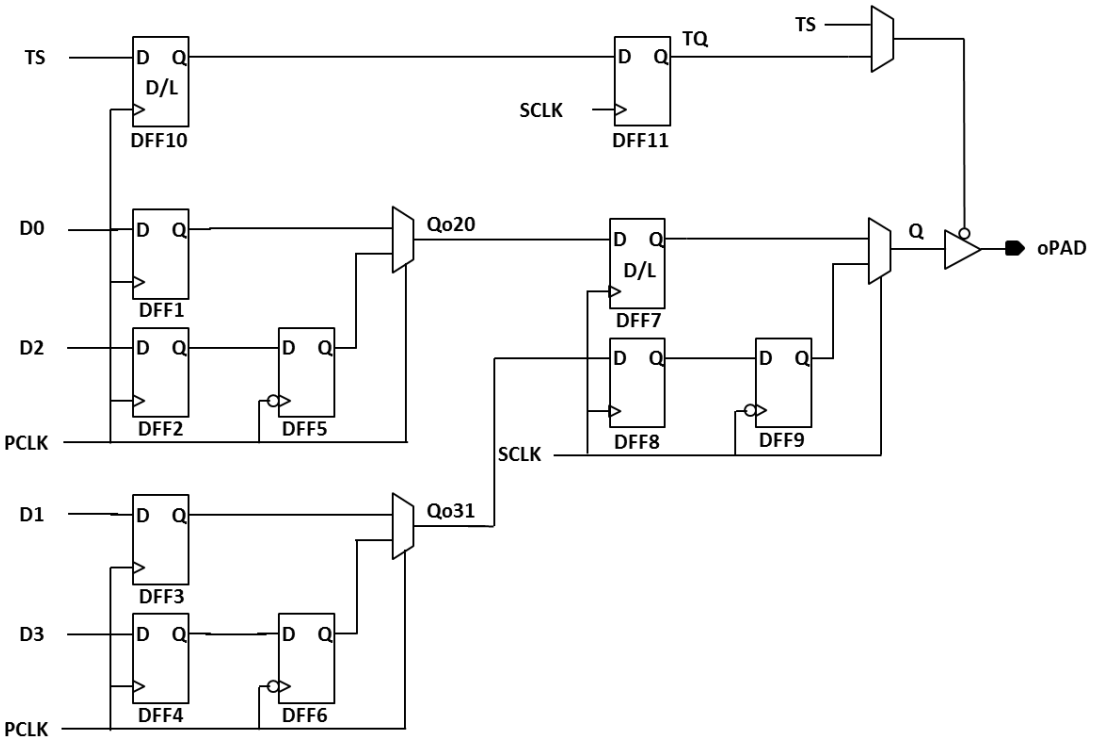


Figure 2-6-15 oDDRx2 output mode

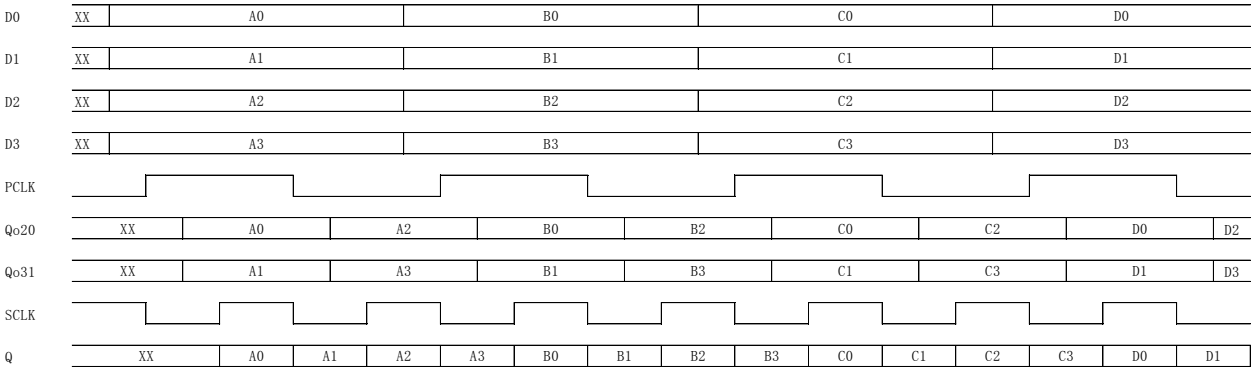


Figure 2-6-16 oDDRx2 Output Mode Timing

■ oDDRx2L output mode

Compared to oDDRx2, oDDRx2L mode directly uses the internal SCLK divide-by-2 as PCLK, saving 1 CLK. The data output is one SCLK clock cycle later than the oDDRx2 mode.

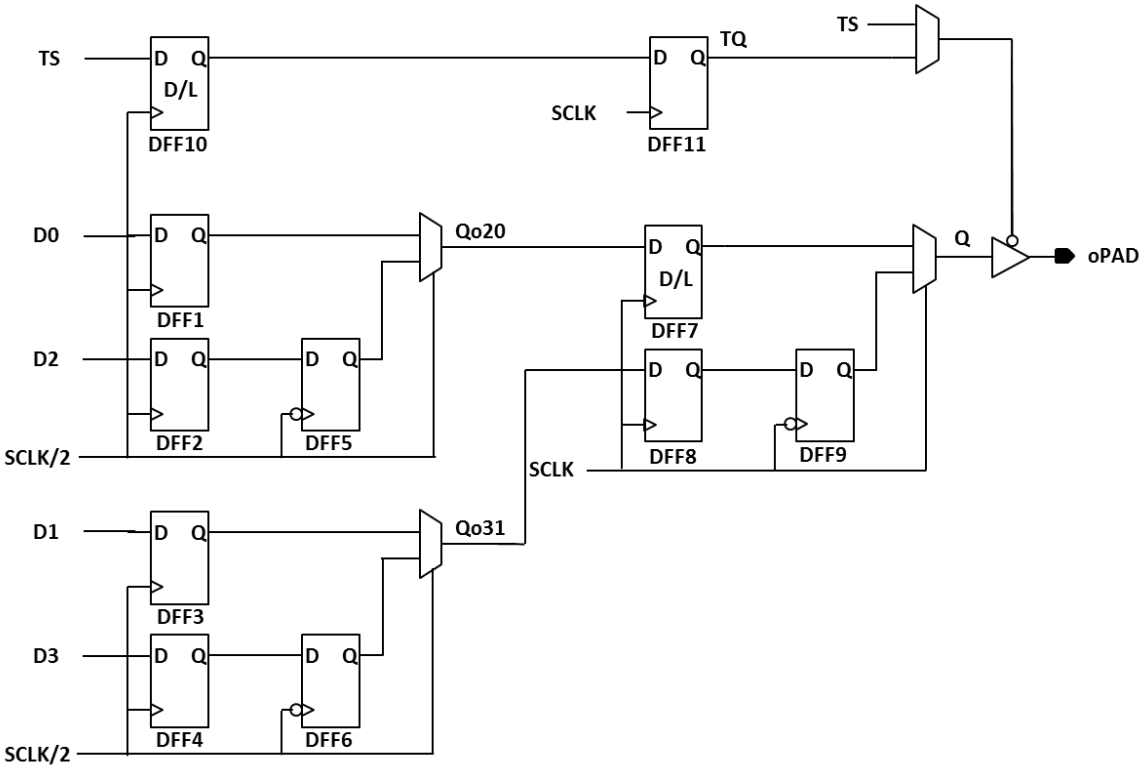


Figure 2-6-17 oDDRx2L output mode

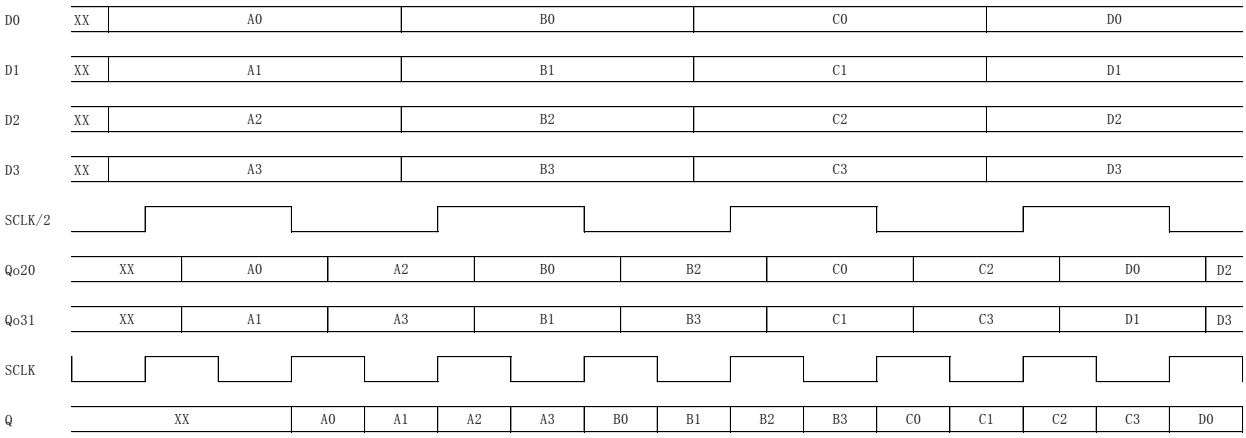


Figure 2-6-18 oDDRx2L Output Mode Timing

d) Output delay unit

Each IOL logic unit contains a programmable output delay unit that supports a total of four levels of regulation with a delay of 100ps per stage. A way to support static control delays.

2.7 Input and output buffer (IOB)

2.7.1 Introduction to IOB

EAGLE features configurable, high-performance I/O drivers and receivers to support a wide variety of standard interfaces. A powerful feature set includes programmable control of output intensity and slope.

Each IOB contains input, output, and tri-state drivers. These drivers can be configured to a variety of I/O standards. Differential I/O uses two IOBs in one module.

- Single-ended I/O standard (LVCMOS, LVTTL, PCI)
- Differential I/O standards (LVDS, LVPECL, BLVDS)

While the IOB supports the above level standards, the IOB supports the following configuration items:

- Output drive capability adjustment
- Output Slew Rate adjustment
- Weak pull-up/pull-down resistor selection configuration
- PCI Clamp enable
- Bus Hold function enable

Figure 2-7- 1 shows the basic IOB and its connections to internal logic and device pads.

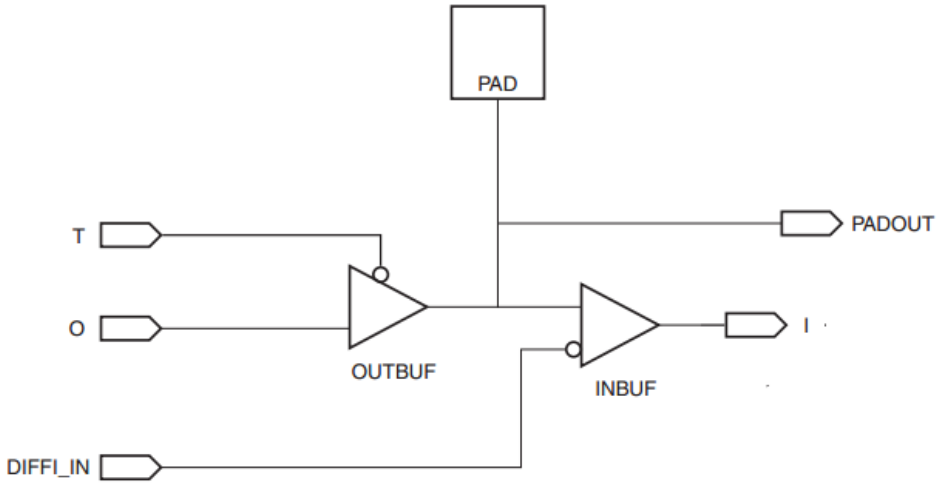


Figure 2-7-1 Basic IOB Block Diagram

Each IOB directly connects to the IOL to form an input-output logical pair that contains input and output logic resources that can be used for three-state control of data and IOB.

2.7.2 High speed LVDS interface

The differential standards supported by EAGLE devices are shown in Table 2-7-1.

Table 2-7-1 Differential Standards Supported by EAGLE

Differential standard	I/O Location	Receive		Send	
		Support	External resistance	Support	External resistance
LVDS	left and right	Yes	No	Yes	No
	up down left right	Yes	Yes	Yes	3 resistor
RSDS	left and right	Yes	No	Yes	No
	up down left right	Yes	Yes	Yes	3 resistor
mini-LVDS	left and right	Yes	No	Yes	No
	up down left right	Yes	Yes	Yes	3 resistor
PPDS	left and right	Yes	No	Yes	No
	up down left right	Yes	Yes	Yes	3 resistor
BLVDS	up down left right	Yes	Yes	Yes	Yes
LVPECL	left and right	Yes	No	-	-
	up down left right	Yes	Yes	Yes	3 resistor

Both True LVDS and Emulated LVDS can be used as standard inputs for LVDS25 with a maximum input frequency of 400 MHz (800 Mbps).

As an output, True LVDS uses the LVDS25 standard to directly output the LVDS level standard, eliminating the need for an external matching resistor, as shown in Figure 2-7-2. The maximum output frequency is 400MHz (800Mbps).

Emulated LVDS uses LVDS25E as the output, the maximum output frequency is 166MHz, and an external 3R resistor network is used to attenuate the output voltage swing to meet the LVDS standard, as shown in Figure 2-7-3. You can reduce power consumption or improve noise margin by changing the resistor network value.

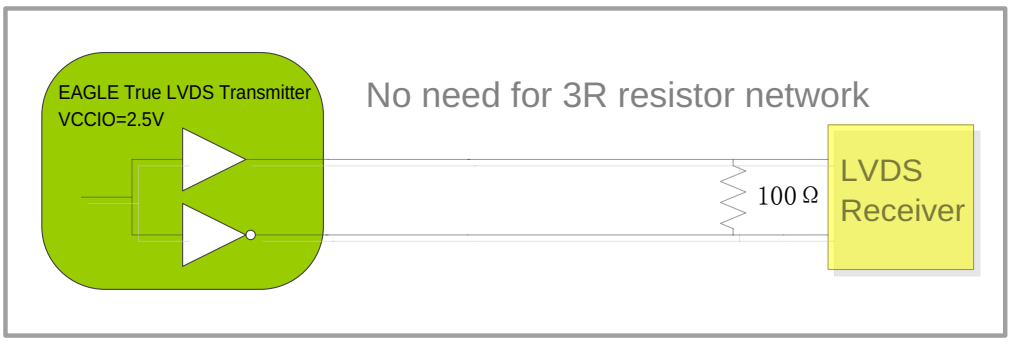


Figure 2-7-2 True LVDS Output

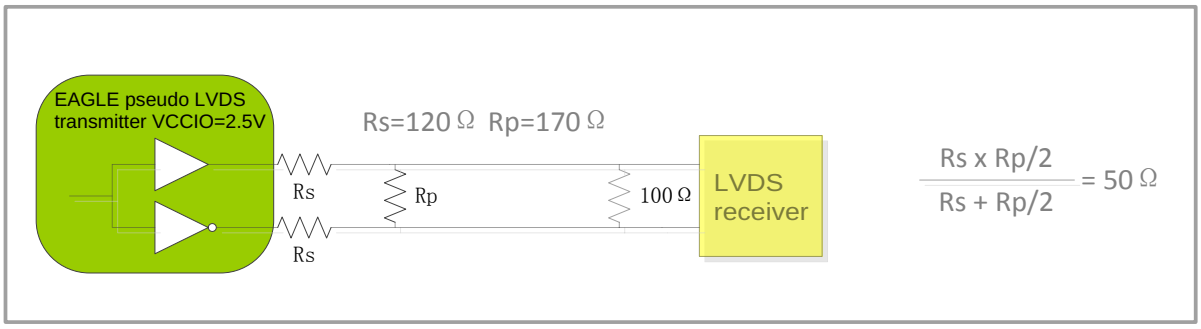


Figure 2-7-3 Emulated LVDS Output 3R Resistor Network

2.7.3 I/O grouping

The EAGLE device has eight I/O groups: two user I/O groups on each side. Group 1 is located near the configuration logic (config) and contains a dedicated/shared configuration interface.

Each I/O group contains two reference voltage inputs. Each I/O group is powered by the corresponding VCCIO.

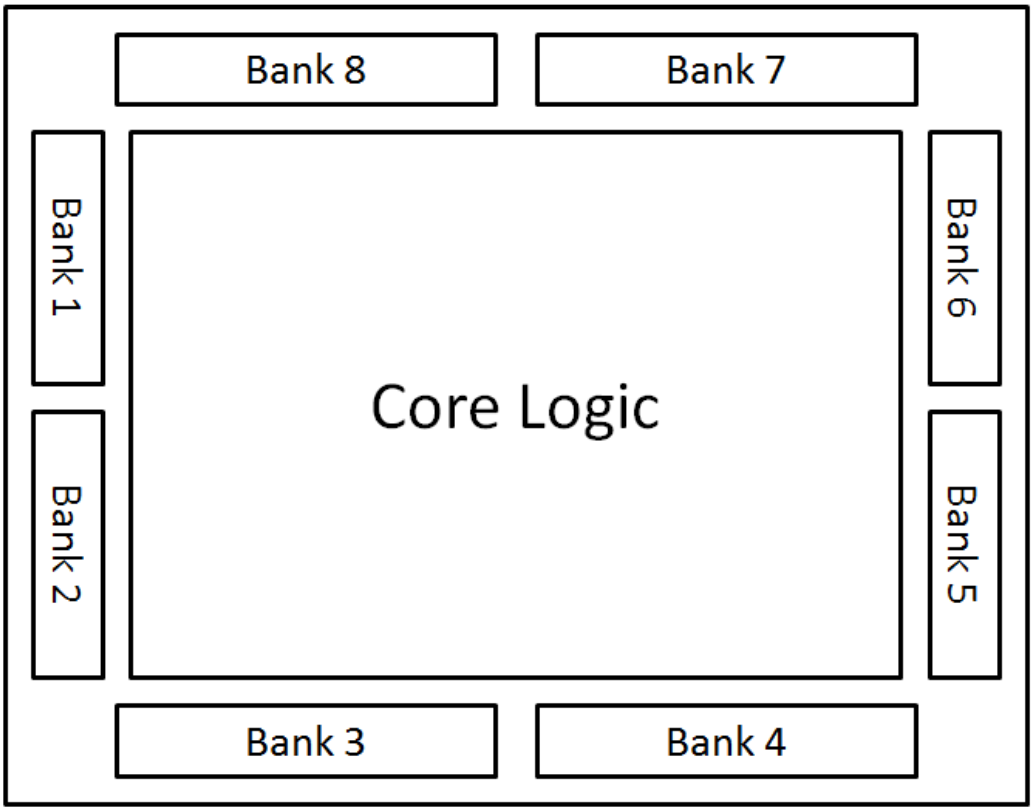
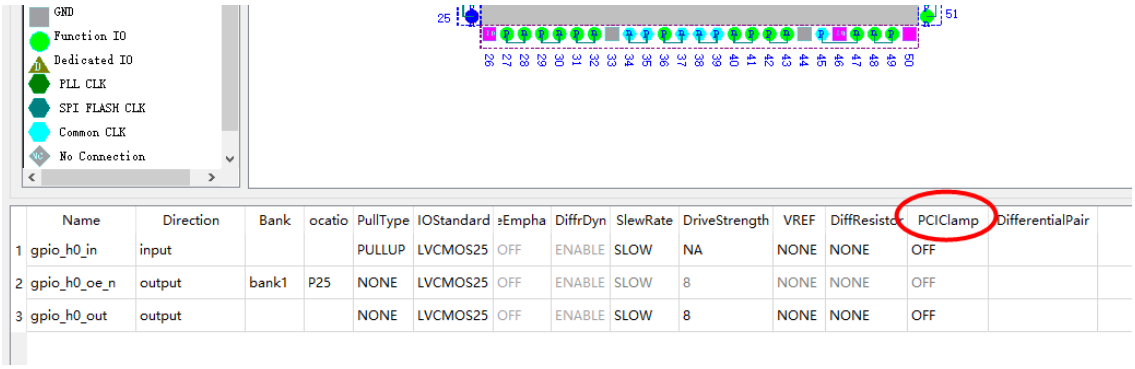


Figure 2-7-4 I/O group diagram

2.7.4 Compatibility with 5V inputs

The EAGLE I/O can operate from a 1.2-3.3V voltage range and cannot directly receive a 5V input. If the 5V voltage signal is driven to the input of the Eagle device, an external series resistor is required, and the PCI clamp diode inside the Eagle I/O is turned on in the software to reduce the voltage received by the input port to the safe range of the device, as shown in Figure 2 7- 5 is shown.

The value of the resistor R depends on the current characteristics of the PCI clamp diode. The voltage and current characteristics of the diode are shown in Table 2-7-2.



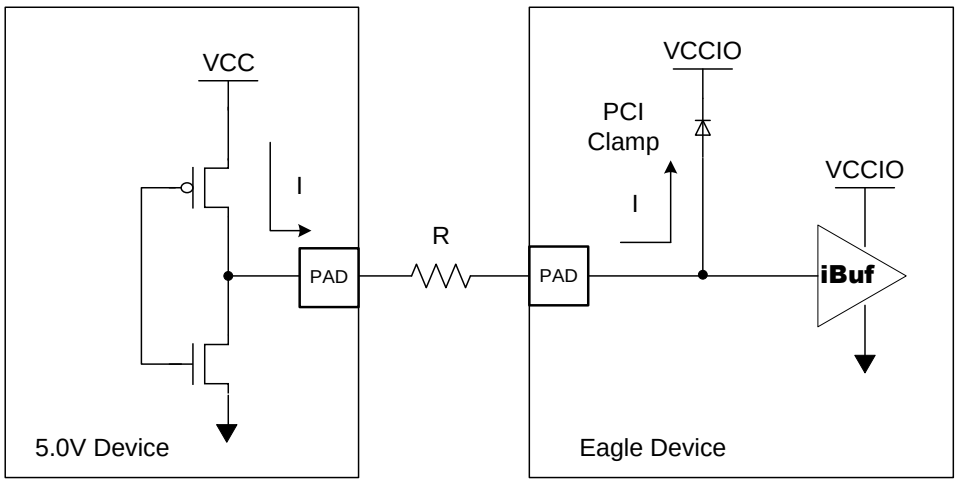


Figure 2-7-5 5V Input Drive Eagle Device

Table 2-7-2 Current Characteristics of PCI Clamping Diodes

V_D (V)	I_{max}	Unit
0.0	0.92	Ua
0.1	9.2	Ua
0.2	20	Ua
0.3	30.4	Ua
0.4	43.3	Ua
0.5	76.5	Ua
0.6	0.15	Ma
0.7	0.36	Ma
0.8	2.85	Ma
0.9	9.42	Ma

To support 5V input, it is recommended that the VCCIO voltage be in the 2.5-3.0V range. Otherwise, the IO voltage will

exceed the safe voltage, and long-term use will reduce the device lifetime.

The maximum tolerance of the I/O device is VIMAX=3.7V, set VCCIO=2.5V, and the voltage received by the IO input after dividing the voltage is VI=3.3V, then the voltage drop across the diode is VDIO = VI - VCCIO = 3.3 - 2.5 = 0.8V. IDIO @0.8V = 2.85Ma, R = (5 - 3.3)V/2.85Ma = 596Ohm.

In the input clamp channel, different resistance resistors are connected in series, and the waveform measured at the EAGLE receiving end is shown in Figure 2-7-6 ~ Figure 2-7-7. Series resistor R=330 Ohm, rise time is 7.8ns, fall time is 12ns, see Figure 2-7-6

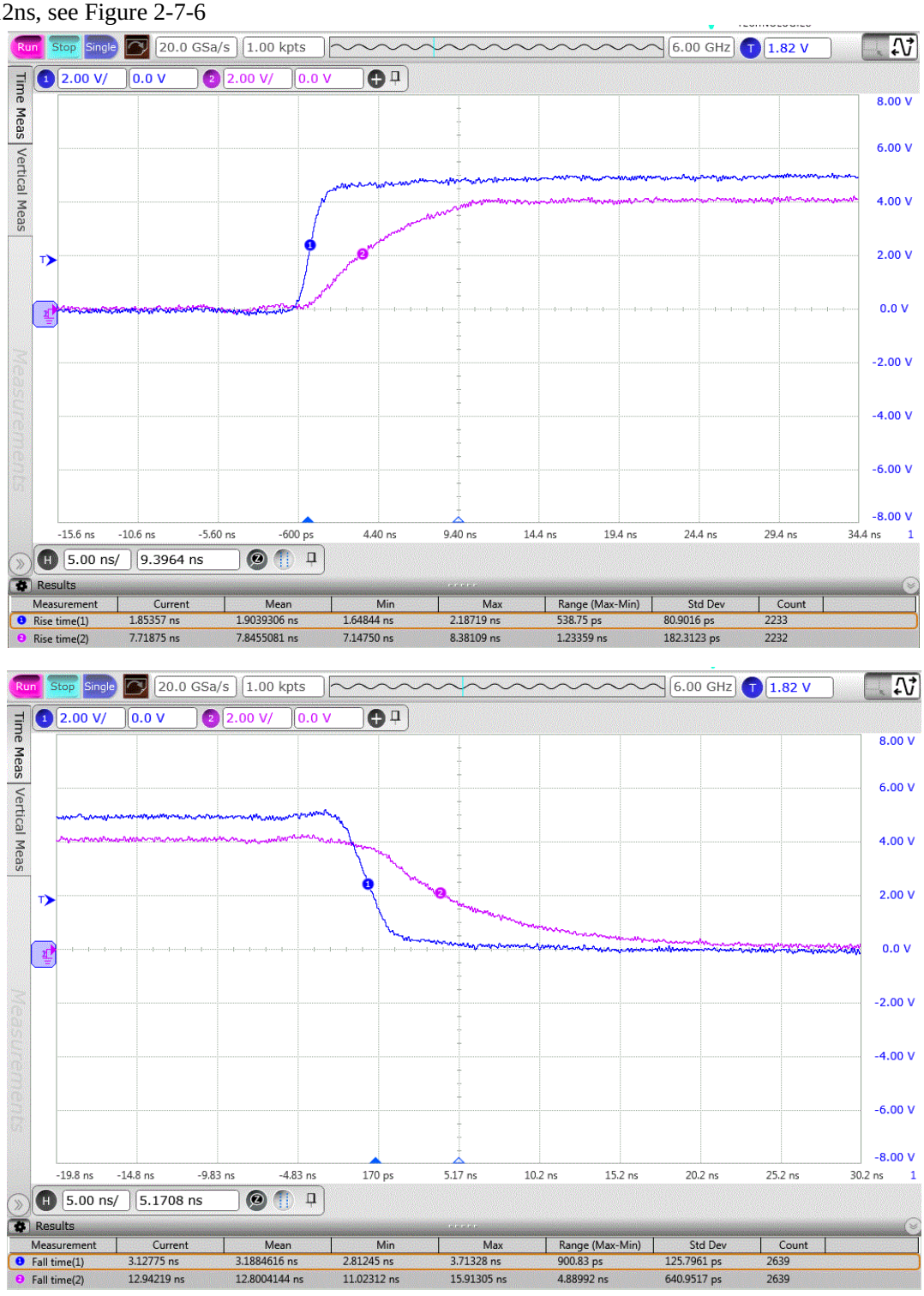


Figure 2-7-6 5V Input Drive EAGLE Device Receiver Waveform @R=330 Ohm

Series resistor R=600 Ohm, rise time is 12ns, and fall time is 21ns, see Figure 2-7-7

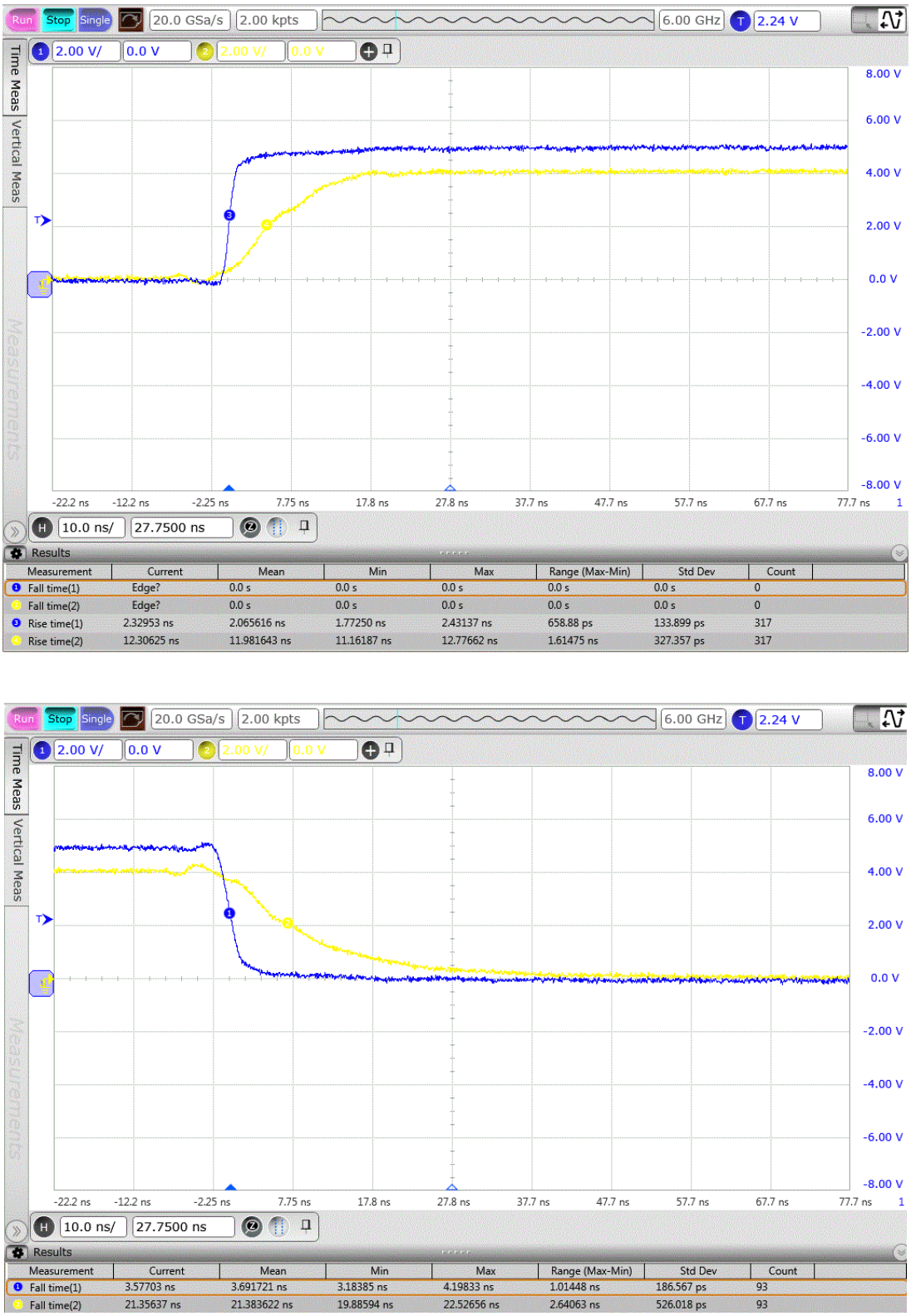


Figure 2-7-7 5V Input Drive EAGLE Device Rise/Fall Edge @R=600 Ohm

2.8 Power monitoring module

The EAGLE device includes a power monitoring module that monitors the power supply in harsh power applications. When the monitored power supply is lower than the set level, pwr_dwn_n changes from "H" to "L" to give an indication that the power supply is not working properly. Pwr1 and pwr2 are connected to the BANK voltage, which allows the user to monitor different power supplies and record or take appropriate action when a power failure is detected.

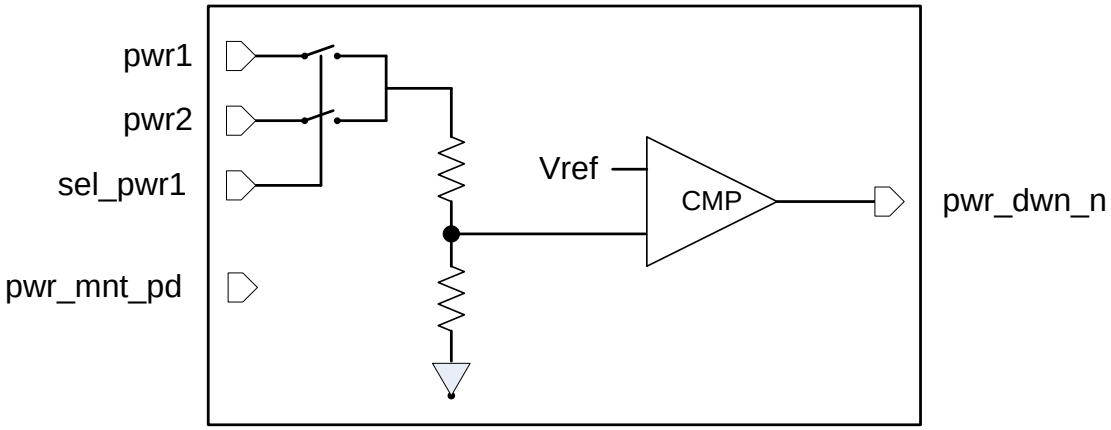


Figure 2-8-1 Power Supply Monitoring Module Block Diagram

The user can dynamically control the power monitoring module by calling EF2_PHY_PWRMNT IP.

```
module EF2_PHY_PWRMNT (sel_pwr, pwr_mnt_pd, pwr_dwn_n);
    output pwr_dwn_n;
    input sel_pwr;
    input pwr_mnt_pd;
  parameter MNT_LVL = 0; //1-7 1:1.86v 2:2.00v 3:2.17v 4:2.36v 5:2.60v 6:2.89v 7:3.25v
endmodule
```

Table 2-8-1 Configuring the port list

EF2_PHY_PWRMNT	Direction	Description
sel_pwr	Input	Monitoring port
pwr_mnt_pd	Input	Power down enable
pwr_dwn_n	Output	Monitor status output
MNT_LVL	parameter	Voltage threshold selection

Note 1: The sel_pwr monitor objects for different packages have slight differences, please refer to the pin list comments

Note 2: For the correspondence between MNT_LVL and voltage threshold, please refer to 3.1.10 Electrical Characteristics of Power Monitoring Module.

2.9 EAGLE FPGA Configuration instructions

The EAGLE FPGA chip has two IO layouts: EG4A and EG4X, which are compatible with the configuration modes of A and X respectively. Configuration is accomplished by loading configuration data into the chip. Some of the EAGLE FPGA chips are dedicated configuration pins, and the other part is a multiplexed pin. The TD software provides the configuration function of the multiplexed pins, which can be used as general input and output after the configuration is completed.

2.9.1 Configuration mode

EAGLE FPGA supports 5 configuration modes: slave serial, slave parallel, active parallel, MSPI mode and JTAG configuration mode. The configuration mode is selected by the mode selection signals of EG4A MSEL[2:0] and EG4X M[1:0] respectively. The specific selection relationship is shown in Table 2-9-1 and Table 2-9-2.

The EAGLE series FPGA configuration bitstream length is 4.8M~6Mbits. The bitstream length is related to the BRAM initialization data length. The chip capacity needs to be configured to be greater than or equal to 6M bits. The configuration chip can use industry-standard serial SPI interface FLASH, such as M25Pxx, SST25LFxxx, S25FLxxx and so on. EAGLE FPGA supports SPI FLASH for 0X03 read commands.

a) EG4A configuration mode

Table 2-9-1 EG4A Configuration Mode and Pins

Configuration mode						
Configuration pin	Types of	SS	SP	MSPI	MP	JTAG
		Slave serial	Slave Parallel	Standard SPI Master SPI Standard	Active parallelism Master Parallel (X8)	
MSEL[2:0]	Multiplexing	000/001	110/111	010/011/100	101	XXX
PROGRAMN	Multiplexing	PROGRAMN				
INITN	Multiplexing	INITN				
DONE	Multiplexing	DONE				
CCLK	Multiplexing	CCLK				
CSN	Multiplexing	CSN	CSN	CSN	CSN	
TMS TCK TDO TDI	Multiplexing					TMS CK TDO TDI
D[7:2]	Multiplexing	-	D[7:2]		D[7:2]	
D[1]/ MOSI	Multiplexing	-	D[1]	MOSI	D[1]	
D[0]/DIN/ MISO	Multiplexing	DIN	D[0]	MISO	D[0]	
SPICSN	Multiplexing			SPICSN		
CSON/DOUT	Multiplexing	CSON /DOUT	CSON	CSON /DOUT	CSON	

Below is the EG4A multiplexing configuration pin:

- Configuration Configuration Mode Select Pin (MSEL[0], MSEL[1], MSEL[2])
- Configuring the clock pin (CCLK)
- Configuration start signal pin (PROGRAM)
- Configuration completion pin (DONE)
- Configuration error indication pin (INITN)
- Mode Configuration Chip Select Pin (CSN)
- Configure cascaded chip select and data output pins (CSON/DOUT)
- Boundary scan related pins (TDI, TDO, TMS, TCK)
- Configure the data input pin (D[7:0]), where D[1] can also be used as MOSI in MSPI mode. D[0] can also be used as DIN in slave mode and MISO in MSPI mode.
- MSPI mode Flash Chip Select Pin (SPICSN)
- Multiplexing of signals such as PROG ININ DONE may cause problems such as reloading and is not recommended as an input. However, it can be used as an output pin.

b) EG4X configuration mode

Table 2-9-2 EG4X Configuration Modes and Pins

Configuration mode						
Configuration pin	Types of	SS	SP	MSPI	MP	JTAG
		Slave serial	Slave Parallel	Standard SPI Master SPI Standard	Active parallelism Master Parallel (X8)	
MSEL[1:0]	Multiplexing	11	10	01	00	XX
PROGRAMN_B	Multiplexing	PROGRAMN_B				
INIT_B	Multiplexing	INITN_B				
DONE	Multiplexing	DONE				
CCLK	Multiplexing	CCLK				
CSI_B/MOSI	Multiplexing		CSI_B	MOSI	CSI_B	
TMS TCK TDO TDI	Multiplexing					TMS CK TDO TDI
D[7:1]	Multiplexing	-	D[7:1]		D[7:1]	
D[0]/DIN/ MISO	Multiplexing	DIN	D[0]	MISO	D[0]	
CSO_B	Multiplexing		CSO_B	CSO_B	CSO_B	
DOUT	Multiplexing	DOUT		DOUT		

下面是 EG4A 复用配置引脚：

- Configuration mode selection pin (M[0], M[1])
- Configuring the clock pin (CCLK)
- Configuration start signal pin (PROGRAM_B)
- Configuration completion pin (DONE)
- Configuration error indication pin (INIT_B)
- Parallel mode configuration chip select pin (CSI_B)
- MOSI (MOSI) in MSPI mode
- Configuring Parallel Concatenated Chip Selector (CSO_B)
- Configuring cascaded serial data output pins (DOUT)
- Boundary scan related pins (TDI, TDO, TMS, TCK)
- Configure the data input pins (D[7:0]), where D[0] can also be used as DIN in slave mode and MISO in MSPI mode.

Depending on the configuration, CCLK can be the clock output generated by the FPGA chip or the input FPGA chip generated by the peripheral circuit. DONE/INITN/INIT_B is an open-drain output with an internal pull-up.

Multiplexing of signals such as PROG ININ DONE may cause problems such as reloading and is not recommended as an input. However, it can be used as an output pin.

2.9.2 Configuration process

The entire configuration process of the EAGLE FPGA chip can be divided into three parts. First, after the chip power-on reset or the system reset signal is valid, it enters the reset. After the internal signal and power supply are stable, the system enters the initialization phase, and the internal configuration information is cleared. After the initialization is completed, the FPGA starts to accept the configuration data write. After the write is completed, , FPGA chip startup phase, as shown in Figure 2-9-1.

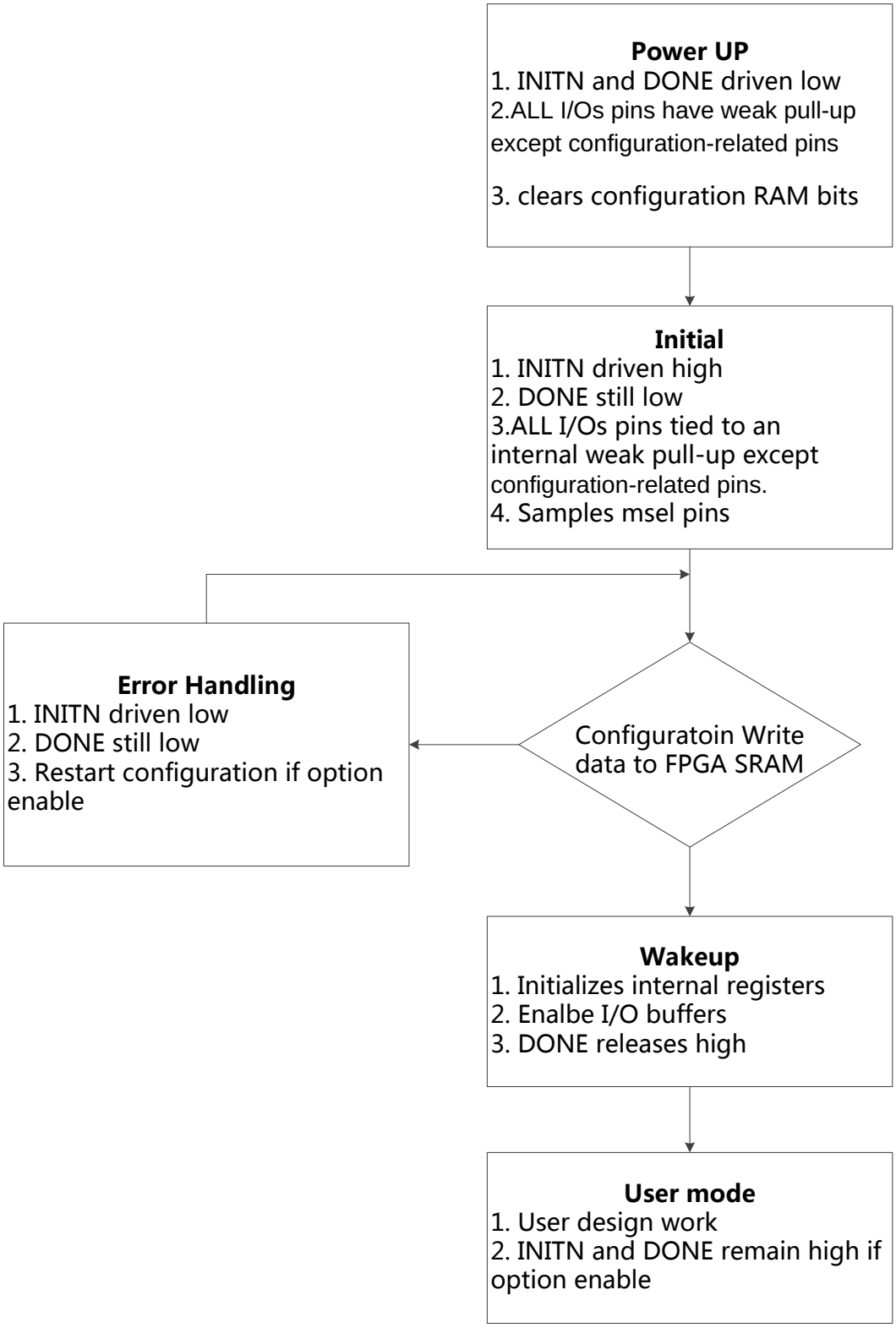


Figure 2-9-1 EG4A MSPI Configuration Mode

1. **Power-on initialization process**

After the EAGLE FPGA chip is powered on, the system needs to go through the initialization process to enter the configuration download state. In addition, if the user needs to re-download the configuration data, after pulling down PROGRAMN/PROGRAM_B, the system enters the initialization process. During the initialization process, the FPGA will clear all internal configuration points and reset the internal register.

2. **Configuration data write**

After initialization is complete, the INITN/INIT_B signal goes high and user configuration data can be written to the EAGLE FPGA.

When the INITN/INIT_B signal goes high, the FPGA sampling mode selects the signal level to determine the configuration mode. JTAG Configuration Mode After the INITN/INIT_B signal goes high, it can be entered in any mode.

During the configuration process, the INITN/INIT_B signal goes low to indicate that the configuration bitstream is faulty, and the bitstream can be reloaded after an error.

3. **Start-up phase**

After the EAGLE FPGA completes the data writes for all configuration points and block RAM, it enters the boot process. The EAGLE FPGA startup mainly performs the following functions:

1) Release the DONE signal. A low-to-high transition of the DONE signal indicates that the EAGLE FPGA has successfully completed the data configuration, which in turn indicates that the configuration has not completed successfully.
2) Release the global tristate signal GTS. The release of the global tri-state signal GTS releases all I/O pins.
3) The global reset/set signal GSR is released, allowing all flip-flops to change state.
4) The global write enable signal, GWE, is released, allowing all RAM and flip-flops to be written.

2.9.3 MIPI configuration mode

In MSPI mode, EG4A provides two dedicated signals MOSI and SPICSN for the SPI interface. The MOSI signal provides read commands, addresses and other information. SPICSN is the SPI chip select; EG4X provides two dedicated signals MOSI and CSO_B for the SPI interface. The MOSI signal provides read commands, addresses, etc., and CSO_B is the SPI chip select.

The CCLK clock in MSPI mode is generated by the internal oscillator and the user can select the CCLK frequency range. When the chip is powered up, CCLK is set to a default low frequency value. The user can change the CCLK frequency through the bitstream software frequency option. The CCLK frequency ranges from 2MHz to 64MHz.

SPI FPLASH data can be written by JTAG online using the Anlu FPGA download line. It can also be written directly by the On-line downloader or other dedicated programming tools during mass production.

Figure 2-9-2 shows the connection diagram of the EG4A MSPI configuration mode. The PROGRAM signal control resets the EAGLE FPGA configuration. The INITN and DONE signals are open-drain output signals with internal pull-ups. The DONE signal goes high, indicating that the configuration is successful and the chip starts to work. . The configuration timing is shown in Figure 2-9-3.

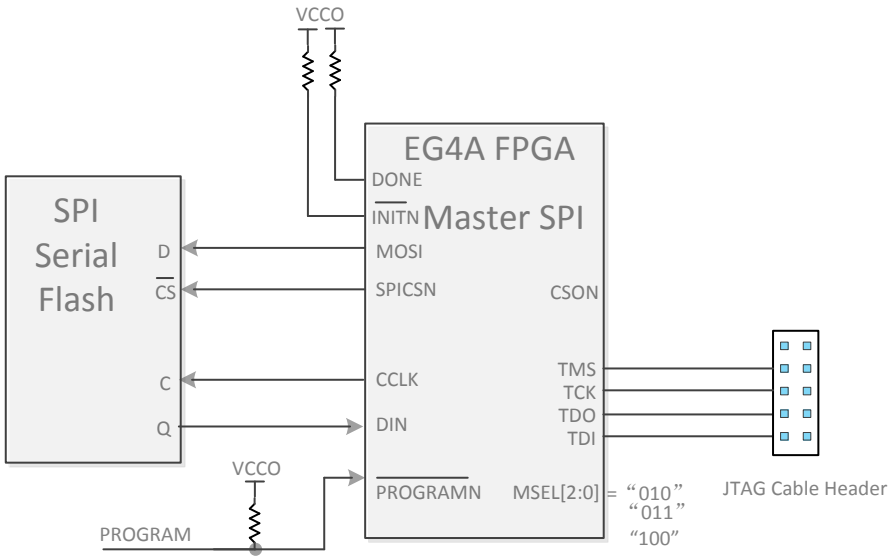


Figure 2-9-2 EG4A MSPI Configuration Mode

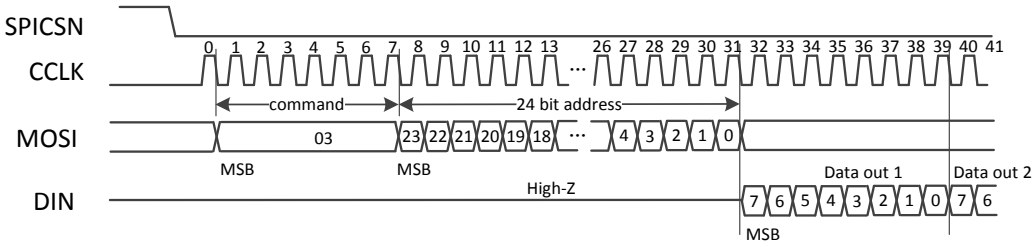


Figure 2-9-3 EG4A MSPI Configuration Mode Timing Diagram

2.9.4 Slave serial configuration mode

In Slave Serial (SS) mode, the FPGA can be loaded via the MCU. The TD software can generate bin files (EG4X) or rbf files (EG4A) for MCU loading.

The MCU writes data to the FPGA serially using the CCLK, DIN signals. The EAGLE FPGA chip receives data on the rising edge of each CCLK. After the data is sent, DONE is pulled high to indicate that the configuration is complete. If the configuration is wrong, the INITN/INIT_B signal will be pulled low.

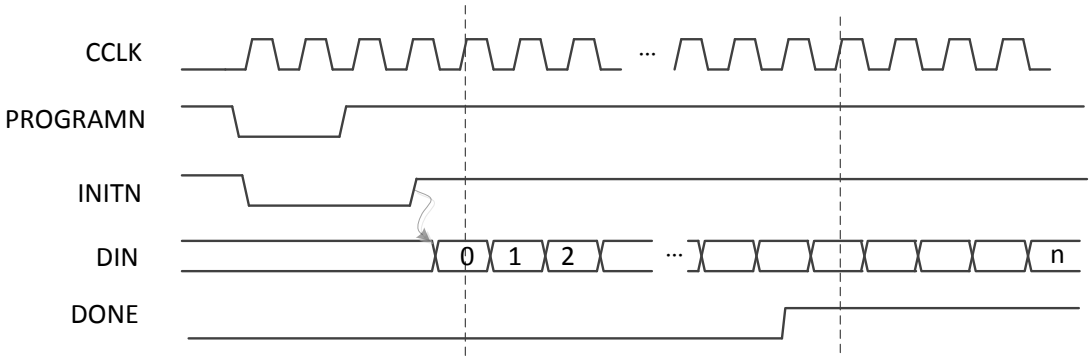


Figure 2-9-4 EG4A Serial Configuration Mode Timing Diagram

The timing of the EG4A slave serial configuration mode is shown in Figure 2-9-4. After PROGRAMN is pulled low,

the INITN signal is pulled down, indicating that the chip starts to initialize. After about 5ms, the chip initialization is completed, INITN returns to high level, the configuration starts, and the FPGA collects configuration data on the rising edge of the clock. After the configuration is completed, the DONE signal is completed. Going high means the configuration is successful and the chip starts working.

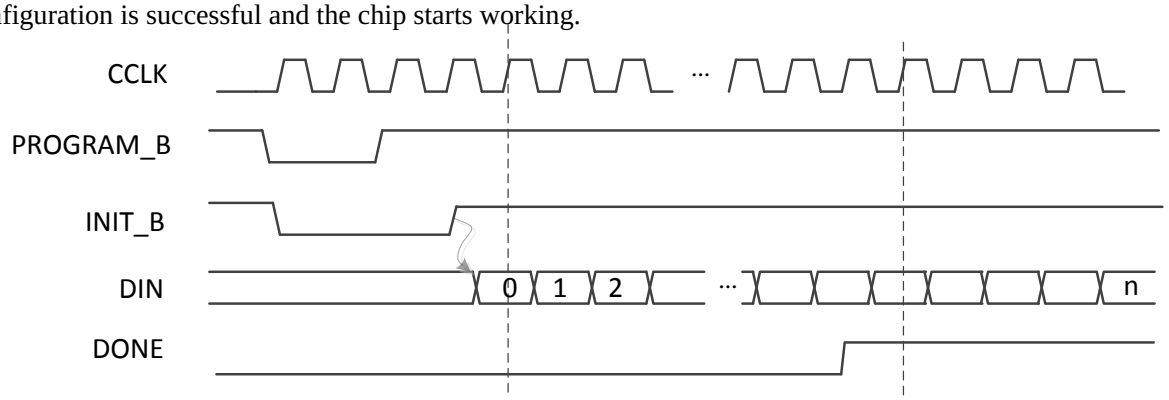


Figure 2-9-5 EG4X Serial Configuration Mode Timing Diagram

The timing of the EG4X slave serial configuration is shown in Figure 2-9-5. The process is similar to the EG4A.

2.9.5 Serial configuration mode cascading

When multiple FPGAs are required to work together, a cascading configuration method can be used. EAGLE FPGA supports 2 cascading modes:

In Flow-Through and Bypass modes, the cascading mode of operation is specified by commands in the bitstream. The EG4A supports Flow-Through and Bypass modes. EG4X only supports Bypass mode.

When the configuration data of the EG4A chip is downloaded, if Flow-Through mode is used, after the first fast FPGA configuration is completed, the output CSON starts the second chip to enter the configuration. In Bypass mode, after the first chip configuration is completed, the data configured for other FPGAs is output to the DOUT pin every CCLK rise time. The DONE and INITN pins of the cascading configuration chip are connected together by a pull-up resistor line. After only 2 pieces are configured, the DONE chip starts working at the same time.

Figure 2-9-6 shows the EG4A serial configuration mode Flow-Through cascading mode diagram. There are two FPGA cascaded configurations in the figure. The first one uses the active serial mode and the second uses the slave serial mode. Figure 2-9- 7 is a serial configuration mode Bypass cascading mode diagram.

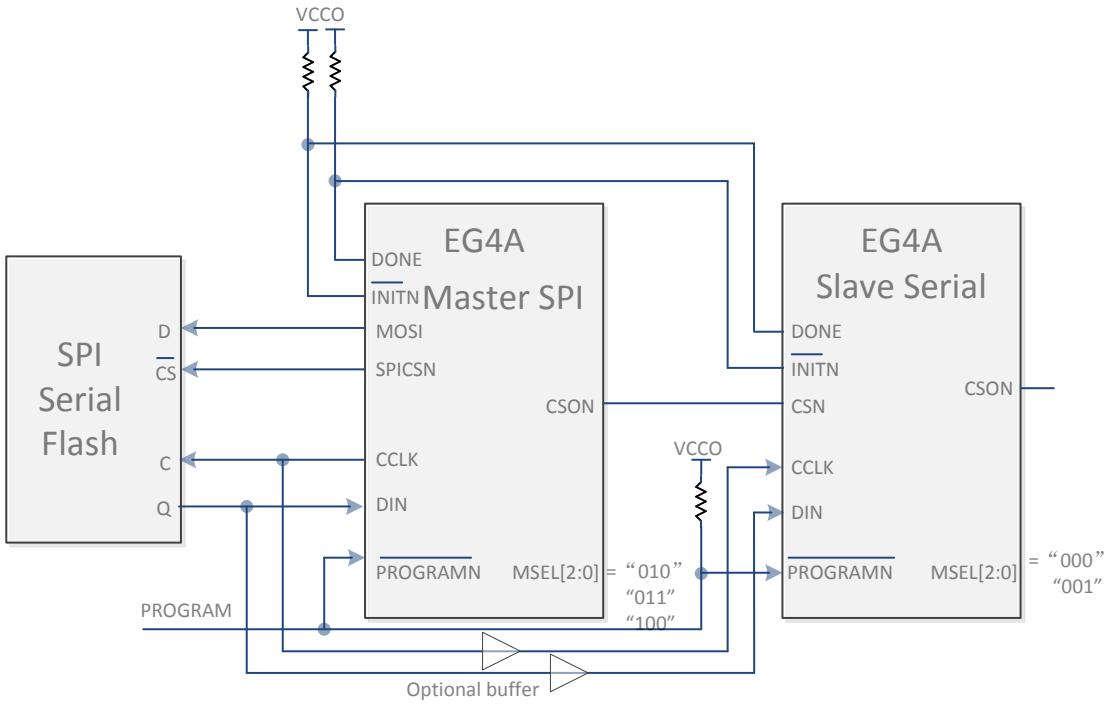


Figure 2-9-6 EFF4A active and slave serial adopts Flow-Through cascade configuration diagram

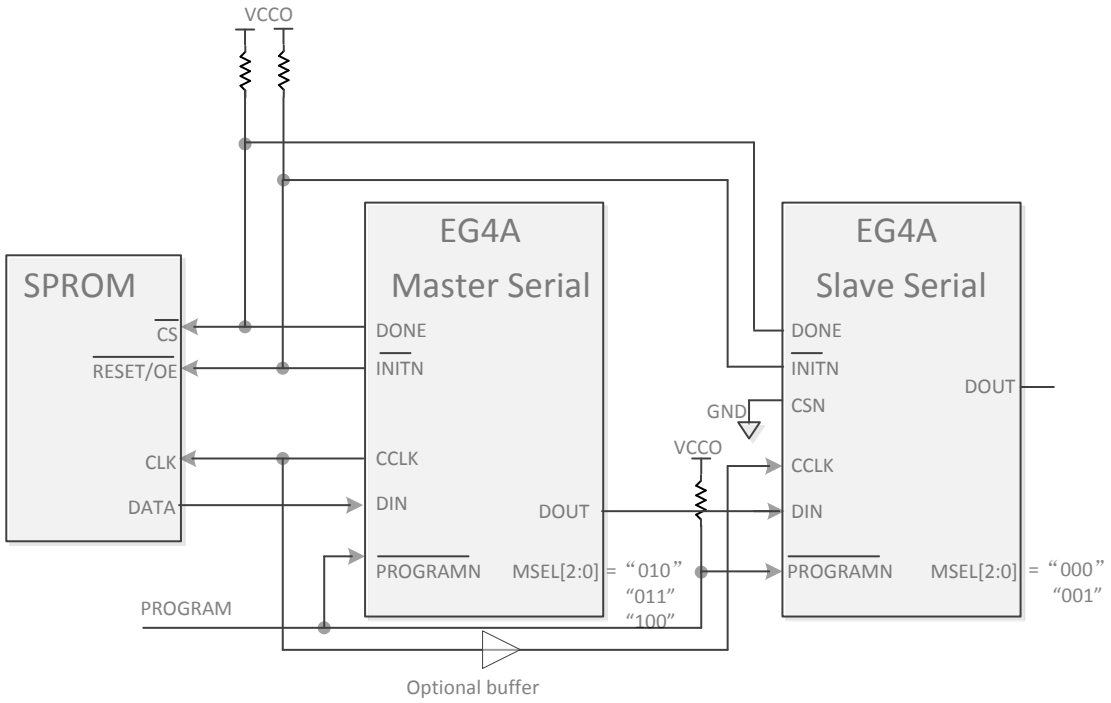


Figure 2-9-7 EG4A active and slave serial adopts Bypass cascading configuration diagram

Figure 2-9- 8 is the EG4X serial configuration mode Bypass cascading mode diagram. The memory can be SPI flash or SPROM.

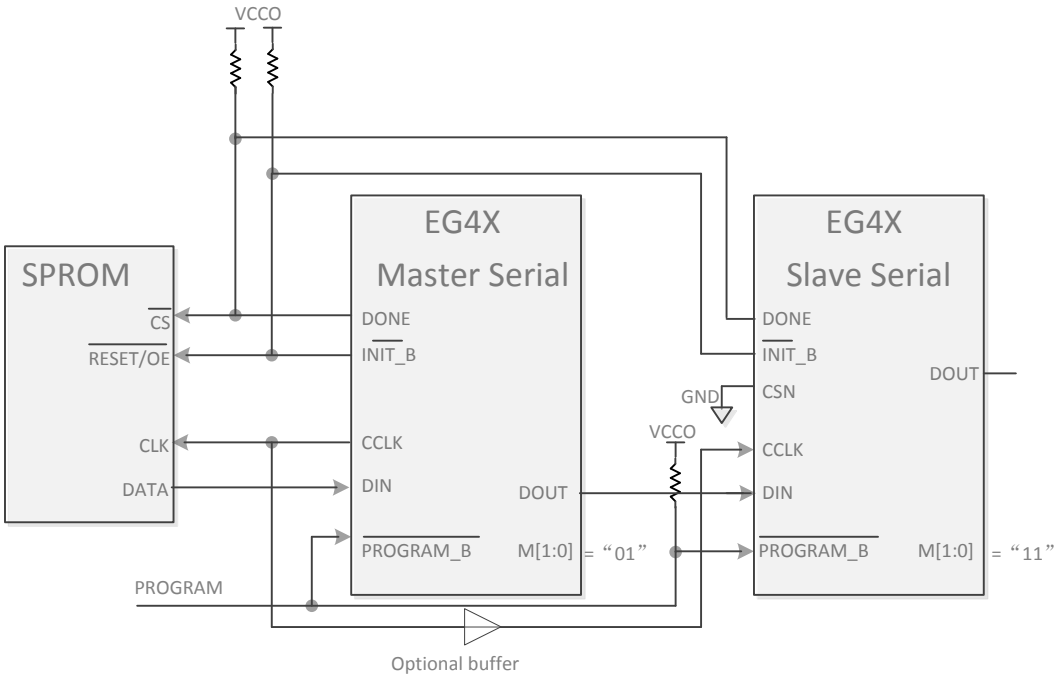


Figure 2-9-8 EG4X active and slave serial adopts Bypass cascading configuration diagram

2.9.6 Slave parallel configuration mode

The slave parallel configuration is suitable for use by controllers such as MCUs or CPUs. Slave parallel configuration enables faster configuration speeds with 8-bit parallel data writes.

The slave parallel configuration mode of EG4A MSEL[2:0] is set to 110/111, as shown in Figure 2-9-9, where multiple CSN signals can select multiple configuration chips.

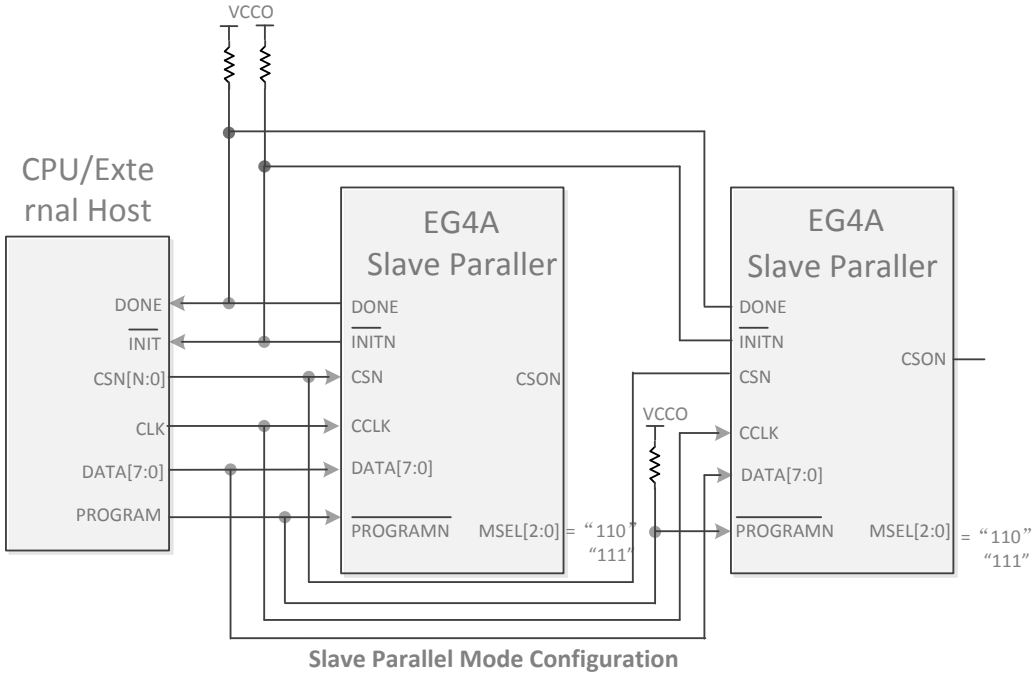


Figure 2-9-9 EG4A slave parallel configuration mode

The timing of the EG4A slave parallel configuration mode is shown in Figure 2-9-10. The initial initialization process is the same as the serial configuration. After the initialization is complete, the configuration data is written to the EAGLE FPGA on the rising edge of the clock when the chip select CSN is active. Similarly, after the configuration is complete, the DONE signal will go high.

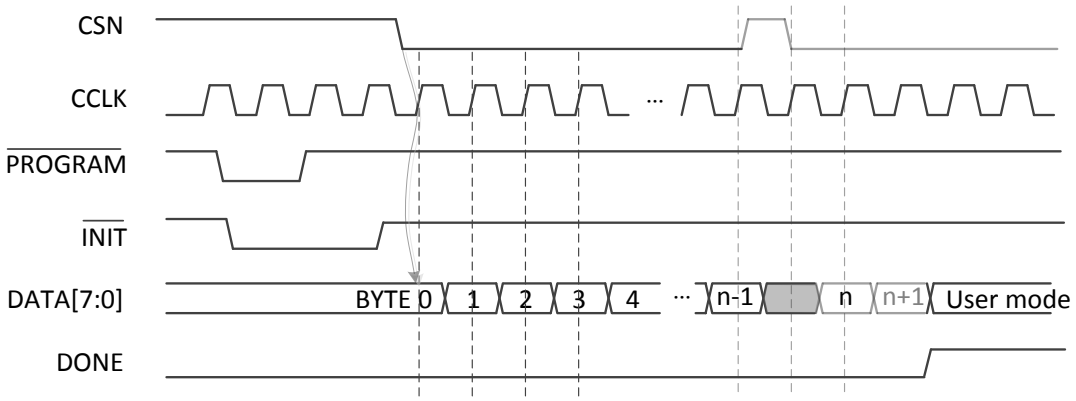


Figure 2-9-10 EG4A slave parallel configuration timing diagram

The EG4X's slave parallel configuration mode M[1:0] is set to 10, as shown in Figure 2-9-11, where multiple CSN signals can select multiple configuration chips.

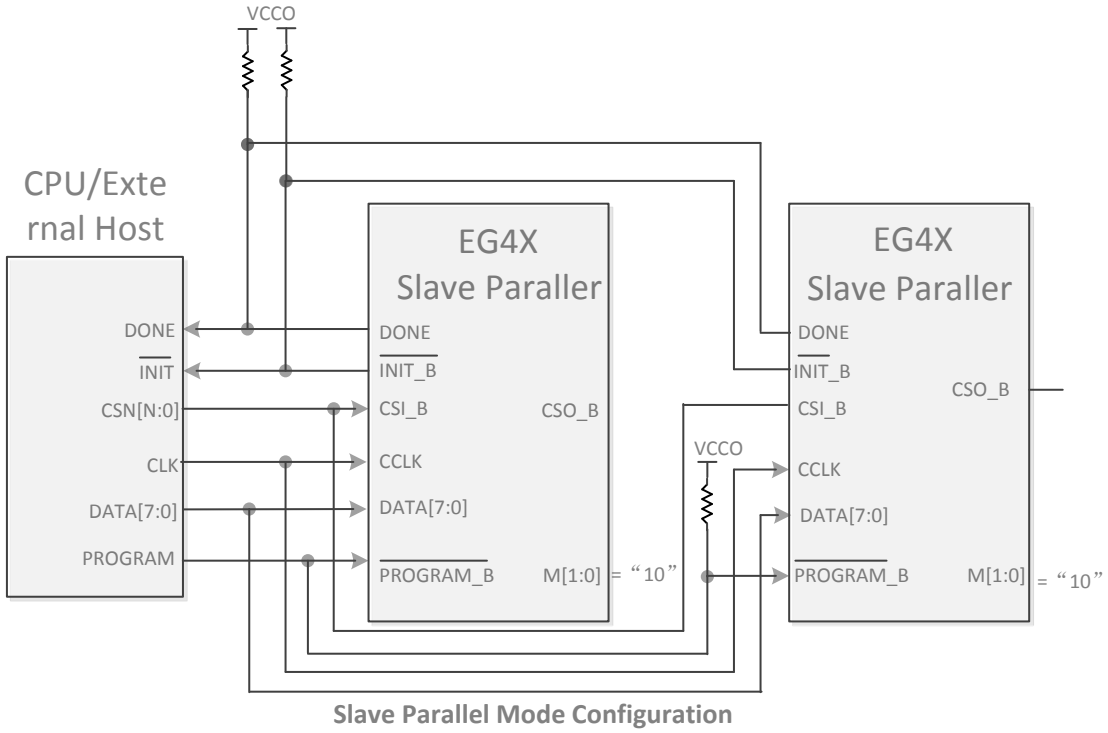


Figure 2-9-11 EG4X slave parallel configuration timing diagram

The timing of the EG4X slave parallel configuration mode is shown in Figure 2-9-12. The initial initialization process is the same as the serial configuration. After the initialization is completed, the data is written to the EAGLE FPGA on the rising edge of the clock when the chip select CSI_B is active. Similarly, after the configuration is complete, the DONE signal will go high.

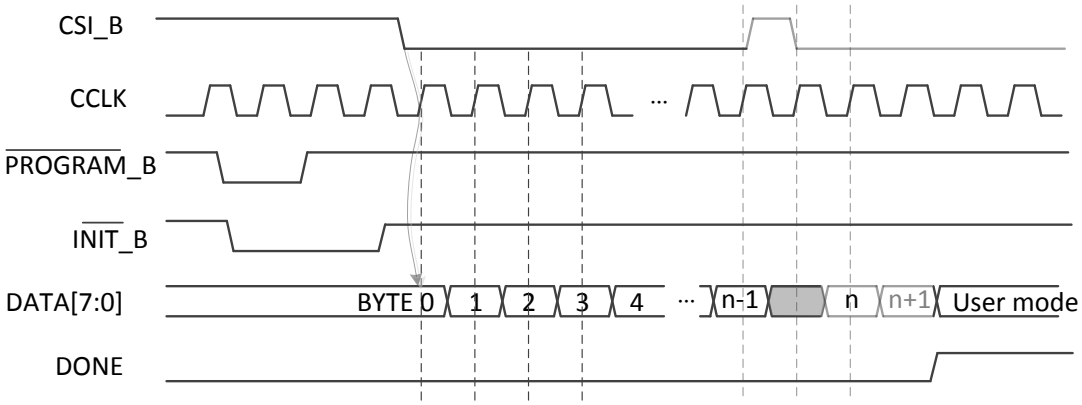


Figure 2-9-12 EG4X slave parallel configuration timing diagram

2.9.7 Active parallel configuration mode

Active parallel configuration is similar to slave parallel configuration, except that the CCLK clock is provided by the FPGA.

2.9.8 JTAG configuration mode

EAGLE FPGAs can also be configured in JTAG mode. The JTAG mode configuration is performed through the configuration pins (TDI, TDO, TMS, TCK) of the EAGLE FPGA. JTAG Configuration Mode After the INITN/INIT_B signal goes high, regardless of the mode selected by the mode select pin, or other modes are being configured, the JTAG mode can interrupt other modes by instruction to enter the JTAG configuration mode.

The JTAG configuration uses the USB download line dedicated to Anlu, and is used with the TD software. You can check whether the configuration is successful through software.

2.9.9 MSPI DUAL-BOOT function

ESPILE FPGA supports MSPI dual-boot function when SPI flash capacity is greater than 12Mbit in MSPI mode. When the Primary bitstream fails to download, the EAGLE FPGA automatically jumps to the user-set address to read the golden bitstream. Figure 2-9- 13 shows the data space distribution of spi flash under dual-boot.

Dual-boot flash map	
0x000000	Primary bitstream
……	
0x0C0000	Dummy
……	
0x0D0000	Golden address
……	Golden bitstream

Figure 2-9-13 Data space distribution of EAGLE FPGA dual-boot spi flash

2.9.10 MSPI MULT-BOOT function

In MSPI mode, the user can use the TD software to set the mult-boot function. When entering user mode, the application itself can restart the download of the bitstream from the specified spi flash address via the interface trigger signal mult_bootn=0. This specified address can be selected from the user interface or provided by the TD software.

2.9.11 FPGA DNA security features

EAGLE FPGA provides a unique 64-bit DNA data for each chip during the production process. This data cannot be modified and erased. Users can protect the user with DNA data. The TD software will provide an IP interface that allows the user to read out the DNA data. As shown in Figure 2-9- 14, Figure 2-9-15. Usr_dna_in is a shift data input for interface testing.

Dna_clk Clock frequency range 0~20MHz, dna_shift It is recommended to use the falling edge of the clock to send out, which is convenient for timing requirements.

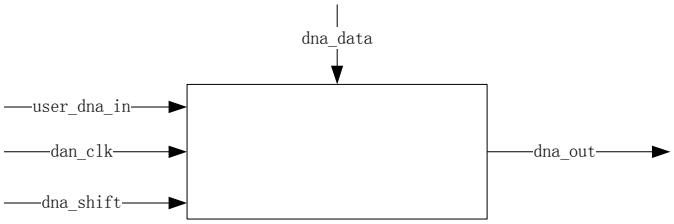


Figure 2-9-14 EAGLE FPGA DNA IP

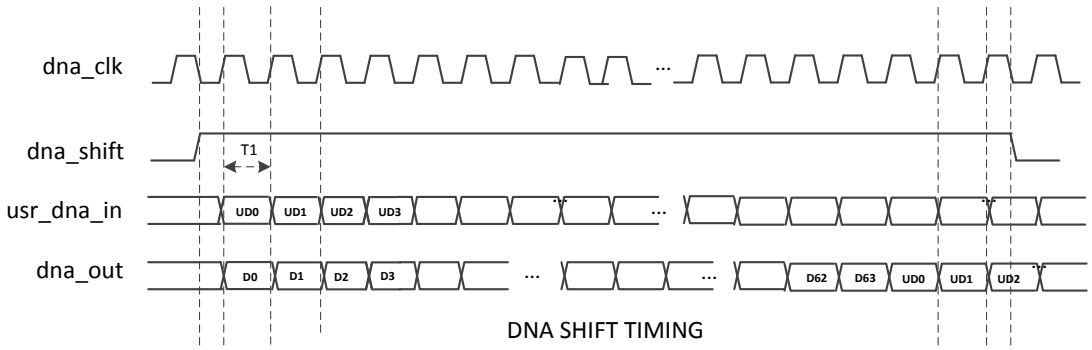


Figure 2-9-15 EAGLE FPGA DNA Timing Diagram

2.9.12 FPGA I/O pin settings during configuration

During the configuration phase, some FPGA pins have dedicated pull-up/pull-down resistors. Most user I/O pins have an optional pull-up resistor during configuration. During configuration, the EG4A and EG4X use the HSWAPEN signal to determine if the pull-up resistor is enabled on the I/O pin.

2.9.13 Status of the FPGA I/O pins during the configuration phase

(1) Non-configuration related IO

The non-configuration related IO is tri-stated before the program is loaded after the chip is powered on.

During the loading process, the state of the normal IO can be weakly pulled up or tri-stated by the HSWAPEN pin.

After entering user mode, the IO pin status used by the user is code controlled, and the unused pins are weakly pulled.

(2) The configuration related pins are related to the configuration settings, as shown in Table 2-9-3 and Table 2-9-4.

In EG4A, HSWAPEN is a control register CTRL[31]. The default value is 1, which can only be overwritten by the bitstream.

表 2-9-3 EG4A Configuration Pin Termination

Pin	Pre-configureation		Post-configureation
	HSWAPEN=0(enable)	HSWAPEN=1(disable)	
MSEL[2:0]	Pull-up to Vccio	Pull-up to Vccio	User I/O
PROGRAMN	Pull-up to Vccio	Pull-up to Vccio	Software ProgPin settings
INITN	Pull-up to Vccio	Pull-up to Vccio	Software InitPin settings
DONE	Pull-up to Vccio	Pull-up to Vccio	Software DonePin settings
CCLK	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin settings
CSN	Pull-down to Gnd	Pull-down to Gnd	User I/O
TMS TCK TDO TDI	Pull-up to Vccio	Pull-up to Vccio	Software JTAGPin settings
D[7:2]	Pull-up to Vccio	Pull-up to Vccio	User I/O
D[1]/ MOSI	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin settings
D[0]/DIN/MISO	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin settings
SPICSN	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin settings
CSON/DOUT	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin settings
Others	Pull-up to Vccio	High-Z	User I/O

In the EG4X, HSWAPEN is an I/O pin and defaults to a weak pull-up. As shown in Table 2-9-4.

表 2-9-4 EG4X Configuration Pin Termination

Pin	Pre-configureation		Post-configuration
	HSWAPEN=0(enable)	HSWAPEN=1(disable)	
M[1:0]	Pull-up to Vccio	Pull-up to Vccio	User I/O
PROGRAM_B	Pull-up to Vccio	Pull-up to Vccio	Software ProgPin settings
INIT_B	Pull-up to Vccio	Pull-up to Vccio	User I/O
DONE	Pull-up to Vccio	Pull-up to Vccio	Software DonePin settings
CCLK	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin settings

CSI_B/MOSI	Pull-down to Gnd	Pull-down to Gnd	Software SpiPin settings
TMS TCK TDO TDI	Pull-up to Vccio	Pull-up to Vccio	Software JtagPin settings
D[7:1]	Pull-up to Vccio	Pull-up to Vccio	User I/O
D[0]/DIN/MISO	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin settings
CSO_B	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin settings
DOUT	Pull-up to Vccio	Pull-up to Vccio	Software SpiPin settings
HSWAPEN	Pull-up to Vccio	Pull-up to Vccio	User I/O
Others	Pull-up to Vccio	High-Z	User I/O

2.10 Embedded ADC module

Eagle has an 8-channel 12-bit 1MSPS ADC embedded in it. The ADC requires a separate 3.3V analog operating voltage and analog ground as well as a separate VREF voltage input. 8 channel inputs and user IO multiplexing, can be used as normal user IO when the user does not need ADC, the multiplexed IO settings are independent of each other, and the unused ADC channel pins can be used as normal IO. When using an ADC, the VCCIO voltage of the associated BANK should not be lower than the ADC analog supply voltage.

Table 2-10-1 ADC External/Internal Port

Chip port name	Port type	Description
ADC_VDDD	Power supply PAD	3.3V digital power input
ADC_VDDA	External power supply PAD	3.3V analog power input
ADC_VSSA	External power supply PAD	3.3V analog ground
ADC_VREF	External PAD	Independent input, sampling reference analog potential input, input voltage range 2.0V~3.3V, not greater than VDDA
ADC_HC<7:0>	External PAD	8 sampling signal inputs, multiplexed with user IO
Internal port name	**Port direction**	**Description**
Channel_s<2:0>	Input (from FPGA)	ADC channel select signal input
SOC	Input (from FPGA)	ADC sample enable signal input, high efficiency
EOC	Output (to FPGA)	ADC conversion complete output, high effective
B<11:0>	Output (to FPGA)	ADC conversion result for the corresponding channel

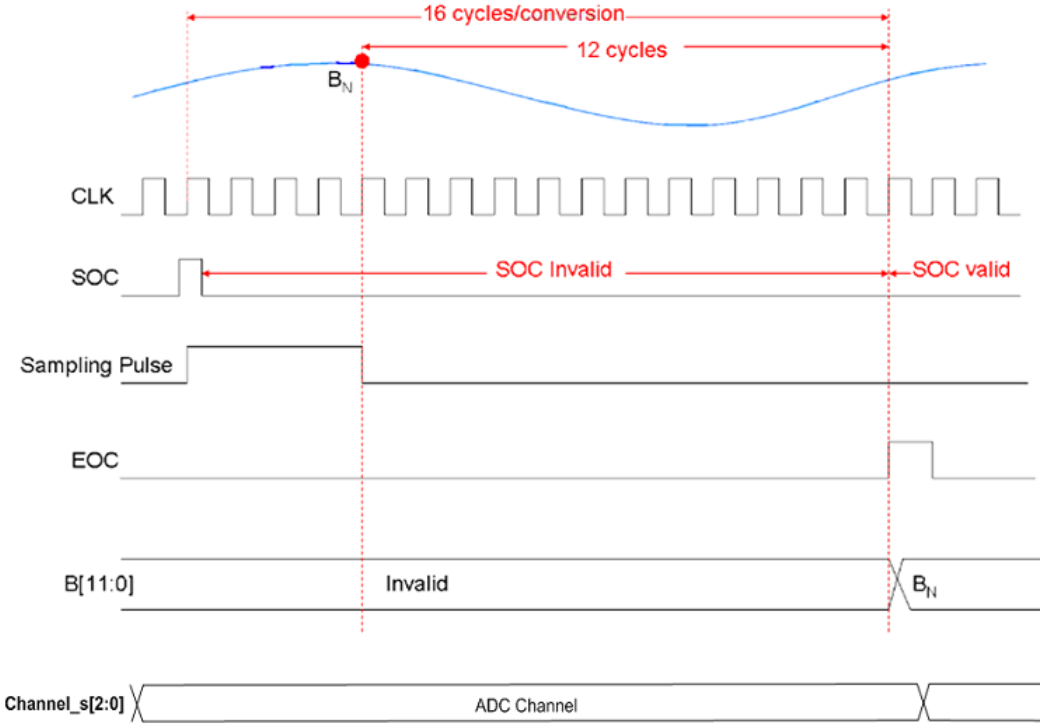


Figure 2-10-1 Eagle ADC Sampling Control Timing

3 DC communication characteristics

All parameters refer to the worst-case supply voltage and junction temperature. Unless otherwise stated, the following information applies to: AC and DC characteristics specified at the same commercial and industrial level. All parameters are values when voltage is applied to ground.

3.1 DC electrical characteristics

3.1.1 Absolute rating

Table 3-1-1 Maximum absolute rating

SYMBOL	Parameter	Minimum	Maximum	Unit
V_{CC}	Core supply voltage	-0.5	1.32	V
V_{CCAUX}	Auxiliary power	-0.5	3.75	V
V_{CCIO}	I/O drive supply voltage	-0.5	3.75	V
V_I	DC input voltage	-0.5	3.75	V
V_{ESDHBM}	Human body model electrostatic discharge voltage		±2000	V
V_{ESDCDM}	Machine model electrostatic discharge voltage		±500	V
T_{STG}	storage temperature	-65	150	℃
T_J	Junction temperature	-40	125	℃

Exceeding the above maximum absolute ratings may result in permanent damage to the device. These values only indicate that operation at this rating will not damage the device, but does not indicate that the device will function properly at this limit. Functional operation of the device or any condition based on this maximum absolute rating may cause permanent damage to the device. Long-term operation of the device under extreme conditions can seriously affect the reliability of the device.

During signal conversion, the input signal overshoot/undershoot may exceed the values given in the above table, but must meet both the current less than 100Ma and the pulse width less than 20ns.

3.1.2 Recommended basic operating conditions

Table 3-1-2 Recommended basic operating conditions

SYMBOL	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Core supply voltage	1.14	1.2	1.26	V
V_{CCAUX}	Auxiliary power	2.375	2.5/3.3	3.63	V
VCCIO[3]	I/O supply voltage @ 3.3V	3.135	3.3	3.465	V
	I/O supply voltage @ 2.5V	2.375	2.5	2.625	V
	I/O supply voltage @ 1.8V	1.71	1.8	1.89	V
	I/O supply voltage @ 1.5V	1.425	1.5	1.575	V
	I/O supply voltage @ 1.2V	1.14	1.2	1.26	V
V_I	DC input voltage	-0.5	—	3.6	V
V_O	The output voltage	0	—	V_{CCIO}	V

T_J	Junction temperature	business	0	—	85	℃
		industry	-40	—	100	℃
T_{RAMP}	Power ramp rate		0.01	-	100	V/ms
I_{Diode}	PCI-clamp diode current		—	—	10	mA

1. The device requires all the I/O's VCCIO to be connected to the power supply.
2. All input buffers are powered by VCCIO

3.1.3 Static supply current

Table 3-1-3 Static Supply Current

SYMBOL	Parameter	Device	Typical	Unit
I_{VCC}	Core supply voltage	EAGLEA_05	2	mA
		EAGLEA_10	3	mA
		EAGLEA_20	5	mA
		EAGLEA_50	10	mA
I_{VCCIO}	I/O group power supply, @V CCIO =2.5V	EAGLEA_05	0.2	mA
		EAGLEA_10	0.4	mA
		EAGLEA_20	0.6	mA
		EAGLEA_50	2	mA
		EAGLEA_05	2	mA
		EAGLEA_10	2	mA
I_{VCCAUX}	Auxiliary power	EAGLEA_20	2.5	mA
		EAGLEA_50	3	mA
		EAGLEA_05	2	mA
		EAGLEA_10	3	mA
		EAGLEA_20	5	mA

1. The values in this table are based on common recommended operating conditions and are measured using a typical device at room temperature (TJ = 25 °C).
2. Typical values are blank devices, no output current load, high-impedance state, and all I/O-driven quiescent supply currents measured when all pull-up/pull-down resistors are disabled on the I/O pin.

3.1.4 Hot swap specification

Table 3-1-4 is hot swap specifications

SYMBOL	Parameter	Largest	Unit
$I_{IOPIN(DC)}$	DC current, each I/O	1	mA
$I_{IOPIN(AC)}$	AC current, per I/O	8[1]	mA

1. The power ramp rate is equal to or greater than 10ns.

3.1.5 Power-on reset voltage threshold

Table 3-1-5 Power-on reset voltage threshold

SYMBOL	Parameter	Minimum	Typical	Maximum	Unit
V_{CC_PORUP}	V_{CC} Power-on detection threshold	0.95	1	1.05	V
V_{CCAUX_PORUP}	V_{CCAUX} Power-on detection threshold	2	2.1	2.2	V
V_{CC_PORDN}	VCC power failure detection threshold	—	—	0.9	V
V_{CCAUX_PORDN}	VCCAUX power failure detection threshold	—	—	1.9	V
V_{SRAM_PORDN}	SRAM power failure detection threshold	—	—	0.85	V

3.1.6 I/O DC electrical characteristics

Table 3-1-6 Recommended basic operating conditions

SYMBOL	Parameter	Condition	Minimum	Typical	Maximum	Unit
I_{IL}, I_{IH}	Input leakage current	$0 \leqq V_I \leqq V_{CCIO}$-0.5V	-10	—	10	uA
I_{IH}	Input leakage current	V_{CCIO}-0.5V $\leqq V_I \leqq V_{IH\_MAX}$	—	—	150	uA
I_{PU}	I/O weak pull-up current		35	—	250	uA
I_{PD}	I/O weak pull-down current		35	—	250	uA
I_{BHLS}	Bus hold 0 hold current		40	—	—	uA
I_{BHHS}	Bus hold 1 hold current		40	—	—	uA
I_{BHLO}	Bus hold 0 rewrite current	$0 \leqq V_I \leqq V_{CCIO}$	—	—	350	uA
I_{BHHO}	Bus hold 1 rewrite current	$0 \leqq V_I \leqq V_{CCIO}$	—	—	350	uA
V_{BHT}	Bus hold trigger level	—	V_{IL_max}	—	V_{IH_min}	V
V_{HYST}	Schmitt trigger input hysteresis	V_{CCIO}=3.3V,HYST=Large	—	450	—	mV
		V_{CCIO}=3.3V,HYST=Small	—	250	—	mV
		V_{CCIO}=2.5V,HYST=Large	—	250	—	mV
		V_{CCIO}=2.5V,HYST=Small	—	150	—	mV
		V_{CCIO}=1.8V,HYST=Large	—	125	—	mV
		V_{CCIO}=1.8V,HYST=Small	—	60	—	mV
		V_{CCIO}=1.5V,HYST=Large	—	100	—	mV
		V_{CCIO}=1.5V,HYST=Small	—	40	—	mV

3.1.7 I/O pin capacitance

Table 3-1-7 EAGLE Device Pin Capacitance

SYMBOL	Parameter	QFP	FBGA	Unit
C_{IOTB}	Upper and lower pin input capacitor	7	6	pF
C_{IOLR}	Left and right pin input capacitors	8	7	pF

3.1.8 Single-ended I/O DC characteristics

Table 3-1-8 EAGLE Device Single-Ended I/O Standard Specifications

Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} 最大	V_{OH} 最小	I_{OL}	I_{OH}
	Min	Max	Min	Max	(V)	(V)	(mA)	(mA)
LVTTL33 LVCMOS33	-0.3	0.8	1.9	Vccio+0.3	0.4	V_{CCIO} – 0.4	4	-4
							8	-8
							12	-12
							16	-16
							20	-20
							24	-24
					0.2	V_{CCIO} – 0.2	0.1	-0.1
LVCMOS25	-0.3	0.7	1.7	Vccio+0.3	0.4	V_{CCIO} – 0.4	4	-4
							8	-8
							12	-12
							16	-16
							20	-20
					0.2	V_{CCIO} – 0.2	0.1	-0.1
LVCMOS18	-0.3	0.35*V_{CCIO}	0.65*V_{CCIO}	Vccio+0.3	0.4	V_{CCIO} – 0.4	4	-4
							8	-8
							12	-12
					0.2	V_{CCIO} – 0.2	0.1	-0.1
LVCMOS15	-0.3	0.35*V_{CCIO}	0.65*V_{CCIO}	Vccio+0.3	0.4	V_{CCIO} – 0.4	4	-4
							8	-8
					0.2	V_{CCIO} – 0.2	0.1	-0.1
LVCMOS12	-0.3	0.35*V_{CCIO}	0.65*V_{CCIO}	Vccio+0.3	0.4	V_{CCIO} – 0.4	4	-3
							8	-6
					0.2	V_{CCIO} – 0.2	0.1	-0.1
PCI33	-0.3	0.3*V_{CCIO}	0. 5*V_{CCIO}	Vccio+0.3	0.1*V_{CCIO}	0.9*V_{CCIO}	1.5	-0.5
PCIX33	-0.3	0.35*V_{CCIO}	0. 5*V_{CCIO}	Vccio+0.3	0.1*V_{CCIO}	0.9*V_{CCIO}	1.5	-0.5

表 3-1-9 Single-Ended Interfaces

INPUT STANDARD	VCCIO (TYP.)				
	3.3V	2.5 V	1.8V	1.5V	1.2V
LVTTL33	√	√	√	√	√
LVCMOS33	√	√	√	√	√
LVCMOS25	√ 1	√	√	√	√
LVCMOS18		√ 1	√	√	√
LVCMOS15			√ 1	√	√
LVCMOS12				√ 1	√

Note: 1.Under-drive causes higher DC current when the IO is at logic high

3.1.9 Differential I/O electrical characteristics

Table 3-1-10 Recommended Differential Operating Conditions

Parameter	Description	Test Conditions	Min	Typical	Max	Unit
V_{IP}, V_{IN}	Input level	V_{CCIO}=2.5	0	—	2.4	V
V_{ID}	Input differential swing		150	350		mV
V_{ICM}	Input common mode voltage	V_{CCIO}=2.5	0.05	—	2.35	V
I_{IN}	Input Current	上电过程	—	—	±15	uA
V_{OD}	Standard differential output swing	$\|V_{OP} - V_{ON}\|$, R_T = 100 ohm	150	250	350	mV
V_{OD}	Differential output large swing	$\|V_{OP} - V_{ON}\|$, R_T = 100 ohm	450	480	550	mV
ΔV_{OD}	Differential output swing variation				50	mV
V_{OCM}	Output common mode voltage	$(V_{OP} + V_{ON})/2$, R_T = 100 ohm	0.8	1.2	—	V
ΔV_{OCM}	Output common mode voltage deviation				50	mV

3.1.10 Power monitoring module

Table 3-1-11 Power Monitoring Module Monitoring Level

Level Selection	Monitoring level (V)
1	1.86
2	2.00
3	2.17
4	2.36
5	2.60
6	2.89
7	3.25

3.2 AC electrical characteristics

This section provides performance parameters for the EAGLE core and peripheral modules. The timing parameters and their typical values are important design parameters and are the basic performance parameters of the device. These parameters reflect the actual performance of the device under worst-case conditions.

3.2.1 Clock performance

Table 3-2-1 Recommended maximum clock operating frequency

Device	Speed	Unit
EAGLEA_05	440	MHz
EAGLEA_10	440	MHz
EAGLEA_20	440	MHz
EAGLEA_50	440	MHz

3.2.2 Phase-locked loop (PLL) specifications

Table 3-2-2 PLL Specifications for EAGLE Devices

Parameter	Description	Min	Typical	Max	Unit
f_{IN}	Input clock frequency	10	—	400	MHz
f_{PFD}	Frequency discrimination phase detector (PFD) input frequency	10	—	400	MHz
f_{VCO}	Phase-locked loop internal oscillator frequency range	300	—	1200	MHz
f_{OUT}	Output clock frequency	—	—	400	MHz
Communication characteristics					
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$[1]	Input clock jitter,f_{PFD} ≧ 20 MHz	—	—	800	ps p-p
	Input clock jitter,f_{PFD} < 20 MHz	—	—	0.02	UI
$t_{OUTDUTY}$	Output clock duty cycle	45	50	55	%
$t_{OUTJITTER}$[2]	Output clock period jitter (Period Jitter), f_{OUT} > 100MHz	—	—	160	ps p-p
	Output clock period jitter (Period Jitter), f_{OUT} < 100MHz	—	—	0.009	UI
	Output Clock Cycle-to-cycle Jitter, f_{OUT} > 100MHz	—	—	200	ps p-p
	Output Clock Cycle-to-cycle Jitter, f_{OUT} < 100MHz	—	—	0.01	UI
	Output Clock Phase Jitter, f_{OUT} > 100MHz	—	—	180	ps p-p
	Output Clock Phase Jitter, f_{OUT} < 100MHz	—	—	0.013	UI
t_{LOCK}[3]	PLL lock time	—	—	15	ms
t_{DLOCK}	Dynamic lock time (after switching, reconfiguration)	—	—	15	ms
t_{PLL_PS}	PLL phase shift accuracy	—	—	±125	ps
t_{RST}	Reset pulse minimum width	1	—	—	ns
t_{RSTREC}	Reset recovery time	1	—	—	ns

$t_{CONFIGPLL}$	PLL phase dynamic configuration time	—	3.5	—	cycles
$f_{SCANCLK}$	SCANCLK frequency	—	—	100	MHz

1. The maximum input jitter allowed by the reference clock. In order to get a low jitter output clock, a clean reference clock must be provided.

2. The period jitter is obtained by sampling 10,000 measurements of the PLL output. The jitter is sampled 1000 times between adjacent periods. Phase jitter is sampled 2000 times. The reference clock is jittered at 30ps.

3. After tLOCK, a stable clock is obtained at the output.

3.2.3 Embedded Digital Signal Processing Module (DSP) Specifications

Table 3-2-3 EAGLE Embedded DSP Specification Sheet

Mode	Performance			Unit
	6	7	8	
M9×9(All registers)	400	350	320	MHz
M18×18(All registers)	400	350	320	MHz

3.2.4 Memory Module (BRAM) Specifications

Table 3-2-4 EAGLE Memory Module Specification Sheet

Memory	Mode	Performance			Unit
		6	7	8	
M9K	FIFO 512 x 18	250	220	200	MHz
	Single port 512 x 18	250	220	200	MHz
	Simple dual-port 512 x 18	250	220	200	MHz
	True dual-port 1024 x 9	250	220	200	MHz

3.2.5 High-speed I/O interface performance

Table 3-2-5 High-speed I/O interface performance table

Input/output standard	Description	Max	Unit
Maximum input frequency			
LVDS25	LVDS, VCCIO = 2.5V	400	MHz
RSDS25	RSDS, VCCIO = 2.5V	400	MHz
MINILVDS	Mini-LVDS, VCCIO = 2.5V	400	MHz

PPDS25	PPDS	400	MHz
LVPECL33	LVPECL, VCCIO = 3.3V	400	MHz
BLVDS25	BLVDS, VCCIO = 2.5V	400	MHz
MLVDS25	MLVDS, VCCIO = 2.5V	400	MHz
LVTTL33	LVTTL, VCCIO = 3.3V	166	MHz
LVCMOS33	LVCMOS, VCCIO = 3.3V	166	MHz
LVCMOS25	LVCMOS, VCCIO = 2.5V	166	MHz
LVCMOS18	LVCMOS, VCCIO = 1.8V	166	MHz
LVCMOS15	LVCMOS, VCCIO = 1.5V	166	MHz
LVCMOS12	LVCMOS, VCCIO = 1.2V	166	MHz
PCI33		133	MHz
Maximum output frequency			
LVDS25	LVDS, VCCIO = 2.5V	400	MHz
LVDS25E	LVDS, Emulated, VCCIO = 2.5V	166	MHz
RSDS25	RSDS, VCCIO = 2.5V	400	MHz
RSDS25E	RSDS, Emulated, VCCIO = 2.5V	166	MHz
MINILVDS	MINILVDS , VCCIO = 2.5V	400	MHz
MINILVDS25E	Mini-LVDS, Emulated, VCCIO = 2.5V	166	MHz
PPDS	Ponit-to-ponit LVDS	400	MHz
LVPECL33E	LVPECL, Emulated, VCCIO = 3.3V	166	MHz
BLVDS25E	BLVDS, Emulated, VCCIO = 2.5V	166	MHz
MLVDS25E	MLVDS, Emulated, VCCIO = 2.5V	166	MHz
LVTTL33	LVTTL, VCCIO = 3.3V	166	MHz
LVCMOS33	LVCMOS, VCCIO = 3.3V	166	MHz
LVCMOS25	LVCMOS, VCCIO = 2.5V	166	MHz
LVCMOS18	LVCMOS, VCCIO = 1.8V	166	MHz
LVCMOS15	LVCMOS, VCCIO = 1.5V	166	MHz
LVCMOS12	LVCMOS, VCCIO = 1.2V	100	MHz
PCI33		133	MHz

3.2.6 Configuration module and JTAG specifications

Table 3-2-6 EAGLE Device Configuration Mode Timing Specifications

Download mode	Min	Typical	Max	Unit
Main mode serial PROM (MS)	2.5	—	66	MHz
Main mode serial SPI (MSPI)	2.5	—	66	MHz
Main mode parallel x8 (MP)	2.5	—	66	MHz
Slave mode serial (SS)	—	66	—	MHz
Slave mode parallel x8 (SP)	—	66	—	MHz

Table 3-2-7 EAGLE Device JTAG Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
t_{JCP}	TCK cycle	40	—	ns
t_{JCH}	TCK high time	20	—	ns
t_{JCL}	TCK low time	20	—	ns
t_{JPSU_TDI}	TDI setup time	1	—	ns
t_{JPSU_TMS}	TMS setup time	3	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output delay	—	15	ns
t_{JPZX}	JTAG port valid output to high-impedance conversion time	—	15	ns
t_{JPXZ}	Capture register setup time	—	15	ns
t_{JSSU}	Grab register hold time	5	—	ns
t_{JSH}	Update register setup time	10	—	ns
t_{JSCO}	Update register clock to output delay	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high resistance	—	25	ns

3.2.7 ADC performance

Table 3-2-8 ADC Performance

Parameter	Performance
Operating Voltage	3.3V analog power supply and 3.3V digital power supply
Highest sampling rate	1Mhz
Number of channels	8
Sampling range	0.01*VREF ~ 0.99*VREF
Dynamic performance	>81Db SFDR >62Db SINAD
Linearity performance	INL<1 LSB,DNL<0.5 LSB
Highest clock frequency	16Mhz

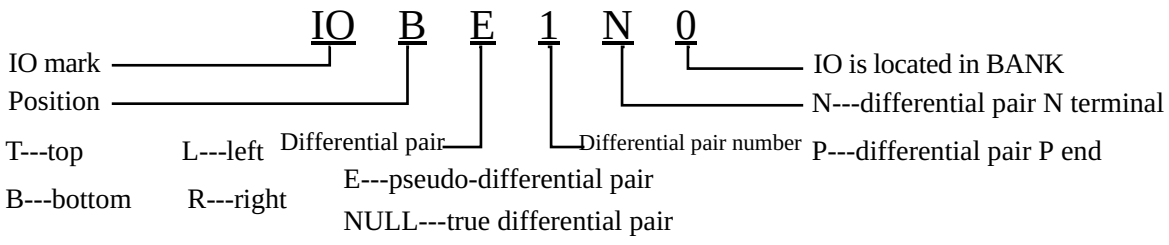
4 Pin and package

4.1 Pin definitions and rules

Table 4-1-1 Pin Definition Rules

Pin name	Direction	Description
Normal I/O		
NC	—	no connection
GND	—	Power ground
VCC	—	Internal core module power supply
VCCIOx	—	I/O group power supply
VCCAUX	—	Auxiliary power
VCC_PLLX	—	PLL power supply
GND_PLLx	—	PLL ground
JTAG dedicated pin		
TCK	Input	TCK input boundary scan clock
TDI	Input	Boundary scan data input
TDO	Output	Boundary scan data output
TMS	Input	Boundary scan mode selection
Configure dedicated pins		
CSN	Input	Parallel download mode chip select signal, low effective
MSEL[2:0]	Input	Download mode selection
PROGRAMN	Input	Global reset input, low effective
CCLK	I/O	
DONE	I/O	Dedicated configuration status pin, output high after configuration, open source
INITN	I/O	Dedicated configuration status pin, high output indicates that the FPGA is ready for configuration, the source is open
ADC function pin		
ADC_CHx	Input	ADC analog signal input
ADC_VREF	Input	ADC reference voltage
ADC_VDDA	Input	ADC analog power supply
ADC_VDDD	Input	ADC digital power supply

4.2 IO naming rules



4.3 EG4X20BG256 Pin Description

Numbering	BANK	Pin description		Numbering	BANK	Pin description
C4	0	IO_BE1P_HSWAPEN_0		F9	0	IO_BE15P_0
A4	0	IO_BE1N_VREF_0		D9	0	IO_BE15N_0
B5	0	IO_BE2P_0		B12	0	IO_BE16P_0
A5	0	IO_BE2N_0		A12	0	IO_BE16N_VREF_0
D5	0	IO_BE3P_GPLL3_OUTP_0		C13	0	IO_BE17P_0
C5	0	IO_BE3N_GPLL3_OUTN_0		A13	0	IO_BE17N_0
B6	0	IO_BE4P_0		F10	0	IO_BE18P_0
A6	0	IO_BE4N_0		E11	0	IO_BE18N_0
F7	0	IO_BE5P_0		B14	0	IO_BE19P_GPLL0_CLKIN0_0
E6	0	IO_BE5N_0		A14	0	IO_BE19N_GPLL0_CLKIN1_0
C7	0	IO_BE6P_0		D11	0	IO_BE20P_GPLL0_OUTP_0
A7	0	IO_BE6N_0		D12	0	IO_BE20N_GPLL0_OUTN_0
D6	0	IO_BE7P_0				
C6	0	IO_BE7N_0				
B8	0	IO_BE8P_0				
A8	0	IO_BE8N_0				
C9	0	IO_BE9P_GCLKIOB_7_0				
A9	0	IO_BE9N_GCLKIOB_6_0				
B10	0	IO_BE10P_GCLKIOB_5_0				
A10	0	IO_BE10N_GCLKIOB_4_0				
E7	0	IO_BE11P_GCLKIOB_3_0				
E8	0	IO_BE11N_GCLKIOB_2_0				
E10	0	IO_BE12P_GCLKIOB_1_0				
C10	0	IO_BE12N_GCLKIOB_0_0				
D8	0	IO_BE13P_0				
C8	0	IO_BE13N_VREF_0				
C11	0	IO_BE14P_0				
A11	0	IO_BE14N_0				

Numbering	BANK	Pin description		Numbering	BANK	Pin description
E13	1	IO_L1P_1		K14	1	IO_L14N_GCLKIOL_4_1
E12	1	IO_L1N_VREF_1		K12	1	IO_L15P_GCLKIOL_3_1
B15	1	IO_L2P_1		K11	1	IO_L15N_GCLKIOL_2_1
B16	1	IO_L2N_1		J14	1	IO_L16P_GCLKIOL_1_1
F12	1	IO_L3P_1		J16	1	IO_L16N_GCLKIOL_0_1
G11	1	IO_L3N_1		K15	1	IO_L17P_1
D14	1	IO_L4P_1		K16	1	IO_L17N_1
D16	1	IO_L4N_1		N14	1	IO_L18P_1
F13	1	IO_L5P_1		N16	1	IO_L18N_1
F14	1	IO_L5N_1		M15	1	IO_L19P_1
C15	1	IO_L6P_1		M16	1	IO_L19N_1
C16	1	IO_L6N_1		L14	1	IO_L20P_1
E15	1	IO_L7P_1		L16	1	IO_L20N_1
E16	1	IO_L7N_1		P15	1	IO_L21P_1
F15	1	IO_L8P_1		P16	1	IO_L21N_1
F16	1	IO_L8N_1		R15	1	IO_L22P_1
G14	1	IO_L9P_1		R16	1	IO_L22N_1
G16	1	IO_L9N_1		R14	1	IO_L23P_1
H15	1	IO_L10P_1		T15	1	IO_L23N_1
H16	1	IO_L10N_1		T14	1	IO_L24P_1
G12	1	IO_L11P_1		T13	1	IO_L24N_1
H11	1	IO_L11N_1		R12	1	IO_L25P_1
H13	1	IO_L12P_1		T12	1	IO_L25N_1
H14	1	IO_L12N_1		L12	1	IO_L26P_1
J11	1	IO_L13P_GCLKIOL_7_1		L13	1	IO_L26N_VREF_1
J12	1	IO_L13N_GCLKIOL_6_1		M13	1	IO_AWAKE_1
J13	1	IO_L14P_GCLKIOL_5_1		M14	1	IO_DOUT_BUSY_1

Numbering	BANK	Pin description		Numbering	BANK	Pin description
R11	2	IO_CCLK_2		R5	2	IO_TE14P_D7_2
T11	2	IO_M0_2		T5	2	IO_TE14N_VREF_2
M12	2	IO_TE2P_GPLL1_CLKIN0_ADC_CH4_2		N5	2	IO_TE15P_D3_2
M11	2	IO_TE2N_GPLL1_CLKIN1_ADC_CH7_2		P5	2	IO_TE15N_D4_2
P10	2	IO_D0_DIN_MISO_2		L8	2	IO_TE16P_D5_2
T10	2	IO_MOSI_CSI_B_2		L7	2	IO_TE16N_D6_2
N12	2	IO_TE4P_ADC_CH5_D1_2		P4	2	IO_TE17P_2
P12	2	IO_TE4N_ADC_CH6_D2_2		T4	2	IO_TE17N_2
N11	2	IO_TE5P_M1_ADC_CH0_2		M6	2	IO_TE18P_2
P11	2	IO_TE5N_ADC_CH2_VERF_2		N6	2	IO_TE18N_2
N9	2	IO_TE6P_2		R3	2	IO_INIT_B_2
P9	2	IO_TE6N_2		T3	2	IO_CSO_B_2
L10	2	IO_TE7P_ADC_CH1_2				
M10	2	IO_TE7N_ADC_CH3_2				
R9	2	IO_TE8P_2				
T9	2	IO_TE8N_2				
M9	2	IO_TE9P_GCLKIOT_3_2				
N8	2	IO_TE9N_GCLKIOT_2_2				
P8	2	IO_TE10P_GCLKIOT_1_2				
T8	2	IO_TE10N_GCLKIOT_0_2				
P7	2	IO_TE11P_GCLKIOT_7_2				
M7	2	IO_TE11N_GCLKIOT_6_2				
R7	2	IO_TE12P_GCLKIOT_5_2				
T7	2	IO_TE12N_GCLKIOT_4_2				
P6	2	IO_TE13P_2				
T6	2	IO_TE13N_2				

Numbering	BANK	Pin description		Numbering	BANK	Pin description
M4	3	IO_R1P_3		H5	3	IO_R14N_GCLKIOR_2_3
M3	3	IO_R1N_VREF_3		H4	3	IO_R15P_GCLKIOR_1_3
M5	3	IO_R2P_3		H3	3	IO_R15N_GCLKIOR_0_3
N4	3	IO_R2N_3		L4	3	IO_R16P_3
R2	3	IO_R3P_GPLL2_CLKIN0_3		L5	3	IO_R16N_3
R1	3	IO_R3N_GPLL2_CLKIN1_3		E2	3	IO_R17P_3
P2	3	IO_R4P_3		E1	3	IO_R17N_3
P1	3	IO_R4N_3		K5	3	IO_R18P_3
N3	3	IO_R5P_3		K6	3	IO_R18N_3
N1	3	IO_R5N_3		C3	3	IO_R19P_3
M2	3	IO_R6P_3		C2	3	IO_R19N_3
M1	3	IO_R6N_3		D3	3	IO_R20P_3
L3	3	IO_R7P_3		D1	3	IO_R20N_3
L1	3	IO_R7N_3		C1	3	IO_R21P_3
K2	3	IO_R8P_3		B1	3	IO_R21N_3
K1	3	IO_R8N_3		G6	3	IO_R22P_3
J3	3	IO_R9P_3		G5	3	IO_R22N_3
J1	3	IO_R9N_3		B2	3	IO_R23P_3
H2	3	IO_R10P_3		A2	3	IO_R23N_3
H1	3	IO_R10N_3		F4	3	IO_R24P_3
G3	3	IO_R11P_3		F3	3	IO_R24N_3
G1	3	IO_R11N_3		E4	3	IO_R25P_3
F2	3	IO_R12P_GCLKIOR_7_3		E3	3	IO_R25N_3
F1	3	IO_R12N_GCLKIOR_6_3		F6	3	IO_R26P_3
K3	3	IO_R13P_GCLKIOR_5_3		F5	3	IO_R26N_3
J4	3	IO_R13N_GCLKIOR_4_3		B3	3	IO_R27P_3
J6	3	IO_R14P_GCLKIOR_3_3		A3	3	IO_R27N_3

Numbering	BANK	Pin description		Numbering	BANK	Pin description
P13	1	IO_DONE		L9	-	VCCAUX
T2	2	IO_PROGRAM_B		G7	-	VCCINT
P14	1	IO		G9	-	VCCINT
C14	0	TCK		H10	-	VCCINT
C12	0	TDI		H8	-	VCCINT
E14	1	TDO		J7	-	VCCINT
A15	1	TMS		J9	-	VCCINT
L11	-	ADC_VREF		K10	-	VCCINT
B13	-	VCCO_0		K8	-	VCCINT
B4	-	VCCO_0		A1		GND
B9	-	VCCO_0		A16		GND
D10	-	VCCO_0		B11		GND
D7	-	VCCO_0		B7		GND
D15	-	VCCO_1		D13		GND
G13	-	VCCO_1		D4		GND
J15	-	VCCO_1		E9		GND
K13	-	VCCO_1		G15		GND
N15	-	VCCO_1		G2		GND
R13	-	ADC_VDDA		G8		GND
N10	-	VCCO_2		H12		GND
N7	-	VCCO_2		H7		GND
R4	-	VCCO_2		H9		GND
R8	-	VCCO_2		J5		GND
D2	-	VCCO_3		J8		GND
G4	-	VCCO_3		K7		GND
J2	-	VCCO_3		K9		GND
K4	-	VCCO_3		L15		GND
N2	-	VCCO_3		L2		GND
E5	-	VCCAUX		M8		GND

F11	-	VCCAUX		N13	-	GND
F8	-	VCCAUX		P3	-	GND
G10	-	VCCAUX		R10		GND
H6	-	VCCAUX		R6		GND
J10	-	VCCAUX		T1		GND
L6	-	VCCAUX		T16		GND

Note 1: The ADC module is located on the chip BANK2. The ADC_VDDD is fixedly connected to VCCIO2 inside the chip. When using the ADC, the BANK2 voltage should not be lower than the ADC analog supply voltage.

Note 2: When sel_pwr =0, the power monitoring module monitors BANK1. When sel_pwr =1, the voltage of BANK2 is monitored.

4.4 EG4A20BG256 Pin Description

Numbering	BANK	Pin description		Numbering	BANK	Pin description
D4	1	IO_L1P_1		M2	2	IO_L1P_GCLKIOL_5_2
B1	1	IO_L1N_1		M1	2	IO_L1N_GCLKIOL_4_2
C1	1	IO_L_MOSI_1		J1	2	IO_L2N_GCLKIOL_6_2
C2	1	IO_L_1		J2	2	IO_L2P_GCLKIOL_7_2
E5	1	IO_L3P_1		K1	2	IO_L3N_2
F5	1	IO_L3N_1		K2	2	IO_L3P_2
D1	1	IO_L_1		J6	2	IO_L_2
D2	1	IO_SPICSN_1		L1	2	IO_L4N_2
G5	1	IO_L5P_1		L2	2	IO_L4P_2
G4	1	IO_L5N_1		L3	2	IO_L5N_VREF_2
F4	1	IO_INITN_1		R1	2	IO_L5P_2
F3	1	IO_VREF_1		K5	2	IO_L6N_2
F2	1	IO_L7P_1		L4	2	IO_L6P_2
F1	1	IO_L7N_1		N1	2	IO_L7N_2
H3	1	IO_L8P_TCK_1		N2	2	IO_L7P_2
H4	1	IO_L8N_TDI_1		L6	2	IO_L8N_2
H5	1	IO_L9N_PROGRAMN_1		K6	2	IO_L8P_2
J5	1	IO_L9P_TMS_1		N4	2	IO_L_2
H2	1	IO_L_DATA0_1		P2	2	IO_L9P_2
H1	1	IO_L_CCLK_1		P1	2	IO_L9N_2
J3	1	IO_L11N_Nce_1				
J4	1	IO_L11P_TDO_1				
G2	1	IO_L12P_GCLKIOL_3_1				
G1	1	IO_L12N_GCLKIOL_2_1				
E1	1	IO_GCLKIOL_0_1				

Numbering	BANK	Pin description		Numbering	BANK	Pin description
P3	3	IO_BE1N_GPLL0_CLKIN1_3		R8	4	IO_BE1P_GCLKIOB_7_4
N3	3	IO_BE1P_GPLL0_CLKIN0_3		T8	4	IO_BE1N_GCLKIOB_6_4
M6	3	IO_BE2P_3		T9	4	IO_BE2N_GCLKIOB_2_4
L7	3	IO_BE2N_3		R9	4	IO_BE2P_GCLKIOB_3_4
P6	3	IO_BE3N_3		R10	4	IO_BE3P_4
T2	3	IO_BE3P_3		T10	4	IO_BE3N_4
R3	3	IO_BE4P_3		P9	4	IO_BE4N_4
T3	3	IO_BE4N_3		P11	4	IO_BE4P_4
T4	3	IO_BE5N_GPLL0_OUTN_3		M9	4	IO_BE5P_4
R4	3	IO_BE5P_GPLL0_OUTP_3		N9	4	IO_BE5N_4
N6	3	IO_BE6N_3		L9	4	IO_BE6N_4
N5	3	IO_BE6P_3		K9	4	IO_BE6P_4
R5	3	IO_BE7P_3		T11	4	IO_BE7N_4
T5	3	IO_BE7N_3		R11	4	IO_BE7P_4
T6	3	IO_BE8N_3		M10	4	IO_BE8P_4
R6	3	IO_BE8P_3		N11	4	IO_BE8N_4
R7	3	IO_BE9P_3		L10	4	IO_BE9N_4
T7	3	IO_BE9N_3		K10	4	IO_BE9P_4
K8	3	IO_BE10N_3		T12	4	IO_BE10N_GPLL3_OUTN_4
M7	3	IO_BE10P_3		R12	4	IO_BE10P_GPLL3_OUTP_4
N8	3	IO_BE11P_GCLKIOB_1_3		R13	4	IO_BE11P_4
P8	3	IO_BE11N_GCLKIOB_0_3		T13	4	IO_BE11N_4
M8	3	IO_BE12N_GCLKIOB_4_3		N12	4	IO_BE12N_4
L8	3	IO_BE12P_GCLKIOB_5_3		M11	4	IO_BE12P_4
				T14	4	IO_BE13P_4
				T15	4	IO_BE13N_4
				L11	4	IO_BE14N_4
				P14	4	IO_BE14P_4

Numbering	BANK	Pin description		Numbering	BANK	Pin description
R14	5	IO_R1N_GPLL3_CLKIN1_5		H15	6	IO_R1P_GCLKIOR_3_6
P15	5	IO_R1P_GPLL3_CLKIN0_5		H16	6	IO_R1N_GCLKIOR_2_6
R16	5	IO_R2P_5		E16	6	IO_R2N_GCLKIOR_4_6
P16	5	IO_R2N_5		E15	6	IO_R2P_GCLKIOR_5_6
N13	5	IO_R3N_5		G15	6	IO_R3P_6
N14	5	IO_R3P_5		G16	6	IO_R3N_6
N15	5	IO_R4P_5		H13	6	IO_R_MSEL0_6
N16	5	IO_R4N_5		H14	6	IO_R_DONE_6
M12	5	IO_R5P_5		G12	6	IO_R5P_MSEL2_6
L12	5	IO_R5N_5		H12	6	IO_R5N_MSEL1_6
L13	5	IO_R6P_5		F15	6	IO_R_6
L14	5	IO_R6N_5		F16	6	IO_R_DOUT_6
L15	5	IO_R7P_5		F13	6	IO_R7P_6
L16	5	IO_R7N_5		G11	6	IO_R7N_6
K15	5	IO_R8P_5		D16	6	IO_R8N_6
K16	5	IO_R8N_5		D15	6	IO_R8P_6
J11	5	IO_R9P_5		C16	6	IO_R9N_6
K11	5	IO_R9N_5		C15	6	IO_R9P_6
K12	5	IO_R10P_5		B16	6	IO_R10N_6
J13	5	IO_R10N_5		F14	6	IO_R10P_VREF_6
J12	5	IO_R11P_5		D13	6	IO_R_6
J14	5	IO_R11N_5		A15	6	IO_R11P_GPLL2_CLKIN0_6
J15	5	IO_R12P_GCLKIOR_7_5		F11	6	IO_R11N_GPLL2_CLKIN1_6
J16	5	IO_R12N_GCLKIOR_6_5				
M16	5	IO_R13N_GCLKIOR_0_5				
M15	5	IO_R13P_GCLKIOR_1_5				

Numbering	BANK	Pin description		Numbering	BANK	Pin description
D14	7	IO_TE1P_7		A9	7	IO_TE14N_GCLKIOT_6_7
C14	7	IO_TE1N_7		A8	7	IO_TE15N_GCLKIOT_4_7
A14	7	IO_TE2N_GPLL2_OUTN_7		B8	7	IO_TE15P_GCLKIOT_5_7
B14	7	IO_TE2P_GPLL2_OUTP_7		B6	7	IO_TE16P_GCLKIOT_1_7
B13	7	IO_TE3P_7		A6	7	IO_TE16N_GCLKIOT_0_7
A13	7	IO_TE3N_7		E8	7	IO_TE17N_D2_GCLKIOT_2_7
D11	7	IO_TE4N_7		F8	7	IO_TE17P_D3_GCLKIOT_3_7
D12	7	IO_TE4P_7		A5	8	IO_TE1P_D7_8
B12	7	IO_TE5P_7		C6	8	IO_TE1N_8
A12	7	IO_TE5N_7		E7	8	IO_TE2N_D5_8
C11	7	IO_TE6P_VREF_7		E6	8	IO_TE2P_D6_8
E11	7	IO_TE6N_7		D6	8	IO_TE3P_8
A11	7	IO_TE7N_7		D5	8	IO_TE3N_8
B11	7	IO_TE7P_7		F6	8	IO_TE4N_GPLL1_OUTN_8
B10	7	IO_TE8P_7		F7	8	IO_TE4P_GPLL1_OUTP_8
A10	7	IO_TE8N_7		B4	8	IO_TE5P_ADC_CH1_8
F10	7	IO_TE9N_7		A4	8	IO_TE5N_ADC_CH3_8
F9	7	IO_TE9P_7		A3	8	IO_TE6N_ADC_CH2_8
E10	7	IO_TE10P_7		B3	8	IO_TE6P_ADC_CH0_8
E9	7	IO_TE10N_7		E2	8	ADC_VREF
C9	7	IO_TE11N_7		B5	8	IO_TE7P_ADC_CH5_8
D9	7	IO_TE11P_7		A2	8	IO_TE7N_ADC_CH7_8
B7	7	IO_TE12P_D4_7		C3	8	IO_TE8N_GPLL1_CLKIN1_ADC_CH6_8
A7	7	IO_TE12N_7		D3	8	IO_TE8P_GPLL1_CLKIN0_ADC_CH4_8
C8	7	IO_TE13N_7				
D8	7	IO_TE13P_7				
B9	7	IO_TE14P_GCLKIOT_7_7				

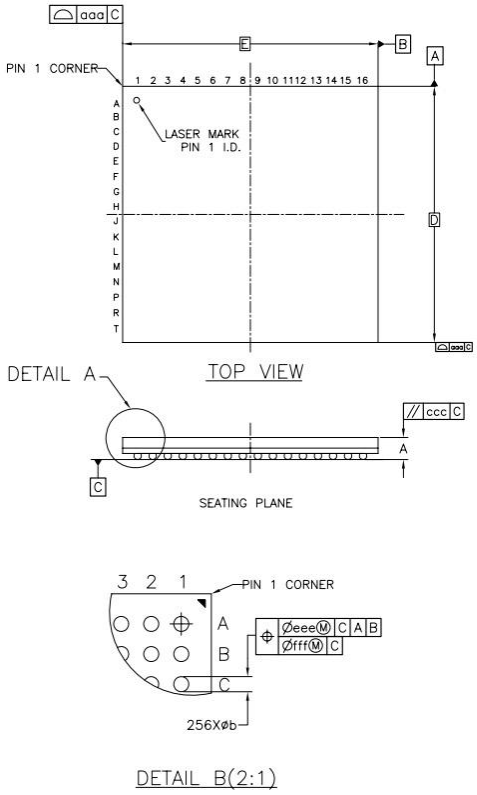
Numbering	BANK	Pin description		Numbering	BANK	Pin description
B2	-	GND		F12	-	VCCAUX
B15	-	GND		L5	-	VCCAUX
C12	-	GND		G6	-	VCCINT
D7	-	ADC_VSSA		G7	-	VCCINT
D10	-	GND		G8	-	VCCINT
E4	-	GND		G9	-	VCCINT
E13	-	GND		G10	-	VCCINT
G13	-	GND		H6	-	VCCINT
H7	-	GND		H11	-	VCCINT
H8	-	GND		K7		VCCINT
H9	-	GND		E3	-	VCCIO1
H10	-	GND		G3	-	VCCIO1
J7	-	GND		K3	-	VCCIO2
J8	-	GND		M3	-	VCCIO2
J9	-	GND		P4	-	VCCIO3
J10	-	GND		P7	-	VCCIO3
K4	-	GND		T1	-	VCCIO3
K13	-	GND		P10	-	VCCIO4
M4	-	GND		P13	-	VCCIO4
N7	-	GND		T16	-	VCCIO4
N10	-	GND		K14	-	VCCIO5
P5	-	GND		M14	-	VCCIO5
P12	-	GND		E14	-	VCCIO6
R2	-	GND		G14	-	VCCIO6
R15	-	GND		A16	-	VCCIO7
M5	-	GND_PLLA0		C10	-	VCCIO7
E12	-	GND_PLLA2		C13	-	VCCIO7
C5		GND_PLLA1		C4	-	VCCIO8
M13		GND_PLLA3		C7	-	VCCIO8
	-			A1	-	ADC_VDDA

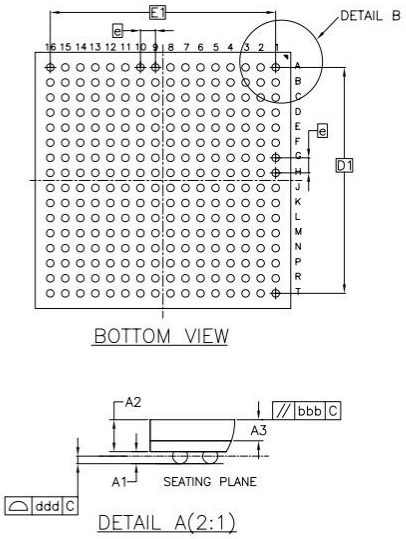
Note 1: The ADC module is located on the chip BANK8. The ADC_VDDD is fixedly connected to VCCIO8 inside the chip. When using the ADC, the BANK8 voltage should not be lower than the ADC analog power supply voltage.

Note 2: When sel_pwr =0, the power monitoring module monitors BANK1. When sel_pwr =1, the voltage of BANK8 is monitored.

4.5 Package information

4.5.1 FBGA256 package specifications





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	1.46	1.56
A1	0.35	0.40	0.45
A2	1.02	1.06	1.10
A3		0.70 BASIC	
D	16.90	17.00	17.10
D1		15.00 BASIC	
E	16.90	17.00	17.10
E1		15.00 BASIC	
e		1.00 BASIC	
b	0.45	0.50	0.55
aaa		0.10	
bbb		0.20	
ccc		0.20	
ddd		0.12	
eee		0.15	
fff		0.08	

5 Ordering Information

Table 5- 1 Device Number Abbreviation

Device name	category	Lookup table capacity	Package type	Temperature class
EAGLE	A	10	BG256	C

- 产品系列
  - ✧ EAGLE 系列
- 类别
  - ✧ A A 型 IO 布局
  - ✧ X X 型 IO 布局
  - ✧ L L 型 IO 布局
- 查找表容量
  - ✧ 05 5K 查找表
  - ✧ 10 10K 查找表
  - ✧ 20 20K 查找表
  - ✧ 50 50K 查找表
- 封装类型：<类型><#>
  - ✧ LG LQFP，lead free
  - ✧ BG FBGA，substrate
  - ✧ # 引脚数（256 指 256 个引脚）
- 温度等级
  - ✧ C 商业（TJ = 0 – 85 ℃）
  - ✧ I 工业（TJ = -40 – 100 ℃）

器件名称

EAGLE FPGA

类型

A A 型 IO 布局

X X 型 IO 布局

L L 型 IO 布局

查找表容量

05 5K 查找表

10 10K 查找表

20 20K 查找表

50 50K 查找表

封装类型

LG LQFP

BG FBGA

温度等级

C 商业（TJ= 0 - 85℃）

I 工业（TJ= -40 - 100℃）

6 版本信息

日期	版本	修订记录
05/04/2016	1.0	首次发布中文版
11/11/2016	1.1	更新封装信息
7/12/2016	1.2	更新 ADC 特殊功能引脚说明
15/02/2017	1.3	更新封装信息
09/03/2017	1.4	更新配置模块信息
02/05/2017	1.5	改正 RAM 信息错误，改正配置波形错误
05/14/2017	1.6	改正 A 封装 LVDS 对标示错误
26/05/2017	1.7	改正 A 封装部分 IO 标示错误
01/09/2017	1.8	完善 ADC IP 相关时序图
14/11/2017	1.9	改正双功能引脚的 LVDS 电平可用性错误
23/05/2018	2.0	修正 EG4X20 器件的引脚表错误
28/05/2018	2.1	删除速度等级的描述
06/06/2018	2.2	添加 ADC 所在 BANK 电压要求等功能描述
21/06/2018	2.3	修改文档格式
10/07/2018	2.4	修改了 IOB 简介部分的描述，删除了 144 封装的说明
07/08/2018	2.5	删除 MS 配置说明
10/08/2018	2.6	修正引脚标识
30/08/2018	2.7	添加动态相移时钟与脉宽说明
06/09/2018	2.8	文档格式统一化，增加 PLL 使用建议、IO 引脚在配置过程中的状态等

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