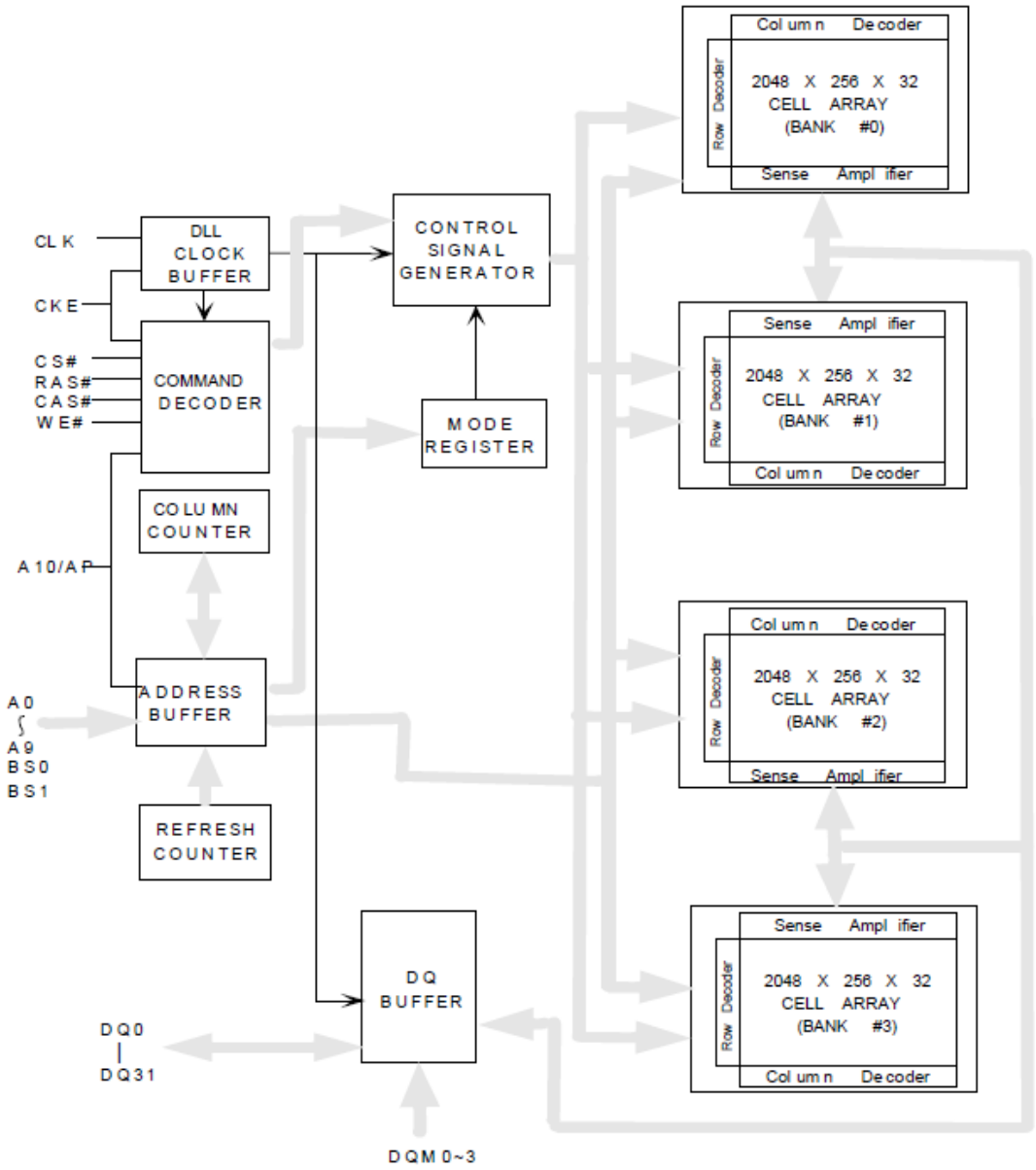
4. EG4S20 internal SDRAM

EG4S20 embeds a piece of 2M x 32bit SDRAM (EM638325), the highest operating frequency is 200Mhz, and the maximum read and write bandwidth up to 800MB/s. It is internally configured as a quad 512K x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK).

Each of the 512K x 32 bit banks is organized as 2048 rows by 256 columns by 32 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command.

The SDRAM provides for programmable Read or Write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. By having a programmable mode register, the system can choose the most suitable modes to maximize its performance.

Block Diagram



SDRAM and FPGA are deeply integrated through software, so if you want to use SDRAM, you only need to use IP generate Instantiate, or instantiate the following IP module at the top level. The prototype of the IP is as follows:

```
EG_PHY_SDRAM_2M_32    inst_EG_PHY_SDRAM_2M_32(
        .clk(SD_CLK),              // SDRAM clock 1bit width
        .ras_n(SD_RAS_N),          // SDRAM row strobe 1bit width
        .cas_n(SD_CAN_N),          // SDRAM column strobe 1bit width
        .we_n(SD_WE_N),            // SDRAM write enable 1bit width
        .addr(SD_SA),              // SDRAM address 11bits width
        .ba(SD_BA),                // SDRAM BANK address 2bits width
        .dq(SD_DQ),                // SDRAM data 32bits bit width
        .cke(SD_CKE),              // SDRAM clock enable 1bit width
        .dm(4'b0)                  // SDRAM data mask 4bit width
        );
```

Table 4-1 SDRAM AC parameter

Symbol	AC parameter	min	max	Unit
t.CL	CAS# Latency	3	-	CLK
t.WR	Write recovery time	2	-	
t.CCD	CAS# to CAS# delay time	2	-	
t.MRD	Mode Register Set cycle time	2	-	
t.RFC	Refresh cycle time (same bank)	55	-	ns
t.RRD	Row activate to row activate delay (different banks)	10	-	
t.RCD	RAS# to CAS# delay (same bank)	18	-	
t.RP	Precharge to refresh/row activate command (same bank)	15	-	
t.RAS	Row activate precharge time (same bank)	35	100000	
t.CK	Clock cycle time	5	-	
t.AC	Access time from CLK (positive edge)	-	4.5	
t.OH	Data output hold time	2	-	
t.CH	Clock high time	2	-	
t.CL	Clock low time	2	-	
t.IS	Data/Address/Control input set-up time	1.5	-	
t.IH	Data/Address/Control input hold time	1	-	
t.LZ	Data output low impedance time	1	-	
t.HZ	Data output high impedance time	4.5	-	

Table 4-2 SDRAM pin assignment

SDRAM pin name	SDRAM pin description	pin connection
DQ0	Data pin 0	Connect with IP
DQ1	Data pin 1	Connect with IP
DQ2	Data pin 2	Connect with IP
DQ3	Data pin 3	Connect with IP
DQ4	Data pin 4	Connect with IP
DQ5	Data pin 5	Connect with IP
DQ6	Data pin 6	Connect with IP
DQ7	Data pin 7	Connect with IP
DQ8	Data pin 8	Connect with IP
DQ9	Data pin 9	Connect with IP
DQ10	Data pin 10	Connect with IP
DQ11	Data pin 11	Connect with IP
DQ12	Data pin 12	Connect with IP
DQ13	Data pin 13	Connect with IP
DQ14	Data pin 14	Connect with IP
DQ15	Data pin 15	Connect with IP
DQ16	Data pin 16	Connect with IP
DQ17	Data pin 17	Connect with IP
DQ18	Data pin 18	Connect with IP
DQ19	Data pin 19	Connect with IP
DQ20	Data pin 20	Connect with IP
DQ21	Data pin 21	Connect with IP
DQ22	Data pin 22	Connect with IP
DQ23	Data pin 23	Connect with IP
DQ24	Data pin 24	Connect with IP
DQ25	Data pin 25	Connect with IP
DQ26	Data pin 26	Connect with IP
DQ27	Data pin 27	Connect with IP
DQ28	Data pin 28	Connect with IP
DQ29	Data pin 29	Connect with IP
DQ30	Data pin 30	Connect with IP
DQ31	Data pin 31	Connect with IP
SA0	Address pin 0	Connect with IP
SA1	Address pin 1	Connect with IP
SA2	Address pin 2	Connect with IP
SA3	Address pin 3	Connect with IP
SA4	Address pin 4	Connect with IP
SA5	Address pin 5	Connect with IP
SA6	Address pin 6	Connect with IP
SA7	Address pin 7	Connect with IP
SA8	Address pin 8	Connect with IP
SA9	Address pin 9	Connect with IP
SA10	Address pin 10	Connect with IP
BA0	BANK address pin 0	Connect with IP

BA1	BANK address pin 1	Connect with IP
WE_N	Write enable	Connect with IP
RAS_N	Row strobe	Connect with IP
CAS_N	Column strobe	Connect with IP
CLK	Chip clock	Connect with IP
CS_N	Chip select	**Fixed pull down**
DM0	Data 0-7 shield	**Fixed pull down**
DM1	Data 8-15 shield	**Fixed pull down**
DM2	Data 16-23 shield	**Fixed pull down**
DM3	Data 24-31 shield	**Fixed pull down**
CKE	Clock enable	**Fixed high**