TL505C ANALOG-TO-DIGITAL CONVERTER

D2366, OCTOBER 1977 - REVISED FEBRUARY 1989

13 ZERO CAP 1

12☐ INTEG RES

10 INTEG OUT 9 GND

8 COMP OUT

11 ☐ INTEG IN

N PACKAGE

(TOP VIEW)

ANALOG IN 2

REF OUT 3

REF IN □4

GND 🗍

B IN [

A IN

VCC 1 U14 ZERO CAP 2

- 3-Digit Accuracy (0.1%)
 10-Bit Resolution
- Automatic Zero
 Internal Reference Voltage
- Single-Supply Operation
- High-Impedance MOS Input
- Designed for Use with TMS1000 Type Microprocessors for Cost-Effective High-Volume Applications
- BI-MOS Technology
- Only 40 mW Typical Power Consumption



Caution. This device has limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

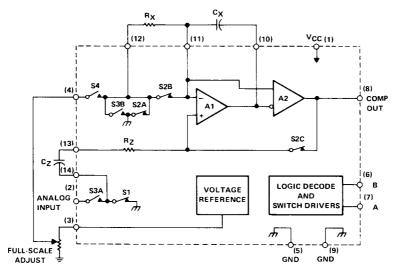
description

The TL505C is an analog-to-digital converter building block designed for use with TMS1000 type microprocessors. It contains the analog elements (operational amplifier, comparator, voltage reference, analog switches, and switch drivers) necessary for a unipolar automatic-zeroing dual-slope converter. The logic for the dual-slope conversion can be performed by the associated MPU as a software routine or can be implemented with other components, such as the TL502 logic-control device.

The high-impedance MOS inputs permit the use of less expensive, lower value capacitors for the integration and offset capacitors and permit conversion speeds from 20 per second to 0.05 per second.

The TL505C is a product of Tl's BI-MOS process, which incorporates bipolar and MOSFET transistors on the same monolithic circuit. The TL505C is characterized for operation from 0°C to 70°C.

functional block diagram



NOTE: Analog and digital GND are internally connected together.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)
Input voltage, pins 2, 4, 6, and 7
Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2) 1150 mW
Operating free-air temperature range
Storage temperature range65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds

- NOTES: 1. Voltage values are with respect to the two ground terminals connected together.
 - 2. For operation above 25 °C free-air temperature, derate linearly to 736 mW at 70 °C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN N	OM MAX	UNIT			
Supply voltage, V _{CC}	7	9 15	V			
Analog input voltage, V _I	0	4				
Reference input voltage, V _{ref(I)}	0.5	3				
High-level input voltage at A or B, VIH	3.6	V _{CC} +1	V			
Low-level input voltage at A or B, V _{IL}	0.2	1.8	V			
Integrator capacitor, CX	See "compon	omponent selection"				
Integrator resistor, R _X	0.5	2	ΜΩ			
Integration time, t ₁	16.6	500	ms			
Operating free-air temperature, TA	0	70	°C			



electrical characteristics, V_{CC} = 9 V, V_{ref(I)} = 1 V, T_A = 25 °C, connected as shown in Figure 1 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voн	High-level output voltage at pin 8	I _{OH} = 0	7.5	8.5		V
ГОН	High-level output current at pin 8	$V_{OH} = 7.5 V$		- 100		μА
VOL	Low-level output voltage at pin 8	I _{OL} = 1.6 mA		200	400	mV
VoM	Maximum peak output voltage swing at integrator output	R _X ≥ 500 kΩ	V _{CC} - 2	V _{CC} - 1		V
V _{ref(0)}	Reference output voltage	$I_{ref} = -100 \mu A$	1.15	1.22	1.35	V
αVref	Temperature coefficient of reference output voltage	$T_A = 0$ °C to 70 °C		± 100		ppm/°C
ΊΗ	High-level input current into A or B	V _I = 9 V		1	10	μΑ
I _{IL}	Low-level input current into A or B	V _I = 1 V		10	200	μΑ
l _l	Current into analog input	V _I = 0 to 4 V, A input at 0 V		± 10	± 200	pA
Iв	Total integrator input bias current			± 10		pА
Icc	Supply current	No load		4.5	8	mA

system electrical characteristics, $V_{CC} = 9 \text{ V}$, $V_{ref(I)} = 1 \text{ V}$, $T_A = 25 \,^{\circ}\text{C}$, connected as shown in Figure 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero error	V ₁ = 0		0.1	0.4	mV
Linearity error	V ₁ = 0 to 4 V		0.02	0.1	%FS
Ratiometric reading	V _I = V _{ref(I)} ≈ 1 V	0.998	1.000	1.002	
Temperature coefficient of ratiometric reading	$V_{ref(I)}$ constant and $\approx 1 \text{ V}$, $T_A = 0 \text{ °C to } 70 \text{ °C}$		± 10		ppm/°C

DEFINITION OF TERMS

Zero Error

The intercept (b) of the anolog-to-digital converter system transfer function y = mx + b, where y is the digital output, x is the analog input, and m is the slope of the transfer function, which is approximated by the ratiometric reading.

Linearity Error

The maximum magnitude of the deviation from a straight line between the end points of the transfer function.

Ratiometric Reading

The ratio of negative integration time (t2) to positive time (t1).

PRINCIPLES OF OPERATION

A block diagram of an MPU system using the TL505C is shown in Figure 1. The TL505C operates in a modified positive-integration, three-step, dual-slope conversion mode. The A/D converter waveforms during the conversion process are illustrated in Figure 2.

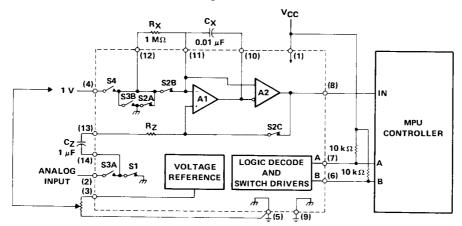


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF TL505C INTERFACE WITH A MICROPROCESSOR SYSTEM

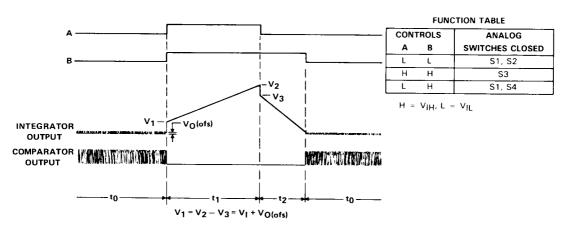


FIGURE 2. CONVERSION PROCESS TIMING DIAGRAMS

PRINCIPLES OF OPERATION (Continued)

The first step of the conversion process is the auto-zero period to. By the end of this period, the integrator offset is stored in the autozero capacitor, and the offset of the comparator is stored in the integrator capacitor. To achieve this end, the MPU takes the A and B inputs low, which closes S1 and S2. The output of the comparator is connected to the input of the integrator through the low-pass filter consisting of R2 and C2. The closed loop of A1 and A2 seeks a null condition in which the offsets of the integrator and comparator are stored in C2 and Cx, respectively. This null condition is characterized by a high-frequency oscillation at the output of the comparator. The purpose of S2B is to shorten the amount of time required to reach the null condition.

At the conclusion of t_0 , the MPU takes the A and B inputs both high, which closes S3 and opens all other switches. The input signal V_1 is applied to the noninverting input of A1 through C_2 . V_1 is then positively integrated by A1. Since the offset of A1 is stored in C_2 , the change in voltage across C_X is due to only the input voltage. Since the input is integrated in a positive integration during t_1 , the output of A1 will be the sum of the input voltage, the integral of the input voltage, and the comparator offset, as shown in Figure 2. The change in voltage across capacitor C_X (V_{CX}) during t_1 is given by

$$\Delta V_{CX(1)} = \frac{V_{I}t_{1}}{R_{1}C_{X}} \tag{1}$$

where $R_1 = R_X + R_{S3B}$ and R_{S3B} is the resistance of switch S3B.

At the end of t₁, the MPU takes the A input low and the B input high, which closes S1 and S4 and opens all other switches. In this state, the reference is integrated by A1 in a negative sense until the integrator output reaches the comparator threshold. At this point, the comparator output goes high. This change in state is sensed by the MPU, which terminates t₂ by again taking the A and B inputs both low. During t₂, the change in voltage across C_X is given by

$$\Delta V_{CX(2)} = \frac{V_{reft2}}{R_{2}C_{Y}} \tag{2}$$

where R₂ = R_X + R_{S4} + R_{ref} and R_{ref} is the equivalent resistance of the reference divider.

Since $\Delta V_{CX1} = -\Delta V_{CX2}$, equations (1) and (2) can be combined to give

$$V_{I} = V_{ref} \frac{R_1 \cdot t_2}{R_2 \cdot t_1} \tag{3}$$

This equation is a variation on the ideal dual-slope equation, which is

$$V_{\parallel} = V_{\text{ref}} \frac{t_2}{t_1} \tag{4}$$

Ideally then, the ratio of R_1/R_2 would be exactly equal to one. In a typical TL505C system where $R_X=1~M\Omega$, the scaling error introduced by the difference in R_1 and R_2 is so small that it can be neglected, and equation (3) reduces to (4).

PRINCIPLES OF OPERATION (Continued)

component selection

The autozero capacitor CZ should be within the recommended range of operating conditions and should have low leakage characteristics. Most film-dielectric capacitors and some tantalum capacitors provide acceptable results. Ceramic and aluminum capacitors are not recommended because of their relatively high leakage characteristics.

The integrator capacitor C_X should also be within the recommended range and must have good voltage linearity and low dielectric absorption. For 10-bit applications, polyster, polycarbonate, and other film dielectrics are usually suitable. If greater precision or stability is required, a polypropylene-dielectric capacitor similar to TRW's X363UW might be appropriate.

Stray coupling from the comparator output to any analog pin (in order of importance, 13, 11, 10, 2, 4) must be minimized to avoid oscillations. In addition, all power supply pins should be bypassed at the package, for example, by a 0.01- μ F ceramic capacitor.

The time constant $R\chi C\chi$ should be kept as near the minimum value as possible and is given by the formula:

Minimum
$$R_X C_X = \frac{V_I(max) t_1}{(V_{CC} - 2 V - V_I(max))}$$

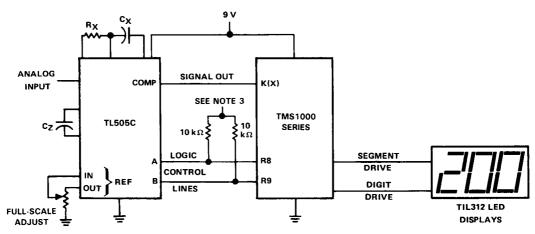
where:

t₁ = Input integration time in seconds,

VI(max) = the maximum value of the analog input voltage,

 $V_{CC}-2 V =$ the maximum voltage swing of the integrator input.

TYPICAL APPLICATION DATA



NOTE 3: Connect to either 9 V or 0 V depending on which device in the TMS1000 series is used and how it is programmed.

FIGURE 3. TL505C IN CONJUNCTION WITH A TMS1000 SERIES MICROPROCESSOR FOR A 3-DIGITAL PANEL METER APPLICATION

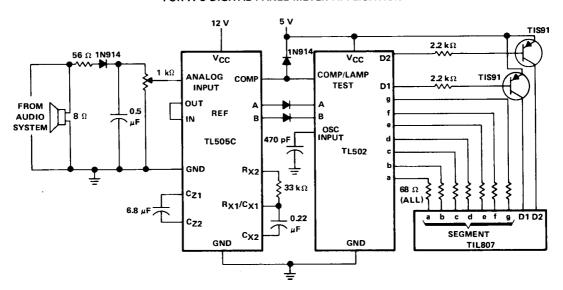


FIGURE 4. AUDIO PEAK POWER METER