PLL Clock Management Features in Altera FPGAs

Altera® FPGAs offer feature-rich phase-locked loops (PLLs) that provide robust clock management capabilities and synthesis for device clock management, external system clock management, and high-speed I/O pin interfaces. Table 1 summarizes and compares the PLL features available in Stratix® IV (E and GX), Stratix III, Stratix II and Stratix II GX, Stratix and Stratix GX, Cyclone® III ,Cyclone II, and Cyclone FPGAs. The PLLs can feed the global clock network or I/O pins.

Table 1. PLL Features

Feature	Stratix III and Stratix IV PLLs		Stratix II and Stratix II GX PLLs		Stratix and Stratix GX PLLs		Cyclone III PLLs	Cyclone II PLLs
	Top / Bottom	Left / Right	Enhanced PLL	Fast PLL	Enhanced PLL	Fast PLL		
Number of PLLs	2-4	4-8	2, 4	4-8	2-4	4-8	2,4 *(1)*	2, 4
Clock Multiplication and Division	*m*/(*n* x post-scale counter)	*m*/(*n* x post-scale counter)	*m*/(*n* x post-scale counter)	*m*/(post-scale counter)	*m*/(*n* x post-scale counter)	*m*/(post-scale counter)	*m*/(*n* x post-scale counter)	*m*/(*n* x post-scale counter)
M Counter Values	1-512	1-512	1-512	1-32	1-512	1-32	1-512	1-32
N Counter Values	1-512	1-512	1-512	1-4	1-512	1-32	1-512	1-4
Post-Scale Counter Values	1-512	1-512	1-256	1-32	1-512	1-32	1-512 *(2)*	1-32
Number of Internal Clock Outputs Available Per PLL	10	7	6	4	6	3 *(3)*	5	3
Number of Dedicated External Clock Outputs (PLL#_OUT) Available Per PLL	6 single-ended, or 4 single-ended and 1 differential pair	2 single-ended, or 1 differential pair	6 single-ended, or 3 differential	*(4)*	8 single-ended, or 4 differential *(5)*	*(4)*	1 single-ended, or differential	1 single-ended or differential
Number of Feedback Clock Inputs Available Per PLL	1 single-ended or differential	1 single-ended only	1 single-ended or differential		1 single-ended or differential *(7)*			
PLL Outputs Can Drive All Clock Network Types			X	X			X	X
Supported Clock Feedback Modes								
Normal Mode	X	X	X	X	X	X	X	X
No Compensation Mode	X	X	X	X	X	X	X	X
Zero Delay Buffer Mode	X	X	X		X		X	X
External Feedback Mode	X	X	X		X			
Source-Synchronous Mode	X	X	X	X			X	
LVDS Compensation Mode		X						
Features								
Phase Shift	Down to 96.125-ps increments	Down to 96.125-ps increments	Down to 125-ps increments	Down to 125-ps increments	Down to 156.25-ps increments	Down to 125-ps increments	Down to 96-ps increments	Down to 125-ps increments
Per Tap Programmable Phase Shift Allowed in All Modes	X	X	X	X	X	X	X	X
Advanced Control Signals (`pllena`, `areset`, `pfdena`)	X *(8)*	X *(8)*	X	X	X	X	X *(8)*	X
Programmable Duty Cycle	X	X	X	X	X	X	X	X
Advanced Features								
Gated Lock	X	X	X	X				X
Automatic Clock Switchover	X	X	X		X		X	

Manual Clock Switchover	X	X	X	X	X		X	X
Programmable Bandwidth	X	X	X	X	X		X	
PLL Reconfiguration	X	X	X	X	X		X	
Reconfigurable Bandwidth	X	X	X	X				
Spread Spectrum Clocking	X	X	X		X		X	
Counter Cascading	X	X	X				X	
Reference Clock Input Sharing Allowed						X		
Ability to Internally Cascade PLLs	X	X	X	X		X *(9)*	X	
Supported PLL Drivers								
Dedicated Input Clock Pin	X	X	X	X	X	X	X	X
GCLK Network*(10)*	X	X	X	X		X	X	
RCLK Network*(10)*	X	X	X	X		X		

Notes:

1. EP3C5 and EP3C10 offer 2 PLLs whereas larger devices offer 4 PLLS.
2. C counters range from 1 through 512 if the output clock uses a 50 percent duty cycle. For any output clocks using a non-50 percent duty cycle, the post-scale counter range from 1 through 256.
3. PLLs 7, 8, 9, and 10 have two output ports per PLL. PLLs 1, 2, 3, and 4 have three output ports per PLL. On Stratix GX devices, PLLs 3, 4, 9, and 10 are not available for general-purpose use.
4. The PLL clock outputs of the fast PLLs can drive to any I/O pin to be used as an external clock output. For high-speed differential I/O pins, the device uses a data channel to generate the transmitter output clock (`txclkout`).
5. Every Stratix and Stratix GX device has two enhanced PLLs (PLLs 5 and 6) with either eight single-ended outputs or four differential outputs each. Two additional enhanced PLLs (PLLs 11 and 12) in EP1S80, EP1S60, EP1S40 (PLL 11 and 12 not supported for F780 package), and EP1SGX40 devices each have one single-ended output.
6. n/a
7. Feedback clock input supported in PLLs 5 and 6 only.
8. `pllena` feature is not supported in Stratix III and Cyclone III devices.
9. Fast PLL in Stratix and Stratix GX devices can support internal PLL cascading provided it is the downstream PLL.
10. The global (GCLK) or regional (RCLK) clock input can be driven by an output from another PLL, a clock pin-driven global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal or general purpose I/O pin cannot drive the PLL.

Literature

Detailed information about the PLLs available in the Altera device families can be found in the appropriate device family handbook:

- *Clock Networks and PLLs in Stratix IV Devices* (PDF)
- *Clock Networks and PLLs in Stratix III Devices* (PDF)
- *PLLs in Stratix II and Stratix II GX Devices* (PDF)
- *General-Purpose PLLs in Stratix & Stratix GX Devices* (PDF)
- *Clock Networks and PLLs in Cyclone III Devices* (PDF)
- *PLLs in Cyclone II Devices* (PDF)
- *Using PLLs in Cyclone Devices* (PDF)

Additional related information is available in the following documents:

- *`altpll` Megafunction User Guide* (PDF)
- *AN 367: Implementing PLL Reconfiguration in Stratix II Devices* (PDF)
- *AN 282: Implementing PLL Reconfiguration in Stratix & Stratix GX Devices* (PDF)
- *AN 313: Implementing Clock Switchover in Stratix & Stratix GX Devices* (PDF)
- Possible Causes for PLL Loss of Lock