Thermal Modeling of Power-electronic Systems

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Increasing power densities, cost pressure and an associated greater utilization of the robustness of modern power semiconductors are making thermal system optimization more and more important in relation to electrical optimization. Simulation models offering a combination of these two domains have not been available up till now.

Abstract

The article describes new SPICE and SABER simulation models which contain a dynamic link between electrical and thermal component descriptions. On the one hand, operating states in which a relevant inherent heating occurs can be simulated under a good approximation of actual conditions. On the other hand, the models offer defined nodes which provide a link to the thermal environment of the component and enable, for example, the study and optimization of heat sink options.
Following a list of the basic properties of the two common thermal equivalent circuit diagrams is a description of the implementation of a dynamic temperature-dependent model in SPICE and SABER using a power MOSFET model as an example. Various possibilities for determining the thermal parameters are demonstrated. The possibilities and limitations of the new models are presented with application-based examples.

Introduction

Today, circuit simulators are standard tools in the development and optimization of electronic systems. However, simulation has until now been limited to electronic functions because, in the simulation models available today, temperature dependence can at best be taken into account by changing the static global temperature. In power-electronic systems in particular, the temperature is one of the critical parameters due to the fact that many properties of power semiconductors are very strongly temperature-dependent – following are some examples:

❑ A maximum junction temperature is specified for all semiconductor components which, when exceeded, can lead to destruction or permanent damage of the component. Even when temporary events such as avalanche or short-circuit conditions occur, it must be ensured that the maximum permissible junction temperature is not

exceeded – a problem which is almost impossible to solve by conventional means, i.e. using a Z_{th}-diagram.

❑ Within the safe operating range, the lifetime of semiconductor components is strongly affected by temperature fluctuations due to loading. Each change in temperature causes mechanical stress in the component which, in particular, affects solder and bond connections. Here it is not the absolute temperature which is decisive but the temperature cycling. As a rule of thumb it can be assumed that the aging of a component is proportional to the fourth (!) power of the temperature deviation [1].

❑ The ON-resistance of a MOSFET and thus the conduction losses are roughly doubled with a temperature increase from 25°C to 150°C.

❑ The threshold voltage of a MOSFET drops with increasing temperature which reduces the signal-to-noise margin at the control node. Ignoring this effect can lead to an undesired – even catastrophic – turn-on of the transistor when it should be inhibited, especially in bridge circuits with high slew rates for the drain-source voltage.

In addition to these aspects, the question of the fluctuation in the junction temperature is also becoming more and more important in the course of circuit design. Some of the overdimensioning for example in the switching of lamps or motors to cover temporary overloads is no longer necessary when the brief, excessive power dissipation can be compensated by suitably coupled thermal capacitances.

Similarly, this applies when one wants to do away with the usual protection circuits when relying on the high robustness of todays power semiconductors. Avalanche energy of modern power MOSFETs for example is specified in such a way that any load current pulse pattern below the rated current is allowed as long as it is ensured that the peak junction temperature does not exceed the maximum value.

In order to be able to simulate the time-dependent temperature curves which occur in all operating states, it is necessary to couple the electrical model of a component dynamically with the description of its thermal properties. For use in an electric circuit simulator, the thermal description by an electric analog model is to be preferred.

Electrical description of thermal systems

Basically, the propagation of heat in a system can take place in three different ways, convection, heat radiation or heat conduction. Electronic components usually have only heat conduction which is described in a homogeneous isotropic material by the equation

$$\frac{\partial^2 T}{\partial x^2} = \frac{c \cdot r}{l_{th}} \cdot \frac{\partial T}{\partial t} \qquad (1)$$

A one-dimensional heat flow is assumed for the sake of simplification. In the

equation, λ_{th} stands for the specific heat conductance, c for the specific thermal capacitance and ρ for the density of the material. T describes the temperature and x the coordinates in the direction of heat propagation.
In the search for an electrical analog model for heat conduction, the comparison with a transmission line comes closest, although its properties are described by a much more complex equation

$$\frac{\partial^2 U}{\partial x^2} = C' L' \frac{\partial^2 U}{\partial t^2} + (C' R' + G' L') \frac{\partial U}{\partial t} + G' R' U \qquad (2)$$

Here C′ is the capacitance per unit length, R′ the resistance per unit length, G′ the transverse conductance value per unit of length and L′ the inductance per unit length. As a wave equation, the transmission line equation describes all the properties typical for a wave such as reflections, standing waves etc. By comparison, the heat conduction equation describes a diffusion or compensation process. These are basically different physical processes which have no direct relationship.

If, however, one considers that, in the field of heat conduction in solid media, there is no direct comparison for the electrical term of inductance and that a volume element cannot cool itself, this can be described formally by L′=0 and G′=0. The equation of an equivalent transmission line is thereby reduced to

$$\frac{\partial^2 U}{\partial x^2} = C' R' \frac{\partial U}{\partial t} \qquad (3)$$

and then has the same structure as the heat conduction equation. Kirchhoff stated as early as 1845 that: "*Two different forms of energy behave identically when the basic differential equations which describe them have the same form and the initial and boundary conditions are identical*". [2]
According to the equations (1) and (3) heat conduction processes can therefore be modeled by a transmission line equivalent circuit diagram which, as shown in figure 1, consists of R/C elements only. In addition the equivalences listed in table 1 exist between the electrical and thermal variables.

Thermal		Û	Electrical
Temperature	T in K	Voltage	U in V
Heat flow	P in W	Current	I in A
Thermal resistance	R_{th} in K/W	Resistance	R in V/A
Thermal capacitance	C_{th} in Ws/K	Capacitance	C in As/V

Table 1: Corresponding physical variables

Related to a power transistor, the heat path from the chip to the back of the lead frame or to a heat sink can be modeled, for example, with the transmission line equi-

valent circuit diagram. In this case, the electrical power source P(t) represents the power dissipation (heat flow) occurring in the chip in the thermal equivalent.

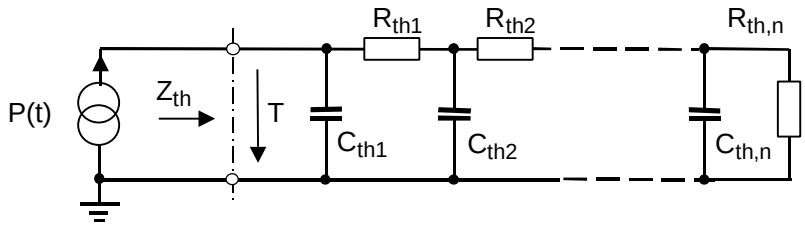


Fig. 1: Electrical transmission line equivalent circuit diagram for modeling heat conduction properties; the physical variables are specified in their thermal equivalents.

Analogous to the electrical transmission line, thermal resistance and thermal capacitance per unit length need to be considered for exact characterization of the thermal properties of a component. However, to simplify the description, it is helpful and permissible to combine single volume elements in lumped equivalent elements (R_{th}, C_{th}).

Due to the close relationship with physical reality, the parameters for the transmission line equivalent circuit diagram can be derived directly from the structure of the element when it basically exhibits one-dimensional heat flow. In figure 2 this is illustrated by the example of a typical power transistor in a package with a solid cooling tab – e.g. TO-220 or D-Pak.

In practice, it has been shown that the segmentation of the structure into partial volumes is not critical as long as the following points are considered:

a. The graduation of layer thickness should be chosen so that progressively larger thermal time constants ($R_{th,i} \cdot C_{th,i}$) are produced in the direction of heat propagation (experience has shown that the time constants should differ respectively by a factor of 2...8 for the best results). If the heat inducing area is smaller than the heat conducting material cross section, a „heat spreading“ effect occurs – as shown in figure 2 – which needs to be taken into account by enlarging the heat conducting cross section A. For heat propagation in homogeneous media it has been helpful to assume a spreading angle α of about 40°. In practice however, this only applies as long as the heat propagation is not obstructed by subsequent layers with low heat conductivity (heat accumulation effect).

b. Unlike the division of layers through which heat is conducted, the size of every volume element in which heat is produced must be determined exactly because its thermal capacitance has a decisive influence on the thermal impedance of the system when power dissipation pulses, with a very short duration, occur. In the equivalent circuit diagram, the thermal capacitances of these volumes always appear directly parallel to the heat flow source. In power MOSFETs, the cell array

and epitaxy layer correspond to the heat generating volume. Because of different epi-thickness requirements, the volume depends on the voltage class of the transistor in addition to the active chip area. The area with homogeneous volume heating also determines the minimum thermal time constant of the component. Based on this, the further layer division can be made according to the points outlined in a.

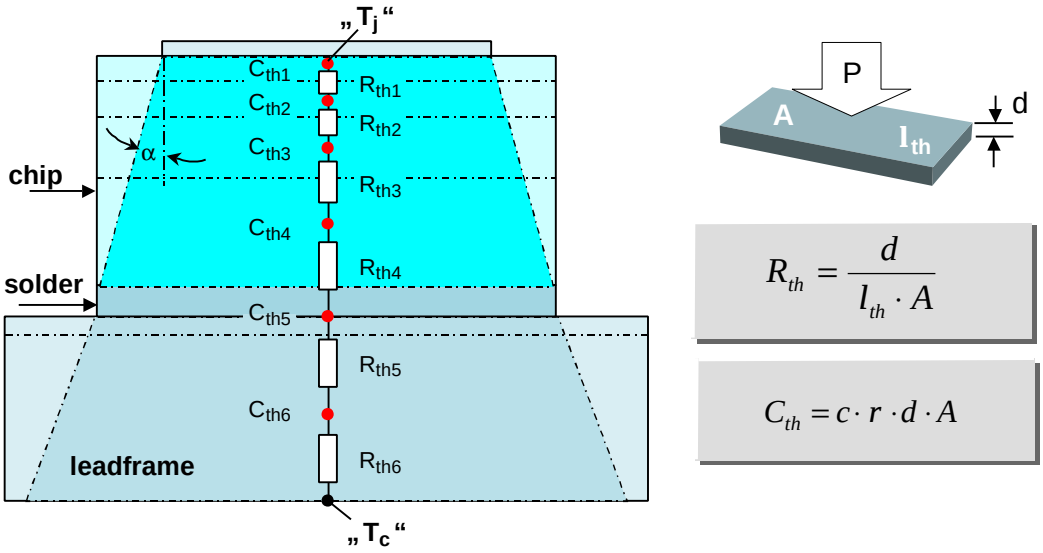


Fig. 2: For simple structures, the thermal equivalent elements can be determined directly from the physical structure. For the sake of clarity, the actual thickness relationships are not shown to scale.

If complicated heat flow conditions exist – as for example in typical SO packages – the thermal equivalent elements can only be roughly estimated in the manner described.

An alternate solution in this case, would be to calculate the heat flow using the “finite element analysis” method (FEA). However, for the practical use of the FEA results within the scope of a circuit simulation, it is necessary to divide the entire structure, which sometimes covers several tens or hundred thousand “ finite” elements, into suitable sub-structures and to determine lumped equivalent elements for these. Since this process is not yet supported by standard FEA tools, this solution is too complex for most applications.

Much simpler, even though it only possible with a system which is available at least in the form of a prototype, is the parameterization of the elements of the equivalent circuit diagram based on measurements and related curve fitting.

The usual procedure, in practice, is to first heat the component with a defined power dissipation P_1 until it assumes a stationary temperature $T_{j1.}$ If one knows the exact temperature dependence of a parameter of the chip – generally the forward voltage drop of an integrated diode structure is used – the “cooling curve“ Tj(t) of the affec-

ted region of the chip (frequently referred to as the depletion or junction layer) can be determined after reducing the power dissipation to zero. This cooling curve gives one the transient thermal impedance $Z_{th}(t)$ of the component according to:

$$Z_{th}(t) = \frac{T_{j1} - T_j(t)}{P_1} \tag{4}$$

This transient thermal impedance corresponds in system theory to the step response and therefore contains the full thermal description of the system.

A linear system is generally assumed for these observations, which is the case to a first approximation, as long as one ignores the sometimes considerable temperature dependences of the specific material parameters and, in particular, that of the heat conductance of silicon.

The measuring method described for determining $Z_{th}(t)$ obviously leads to the same result when the heating curve is used instead of the cooling curve. However, in practice the heating curve is less suitable for chip measurements because of the necessity to heat and measure the temperature at the same time.

Since the transient thermal impedance fully characterizes the thermal properties of the component, it can be used to generate a plot of the junction temperature vs time for any power dissipation profile P(t):

$$T_j(t) = T_0 + \int_0^t P(\tau)\, dZ_{th}(t-\tau)\, d\tau \tag{5}$$

T_0 is the initial temperature and $dZ_{th}(t)$ the derivative with respect to time of equ.(4), which corresponds to the thermal pulse response of the system (which cannot be measured directly).

In order to be able to use the results of the thermal measurement for modeling in an electrical circuit simulator, it is necessary to find an electrical equivalent network whose step response describes the transient thermal impedance.

If only a plot of the junction temperature is of interest and not the exact internal temperature distribution, other equivalent circuit diagrams can be used in addition to the thermal equivalent circuit diagram shown in figure 1.

Actually, there is an unlimited number of networks whose step response describes the cooling curve with the required accuracy and which can be used accordingly for modeling. Among this large number of possible networks, there are two dominant topologies:

First, the transmission line equivalent circuit diagram shown in figure 1, which is derived directly from transmission line theory, and therefore often referred to as the “natural“ equivalent circuit diagram of heat conduction. It is the only network which also describes the internal temperature distribution of the system correctly and

enables a clear correlation of equivalent elements to real structural elements (chip, solder layer, etc.).
The second most frequently used thermal equivalent network is shown in figure 3. The individual RC elements represent the terms of a partial fractional division of the thermal transfer function of the system, whereby the order of the individual terms is arbitrary. The partial fractional representation directly shows the uniqueness of this network which is given by the fact that it has a mathematically simple, closed-form specifiable step response:

$$Z_{th}(t) = \sum_{n=1}^{n} R_n \left(1 - e^{-\frac{t}{R_n C_n}} \right) \tag{6}$$

This property simplifies both determining the values of the equivalent elements and closed-form calculation of temperature curves for simple power dissipation profiles. This explains the wide application and popularity of this equivalent network.
Unfortunately, often hair-raising misinterpretations are met with in connection with this network, even in the literature. We therefore point out expressly that the network illustrated in figure 3 is a purely formal structure! This means that the network is able to correctly describe the thermal behavior at the input terminals of the " black-box" and therefore, for example, the curve of the junction temperature with any excitation, but with the restriction that the internal structure of the network is neither related to the real physical structure nor can the temperature distribution in the real system be described from the internal node voltages!
It therefore follows in practice that it is not possible, for example, to assign the reference plane "package backside" to node x in figure 3. Accordingly, it is not pos-

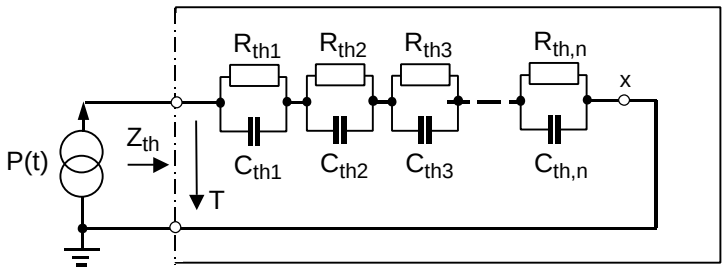


Fig. 3: The most frequently used thermal equivalent circuit diagram is mathematically very simple to use but as a purely formal description has no relation to the real physical structure.

sible to partition the network at this point in order to extend it (e.g. with the thermal equivalent circuit diagram of a heat sink). To model the component with a heat sink, it would be necessary to remeasure the system and then recalculate the values for all of the R/C elements.
The following considerations should help to explain the absence of a relationship

between the physical nodes and the internal structure of this network: let us assume that the network in figure 3 has been parameterized to the thermal impedance of the packaged chip ($Z_{thjc)}$ and would actually reflect the physical structure of the component. Then, the network could be separated at node x – which would represent the rear of the package – and an additional high resistance added to simulate the thermal resistance of the package to its environment (Z_{thca}) (free convection). If this network is then driven with a temperature step at the input node, this step would appear in differentiated form at the network output, i.e. the component package, due to the capacitor network. This obviously contradicts reality as well as the property that any heat flow fed in at the input, according to Kirchhoff´s law, flows without a delay through the "package node". In addition, this equivalent circuit diagram shows that the energy stored in the thermal capacitors depends on the temperature difference between adjacent nodes whereas, in reality, the stored energy is proportional to the absolute temperature of a volume element. In summary, this means that the equivalent network shown in figure 3 is suited for thermal model calculations but only to model that system for which the network elements were determined and only when no access to system-internal temperatures is required. It follows further that this network is unsuitable for use in simulation models as soon as the user needs to have the possibility of application-specific extension of the thermal description. In this case the equivalent circuit diagram of a transmission line must be used

If the elements of the transmission line equivalent circuit diagram cannot be determined from the physical structure and a cooling measurement has to be used instead, the parameter extraction is not trivial due to the fact that the step response of this network is not mathematically directly accessible. The authors prefer the method of transforming the $Z_{th}(t)$-curve - calculated from the cooling down curve according to equation (4) - initially into the Laplace (frequency) domain because there the input impedance (= transfer function) of the transmission line network is specified very simply by:

$$Z_{th}(s) = \cfrac{1}{sC_{th,1} + \cfrac{1}{R_{th,1} + \cfrac{1}{sC_{th,2} + \ldots + \cfrac{1}{R_{th,n}}}}} \tag{7}$$

With the help of standard curve fitting algorithms (available for example in MathCAD®) the $R_{th,i}$ and $C_{th,i}$ can then be adapted so that a plot of the transfer function corresponds to the "transformed cooling curve" (cf. figure 4).

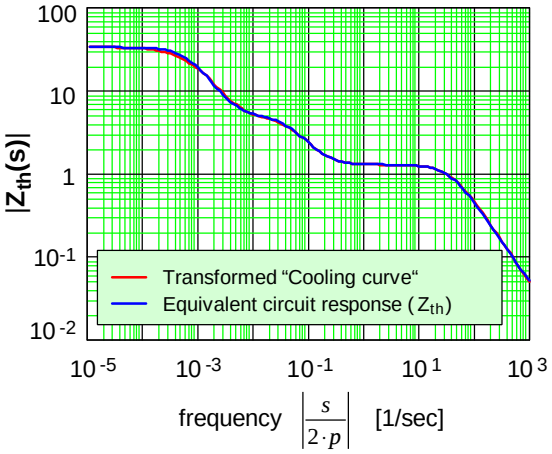


Fig. 4: A $Z_{thja}(s)$ curve determined from a cooling curve and an adapted line equivalent circuit diagram (here: SMD package on board).

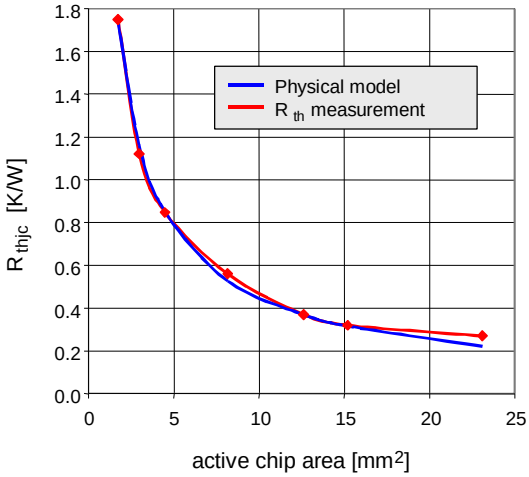


Fig. 5: Comparison of the thermal resistance calculated according to figure 2 with measured values for different chip surfaces in a TO-220 package

In figure 5, the measured static thermal impedance R_{thjc} of a 55V S-FET transistor in a TO-220 package (cf. Figure 2) is compared with the results of a calculation based on the model and its corresponding material parameters.

If one compares these R_{thjc} values with data sheet specifications, one will find considerable discrepancy between the measured values (generally lower) and the data-sheet values. The reason for the different values is that in figure 5, the thermal resistance between "Junction" and the ideal reference plane "case" is specified – a value which can only be achieved in practice with very special cooling techniques (e.g. direct liquid cooling of the case). In order to take into account the otherwise unavoidable thermal transition resistance, even with ideally prepared assembly surfaces and for safety in the event of fluctuations in the assembly process, data sheets generally have a built-in safety factor. Note that the measuring and analysis required for calculation of R_{thjc} is susceptible to error and requires a very sophisticated measuring setup – especially for the parameterization of large-area chips with subsequently low thermal resistance.

DMOS model

A basic model for DMOS transistors has been in use for well over 10 years. The model is based on a vertical structure implemented using an N- epitaxial layer on an N+ doped substrate. The graphics in Figure 6 depict the construction of a unit DMOS cell as well as a cross section showing the various elements of the model. The elements are then arranged for simplicity into the schematic representation of Figure 7.

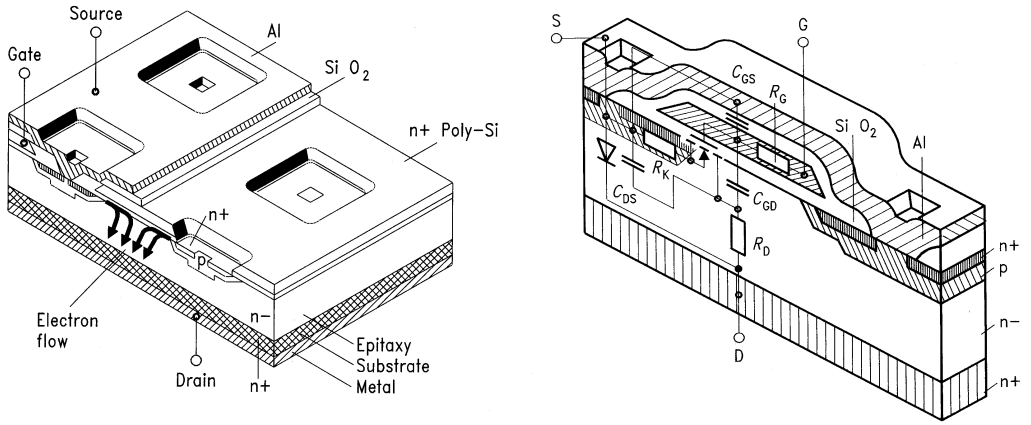


Fig. 6: Structure of a power MOSFET (DMOS) with the parasitic elements important for the component behavior

Although this model has been in wide use, its impementation and parameterization have left much to be desired – especially in SPICE. A great improvement has been made possible by the extensions now available in SPICE, especially the analog behavior models ABM. This has led to a much better description of the non-linear elements such as the drain resistance and "Miller" capacitance.

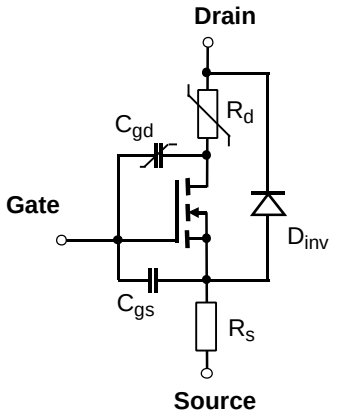


Fig. 7: The circuit diagram of a DMOS model shows the principals and reflects the structural elements of figure 6

Now all modern SPICE-based simulators offer such possibilities – but unfortunately without a uniform syntax. This means that the compatibility of models is no longer to be taken for granted as is the case when standard SPICE 2G6 models are used. However, with the capabilities of modern SPICE simulators, the old dream of all power electronic designers has become true, integration of dynamic self-heating into the models.

Modeling of temperature dependent component parameters

The temperature dependence of semiconductor device parameters is often regarded as a second order effect and often delt with based on rules of thumb or experience. This is not possible in the case of power semiconductors, as the power generated within the device significantly effects its characteristics. The temperature dependent

parameters having the most significant impact are mobility (both bulk and surface values) and threshold voltage. These appear in the channel model for MOS transistors and are well defined. This presents a problem in that most models do not include a temperature node (the solution to this will be discussed later when the specific simulation programs are addressed).

Additional elements in the power transistor model are the drain resistance and various capacitances. The oxide capacitances typically have a temperature coefficient of 10 to 20 ppm. This is insignificant in terms of effecting the accuracy of the model. Junction capacitances are assumed to remain constant over the operating range of the transistor.

The Miller capacitance exhibits minimal temperature dependence and this is due the voltage drop across the epi drain resistor (epitaxial layer).

The drain resistance (epi layer) is both temperature and electric field dependent. The electric field effect is neglected for normal operation due to the fact that it plays a significant role only when the device is in saturation. When not in saturation, the electric field has a low value and the mobility remains for all practical purposes a constant. The temperature dependence of the bulk mobility does play a significant role however, causing an increasing resistance with a rise in temperature.

In order to be able to simulate the inherent heating dynamically, an interactive coupling of the thermal description with the MOSFET model is necessary as shown schematically in figure 8. For this, the instantaneous power dissipation in the transistor (Id x Uds) is determined at all times and a current proportional to the dissipated

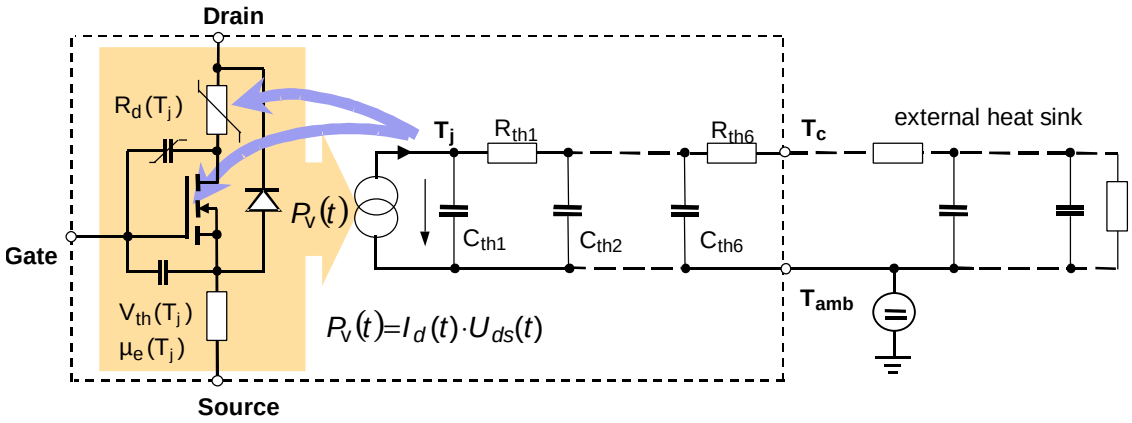


Fig. 8: Principle circuit diagram of a model with interactive coupling of electrical and thermal component description ("Level-3_{th}" model).

power is fed into the thermal equivalent network. The voltage at node T_j then contains information regarding the momentary junction temperature which on the other

hand interacts directly with the temperature-dependent parameters of the MOSFET. Infineon Technologies offers worldwide, for the first time, such models for its power semiconductors. The circuit simulators PSPICE® and SABER® are supported under the designation of "Level-3$_{th}$ models" (Spice level 3 models with thermal networks).

Implementation in SPICE

As already mentioned, no direct access is available to the temperature, e.g. in the form of a temperature node in the SPICE-internal MOSFET models. However, this problem can be overcome by means of the "trick" shown in figure 9.
To implement this, the MOS channel is described quite conventionally with a Level-3 MOS model (X1) which is part of the simulator. However, since the transistor X1 only sees the temperature defined by the global SPICE variable "Temp", it is necessary to scale the threshold voltage, the drain current and the drain resistance according to the current junction temperature. The threshold voltage has a temperature coefficient of –2.5mV/K; accordingly the effective gate voltage, fed to the transistor X1 with the help of the "analog behavior model" E_Vth, is temperature dependent.

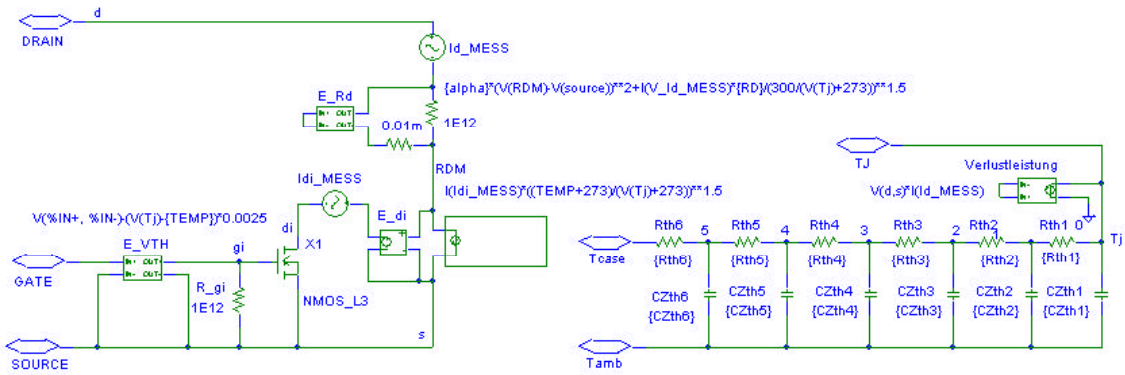


Fig. 9: MOSFET model created in PSPICE with dynamically temperature-dependent parameters

In order to be able to scale the temperature effect on the drain current, the channel model X1 which is only valid at the global temperature "Temp" must be decoupled from the actual drain and source connection of the transistor. The voltage-controlled power source E_di which is connected as a 1:1 buffer is used to accomplish this. This enables modeling of the channel function with the "correct" values, i.e. the values valid at temperature "Temp", of the gate source and drain source voltage. The drain current Idi(Temp) flowing through X1 is then scaled with a temperature-dependent factor and implemented in the drain source circuit as Id (Tj). Assuming the conversion of the temperature to the Kelvin scale, it applies that:

$$I_d(T_j) = I_{di}(Temp) \cdot \left(\frac{T_j}{Temp} \right)^{-3/2} \quad (8)$$

The factor $T^{-3/2}$ directly reflects the temperature dependence of the charge carrier mobility and is found again accordingly in the voltage source E_Rd which describes the drain resistance. The exponential 3/2 corresponds to the standard value usually found in the literature, in individual cases slight deviations in the value of this exponent are found.

Implementation in SABER®

SABER®, unlike SPICE® offers the possibility of creating complete system descriptions in MAST®, a programming language unique to SABER® developed by Analogy®.
This offers great freedom in the modeling of complex functions or systems and enables a more intuitive method than that, for example, used to create sub-circuits with analog behavior models as in the case of SPICE. MAST® also enables the clean separation of thermal and electrical variables and therefore avoids error sources such as the accidental loading of a thermal node with an electrical network.
The first step in a SABER® model is also the definition of the external connections. As one can see in the following example, the connection name is defined first followed by the connection type:

```
template name   IN VBB IS OUT Tin Tcase Tamb= model
electrical IN,VBB,IS,OUT
thermal_c  Tin,Tcase, Tamb                                    (9)
```

In the third line the unit " °C " is also assigned to the variables Tin, Tcase and Tamb. Tin is a pin which enables connection of an external (thermal) power source. This is followed by the assignment of the temperature of the pin Tin to the internal variable Tj, which represents the effective "junction" temperature:

```
Tj = tc(Tin)                                                  (10)
```

The threshold voltage can then be changed depending on this junction temperature from the value one determined in the Tmeas measurement. The temperature coefficient corresponds with –2.5mV/K to the value used in the SPICE model.

The following program line shows a very simple implementation of the temperature-dependent threshold voltage in comparison with SPICE:

```
vto = model->vt0 - 0.0025*(Tj -model->tmess)                  (11)
```

This is followed by the implementation of the temperature dependence of the transmission slope in the form of the k-factor (k=kp in A/V2) in the MOSFET equa-

tion. Mu_s stands for surface mobility[1] here:

```
if ( vmos >= vd_sat) {
kp0=(mu_s/(1+mu_s*(vd_sat)/model->l/model->vs))*\
(model->w/model->l)*model->eox*model->e0/model->tox
                  }
else {
kp0=(mu_s/(1+mu_s*abs(vmos)/model->l/model->vs))*(model-
>w/model->l)*\
        model->eox*model->e0/model->tox
     }
k  = kp0*((Tj+273)/(model->tmess+273))**(-1.5)                (12)
```

This is a much more direct method than the behavior models required in SPICE. Experience has shown that the computing time and the convergence properties of this type of description are better. It must of course be taken into account in the comparison that the extended possibilities of SABER® are obtained at considerable extra costs and that the training time on the system is many times that required for SPICE.

Practical applications

The coupling of electrical and thermal systems allows operating conditions, in which a significant heating of the transistor occurs, to be simulated with realistic results for the first time. An extreme example of this is a short-circuit, an operating state in which the transistor itself limits the load current by means of its output characteristic curves – i.e. the drain voltage increases. The simulation of this operating state places very high requirements on a simulation model in two respects:
On the one hand, the model must describe the output characteristic curves correctly in a range which is far outside the usual data sheet specifications. On the other hand, results which are realistic can only be expected when the inherent self-heating is taken into account and with a thermal model which is accurately parameterized.

[1] Typical value 600cm2/Vs at Tj = 27°C; with increased accuracy requirements the value must be extracted from measurements for a given technology.

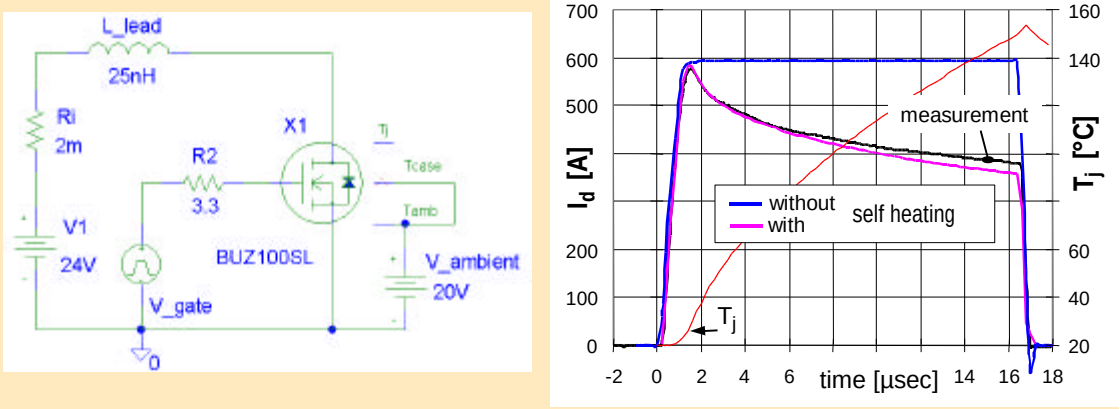


Fig. 10: Result of a short-circuit simulation with and without consideration of the inherent self-heating

Figure 10 depicts this, making a comparison between a short-circuit measurement and the results of a standard model as well as those of a Level-3 $_{th}$ model. The simulated circuit, which corresponds to the applicable measuring setup, is also specified in figure 10. The standard model yields a short-circuit current which is constant due to the constant, power dissipation independent chip temperature, whereas the model with self-heating describes the measurement much more accurately. In addition, the Level-3 $_{th}$ model provides the user information regarding the junction temperature versus time. This is of very great advantage since, in practice, the maximum permissible junction temperature is the most important limit for defining the safe operating area of a power MOSFET.

It should, however, be noted that simulation models are generally parameterized to fit the data of a typical and not a “worst-case” component. For components to which the thermal model shown in figure 2 can be applied, a worst case estimate with respect to the thermal properties can be made in a first approximation by scaling up the resistances Rth4...Rth6 with a common factor so that the sum of all Rthi corresponds to the maximum value for the thermal resistance Rthjc specified in the data sheet.

In the test circuit shown in figure 10, the condition, package temperature equal to ambient temperature, is forced by a short-circuit between the corresponding thermal connections of the transistor symbol – this is equivalent to ideal cooling conditions. The voltage source Vambient determines the ambient temperature at 20°C with its 20V.

It basically applies that an external thermal network can be dispensed with for the simulation of very short processes because the heat front propagates initially in the component and requires a certain time before it reaches the rear of the package. For components in the TO 220 package, this time is about one millisecond. Until then the

simulation results are independent of the wiring of the Tcase pin. To avoid convergence problems, however, a DC path with finite resistance between the Tcase and the Tamb pins should always be assembled because an unwired Tcase pin corresponds to the ideal thermal insulation of the component which can very quickly lead to a thermal “run away” in the simulation.

In the event of a short-circuit, currents occur at high gate voltages which can reach more than ten times the rated current of a MOSFET. Since, at the same time, a high drain source voltage is applied, this corresponds to an operating point which is far to the “ top right” in the output characteristic field – outside the characteristic range usually specified in data sheets.
In this operating state an extremely high power dissipation is produced which may be up to a few kilowatts in low-voltage components and up several ten kW in high-voltage components. As one can see in figure 10, this can lead to extreme heating of the chip within a few microseconds and to a subsequent drop in the current.

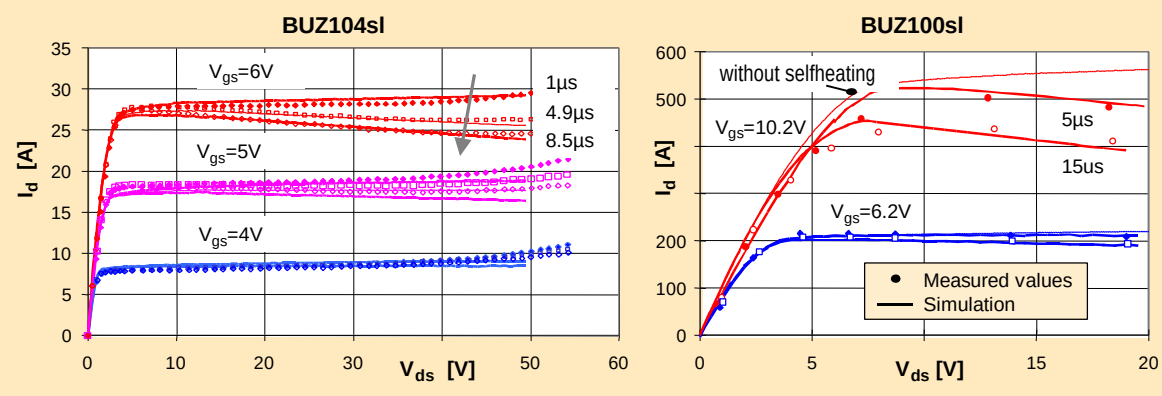


Fig. 11: The current drop due to inherent heating in the output characteristic becomes noticeable already after very short pulses.

The inherent self-heating must be taken into account in measuring the output characteristic field and in every comparison between ones own measurements and the simulation results. How strong this influence is, is clearly shown in figure 11 in which the output characteristic field is shown dependent on the measuring time and the length of the current pulse used for the measurement.
If one compares this with the pulse lengths of commercially available curve tracers with 80 µs and more, it immediately becomes clear that this type of equipment is absolutely unsuitable for proper characterization measurements.

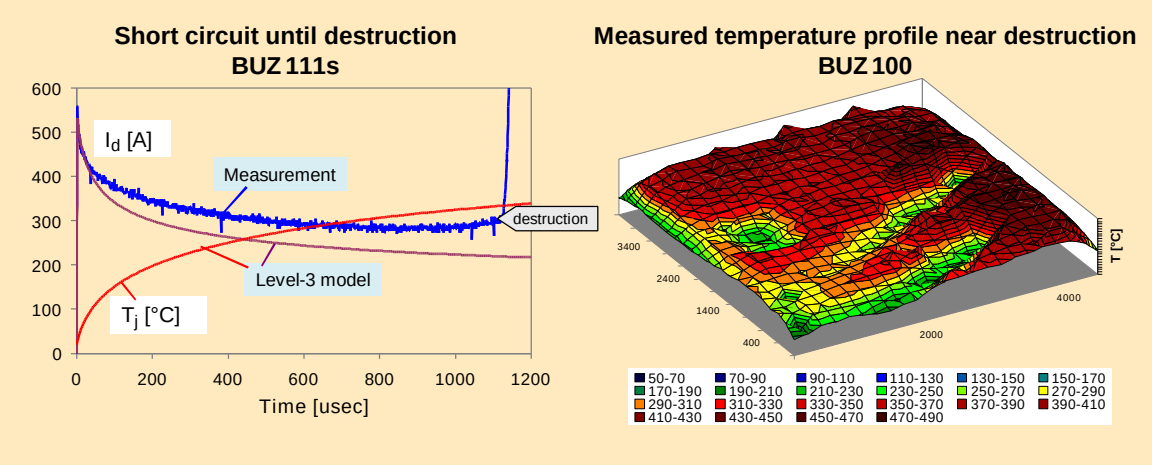


Fig. 12: At very high junction temperatures, larger temperature deviations occur due to influences not taken into account in the model. On the right is a high-speed thermograph photo of the chip surface close to the destruction point.

If one continues the comparison between the short-circuit measurement and simulation up to component destruction, increasing deviations appear with increasing junction temperature (see figure 12). The reasons for this are, in addition to bipolar effects, essentially the inhomogeneous temperature distribution on the chip caused by the influence of the bond wires and second order effects which are obviously not taken into account in the one-dimensional thermal model.
Interestingly the model calculates junction temperatures of more than 300°C close to the destruction limit. This temperature range could be confirmed by high-speed thermograph photos of the chip surface. Figure 12 shows the corresponding temperature profile on the right in which the areas shadowed by the bond wires are clearly visible.

Note: Level-3_{th} models must never be abused for circuit design outside the safe operating area. The final decisive component specification is always the data sheet!!

Due to the presence of exactly defined thermal nodes, the Level 3_{th} models are excellently suited for studying and optimizing the interaction of a transistor with its thermal environment.
The same rules apply basically as described in chapter 2 for the model description of the component-external cooling conditions. Under simple heat flow conditions the thermal equivalent elements, e.g. of a heat sink, can be determined directly from the physical structure. In the case of more complex conditions, measurements or FEA analyses are required.
Figure 13 shows the considerations for obtaining a first approximation of a thermal equivalent circuit in a practical example. A component in a TO220 package, mounted with a 0.3mm thick insulating foil on a small aluminum heat sink is assumed. The

selected heat sink has a thermal resistance of 25K/W and a mass of 2g according to the data sheet.

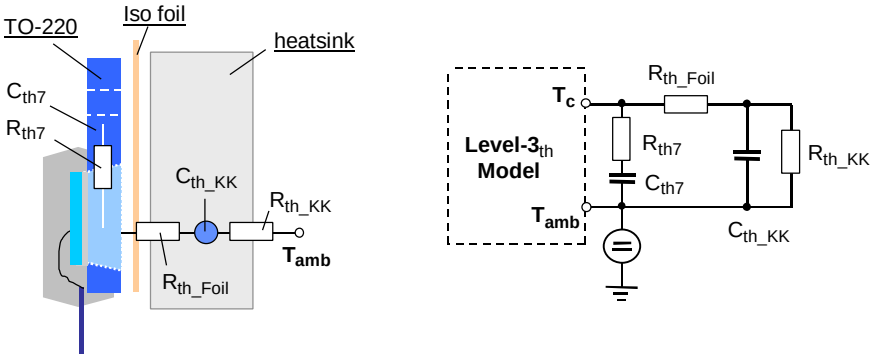


Fig. 13: A practical example of a first order thermal equivalent circuit diagram for a transistor with heat sink.

With the material data specified in table 2 the thermal capacitance of the heat sink is calculated at

$$C_{th\_KK} = 0{,}95\frac{J}{g\cdot K}\cdot 2\,g = 1{,}9\frac{J}{K} \qquad (13)$$

Together with the thermal resistance of the heat sink of Rth_KK = 25K/W the dominant thermal capacitances of the package and heat sink (Cth6, Cth7, Cth_KK) determine the thermal transient time of the whole system. Since this is by definition a small, compact heat sink, there is no need to divide the structure into several RC elements.

The metal surface of a TO-220 package is about 1cm^2. This gives a thermal resistance of the foil according to the formula specified in figure 2 of:

$$R_{th\_Folie} = \frac{0{,}3\,mm}{1.1\frac{W}{m\cdot K}\cdot 1cm^2} = 2{,}7\frac{K}{W} \qquad (14)$$

With this high resistance, the foil causes a heat accumulation effect which in turn leads to an increased lateral heat propagation inside the package. In the transistor model itself only the thermal capacitance of the pyramid stump shaped metal part below the active chip surface is taken into account, the lateral heat propagation also couples the rest of the metal volume however. At an assumed active chip surface area of 10mm^2 about 1g of copper is left over around the pyramid stump from which a value of 0.39J/K can be estimated for Cth7 and about 0.2K/W for Rth7 from the geometry. This completes determination of all the elements of the external thermal equivalent circuit diagram. The example shows how simply and intuitively distributed structures can be modeled by branchings in the line equivalent circuit diagram. Despite the greatly simplified method of observation, appropriate simulations demonstrate a very good match with real measuring results.

The simulation also allows a very simple reference to the classic Zth diagram to be derived. If the transistor is loaded with a constant power dissipation of 1W, the heating curve Tj(t) - Tamb immediately provides the known representation of the transient thermal impedance in double logarithmic form.

	ρ [g/cm3]	λ_{th} [W/(m·K)]	c [J/(g·K)]
Silicon	2,4	140	0,7
Solder (Sn-Pb)	9	60	0,2
Cu	7,6...8,9	310...390	0,385...0,42
Al	2,7	170...230	0,9...0,95
Al_2O_3	3,8	24	0,8
FR4	-	0,3	-
Heat conductive paste	-	0,4...2,6	-
Insulating foil	-	0,9...2,7	-

Table 2: Thermal data for common materials

Figure 14 shows by means of a further example from practice how much the new Level-3_{th} models simplify circuit design. A low voltage MOSFET is considered which switches an unclamped inductive load – in this case an ABS valve.

Due to the missing clamping, the inductance drives the transistor to drain source voltage breakdown (avalanche) each time it is switched off. The high voltage in conjunction with the current flow causes a high peak power dissipation.

In this case the determination of the maximum junction temperature by classic means, i.e. using only the Zth diagram, is rather complicated and susceptible to error – especially with pulse sequences and a power dissipation profile which is not rectangular. On the other hand the simulation not only supplies the results in the shortest time, various influential parameters can also be examined very simply.

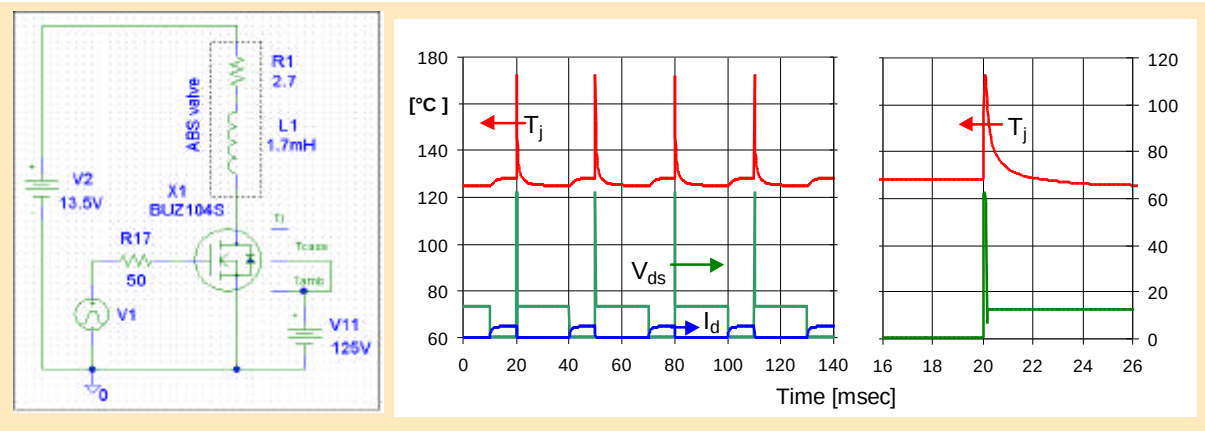


Fig. 14: Simulation of the junction temperature in periodic avalanche operation

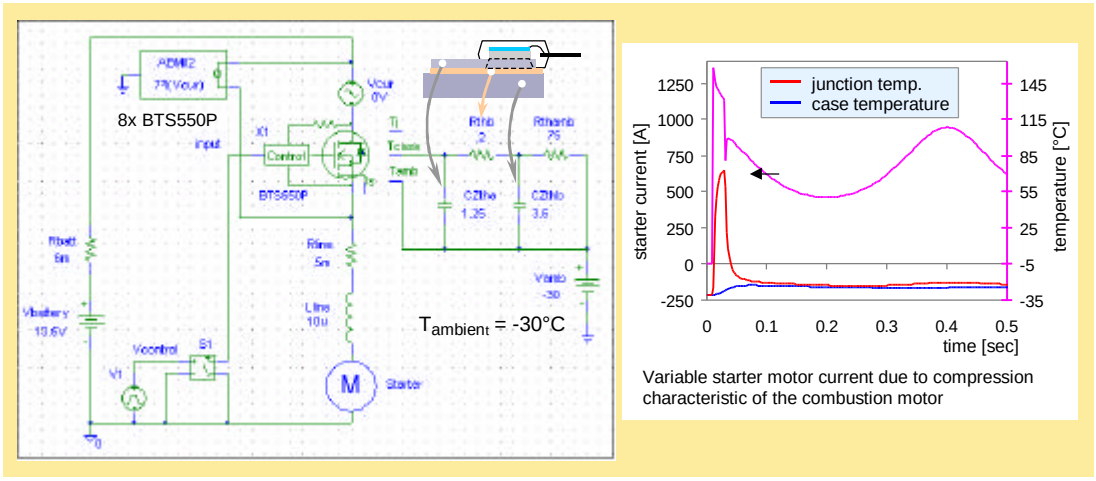
For detailed or worst case conditions, it should be noted that the temperature dependence of the breakdown voltage and the internal resistance in avalanche operation

are not implemented in the present models.

Smart Power models

The modeling of the dynamic inherent heating forms the basis of the simulation models for Smart Power components because basic protection functions are based here on the evaluation of the chip temperature. The example shown in figure 15 illustrates an 8-fold parallel circuit of high-current PROFETs used here to switch a non-linear load – a car starter in this concrete case. The model of the starter contains both the high start-up current and the periodic current changes caused by the changes in load effected by the compression processes of the combustion engine. Due to the high start-up current of the engine, in conjunction with the resulting turn-on losses, the knowledge of the maximum junction temperature in this dynamic process is just as important for the system design as the junction and package temperature which is affected by the load cycle in the ON state. The behavioral models for the components provide the system designer with a very efficient tool for this.

The models of the Smart Power components contain all the important component properties. For example in the high current PROFET models the short-circuit and overtemperature monitors, the overvoltage clamping, the sense current behavior, the inverse current capability and many other properties are implemented as well as the turn-on and turn-off behavior typical for highside switches with charge pump.



Variable starter motor current due to compression characteristic of the combustion motor

Fig. 15: Dynamic temperature modeling forms the basis for Smart Power simulation models. The actuation of a car starter by means of several high current PROFETs is illustrated.

Further information can be found under::
http://www.infineon.com/products/36/36.htm

[1] Datenbuch „*Leistungshalbleiter*“ (02.97), Siemens AG, S. 115ff.

[2] Geiling, L.: *Über die elektrische Nachbildung von Wärmeleitungsvorgängen*, Siemens Zeitschrift **35** (1961), S. 98-104