Technical Requirements
i^2C Protocol for the CPL Platform
AC/DC rectifiers and DC/DC converters

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1 Introduction

The Digital Interface for Power Supplies is fully compliant to the new Power Management Bus PMBus™ requirements. The following is a summary of the code implemented in this document;

'Manufacturer Specific' commands permitted by the PMBus spec were used to support instructions that either do not exist in the general specification or that make the *host-slave* interface simpler, smoother and more efficient. Deviations from the standard protocol of the specification are noted.

In this specification the SMBusAlert# signal gets cleared when a *host* addresses the power supply with the exception of those status/alarm indicators that require a clear_flags instruction to clear. The SMBusAlert# for these indicators gets cleared when the clear_flags is received with the exception of the invalid_data bit that can stay active HI until data within the working range is received.

Status and Alarm reporting is much simpler. These registers are continuously being updated with the latest state of the power supply. An SMBusAlert# is sent out whenever a state change occurs. However, the state of the power supply may have changed from the time the alert is flagged to when the *host controller* actually reads the state of the power supply. There are a number of reasons for retention of only the latest data. First, it makes the firmware code much simpler because the power supply does not have to keep records of various operational states. Second, the *host controller* gets the latest state of the power supply and therefore does not have to issue a number of read requests to verify what the latest state of the power supply is. Providing the latest information and operational efficiency is far more important then the ability to read back the historical state of a single event of the power supply. Since the standard product provides a latch off feature, important events are retained anyhow until the *Host* initiates a restart.

For example, lets say that a voltage surge somehow coupled into the output of the power supply and it shut down for over voltage. The power supply would automatically restart if the Auto Restart feature is invoked. Inquiry of the state of the power supply after the restart event would not indicate that the power supply shut down for over voltage. But it will indicate that a restart has occurred.

2 Hardware Signal Pins

2.1 Isolation

All signals, including Logic_GRD shall be isolated from the main output of the power supply (except for the RS485 protocol which is referenced to Vo(–). Logic_GRD is capacitively coupled to Frame_GRD inside the rectifiers. In the PEMs Logic_GRD and Frame_GRD are resistively coupled by a 100kΩ resistor. The maximum voltage differential between Logic_GRD and Frame_GRD should be less than 100Vdc.

2.2 Signal Definition (CPxxxx product)

All signal lines **(except PFW, OTW, FAULT, and PROTOCOL_SELECT)** shall be pulled HI to 3.3Vdc inside the power supply. An active level normally would pull down the signal to the LO (< 0.4Vdc) state, unless otherwise stated. Unless otherwise noted, signals are referenced to Logic GRD. Normally, 10k pull-ups are used.

Signal definition (continued)

Function	Label	Signal	Description
Enable	Enable	Input	Shortest pin of the power supply connector. A Logic LO (GRD) on this pin turns-ON the power supply. Used when configured for PMBus or analog communications. No impact when RS485 used.
ON/OFF	ON/OFF	Input	Short pin. Used for hot-plug. Ensures turn-ON only after all pins are engaged and turns OFF fast if the rectifier is removed from its shelf. **Ref: Vo(–)**
Power Fail Warning	PFW	Output	A HI indicates that output is ok. Changes to LO at least 5msec before the output voltage goes below permitted regulation. Sink current capability of 20mA. Applicable to rectifiers only.
Alert#	Alert#_0 or 1	Output	Buffered PMBUS compliant signal requesting service from the host.
Fault	Fault	Output	A LO shall indicate that an internal fault exists.
Module Present	MOD_PRES	Output	A 500Ω in series with Logic GRD indicates that a module is present.
Protocol select	Protocol	Input	No_Connect: PMBus or no software; 1 – 3Vdc: RS485; 0.8Vdc: DSP program . **Ref: Vo(–)**
Margining	Margin	Input	Hardware programmability of the output voltage set point
Overtemp warning	OTW	Output	Approximately 5°C prior to OTS this signal shall change to LO
Power Capacity	POWER_CAP	Output	HI indicates high capacity – high line operation. LO indicates low capacity – low line operation
Rectifier address	Unit_addr	Input	Pin configuring the unit address in volts. **Ref: Vo(–)**
Shelf address	Shelf_addr	Input	Pin configuring the shelf address in volts **Ref: Vo(–)**
Back bias	8V_INT	_	Connects diode or'ed 8Vdc between rectifiers. 320mA maximum output current, 80mA required per rectifier. **Ref: Vo(–)**
Mux Reset	Reset	Input	Resets the Philips PCA9541 when a LO is applied
Standby power	5V	–	5V @ 0.75A is provided for external use by either adjacent power supplies or the using system.

Note: PMBus output voltage commands override the hardware margin setting. Once overwritten the margin pin is ignored.

2.3 ALERT#

Accessible via the signal pins of the power supply, the power supply shall pull this signal LO when an **alarm** or a **state_change** occurred. This signal is the indication from the Power Supply *SLAVE* that it wants attention from the *MASTER*. The Alert# line will remain active until a read back occurs from the host to determine the reason for setting the Alert# signal. Please see the section on status and alarms for further definition of this signal. (see the Alert# Notification section below for a possible condition where the Alert# would not get reset by a power supply read operation).

Alert# is equivalent to the i^2C *Interrupt* signal and the SMBus SMBusAlert# signal.

2.3.1 Read back delay recommendation

The power supply issues the Alert# notification as soon as the first state change occurred.

During an event a number of different states can be transitioned to before the final event occurs. If a read back is implemented rapidly by the host a successive Alert# could be triggered by the

transitioning state of the power supply. In order to avoid successive Alert#s and read back and also to avoid reading a transitioning state, it is prudent to wait more than 2 seconds after the receipt of an Alert# before executing a read back. This delay will ensure that only the final state of the power supply is captured.

2.3.2 Successive read backs

Successive read backs to a module should not be attempted at intervals faster than every 1 second.

2.3.3 Alert# notification

The power supply can issue and Alert# from either its internal controller or from the PCA9541 i^2C bus master selector that provides buffering and master selection to the two redundant / independent i^2C lines. The Alert# signal to both i^2C controllers funnels through the PCA9541 master selector that also buffers these signals to both controllers.

The PCA9541 can issue an Alert# even when single bus operation is selected where the bus master selector has not been used or addressed. This may occur because the default state of the PCA9541/01 integrated circuit issues Alert# to both i^2C lines for all possible transitioning states of the device. For example, a RESET caused by a glitch would cause the Alert# to be active.

If the PCA9541 is not going to be used in a specific application (such as when only a single i^2C line is utilized), it is imperative that interrupts from the PCA9541 are de-activated by the host controller. To de-activate the interrupt registers the PCA9541 i^2C port needs to address the device in the 'write' mode, the interrupt enable (IE) register needs to be accessed and the interrupt masks have to be set to HI '1'. (Note: do not mask bit 0 which transmits Alert# from the power supply).The command will take the form

Start	Unit Address								Command Code			IE Register	Stop
1	7	6	5	4	3	2	1	0	1	8	1	8	1
S	1	1	1	0	A2	A1	A0	0	A	0x00	A	0x0E	P

There are two independent interrupt enable (IE) registers, one for each controller channel (i^2C-0 and i^2C-1). The interrupt register of each channel needs to be configured independently. That is, channel i^2C-0 cannot configure the IE register of i^2C-1 or vise-versa.
This command has to be initiated to the PC9541 only once after application of power to the device. However, every time a restart occurs the PCA9541 has to be reconfigured since its default state is to issue Alert# for its internal status change.

If the application did not configure the interrupt enable register the Alert# line can be cleared (de-activated), if it has been activated by the PCA9541, by reading back the data from the interrupt status registers (Istat). Please refer to the PCA9541 product data sheet for further information.

3 Dual Master Controller Capability

The power supply shall be designed to accept redundant master control such that two independent controllers may communicate via separate i2c lines.

Selection of the controlling master is accomplished via the use of the PCA9541 option /01 i^2c mater selector. The device is programmed such that upon start-up channel 0 is connected to the power supply. In this fashion applications that require only a single controller do not have to configure or use the device. For further information on programming this device see the section on PCA9541 Programming. The two communication lines must be referenced to a single Logic GRD.

4 Default State Configuration

The power supply is programmed to a factory set default state**.** Whenever power is removed from the control circuitry the default state shall be reestablished.

This default state cannot be overwritten.

5 Addressing

5.1 Firmware Executed Device ID

Address bits A2, A1, A0 set the specific address of the power supply. The least significant bit x (LSB) of the address byte configures write [0] or read [1] events. In a ***write*** command the system instructs the power supply. In a ***read*** command information is being accessed from the power supply.

	Address Bit							
	7	6	5	4	3	2	1	0
PCA9541 – 2 channel selector	1	1	1	0	A2	A1	A0	R/W
Micro controller	1	0	0	0	A2	A1	A0	R/W
External EEPROM	1	0	1	0	A2	A1	A0	R/W
General Call Address (Global Broadcast)	0	0	0	0	0	0	0	0
Concentrator Card (future use)	1	1	0	1	A2	A1	A0	R/W
	MSB							LSB

The **Global Broadcast** instruction executes a simultaneous ***write*** instruction to all power supplies. A ***read*** instruction cannot be accessed globally.

The three programmable address bits are the same for all i2c accessible devices within the power supply.

5.2 Global Broadcast

This is a powerful command because it can instruct all power supplies to respond simultaneously in one command. But it does have a serious disadvantage. Only a single power supply needs to pull down the ninth *acknowledge* bit. To be certain that each power supply responded to the global instruction, a *READ* instruction should be executed to each power supply to verify that the command

properly executed. The GLOBAL BROADCAST command should only be executed for write instructions to slave devices.

Note: The PCA9541 i2c master selector does not respond to the GLOBAL BROADCAST command.

5.3 Address Configuration

Two signal pins configure the address of the power supply. The *unit address* pin configures the power supply location within the shelf. The *shelf address* pin configures the shelf address. N ote that the I^2C protocol limits the number of selectable power supplies to 8.

The rectifier learns its address the first time it is turned ON either when commercial power is applied or when the rectifier is hot inserted into a live backplane. The rectifier will retain its address as long as bias is supplied to the internal electronics.

Care must be taken to bleed down the internal bias power inside the rectifier when attempting to change the physical slot location. A rule of thumb is to allow the rectifier to power down until the fans stop spinning. If this delay is not implemented, the rectifier may retain its previous slot address and respond incorrectly to bus commands.

Power supply addressing of the Lineage Shelf increments left to right as viewed from the front;

RECTIFIER 1	RECTIFIER 2	RECTIFIER 3	RECTIFIER 4

Within each shelf the rectifier address is configured by connecting a resistor from the **unit_address** pin A-1 to Vout(-). This resistor will complete a divider network that starts from 3.3Vdc via a 10kΩ resistor to the **unit_address** pin. The resistor value should be calculated such as to create the nominal voltage shown below.

			I^2C address	
Rectifier	Resistor Value	Nominal voltage	A1	A0
1	30K	2.477	0	0
2	14K	1.925	0	1
3	6K	1.243	1	0
4	2.5K	0.654	1	1

Shelf addressing is somewhat different because an internal pull-up does not exist. In the Lineage shelf a source voltage 5Vdc is developed by an LDO from the common diode or'ed redundant control Vcc (8V_INT) generated from each supply. This voltage is referenced to Vout (-). Resistors are then used to create the voltage levels shown below for the **shelf_address** pin. Up to 8 shelves can be paralleled. It is up to the user to separate the i2c lines of these shelves to ensure that duplicate addressing does not occur.

Shelf	1	2	3	4	5	6	7	8
Max. voltage	3.45	2.97	2.56	2.14	1.70	1.25	0.80	0.25
Nominal voltage	3.30	2.86	2.4	1.96	1.50	1.10	0.60	0.01
Min. voltage	3.00	2.60	2.18	1.73	1.29	0.84	0.30	0
Address bit- A2	0	1	0	1	0	1	0	1

6 Standard Instruction

The standard instruction takes the form shown below. Up to two bytes of data may follow depending on required data content. PEC is mandatory and includes the address and data fields. Note: Data fields are optional

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave address	Wr	A	Command Code	A	Low Data Byte	A	High Data Byte	A	PEC	A	P

☐ Clear area indicates Master to Slave communications throughout this document.
▒ Shaded area indicates Slave to Master communications throughout this document.
SMBUS annotations; S – Start , Wr – Write, Sr – re-Start, Rd – Read,
A – Acknowledge, NA – not-acknowledged, P - Stop

7 Command Codes

Upon power interruption or turn-ON, the power supply shall default to its factory-programmed state.

FUNCTION	COMMAND	CODE	Data Bytes
ON/OFF	OPERATION	0x01	1
Clear Status Info Registers	CLEAR_INFO_FLAGS	0x03	0
Set Output Voltage	Vout_ Command	0x21	2
Set OV_Fault_Limit	Vout_OV_Fault_Limit	0x40	2
Reads Status & Alarm registers, output voltage, output current and temperature levels	READ_DATA_STRING	0xD0	9
Test LEDs	Flash_LEDs_ON	0xD2	0
Turn-off Test LEDs	Flash_LEDs_OFF	0xD3	0
Turn-ON service LED	Service_LED_ON	0xD4	0
Turn-OFF service LED	Service_LED_OFF	0xD5	0
Enable EEPROM upper memory write	EEPROM_write_ON	0xD6	0
Disable EEPROM upper memory write	EEPROM_write_OFF	0xD7	0
Latch OFF upon failure	INHIBIT_RESTART	0xD8	0
Automatically restart after a failure	AUTO_RESTART	0xD9	0
Start isolation test	ISOLATION_TEST	0xDA	0
Inhibit output droop	INHIBIT_Vout_DROOP	0xDB	0
Read input voltage and input power	READ_INPUT_STRING	0xDC	3
Read Firmware Revision	READ_FIRMWARE_REV	0xDD	3
Accumulated Operational ON state	READ_RUN_TIMER	0xDE	3
Operate Fan at HI Speed	FAN_HI_Speed	0xDF	3
Operate Fan at NORMAL Speed	FAN_NORMAL_Speed	0xE0	0
Read fan speed	READ_FAN_SPEED	0xE1	4

8 Command Descriptions

8.1 ON/OFF

By default the Power supply is turned **ON** at power up as long as *ENABLE* is active LO. The System Controller (SC) uses this signal to request turn **OFF** of individual Power supplies.
This data byte follows the OPERATION command.

FUNCTION	LOW DATA BYTE	FUNCTION	LOW DATA BYTE
Unit ON	0x80	Unit OFF	0x00

Cycling the power supply OFF, waiting at least 2 seconds, and then ON accomplishes a **RESET** instruction. All alarms and shutdowns are cleared during a restart.

8.2 Clear_Info_Flags

This command clears information bits in the STATUS registers, these include :

Isolation OK
Isolation Test Failed
Restarted OK
Invalid command
PEC error

Other bits may be cleared momentarily until another read is captured from the DSP.

8.3 Vout,: Changing Default Settings

Output voltage set-point and voltage protection level of the power supply is adjustable. The program uses the DIRECT mode of data transfer described in the PMBus spec, where $y = [mX + b] * 10^{R}$. The calculated value y is the 10-bit value equivalent of the desired set-point for the controllers' A/D's. Reading data uses the same equation, y is the data sent from the power supply and x is the 'real' computed value. (Note: The 5-byte constants m, b, and R for the DIRECT mode equations reside in the external EEPROM. Refer to the **Extracting Coefficients** section for further information.)

8.3.1 Direct Mode Constants

FUNCTION	Operation	m	b	R
Output voltage	Write / read	400	0	0
Output voltage shutdown	write	400	0	0
Output Current	read	5	0	0
Temperature	read	1	0	0
Input Voltage	read	1	75	0
Input Power	read	1	0	0
Fan Speed setting (%)	read	1	0	0
Fan speed in RPM	read	100	0	0

8.4 Voltage Programming

The output voltage should be margined simultaneously to all power supplies operating in parallel using the Global Address (Broadcast) feature. If only a single power supply is instructed to change its output,

it may attempt to source all the required power which can cause either a power limit or a shutdown condition.

Software programming of the output voltage overrides the set point voltage configured during power_up. The default state cannot be accessed any longer unless power is removed from the DSP.

To properly hot-plug a power supply into a live backplane, the system generated voltage should get re-configured into either the factory adjusted firmware level or the voltage level reconfigured by the margin pin. Otherwise, the voltage state of the plugged in power supply could be significantly different than the powered system.

Voltage margin range: 42Vdc – 58 Vdc. (Product manufactured through first quarter 2008 may not margin down below 44Vdc. In that case the power supply will indicate that the voltage range is outside its data range by setting the Invalid Data Status register bit.)

8.4.1 A Voltage Programming Example

The task: set the output voltage to 50.45Vdc
The constants for voltage programming are: m = 400, b and R = 0.
Multiply the desired set point by the m constant, 50.45 x 400 = 20,180.
Convert this binary number to its hex equivalent: 20,180b = 4ED4h
The standard command: LSB = D4h sent first, then MSB = 4Eh sent next.

8.5 Operate Fan at HI Speed [0xDF]

This command instructs the power supply to increase the speed of the fan. The data byte provides the duty cycle in percent up to 100% , i.e. 64h. The command can only increase fan speed, it cannot instruct the power supply to reduce the fan speed from its internal control.

8.6 Operate Fan at NORMAL Speed [0xE0]

This command returns fan control to the power supply. It does not require a trailing data byte.

8.7 Read_Data_String – (basic READ)

The embedded program continuously updates the STATUS, ALARM, VOLTAGE, CURRENT, and TEMPERATURE data registers of the power supply. These registers store only the latest information. An event that caused the power supply to send an *INTERRUPT,* may have changed by the time the *host* gets around to do a read. If the power supply shut down for any reason and then restarted, this will be noted in the STATUS registers so the *host* will know if a restart occurred.

It is far simpler and less burdensome to maintain only the present state of the power supply. This provides for a much more efficient code because the *host* immediately gets the latest up-to-date information. If the data would have been frozen, the *host* would have required at least two reads, one to get the state of the interrupt and the second to verify the present state of the power supply.

A single *READ* command executes all monitoring and status information in one data string. This command is implemented as ‘MANUFACTURER SPECIFIC’. The reading of individual data strings is not supported.

The *READ* Data String shall take the form:

1	7	1	1	8	1	1	7	1	1
S	Slave address	Wr	A	Command Code 0xD0	A	Sr	Slave Address	Rd	A

8	1	8	1	8	1	8	1	8	1
Byte Count = 9	A	Status-2	A	Status-1	A	Alarm-2	A	Alarm-1	A

8	1	8	1	8	1	8	1	8	1	1
Voltage LSB	A	Voltage MSB	A	Current	A	Temperature	A	PEC	No-ack	P

PEC calculation shall include all data bytes after the restart including the slave address.

The power supply shall correctly respond to a READ instruction even if the command code may have been misinterpreted because the WRITE instruction code was not properly transmitted. The read response will always return this data string and ignore the other READ commands such as input, run timer and fan speed. This modification is implemented to improve the robustness of communications.

8.7.1 Recognition of Loss of input AC

5Vdc, Logic_GRD and 8V_internal bias should be interconnected among power supplies in order to maintain communications with a power supply even if its AC input power is interrupted. (the assumption here is that not all power supplies are connected to the same feeder). Lineage Power shelves are designed with this interconnection between the J1 and J2 connectors.

In the Lineage Power shelf, up to four power supplies are paralleled in a 1U high shelf. If three of the power supplies lose their AC input, the fourth power supply does not have sufficient capacity in its 8V_internal bias to power the internal electronics of the other three power supplies. In this case the 8V_internal bias of the working power supply will likely current limit; thus lowering the 8V_internal bias voltage being delivered to the remaining power supplies. When the 8V_internal bias to the micro gets below the lower voltage threshold the micro stops updating the status and alarm registers to the i2c micro that is powered from the 5Vdc source. The cut-off threshold is independently controlled within each micro controller. It is therefore unknown when precisely a power supply stops its internal communications.

The i2c micro controller within each power supply will detect if internal communications with the internal micro stopped and will set to FF's the STATUS, ALARM, and PEC registers. The voltage, current and temperature readings will still be sent back but they are frozen in the states of the last completed transmission between the internal micro controllers.

The response will look like; 09 FF FF FF FF xx xx xx xx FF . (xx's annotate the actual voltage, current and temperature readings). If this read back is detected it should be interpreted as a loss of AC input to a number of power supplies and not as an unknown communications loss with incorrect information transmitted across the i2c bus.

Event: If the power supply detects the loss of AC voltage it would issue a hardware interrupt followed by changing the ALARM register indicators **Vin_out_of_range**, and possibly **No_primary_detected, External_Fault** or **Primary_fault** for at least 20 – 30 seconds prior to the loss of 8V_internal bias.

8.7.2 Read back Accuracy

The output voltage reading is the measurement on the cathode side of the or'ing function (before the or'ing function). Otherwise the reading would be nothing more than the output bus voltage. The accuracy of the voltage reading is approximately ±6%.

The accuracy of the current reading is approximately ±5% of the full load current of the power supply. That is, as the current becomes lighter the accuracy of the reading is reduced.

The accuracy of the temperature reading is approximately ±5% near the trip level temperatures. The temperature reading is not linear. The accuracy below 60 – 70 C is reduced. The limitation is the monitoring accuracy of the thermistors.

8.7.3 Temperature Reading

The power supply monitors three different heat sinks for control and shutdown. Two of the monitored sections are on the primary side and these are the Boost and the primary side of the DC/DC converter. Monitoring of these events is accomplished on the primary side and information on the actual temperature measurements does not get fed to the secondary side control DSP. The only information fed back is whether the temperature level is too high so that the DSP can issue a warning or notify the *host* that an over temperature condition has occurred on the primary side. So, alarm and shutdown can be triggered by either of these two monitored sections without the ability to assess how hot these sections are running.

The third section monitored is the secondary side of the DC/DC converter. This is the data being read back during a READ instruction. Temperature of the DC/DC section is a function of both inlet air and output load and thus it provides an accurate representation of the temperature inside the box. The power supply is designed to provide an over temperature alarm at approximately 97°C and a shutdown at about 107°C. This information can be used to assess the operating point of the power supply.

8.7.4 A Voltage READ Example

Assume that the read back comes back as D44E.
The read back routine sends back first the LSB and then the MSB. So the actual hex number is 4ED4h.
Convert the hex number into its decimal equivalent; 4ED4h = 20,180d
Divide this value by the m constant 400; 20,180/400 = 50.45Vdc.
The divisor for current read back is 5 and for temperature read back it is 1.

8.7.5 A Current READ Example

Let's assume that the read back is 96h.
Convert the hex number into its decimal equivalent; 96h = 150d
Divide this value by the m constant of 5; 150/5 = 30 amperes.

8.8 Read_Input_String

Some rectifiers report the input voltage and input average power (averaged over 1 – 10 seconds) of the power supply. (Data needs to be converted from hex to binary)

1	7	1	1	8	1	1	7	1	1
S	Slave address	Wr	A	Command Code 0xDC	A	Sr	Slave Address	Rd	A

8	1	8	1	8	1	8	1	8	1	1
Byte Count = 4	A	Voltage	A	Power - LSB	A	Power - MSB	A	PEC	No-ack	P

8.9 Read_Firmware_Revision

A feature recently added to the firmware is the ability to read back the firmware revision of the primary micro controller, the secondary DSP and the i2c micro controller. The host application can determine whether this feature is supported by issuing the read statement during initialization.

1	7	1	1	8	1	1	7	1	1	8
S	Slave address	Wr	A	Command Code 0xDD	A	Sr	Slave Address	Rd	A	Byte Count = 4

1	8	1	8	1	8	1	8	1	1
A	Primary micro revision	A	DSP revision	A	I2c Micro revision	A	PEC	No-ack	P

Each released firmware revision shall increment the count by one.

A revision value of 0 indicates that the revision number for that section is not supported.

The read back returns one byte for each device (i.e. 00.21.14). 0x00 in the first byte indicates that the revision information for the primary micro is not supported. The number 21 for the DSP indicates revision 2.1, and the number 14 for the i2c micro indicates revision 1.4.

8.10 Read_Run_Timer [0xDE]

A feature recently added to the firmware is the ability to read back the run time of the power supply. The host application can determine whether this feature is supported by issuing the read statement during initialization.

1	7	1	1	8	1	1	7	1	1
S	Slave address	Wr	A	Command Code 0xDE	A	Sr	Slave Address	Rd	A

8	1	8	1	8	1	8	1	8	1	1
Byte Count = 4	A	Time - LSB	A	Time	A	Time - MSB	A	PEC	No-ack	P

This instruction records the operational ON state of the power supply in hours. The operational ON state is accumulated from the time the power supply is initially programmed at the factory. The power supply is in the operational ON state both in its standby or Output ON states. Recorded capacity is approximately 10 years of operational state.

Note: Although the accumulated run time is hourly reported the flash memory of the DSP is updated only once a day (every 24 hours) due to write limitations of the internal flash memory of the DSP. Fractional day information is lost if the DSP losses its bias voltage.

The operational ON state is recorded in hours and transmitted LSB first. Three hex data bytes are transmitted and followed by the PEC calculation. The data needs to be converted to binary form for the actual reading.

Once the maximum count is exceeded the count restarts again from 0.

8.11 Read_Fan_Speed [0xE1]

Returns the adjustment percentage and the individual fan speeds in RPM. If a fan does not exist (units may contain from 1 to 3 fans), or if the command is not supported the unit return 0x00.

1	7	1	1	8	1	1	7	1	1
S	Slave address	Wr	A	Command Code 0xE1	A	Sr	Slave Address	Rd	A

8	1	8	1	8	1	8	1	8	1	8	1	1
Byte Count = 5	A	Adjustment %	A	Fan-1	A	Fan-2	A	Fan-3	A	PEC	No-ack	P

Each data byte is in hex format. The data needs to be converted into binary format to represent the actual values. The adjustment % is the fraction of full speed that the DSP commands the fans to spin at. The three fan speed read backs are in RPM. For example; an adjustment of 33h converts to 51d and so the fans are commanded at 51% of full speed. A fan read back of 73h converts to 115 and actually represents 11,500 RPM. So the conversion needs to be multiplied by 100 to obtain RPM.

8.12 Test/Turn_OFF LEDs

Setting this bit will flash-ON the four front panel LEDs of the Power supply sequentially 7 seconds ON and 2 seconds OFF until instructed to turn OFF. The intent of this function is to provide visual identification of the power supply being talked to and also to visually verify that the LEDs operate and driven properly by the micro controller.

8.13 Turn_ON/Turn_OFF Service LED

Requests the power supply to ***flash***-ON the Service (ok-to-remove) LED. The ***flash*** sequence is approximately 0.5 seconds ON and 0.5 seconds OFF.

8.14 Enable/Disable EEPROM memory write

These instructions control write permissions into the upper ¼ of memory locations for the external EEPROM. A write into these locations is normally disabled until commanded through i2c to permit writing into the protected area. A delay of about 10ms is required from the time the instruction is requested to the time that the power supply actually completes the instruction.

8.15 Factory set default state

Currently manufactured CP1800 rectifiers are programmed to automatically restart after a shutdown has occurred. On some rectifiers, the default state is to latch off after a shutdown has occurred until the power supply is instructed to restart again.

Latest revisions of the standard CP1800 have been programmed to stay in a constant current state for up to 20 seconds during power up. This delay has been introduced to permit the orderly application of input power to a subset of paralleled rectifiers during power up. If the overload persists beyond the 20 second delay, the rectifier will revert back into its hiccup mode of overload protection.

The CP2000AC rectifier has a unique default state. As configured from the factory the power supply latches OFF on overvoltage and overtemperature. For overcurrent the power supply is programmed to maintain a constant output current indefinitely. This feature enables the plug-in of individual units one at a time into an overload condition without causing unwanted shutdowns. The intent is to issue a **Enable_Restart** global command to the power supplies after all have been seated in the system so that a shutdown with continuous restart is enabled for overload protection. System software must establish and monitor this feature.
The CP2000DC provides a constant current limit at turn ON. However, once the PEM output reaches its regulation level it will go into the hiccup state automatically.

The **Inhibit_Restart** and **Enable_Restart** commands work identically in both default configurations and therefore backwards compatibility has been maintained.

Example: Power supplies configured for automatic restart as the default state; To change the response state to a **latch off** state the **Inhibit_Restart** command had to be executed. In latter revisions the default state is **latch off.** Early firmware written for systems that defaulted automatically to a restart could still issue the **Inhibit_Restart** command, but obviously nothing will change since the power supply was in the latch off state in the first place.

Warning, Power supplies configured for latchoff as the default state; Systems that desire the restart feature will have to initialize the power supply into the restart configuration the first time after the application of ac power and every time a power supply gets hot plugged into an operational system. The best method of such initialization is to issue the command via the global address that instructs all power supplies to change their state simultaneously.

8.16 Inhibit_Restart

The **Inhibit-restart** command directs the power supply to remain latched off for over_voltage, over_temperature and over_current. The command needs to be sent to the power supply only once. The power supply will remember the INHIBIT instruction as long as internal bias is active.

8.16.1 Restart after a latch off

To restart after a latch_off either of four restart mechanisms are available. The hardware pin **Enable** may be turned OFF and then ON**.** The unit may be commanded to restart via i2c through the *Operation* command by first turning OFF then turning ON . The third way to restart is to remove and reinsert the unit. The fourth way is to turn OFF and then turn ON ac power to the unit. The fifth way is by changing firmware from **latch off** to **restart.** Each of these commands must keep the power supply in the OFF state for at least 2 seconds, with the exception of changing to **restart**.

A successful restart shall clear all alarm registers, set the **restarted successful** bit of the ***Status_2*** register.

For early versions of the software, if the power supply has been physically removed from the backplane, if ac power has been interrupted from all power supplies, or if this is the only power supply in the system, the **Inhibit Restart** should be issued again for the power supply to latch off again.

A power system that is comprised of a number of power supplies could have difficulty restarting after a shutdown event because of the non-synchronized behavior of the individual power supplies. Implementing the latch-off mechanism permits a synchronized restart that guarantees the simultaneous restart of the entire system.
A synchronous restart can be implemented by;

1. Issuing a GLOBAL OFF and then ON command to all power supplies,
2. Toggling Off and then ON the ENABLE signal
3. Removing and reapplying input commercial power to the entire system.

The power supplies should be turned OFF for at least 20 – 30 seconds in order to discharge all internal bias supplies and reset the soft start circuitry of the individual power supplies.

8.17 Auto_Restart

The **Auto_Restart** feature attempts automatic restarts after a shutdown condition.

All three shutdowns, over_voltage, over_current, and temperature can be programmed to restart after a shutdown.

Over-voltage shutdown is programmed for three restarts. Delay from an over-voltage condition is around 1 second before a restart is attempted. After three attempted re-starts within a 1 minute window, the power supply will latch_off. If three restarts were not attempted within 1 minute, the counter is reset and the count for three restarts starts all over again.

The power supply is designed to detect a deep over-current condition by monitoring the output voltage. Deep over_current results when the output voltage falls below the lower monitored threshold documented in the power supply requirements document. (i.e. for the CP1800AC52 this level is 36Vdc). After an over-current shutdown the power supply will shall revert to a hiccup state indefinitely until a recovery from over current is detected. The hiccup state performance is documented in the individual power supply specification.

An over_temperature shutdown recovers when the temperature of the power supply cools down within normal operational levels.

8.18 ISOLATION_TEST

This command verifies functioning of output or'ing. At least two paralleled power supplies are required. The host software should verify that N+1 redundancy is established. If redundancy is not established the test can fail. Only one power supply should be tested at a time.

A READ_BACK to verify the completion of the *isolation test instruction* should be delayed for approximately 30 seconds to allow the power supply sufficient time to properly execute the test.

9 Data Verification – *PEC*

Packet Error Checking (PEC) based on the CRC-8 format, as outlined in the SMBus specification, shall be supported to ensure that the transmitted data stream is accurate.

10 Non-supported Commands or Invalid Data

The power supply shall notify the *HOST* if a non-supported command has been sent or invalid data has been received. Notification shall be implemented by setting the appropriate *Status* and *Alarm* registers.

11 Status Registers

11.1 Status-2

Register	Bit	Title	Description
Status_2 (ON=1=true)	7	PEC Error	The computed PEC does not match the transmitted PEC. The instruction has not been executed. Clear_Flags resets this register.
	6	Will Restart	The power supply will restart after a shutdown
	5	Invalid Instruction	The instruction is not supported. An ALERT# will be issued. Clear_Flags resets this register.
	4	High Power Capacity	High line power capacity of power supply
	3	Isolation test failed	This flag requires replacement of the power supply
	2	Restarted ok	Informs *HOST* that a successful *RESTART* occurred clearing the status and alarm registers
	1	Data out of range	Flag appears until the data value is within range. ALERT# clears after a READBACK. A clear_flags command does not reset this register.
	0	Enable pin HI	Power supply instructed to turn OFF via hardware

11.2 Status-1

Register	Bit	Title	Description
Status_1 (ON=1=true)	7	spare	
	6	Isolation test OK	Indicator that the Isolation_Test requested has been completed successfully.
	5	Internal fault	The power supply is faulty
	4	Shutdown occurred	The power supply is shut down
	3	Service LED ON	Used to identify a particular power supply
	2	External fault	The recorded fault is external, the power supply is OK
	1	LEDs flashing	Tests the LED display of the power supply
	0	Output ON (power good)	

11.2.1 Shutdown Occurred

This STATUS-1 bit clearly annotates that the power supply has shut down. The ALARM registers that follow further clarify what caused the shutdown, but by themselves, these bits do not indicate to the using system that the power supply has in fact been shut down. The Description of the register bit

notes that a shutdown has been implemented. However, with the shutdown bit also set the user does not have to refer to the specification to figure out whether a shutdown should/has-been implemented.

12 Alarm Registers

12.1 Alarm-2

Register	Bit	Title	Description
Alarm_2 (ON=1=true)	7	Fan Fault	A fan failure causes a power supply latched shutdown
	6	No primary detected	Internal fault of the primary section of the power supply
	5	Primary over temperature	Fault detection of either the boost or primary of DC/DC
	4	DC/DC over temperature	Secondary heat sink temperature of the DC/DC stage
	3	Output voltage lower than bus	Internal regulation failure
	2	Thermal sensor failed	Internal failure of a temperature sensing circuit
	1	5V out_of_limits	Either OVP or OCP of the 5V circuit has tripped
	0	Spare	

12.2 Alarm-1

Register	Bit	Title	Description
Alarm_1 (ON=1=true)	7	Unit in power limit	An overload condition that results in constant power
	6	Primary fault	Indicates either primary failure or INPUT not present. Used in conjunction with bit-0 and Status_1 bits 2 and 5 to assess the fault.
	5	Over temp. shutdown	One of the over_temperature sensors tripped the supply
	4	Over temp warning	Temperature is too high, close to shutdown
	3	In over current	Shutdown is triggered by low output voltage < 39Vdc.
	2	Over voltage shutdown	
	1	Vout out_of_limits	Indication the output is not within design limits. This condition may or may not cause an output shutdown.
	0	Vin out_of_limits	The input voltage is outside design limits

13 Predictive Failures

Alarm indicators that do not cause a shutdown are indicators of the potential failures of the power supply. For example, if a thermal sensor failed a warning is issued but an immediate shutdown of the power supply is not warranted. [added in rev 1.22]

Other potential predictive failures can be derived from information such as fan speed. If the speed of the fans vary by more than 25% from each other, this is an indication of a potential wear out condition and the module should be replaced before the fan would catastrophically fail and bring down the module with it.

13.1 Information Only Status and Alarms

The following alarms are for information only and should not cause a shutdown
Over temperature warning
Vout out-of-limits (above 36Vdc)
Output voltage lower than bus
Unit in Power Limit
Thermal sensor failed [added in rev 1.22]

14 Fault Management

The power supply shall record faults in the STATUS and ALARM registers above and notify the *MASTER* controller as described in the **Alarm Notification** section of the non-conforming event.

The STATUS and ALARM registers shall be continuously updated with the latest event registered by the rectifier monitoring circuits. A *host* responding to an SMBusALERT# signal may receive a different state of the rectifier if the state has changed from the time the SMBusALERT# has been triggered by the rectifier.

The power supply differentiates between **internal faults** that are within the power supply and **external faults** that the power supply protects itself from, such as overload or input voltage out of limits. The FAULT LED, FAULT PIN or i2c alarm is not asserted for EXTERNAL FAULTS. Every attempt is made to annunciate External Faults. Some of these annunciations can be observed by looking at the input LEDs;

Input voltage out of range: The Input LED will continue blinking as long as sufficient power is available to power the LED. If the input voltage is completely gone the Input LED is OFF.

Unit in Power Limit or in Current Limit;

When output voltage is > 36Vdc the Output LED will continue blinking.

When output voltage is < 36Vdc, if the unit is in the RESTART mode, it goes into a hiccup. When the unit is ON the output LED is ON, when the unit is OFF the output
LED is OFF.

When the unit is in latched shutdown the output LED is OFF.

15 Alarm or State_Change Notification

The power supply shall support the SMBALERT# signal.

15.1 Alarm Definition

The *SLAVE* power supply must notify the *HOST* of a warning (minor), shutdown (major) alarm, or communication error triggered by non-supported commands, invalid data, or PEC errors.

15.2 State_Change Definition

A **state_change** is an indication that an event has occurred that the *master* should be aware of. The following events shall trigger a **state_change**;

Initial power-up of the system when ac gets turned ON . This is the indication from the rectifier that it has been turned ON for the first time. Note that the *master* needs to read the status of each power supply to reset the system_interrupt. Each power supply will release its *interrupt* after it has been poled.

When a **fault** occurred.

Recovery from a **fault** condition.

The signal shall remain in it's LO state either until:

The power supply is addressed by the *MASTER* and a *READ Data String* occurred

16 FRU-ID

The upper quarter of memory starting from address 6144 shall be reserved for factory ID and factory data.

Memory Location Decimal	Memory Location (HEX)	Length (bytes)	Format	Static Value Type	Description	Notes/Example
6144d	0x1800	12	ASCII	fixed	Lineage - Product ID	CP1800AC52
6156d	0x180C	10	ASCII	fixed	Lineage – Part Number	123456789x or C123456789
6166d	0x1816	6	ASCII	variable	Lineage - Hardware revision	x:xxxx controlled by PDI series #
6172d	0x181C	6	ASCII	variable	spare	
6178d	0x1822	14	ASCII	variable	Lineage - Serial_No	01KZ51018193xx 01 …. Year of manufacture - 2 KZ … factory, in this case Matamoros 51 .. week of manufacture _____018193xx serial # mfg ch
6192d	0x1830	40	ASCII	variable	Lineage - Manufacturing location	"Matamoros, Tamps, Mexico"
6232d	0x1858	8	ASCII	fixed	spare	
6240d	0x1860	2	HEX	fixed	spare	
6242d	0x1862	158	ASCII	fixed	Customer Information	These fields are reserved for use the customer.
6400d	0x1900	5	HEX	Fixed	M, B, & R for voltage read	M & B are 2 bytes each sent as M
6405d	0x1905	5	HEX	Fixed	M, B, & R for current read	and then LSB. R is one byte. Thes
6410d	0x190A	5	HEX	Fixed	M, B, & R temp read	are stored as two's complement.
6415d	0x190F	5	HEX	Fixed	spare	
6420d	0x1914	5	HEX	Fixed	M, B, & R for voltage set	See the section on Direct Mode
6425d	0x1919	5	HEX	Fixed	M, B, & R for input voltage read	Constants Stored in the EEPROM the constants stored in these field
6430d	0x191E	1	HEX	Variable	Validation Checksum	
6431d	9x191F	5	HEX	Fixed	M, B, & R for input power read	
6436d	0x1924	5	HEX	Fixed	M, B, & R for fan percent adjust	
6441d	0x1929	5	HEX	Fixed	M, B, & R for fan RPM read	

Notes:

Input, fan speed and RPM reads are available on only a select set of codes.
Validation checksum has recently been added for factory test purposes.
SUM=Addition from location 0x1800 to location 0x19FF without including serial number and checksum locations. chksum_value = 0xFF - (mask of SUM with 0x0000ff) write chksum_value byte to location 0x191E
Prior to 2007 the week of manufacture was derived by subtracting 20 from the number shown.

17 External EEPROM

A 64k-bit EEPROM is available across the i^2C bus for storing manufacturing data and providing a scratchpad memory function for customer use. The EEPROM is defined along the ST M34D64 part that is partitioned into an upper ¼ memory space that may be *write protected,* and the lower ¾ memory space that can be defined by customer needs.

17.1 Write Protect Feature

Writing into the upper fourth of memory requires defeat of the *write protect* feature (pulling down the Wp pin to ground). The *write protect* feature can be disabled via a software command instruction to the micro controller or by applying a 5Vdc pull-up to the **Module Present** pin of the power supply.

17.2 Page Implementation

The external EEPROM is partitioned into 32 byte pages. For a write operation only the starting address is required and subsequent data is automatically incremented by the EEPROM hardware. If the 32 byte limit is exceeded the device executes a wrap around feature that will start rewriting from the first address specified. Thus byte 33 will replace the first byte written, byte 34 the second byte and so on. One needs to be careful therefore not to exceed the 32 byte page limitation of the device address incrementing feature.

17.3 Protocol

Communications to the external EEPROM is handled directly across the i^2C bus. The protocol is defined in the manufacturer's data sheet. The power supply cannot communicate with the external EEPROM.

18 Dual i^2C Busses

The CPL platform provides two independent, redundant i2c busses that can interface to two independent *host controllers*. Either of the *hosts* can take over control of the communications bus and the power supply.

Steering between the two i2c communications lines is the responsibility of the Philips PCA9541/01 which is a 2-to-1 I²C master selector. The PCA9541 has its own independent address.

Either master at any time can gain control of the power supply

Please consult the Philips data sheet and various applications notes for information on how to communicate and control this device.

For applications that do not require the dual i2c feature of the PCA9541/01, the device is totally transparent. I2c_0 is the default communications bus setting of the device. Applications may communicate directly to the power supply without communicating to the PCA9541.

19 Hot plug procedures

Careful system control is recommended when hot plugging a power supply into a live system. The predominant reason is that it takes about 15 seconds for a module to configure its address on the bus based on the analog voltage levels present on the backplane. If communications are not stopped during this interval, multiple devices may respond to specific instructions because the address of the hot plugged power supply always defaults to _ _ _ _000r/w until the module changes its address. This is especially a concern if EEPROMs are being addressed because this device does not require any start up time, it accepts only standard i^2C commands without the trailing PEC calculation which ensures that only the valid data is responded to, and therefore the EEPROM will communicate immediately, and potentially to the wrong address, after the reinsert before the final addressing is accomplished by the module.

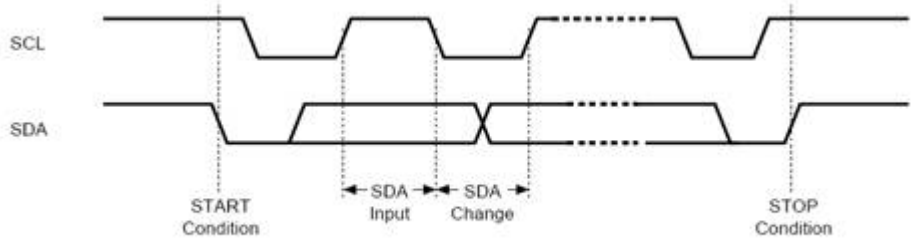
The recommended procedure for hot plug is the following: The system controller should be told which module is to be removed. The controller turns ON the service LED, thus informing the installer that the identified module can be removed from the system. The system controller should then poll the module_present signal to verify when the module is re-inserted. It should time out for 15 seconds after this signal is verified. At the end of the time out all communications can resume.

20 Implementation recommendations

Devices of CPL products that communicate across the bus adhere to the i^2C specification requirements. The μController, EEPROM and the multiplexer each have their own embedded drivers for bus communications that are not controlled by the power supply.

20.1 Change of state of the data line (SDA)

The SDA line changes states when the clock is HI to signify when the START and STOP commands of the protocol are being sent. During data transmission, SDA can only change states when the clock is LO. When the clock is HI the devices interpret the SDA as a data bit of HI or LO. If the SDA would transition while the clock is HI, this would either indicate a RESTART or a STOP condition.



20.2 Clock speed

The CPL platform was not evaluated for clock speeds faster than 100kHz. At the 100kHz rate, bus capacitance is limited to 400pf including contributions by wire-length and internal device capacitance.

Although the data sheets of the individual devices indicate that 400kHz clock speeds are supported we do not recommend speeds higher than 100kHz because we did not evaluate the power supplies at these clock speeds. Higher clock speeds also have additional constraints on bus capacitance, and maximum pulse rise and fall times.

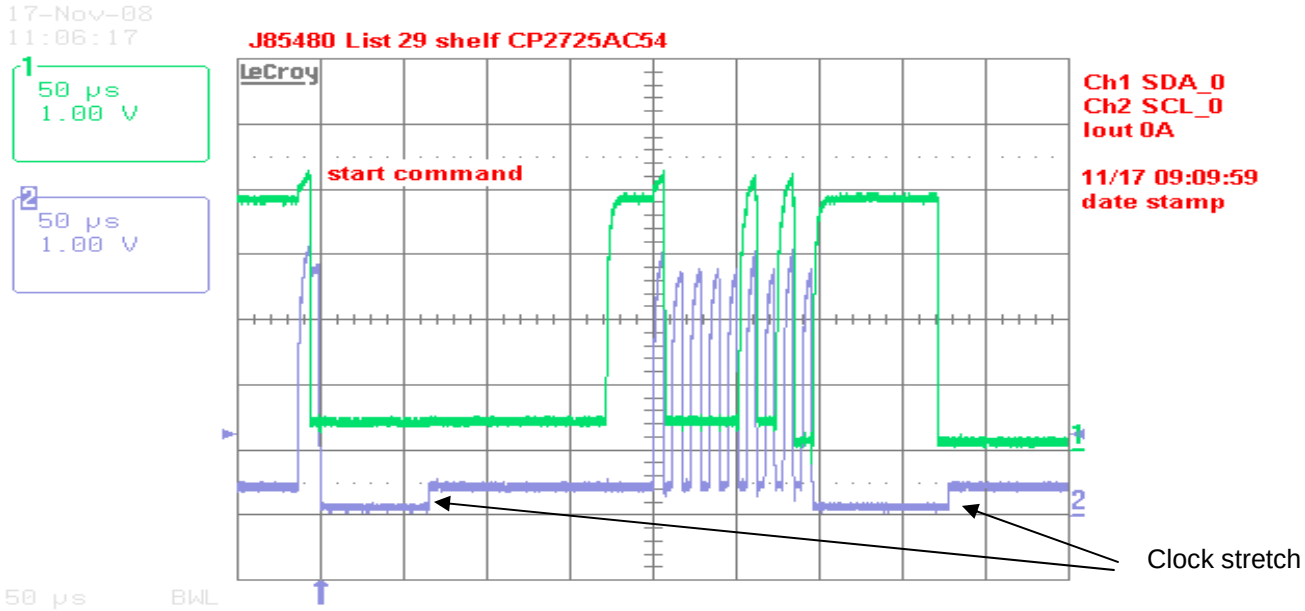
The minimum clock speed specified by SMBus is 10kHz.

20.3 Clock (SCL) stretching

The µController inside the power supply supports standard clock stretching. Basically, the µController will stretch (keep the clock LO) until it is ready to receive further instructions from the host controller. The host controller can recognize clock stretching, and refrain from issuing the next clock signal until the clock line is released, or it needs to delay the next byte of instruction / data beyond the interval of clock stretch of the power supply, which is readily recognized when the clock line goes HI.

A representative waveform below shows clock stretching by the CP2725AC54 power supply µController. Probing of the SCL line at the appropriate point clearly shows who pulls down the clock. When the LO level is closer to GRD the power supply pulls down the clock. The graph shows that clock stretching occurred both after the START command and after responding to the address of the µController. The duration of the clock stretch was slightly different and longer after responding to the address. Using this waveform as a reference suggests that at least 150µs of delay should be added between bytes to ensure the completion of clock stretching prior to starting the transmission of the subsequent byte.

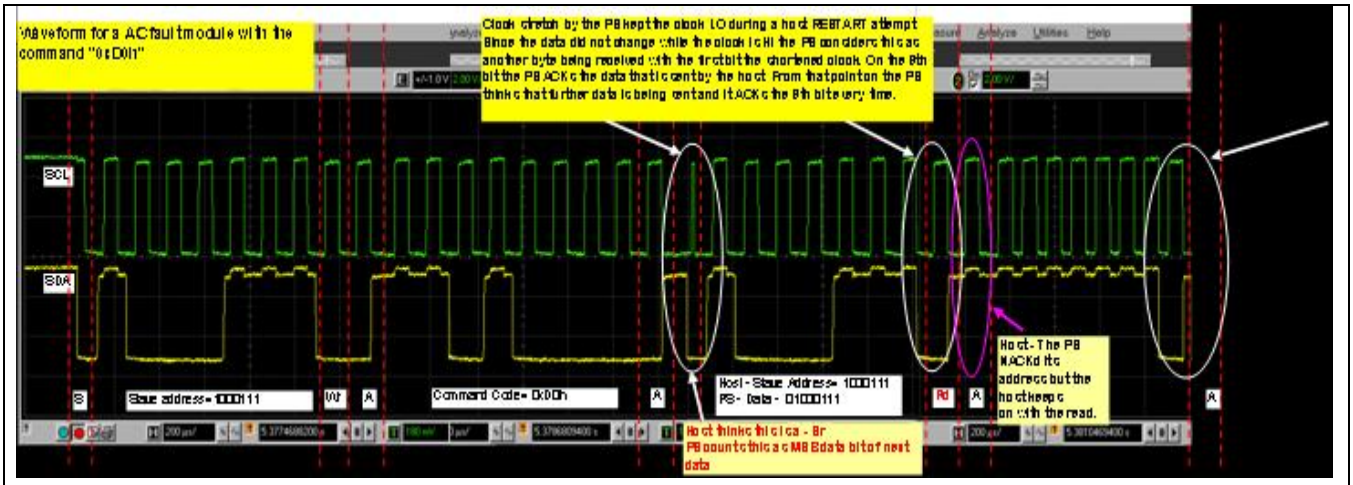
Note that clock stretching can only be performed after completion of transmission of the 9th bit, the exception being the START command.



Clock stretching example

Below is an example of a host controller that did not recognize clock stretching and did not implement any delay. During the RESTART attempt the power supply held the clock LO and therefore instead of a RESTART, only a standard data bit was recognized since SDA changed when clock was LO. The

RESTART followed by an address_read was therefore misinterpreted and the host controller could not read back the proper information.



20.4 Service request

Devices inside the power supply are SLAVE ONLY. Request for service by the power supply is initiated by setting the *SMBusAlert# / Interrupt* line LO. This is the only way that the power supply can alert the system controller that its state has changed and that the controller should verify the present state of the power supply.

20.5 Potential for data errors during hot-plug

When the module gets hot-plugged into an active system, the 5V and 8V source voltages to the communicating ICs are immediately available from the back-bias feature of the backplane. (Back bias provides communications capability even without input power present to the module.) The module is able to respond and communicate on the bus for about 30 seconds prior to the proper configuration of its slot address. During the 30 seconds the plugged-in module configures itself as the slot-1 address.

If during that time slot-1 is being communicated to, both slot-1 and the hot-plugged module will respond because they both have the same address. Read backs are not compromised because, unless both modules have identical data returned, the PEC error check will not compute properly and the data should be declared invalid. However, read back of the state of the PCA9541 multiplexer does not support error checking and therefore incorrect data could get received by the system controller since the state of the device is being fed back from two different sources.

The module_present signal, if properly implemented, provides the proper signal to the system that a new module has been inserted. The system can take action and delay communications to slot-1 for about 45 seconds. This would resolve the potential error reporting or error reading.

20.6 Internal data update rate

The update rate for data from the DSP to the I^2C µController is 200ms. Data going back to the DSP from the I^2C µController is also on a 200ms clock, but the two processes are asynchronous. The DSP/I^2C connection is a full duplex (TX line and RX line), so the data does not collide.

20.7 Re-initialization

The I^2C µController is programmed to re-initialize of no activity is detected on the bus for 5 seconds. This re-initialization is designed to guarantee that the I^2C µController does not hang up the bus. This rate is longer than the timing requirements specified in the SMBus specification, but it had to be extended in order to ensure that a re-initialization would not occur under normal transmission rates. It takes a few µseconds to accomplish the re-initialization and if during that time bus activity would commence the I^2C µController may not recognize the command. (i.e. a start condition).

21 Supporting Documentation

The following documents are accessible through the Lineage Power password protected website. Access to the website can be obtained through the Lineage Sales, marketing, or engineering support teams.

Using the Interface Board

This document describes the usage of an interface board that is connected to the 1U shelf for diagnostics purposes and for mating to the test GUI demonstration tool.

Application Guidelines for the Rectifier

Implementation procedures, optional configurations, setup

Functional Verification and Debugging Tool

Setup of the executable GUI, the general command set, application tips

22 Change History

22.1 Revision 1.2

Removed the SMBusALERT response requirement of section 11.2 The ALERT RESPONSE ADDRESS (ARA) command cannot be implemented. Devices can only recognize 2 addresses, their own specific address and the global command.

22.2 Revision 1.3

- Removed the requirement to support communications both with and without PEC. Communications with PEC of section 5 are always required.
- Under alarm response of section 10.5 deleted Fan Fault and Thermal Sensor Failed as errors that would not cause a shutdown.

22.3 Revision 1.4

- Modified Margining definition and adjacent foot note
- Added a **command** to turn-ON the HOST_NOTIFY_PROTOCOL feature. Added Status-1 bit-7 as the indicator to inform the *HOST* that this command will get executed.
- Added a **command** to read_back the program software revision. Modified section on software revision control.
- Changed constants of the DIRECT format to be consistent with implemented software
- Alert# has been further defined to include **state_change** events that would also trigger the Alert# line.

22.4 Revision 1.6

Removed the **Data Format Inquiry** command.

22.5 Revision 1.7

Added various operational clarifications throughout the document. These sections are noted with a bar on the left side of the document.

22.6 Revision 1.13

- Changed latch off as the standard shutdown feature
- Changed the status bit **Busy** to **Restart Implemented**
- Minor editorial changes made for clarity to the Status and Alarm register tables
- Changed the data format of the **Vendor name** and **Vendor IANA** number fields from HEX to ASCII to improve read back of these fields and enable better record capture in the labview GUI program
- Improved the robustness of the ENABLE signal by introducing a 30msec delay and a 5ms monitoring interval to ensure that noise or signal bounce would not trigger an event.
- All communications errors trigger a SMBusAlert#. (PEC error, data_out_of_range, invalid _command)
- Since we implemented only a single READ command, a READ instruction that does not follow the standard instruction set by issuing a WRITE first is also executed.

22.7 Revision 1.14

Added the command INHIBIT_Vout_DROOP for a new rectifier Family that is configured from the factory with an output voltage droop feature that is proportional to delivered output current.

22.8 Revision 1.15

Corrected power supply addressing instruction errors.

22.9 Revision 1.16

Added 10ms delay response between instruction completion that enables/disables the write protect feature of the EEPROM and execution of the event.

22.10 Revision 1.18

- The standard default state has been changed from latch off to hiccup.

22.11 Revision 1.19

Changed FRU-ID IANA number to HEX from ASCII. It was HEX originally and with only 2 bytes of storage area it cannot be changed.

22.12 Revision 1.20

Added voltage tolerance around the shelf ID programming voltage level.

22.13 Revision 1.21

Added input voltage and current read back for the new CP2725 platform.

22.14 Revision 1.22

- Changed read back of input current to read back of averaged input power over 1 – 10 seconds. This change resulted from feedback of OEMs of desired input data in a PMBus conference in 2007.
- Clarified that the power supply should not shut down if a thermal sensor failed but should only issue a warning.

22.15 Revision 1.23

- Clarified the need for configuring the PCA9541 mux interrupt enable (IE) registers so that the PCA9541 would not trigger undesired interrupts.
- Made some minor typo and other simple corrections.
- Added run_time recorder
- Added revision read back for DSP and secondary micro controller
- Changed read back of input voltage and input power for the CP2725 rectifier

22.16 Revision 1.24

- Deleted the capability to reduce the current limit or over temperature shutdown set points.
- Added software commanded output voltage adjust range of 42Vdc – 58Vdc to the Voltage Margin section.
- Added fan control and fan speed read to the protocol. Added read back constant for the conversion.
- Removed the protocol information for the PCA9541/01 and noted that this information should be obtained from the manufacturer.

22.17 Revision 1.25

- Changed multiplier for fan % to 1

- Added multiplier for fan RPM read to 100
- Added ability to read back fan % adjust level as well as individual RPMs.
- Added monitoring ability to issue an alarm if fan speed difference is more than 25%. Do not shut down but issue a predictive failure alarm.
- Changed the FRU-ID table to add the fan % adjust level and RPM constants and removed the current limit and Over temperature shutdown constants.
- Changed in the ALARM information 'over current shutdown' to ' in over current' to properly reflect the actual indication.
- Added FRU-ID validation checksum byte and deleted constants for thermal and overload write commands that have been removed.
- Added hot-plug recommendation section for EEPROM read/write
- Added read back recommendation no faster than every 1 second
- Explained the read back information for controller software revision.
- Removed Tyco reference (JEDEC and IANA number association) and firmware revision from the FRU-ID table. Clarified comcode number insertion in the FRU-ID field.

22.18 Revision 1.26

- Added note on run timer flash memory retention that is updated only once every 24 hours.
- Changed alarm register bit-3 from 'over current shutdown' to 'in over current' since the module could be either in latched shutdown or a hiccup condition.

22.19 Revision 1.27

- The description of isolation_test has been modified.
- Added FAULT reporting when input AC power and 8V_internal bias are not present

22.20 Revision 1.28

Added checksum derivation for FRU-ID validation.

22.21 Revision 1.29

- Corrected that a PEC error should get cleared by the clear_flags command.
- Corrected that a clear-flags command should not clear an invalid_data command until the proper data instruction is received.
- Corrected that a normal read back should not clear those STATUS/ALARM bits cleared specifically by the Clear_Flags command. The INTERRUPT/SMBus_Alert# signal should be active LO until all STATUS/ALARM signals are cleared.

22.22 Revision 1.30

- Date code embedded in the serial number of the FRU-ID is modified to reflect the latest factory practice.

- Added the section on Communications recommendation.

22.23 Revision 1.31

- Clarified input and fan read back
- Clarified the reason for the SHUTDOWN bit of the STATUS-1 register
- Added sections for re-initialization and internal communication rates.