6 MTOPS

Table 33 shows Composite Theoretical Performance (CTP) calculations. The calculations are stated in Millions of Theoretical Operations per Second (MTOPS) and are based upon a formula in the United States Department of Commerce Export Administration Regulations 15 CFR 774 (Advisory Note 4 for Category 4).

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Table 33. Composite Theoretical Performance (CTP) Calculation

Frequency	MTOPS Single-Core	MTOPS Dual-Core	MTOPS Triple-Core	MTOPS Quad-Core	MTOPS Six-Core
1600	8,667	16,267	23,867	31,467	46,667
1700	9,209	17,284	25,359	33,434	49,584
1800	9,750	18,300	26,850	35,400	52,500
1900	10,292	19,317	28,342	37,367	55,417
2000	10,834	20,334	29,834	39,334	58,334
2100	11,375	21,350	31,325	41,300	61,250
2200	11,917	22,367	32,817	43,267	64,167
2300	12,459	23,384	34,309	45,234	67,084
2400	13,000	24,400	35,800	47,200	70,000
2500	13,542	25,417	37,292	49,167	72,917
2600	14,084	26,434	38,784	51,134	75,834
2700	14,625	27,450	40,275	53,100	78,750
2800	15,167	28,467	41,767	55,067	81,667
2900	15,709	29,484	43,259	57,034	84,584
3000	16,250	30,500	44,750	59,000	87,500
3100	16,792	31,517	46,242	60,967	90,417
3200	17,334	32,534	47,734	62,934	93,334
3300	17,875	33,550	49,225	64,900	96,250
3400	18,417	34,567	50,717	66,867	99,167

7 APP

Table 34 shows the Adjusted Peak Performance (APP) calculations for the AMD Phenom™ processor and the AMD Athlon™ processor. The calculations are stated in millions of Weighted Teraflops (WT) and are based upon a formula in the United States Department of Commerce Export Administration Regulations 15 CFR 774 (Advisory Note 4 for Category 4).

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Table 34. Adjusted Peak Performance (APP) Calculation

Frequency	APP Single-Core	APP Dual-Core	APP Triple-Core	APP Quad-Core	APP Six-Core
1600	0.0019	0.0038	0.0058	0.0077	0.0115
1700	0.0020	0.0041	0.0061	0.0082	0.0122
1800	0.0022	0.0043	0.0065	0.0086	0.0130
1900	0.0023	0.0046	0.0068	0.0091	0.0137
2000	0.0024	0.0048	0.0072	0.0096	0.0144
2100	0.0025	0.0050	0.0076	0.0101	0.0151
2200	0.0026	0.0053	0.0079	0.0106	0.0158
2300	0.0028	0.0055	0.0083	0.0110	0.0166
2400	0.0029	0.0058	0.0086	0.0115	0.0173
2500	0.0030	0.0060	0.0090	0.0120	0.0180
2600	0.0031	0.0062	0.0094	0.0125	0.0187
2700	0.0032	0.0065	0.0097	0.0130	0.0194
2800	0.0034	0.0067	0.0101	0.0134	0.0202
2900	0.0035	0.0070	0.0104	0.0139	0.0209
3000	0.0036	0.0072	0.0108	0.0144	0.0216
3100	0.0037	0.0074	0.0112	0.0149	0.0223
3200	0.0038	0.0077	0.0115	0.0154	0.0230
3300	0.0040	0.0079	0.0119	0.0158	0.0238
3400	0.0041	0.0082	0.0122	0.0163	0.0245

2.3.16 HD mmmm FB pnc GR (125 W, DT, AM3) Thermal and Power Specifications

OPN			Phenom II X6 1055T HDT55TFBK6DGR[21]		Phenom II X6 1090T HDT90ZFBK6DGR[21]	
State	Specification[8]	Notes	Single-Plane	Dual-Plane	Single-Plane	Dual-Plane
S0.C0.Px	Tcase Max	1	55 °C to 62 °C		55 °C to 62 °C	
	Tctl Max	2	70 °C		70 °C	
	Tambient Min		5 °C		5 °C	
	Thermal Profile		AE		AE	
	Startup P-State	5	S0.C0.P0	S0.C0.P3	S0.C0.P0	S0.C0.P3
	HTC P-State	4	S0.C0.P0	S0.C0.P3	S0.C0.P0	S0.C0.P3
S0.Cx.Px	NB COF	6,7	2000 MHz	2000 MHz	2000 MHz	2000 MHz
	VID_VDDNB Min	11,7	N/A	1.050 V	N/A	1.050 V
	VID_VDDNB Max	11,7	N/A	1.175 V	N/A	1.175 V
	IDDNB Max	12	N/A	17.0 A	N/A	16.2 A
S0.C0.Pb0	CPU COF	6	N/A	3300 MHz	N/A	3600 MHz
	C-State Count	23	N/A	3	N/A	3
	TDP	22	N/A	125.0 W	N/A	125.0 W
	VID_VDD Min	9	N/A	1.250 V	N/A	1.250 V
	VID_VDD Max	9	N/A	1.475 V	N/A	1.475 V
	IDD Max	3,10	N/A	95.0 A	N/A	95.0 A
S0.C0.P0	CPU COF	6	800 MHz	2800 MHz	800 MHz	3200 MHz
	TDP	3,7	55.4 W	125.0 W	53.1 W	125.0 W
	VID_VDD Min	9	1.000 V	1.150 V	1.000 V	1.150 V
	VID_VDD Max	9	1.225 V	1.475 V	1.225 V	1.475 V
	IDD Max	3,10	32.9 A	89.7 A	31.4 A	92.8 A
S0.C0.P1	CPU COF	6	N/A	2200 MHz	N/A	2400 MHz
	TDP	3,7	N/A	101.0 W	N/A	98.5 W
	VID_VDD Min	9	N/A	1.100 V	N/A	1.100 V
	VID_VDD Max	9	N/A	1.400 V	N/A	1.400 V
	IDD Max	3,10	N/A	69.5 A	N/A	69.9 A
S0.C0.P2	CPU COF	6	N/A	1500 MHz	N/A	1600 MHz
	TDP	3,7	N/A	77.3 W	N/A	75.7 W
	VID_VDD Min	9	N/A	1.050 V	N/A	1.050 V
	VID_VDD Max	9	N/A	1.325 V	N/A	1.325 V
	IDD Max	3,10	N/A	50.9 A	N/A	50.4 A
S0.C0.P3	CPU COF	6	N/A	800 MHz	N/A	800 MHz
	TDP	3,7	N/A	55.4 W	N/A	53.1 W
	VID_VDD Min	9	N/A	1.000 V	N/A	1.000 V
	VID_VDD Max	9	N/A	1.225 V	N/A	1.225 V
	IDD Max	3,10	N/A	32.9 A	N/A	31.4 A
S0.C1.Pmin	Core Power (Pre-Flush)	20	N/A	16.4 W	N/A	15.4 W
	Core Power (Post-Flush)	20	N/A	12.9 W	N/A	12.0 W
	NB Power	17	N/A	10.8 W	N/A	10.3 W
	I/O Power	13	N/A	6.1 W	N/A	6.1 W
S0.C1E.Pmin	TDP	16	N/A	15.8 W	N/A	14.8 W
S3	I/O Power	13	N/A	300 mW	N/A	300 mW

The notes for this table are on page 60 and page 61.

AMD Phenom™ Processor Thermal and Power Specification Table Notes:

1. *Tcase Max is the maximum case temperature specification which is a physical value in degrees Celsius. Tcase Max can be any valid Tcase Max value in the range specified for the corresponding OPN.*
2. *Tctl Max (maximum control temperature) is a non-physical temperature on an arbitrary scale that can be used for system thermal management policies. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116.*
3. *The processor thermal solution should be designed to accommodate thermal design power (TDP) at Tcase Max. TDP is measured under the conditions of all cores operating at CPU COF, Tcase Max, and VDD at the voltage requested by the processor. TDP includes all power dissipated on-die from VDD, VDDNB, VDDIO, VLDT, VTT, and VDDA. TDP is not the maximum power of the processor.*
4. *P-state limit when HTC is active. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116 for more information.*
5. *Hardware transitions the part to startup P-state at cold boot. During initialization, the startup NB COF and VID_VDDNB values may differ from those of the startup P-state. Please see the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116 for detailed power sequencing information.*
6. *Frequency reported to the OS is rounded to the nearest 100-MHz boundary.*
7. *During initialization, the startup NB COF and VID_VDDNB values may differ from those of the startup P-state. Please see the* BIOS and Kernel Developer's Guide (BKDG) For AMD Family 10h Processors*, order# 31116 for specific power sequencing information.*
8. *Specifications for multi-core processors assume equivalent P-states (voltage and frequency) and equivalent Tcase conditions for all cores. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order #31116, for details on P-state operation for multi-core processors.*
9. *Variable voltage, any valid voltage between VID_VDD Min and VID_VDD Max is allowed.*
10. *TDP IDD conditions: single-plane platforms supply IDD and IDDNB tied together and use the IDD Max specification.*
11. *Single-plane platforms have VID_VDD and VID_VDDNB tied together, and use the VID_VDD specification.*
12. *TDP IDDNB conditions: single-plane platforms supply IDD and IDDNB tied together and use the IDDNB Max specification.*
13. *Thermal Design Power dissipated by the processor VDDIO and VTT power planes only. Assumes VDDIO = 1.8 V and VTT = VDDIO / 2.*
14. *Refer to erratum 308 in the* Revision Guide for AMD Family 10h Processors*, order# 41322 for the appropriate clock divisor setting.*
15. *Assumes 50°C, Min P-state VID_VDD, core clock divider set to 128, and L2 and data cache scrubbing disabled. Refer to the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*,* order# 31116 *for recommended settings.*
16. *Assumes 35°C, min P-state VID_VDD, core clock divider set to 16, HyperTransport™ links disconnected, memory in self-refresh mode, and DDR2 SDRAM interface tristated. Recommended settings in the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116, provide improved power values.*
17. *Thermal Design Power dissipated by the processor at min P-state VID_VDDNB.*
18. *Thermal Design Power dissipated by the processor at min P-state VID_VDD.*
19. *This product is recommended for dual-plane platforms only.*
20. *Core Power (Pre-Flush) and (Post-Flush) refers to the Cache Flush On Halt feature described in the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116. Core Power pre-flush and post-flush values are based on the recommended* BKDG *settings. Actual C1 idle core power varies with system usage according to the following equation:*
    *C1 idle Core Power = F3xDC[CashFlushOnHaltTmr]/OS timer tick interval * Core Power (Pre-Flush) + (1 - F3xDC[CachFlushOnHaltTmr]/OS timer tick interval * Core Power (Post-Flush))*
    The default Microsoft® Windows Vista® timer tick interval is 15.6 ms. This interval varies between operating systems and within an operating system depending on usage.
21. *Valid for dual-plane operation only.*

AMD Phenom™ Processor Thermal and Power Specification Table Notes (Continued):

22. *The processor thermal solution should be designed to accommodate thermal design power (TDP) at Tcase Max. TDP in this state is measured at Tcase Max and VDD at the voltage requested by the processor with the number of cores in the C1 state specified by C-State Count. TDP includes all power dissipated on-die from VDD, VDDNB, VDDIO, VLDT, VTT, and VDDA. Due to increased power density in the state, the processor has an increased probability of hardware thermal control (HTC) activation compared to S0.C0.P1 at the same ambient temperature. TDP is not the maximum power of the processor.*
23. *C-State Count indicates the minimum number of cores in the C1 state required for the remaining cores to enter this P-state. Refer to F4x164[CstateCnt] in the* BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116, for more details about the entry requirements into this P-state.*

Table 7. AMD Phenom™ Processor Thermal Profiles (Continued)

Thermal Profile	AD
Heat Sink Class	**HS65**
Heat Sink Thermal Resistance	0.30°C/W
Heat Sink Local Ambient	42.0°C
Profile Thermal Resistance	0.242°C/W
Profile Ambient	48.0°C
TDP	**Tcase Max**
0 W	55.0°C
10 W	55.0°C
20 W	55.0°C
30 W	55.3°C
40 W	57.7°C
50 W	60.1°C
60 W	62.5°C
70 W	64.9°C
80 W	67.4°C
90 W	69.8°C
95 W	71.0°C

Phenom II x6 1055/90T

Thermal Profile	AE
Heat Sink Class	**HS78**
Heat Sink Thermal Resistance	0.19°C/W
Heat Sink Local Ambient	38.0°C
Profile Thermal Resistance	0.144°C/W
Profile Ambient	44.0°C
TDP	**Tcase Max**
0 W	55.0°C
10 W	55.0°C
20 W	55.0°C
30 W	55.0°C
40 W	55.0°C
50 W	55.0°C
60 W	55.0°C
70 W	55.0°C
80 W	55.5°C
90 W	57.0°C
95 W	57.7°C
100 W	58.4°C
105 W	59.1°C
110 W	59.8°C
115 W	60.6°C
120 W	61.3°C
125 W	62.0°C

Note: *The thermal profile is used to define the relationship between Tcase max and device-specific Thermal Design Power. The heat sink thermal resistance and heat sink local ambient values specify heat sink design targets. The profile thermal resistance and profile ambient values specify the relationship between part-specific power and part-specific Tcase Max. If the heat sink design targets are met, the thermal profile specifications are met.*

5.2 bsmmmmrr K ncdd – AM3 Power Supply Operating Conditions

Table 29. bsmmmmrr K ncdd DC Operating Conditions for VDD Power Supply

Symbol	Parameter	Units	Min	Typ	Max	Notes
VID_VDD	VID-Requested VDD Supply Level	V	Refer to the thermal/power tables under the appropriate SOPN section for this OPN-specific parameter.			
VDD_dc	DC Tolerance - VDD Supply Voltage	V	VID_VDD –50 mV	VID_VDD	VID_VDD + 50 mV	
VDD_PON	Metal Mask VID	V	0.95	1.00	MaxVID_VDD	1,2
VDDNB_dc	VDDNB Supply voltage	V	VID_VDDNB –50 mV	VID_VDDNB	VID_VDDNB + 50 mV	
VID_VDDNB	VDDNB Supply voltage	V	Refer to the thermal/power tables under the appropriate SOPN section for this OPN-specific parameter.			
VDDNB_PON	Metal Mask VDDNB	V	0.95	1.00	MaxVID_VDD	1,2

Notes:

1) After PWROK assertion, the VID signals change from the Metal Mask VID to the value programmed during device manufacturing.

2) MaxVID is reported in MSRC001_0071 (COFVID_STATUS).

Table 30. bsmmmmrr K ncdd AC Operating Conditions for VDD Power Supply

Symbol	Parameter	Units	Min	Typ	Max	Notes
VDD_ac	VDD Supply Voltage	V	VID_VDD –140 mV	VID_VDD	VID_VDD + 150 mV	1
VDDNB_ac	VDDNB Supply Voltage	V	VID_VDDNB –140 mV	VID_VDDNB	VID_VDDNB + 150 mV	1

Notes:

1) The voltage set-point must be contained within the DC specification in order to ensure proper operation. Voltage ripple and transient events outside the DC specification must remain within the AC specification at all. times. Transients above dc max must return to within the DC specification within 30 µS and must stay under a triangle described by the AC limit at one end and the DC limit at the other, as shown in Figure 8 on page 93.

Table 31. bsmmmmrr K ncdd Maximum Power-Up and Power-Down Conditions for Power Supplies

Symbol	Parameter	Units	Max
VDDIO	VDDIO Supply Voltage for DDR2 electricals	V	2.05
VDDIO	VDDIO Supply Voltage for DDR3 electricals	V	1.65
VLDT	VLDT Supply Voltage	V	1.32
VDDA	VDDA Supply Voltage	V	2.70
VDD, VDDNB	VDD, VDDNB Supply Voltage	V	Max AC Voltage

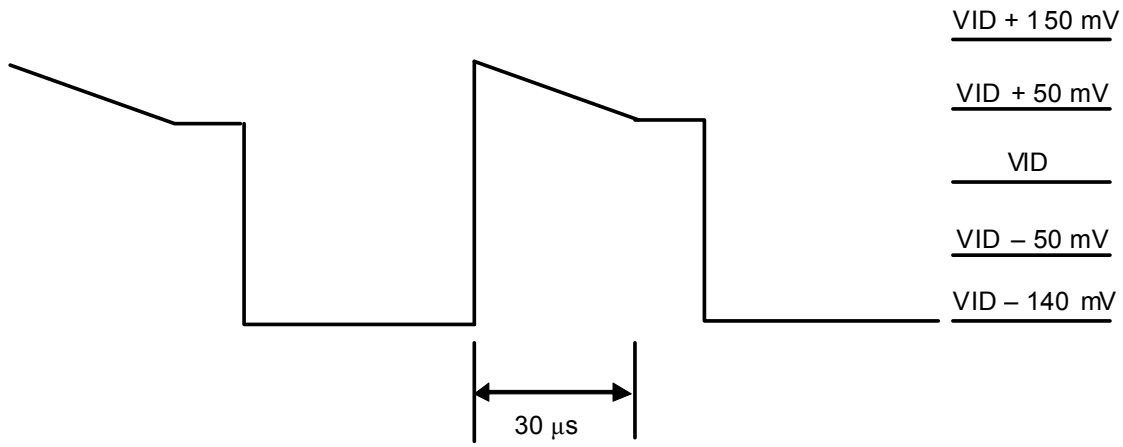

Figure 8. Socket AM3 AC and DC Transient Limits