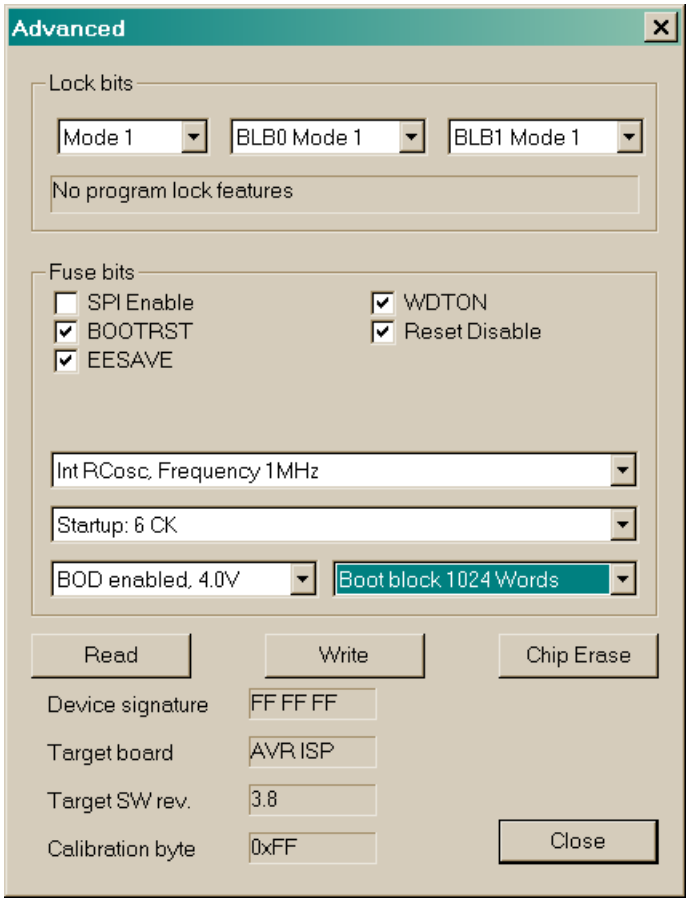
Advanced
Lock bits
Mode 1
BLB0 Mode 1
BLB1 Mode 1
No program lock features
Fuse bits
SPI Enable
BOOTRST
EESAVE
WDTON
Reset Disable
Int RCosc, Frequency 1MHz
Startup: 6 CK
BOD enabled, 4.0V
Boot block 1024 Words
Read
Write
Chip Erase
Device signature
FF FF FF
Target board
AVR ISP
Target SW rev.
3.8
Calibration byte
0xFF
Close