3 FPGA

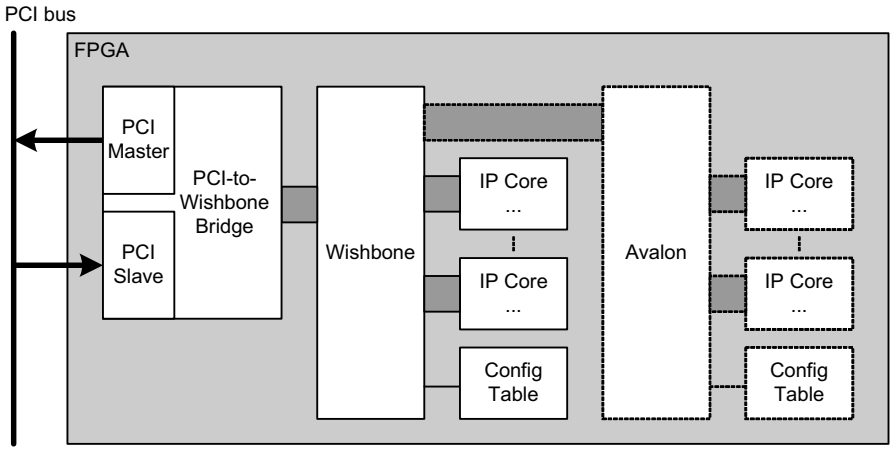
3.1 General

The FPGA – as a part of the EM9 – represents an interface between a user-selectable configuration of I/O modules (IP cores) and the PCI bus. The PCI core included in the FPGA can be a PCI target or master. It can be accessed via memory single/burst read/write cycles.

The Wishbone bus is the uniform interface to the PCI bus. However, the FPGA may have multiple internal buses, so that IP cores can be connected to one of several internal buses, e.g. Wishbone or Avalon. This guarantees the highest possible flexibility for different configurations of the FPGA.

Typically each implementation contains basic system functions such as reset and interrupt control etc. and the system library, which are also IP cores.

Figure 2. *FPGA – Block diagram (exemplary)*



A configuration table provides the information which modules are implemented in the current configuration. Furthermore the revision, the instance number (one module can be instantiated more than one time), the interrupt routing and the base address of the module are stored. At initialization time, the CPU has to read the configuration table to get the information of the base addresses of the included modules.

Note that with regard to the FPGA resources such as available logic elements or pins it is not possible to grant all possible combinations of the FPGA IP cores. The following chapter describes one possible configuration of the FPGA. Please ask our sales staff for other configurations.

You can find an overview and descriptions of all available FPGA IP cores on MEN's website.

3.2 Standard Factory FPGA Configuration

3.2.1 IP Cores

The factory FPGA configuration for standard boards comprises the following FPGA IP cores:

- Main bus interface
- 16Z024-01_Chameleon – Chameleon V2 table
- 16Z069_RST – Reset controller
- 16Z052_GIRQ – Interrupt controller
- 16Z070_IDEDISK – IDE controller for NAND Flash
- 16Z043_SDRAM – Additional SDRAM controller (32 MB DDR2, 8 MB used as NAND Flash main memory, 8 MB used as graphics RAM, 16 MB unused)
- 16Z016_IDE – IDE controller (PIO mode 0 and UDMA mode 5 / UDMA100)
- 16Z044_DISP – Display controller (800 x 600, 60Hz/75Hz, 6-bit RGB)
- 16Z031_SPI – SPI touch panel controller
- 16Z125_UART – UART controller (controls COM10..COM12)
- 16Z034_GPIO – GPIO controller (2 cores; 8 general I/O lines; *PWR_FAIL*, LEDs and other system control signals)

3.2.2 FPGA Configuration Table

The resulting configuration table of the standard FPGA is as follows:

Note: 16Z070_IDEDISK consists of three cores:

- 16Z053_IDEATA
- 16Z068_IDETGT
- 16Z063_NANDRAW

Table 13. *FPGA – Factory standard configuration table for EM9*

IP Core	Device	Variant	Revision	Interrupt	Group	Instance	BAR	Offset	Size
Chameleon Table	24	1	5	3F	0	0	0	0	200
16Z069_RST	69	0	2	3F	0	0	0	200	100
16Z052_GIRQ	52	0	2	3F	0	0	0	300	100
16Z016_IDE	116	0	1	1	0	0	0	400	100
16Z031_SPI	31	0	4	4	0	0	0	500	100
16Z044_DISP	44	1	1	3F	1	0	0	600	100
16Z034_GPIO	34	0	3	2	0	0	0	700	100
16Z034_GPIO	34	0	3	2	0	1	0	800	100
16Z125_UART	125	0	7	3	0	0	0	900	10
16Z125_UART	125	0	7	3	0	1	0	910	10
16Z125_UART	125	0	7	3	0	2	0	920	10
16Z063_NANDRAW	63	0	7	3F	2	0	0	4600	100
16Z068_IDETGT	68	0	F	5	2	0	0	6000	800
16Z053_IDEATA	53	0	F	5	2	0	0	A000	400
16Z043_SDRAM	43	1	1	3F	1	0	1	0	1E+06
16Z043_SDRAM	43	1	1	3F	2	1	1	1E+06	1E+06
Usermodule_0	900	0	0	6	0	0	0	8000	1000
Usermodule_1	900	0	0	7	0	0	0	9000	1000

All values in the tables are given in hexadecimal notation.