TELEFUNKEN electronic
Creative Technologies

U 145 M

Monolithic Integrated Circuit – P channel MOS, ion implantation

Applications: Cross point array 5 x 2, especially for space division multiplex systems of PABX's (**P**rivate **A**utomatic **B**ranch **Ex**change)

Features:

- Integrated driver logic
- Balanced switching network
- Without operating current flow in the speech path
- TTL compatible logic control
- Internally protected inputs
- Signal inputs are galvanically separated from signal path

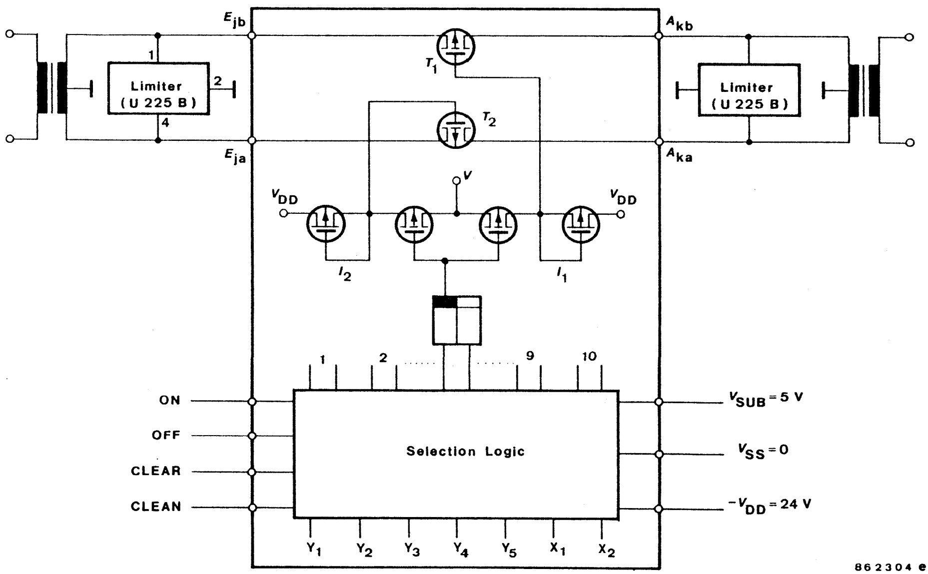

Fig. 1 Basic circuit diagram of speech-branch conductors

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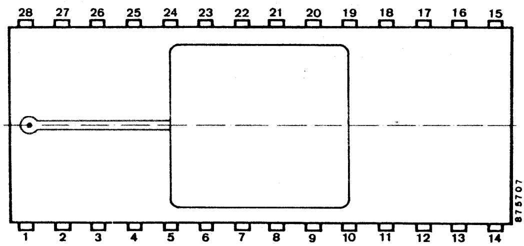
U 145 M

Pin Connection



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	8	E_{3a}	15	A_{2b}	22	off
2	A_{1a}	9	Y_4	16	Pu (clean)	23	E_{2b}
3	Y_1	10	E_{4a}	17	E_{5b}	24	ON
4	E_{1a}	11	Y_5	18	V_{DD}	25	E_{1b}
5	Y_2	12	E_{5a}	19	E_{4b}	26	X_1
6	E_{2a}	13	X_2	20	Lö (clear)	27	A_{1b}
7	Y_3	14	A_{2a}	21	E_{3b}	28	V_{SUB}

Absolute maximum ratings

Supply voltage range I $V_{DD} = -24$ V	V_{SUB}	$-0.3 \ldots + 8.5$	V
Supply voltage range II $V_{SUB} = +5$ V	$-V_{DD}$	$-0.3 \ldots +27.5$	V
Voltage on speech channels $V_{DD} = -24$ V	$V_{i,\,SPR}$	$-15 \ldots + 0.3$	V
Sum current of all speech channels	I_{SUM}	70	mA
Current per control input	I_{LOG}	$-1 \ldots +10$	mA
Non-repetitive voltage at speech channels	$V_{S,\,SPR}$ *)	$-3 \ldots + 3$	kV
Non-repetitive voltage at control inputs	$V_{S,\,LOG}$ *)	$-0.5 \ldots + 1$	kV
Power dissipation $T_j = +70$ °C	P_{tot}	780	mW
Junction temperature	T_j	+125	°C
Ambient temperature range	T_{amb}	$0 \ldots + 70$	°C
Storage temperature range	T_{stg}	$-55 \ldots +150$	°C

Electrical characteristics

$T_{amb} = 0 \ldots +70$ °C, $V_{SUB} = +5$ V ± 5 %,
$V_{DD} = -24$ V ± 5 %, unless otherwise specified

		Min.	Typ.	Max.	
Current consumption I	I_{SUB}			14.5	mA
Current consumtion II	$-I_{DD}$			12	mA

*) Discharge of 200 pF across 1.5 kΩ series resistance of the input

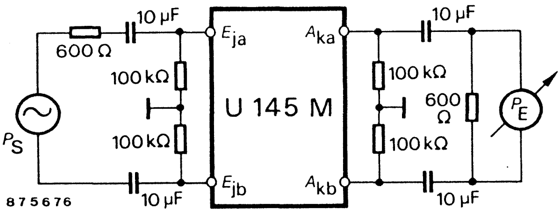
			Min.	Typ.	Max.	
ON resistance						
$T_j = +25$ °C	Fig. 3	R_D			50	Ω
$T_j = +70$ °C	Fig. 3	R_D			60	Ω
Resistance difference ring/tip wire	Fig. 3	ΔR_D			5	Ω
Maximum signal level $f = 800$ Hz, $\Delta a_E \leqq 0.1$ dB	Fig. 2	P_A	13			dBm
Insertion loss $f \leqq 100$ kHz, $p_s = 0$ dBm	Fig. 2	a_E			0.45	dB
Harmonic distortion $f = 1$ kHz, $p_K = 0$ dB	Fig. 2	a_{Kn}	62			dB
Intermodulation distance	Fig. 4	a_M	52			dB
Attenuation of unsymmetric cross point switched ON	Fig. 5	$a_{US, ON}$	40			dB
Attenuation of unsymmetric cross point switched OFF	Fig. 6	$a_{US, OFF}$	86			dB
Crosspoint noise, crosspoint switched ON	Fig. 7	$P_{G, ON}$			−86	dBmp
Crosspoint noise, crosspoint switched OFF	Fig. 7	$P_{G, OFF}$			−106	dBmp
OFF attenuation $p_S \leqq 17.5$ dBm, $f = 4$ kHz	Fig. 8	a_S	120			dB
Crosstalk between Input/Output $p_S \leqq 17.5$ dBm, $f = 4$ kHz	Fig. 9	a_{UE}	130			dB
Crosstalk between Z-S-Z/Z-S-Z connections *) $p_S \leqq 17.5$ dBm, $f = 4$ kHz	Fig. 11	$a_{ÜV, 1}$	115			dB
Crosstalk between Z-S/Z-S connections *) $p_S \leqq 17.5$ dBm, $f = 4$ kHz	Fig. 11	$a_{ÜV, 2}$	115			dB
Leakage current at speech path inputs		$-I_R$			1.5	μA
LOW input voltage at control inputs		V_{IL}			0.8	V
HIGH input voltage at control inputs		V_{IH}	3.5			V
LOW input current per control input		$-I_{IL}$			300	μA
HIGH input current per control input $V_{IH} = V_{SUB} - 1.75$ V, $V_{IE} = V_{SUB}$		$-I_{IH}$	12.5			μA

Intermedia values may be calculated by this formula: $I_{IH} \leqq \frac{V_{SUB} - V_{IH}}{140\ k\Omega}$

*) Z-S-Z-/Z-S = "ON" switched signal path: row-column-row/row-column

		Min.	Typ.	Max.	
Overlap of control pulses $X_n + Y_m$ + ON or $X_n + Y_m$ + OFF or Y_m + CLEAR	$t_Ü$	4			µs
Duration of clear pulses	t_L	4			µs
Switching time start of the coincident control pulses: $R_D \leqq 60\ \Omega$, $R_D \geqq 100\ k\Omega$	t_S			100	µs
Max. duration of noise pulses	t_I			15	ns
Capacitor of the control inputs	C_E		6	12	pF

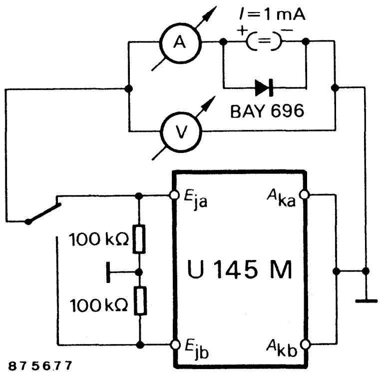
At all measurements pay attention to the influence of the measuring circuit.



$j = 1 \ldots 5$, $k = 1; 2$
Only cross point $E_j - A_k$ is conducting

1. **limit of modulation**
   $P_A = P_S - 6$ (dBm)
   $\Delta a_E = a_E$ (at $P_S = P_A + 6$ dBm) $- a_E$ (at $P_S = 0$ dBm)
2. **insertion attenat.**
   $a_E = P_S - 6 - P_E$ (dB)
3. **harmonic distortion**
   $P_K = P_S - 6$ (dBm)
   $a_{Kn} = P_E$ (at 1 kHz) $- P_E$ (at n·1 kHz) (dB)

Fig. 2 **Circuit 1**



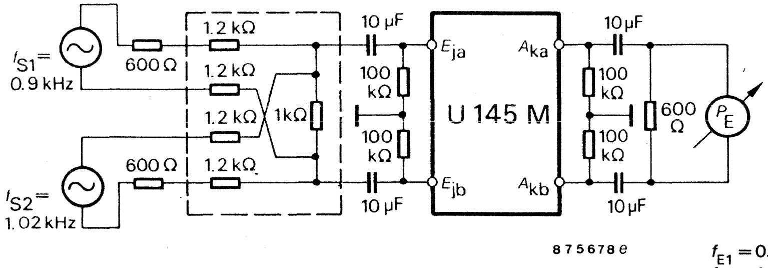
$R_{Da(b)} = \frac{V}{I}$

$R_D = R_{Da} + R_{Db}$

$\Delta R_D = P_{Da} - R_{Db}$

$j = 1 \ldots 5$, $k = 1; 2$
Only cross point $E_j - A_k$ is conducting

Fig. 3 Circuit 2

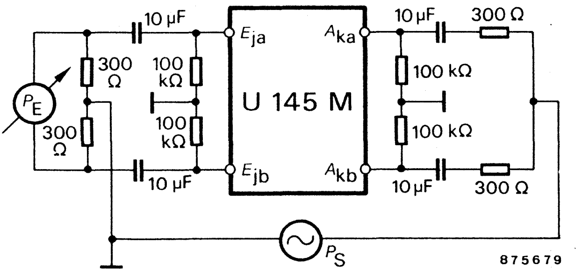


f_{E1} = 0.78 kHz
f_{E2} = 1.14 kHz
$P_{E(fS1)} = P_{E(fS2)}$ = 0 dBm

$a_M = |P_E|$ at f_{E1} (dB)
$a_M = |P_E|$ at f_{E2} (dB)

j = 1 ... 5, k = 1, 2
Only cross point $E_j - A_k$ is conducting

Fig. 4 Circuit 3



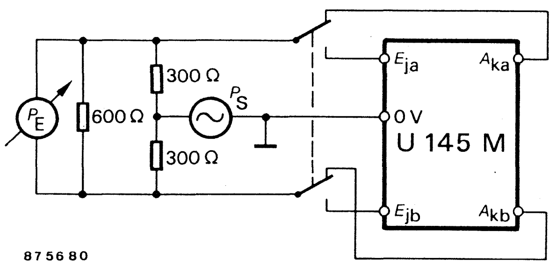
P_S = 0 dBm

$O_{US, ON} = |P_E|$ (dB)

adjust measuring resistor (300 Ω)

j = 1 ... 5, k = 1, 2
Only cross point $E_j - A_K$ is conducting

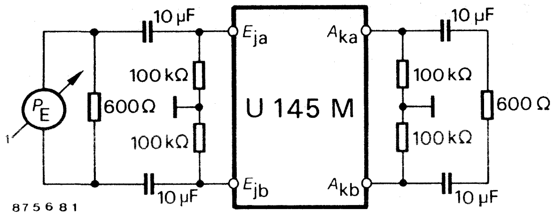
Fig. 5 Circuit 4



P_S = 0 dBm
$a_{US, OFF} = |P_E|$ (dB)

j = 1 ... 5, k = 1, 2
all cross points are non-conducting

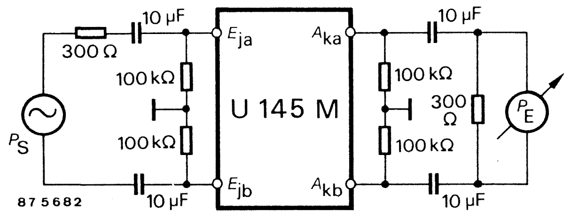
Fig. 6 Circuit 5



$P_{G,\,ON} = P_E$ (dBmp)
only cross point
$E_j - A_K$ is conducting
$P_{G,\,OFF} = P_E$ (dBmp)
all cross points are
non conducting

Fig. 7 Circuit 6

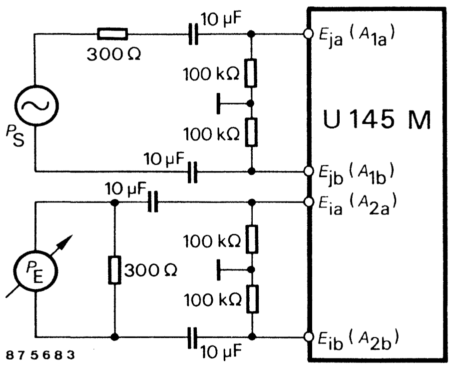
j = 1 ... 5, k = 1, 2



$a_S = P_S - P_E$ (dB)

Fig. 8 Circuit 7

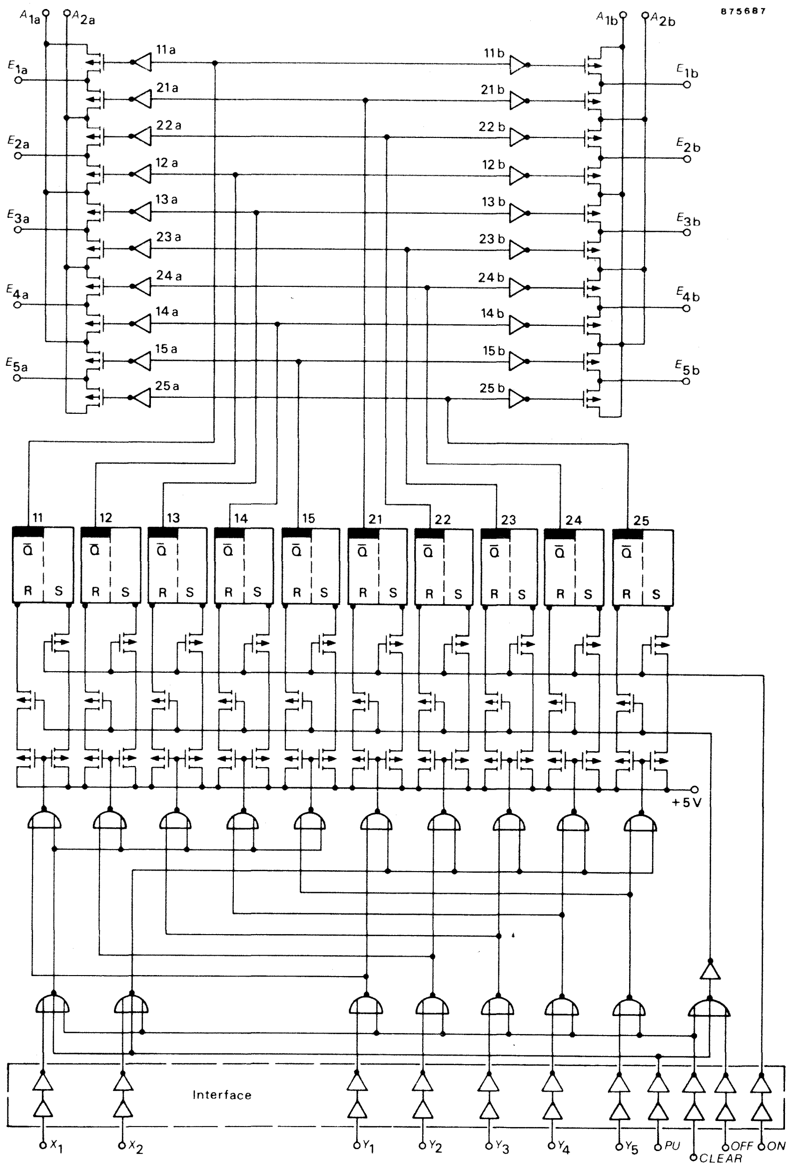
j = 1 ... 5, k = 1, 2
all cross points are non-conducting



$a_{ÜE} = P_S - P_E$ (dB)

Fig. 9 Circuit 8

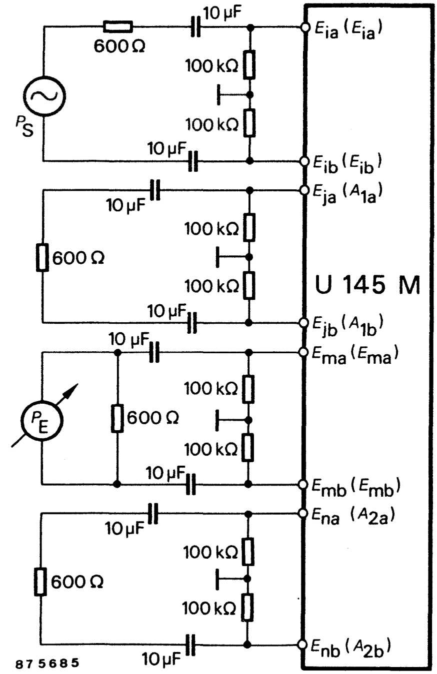
j = 1 ... 5, i = 1 ... 5, i ≠ j
all cross points are non-conducting



Logic control: The "LOW"-level 0...0.8 V activates the logical network for switching ON or OFF. The "HIGH"-level 3.5...5 V corresponds to the standby mode. The ON/OFF state of the crosspoint switches is stored internally.

Fig. 10 Logic diagram

(≙ 0 dB ±1 dB)



i = 1...5, j = 1...5, m = 1...5, n = 1...5

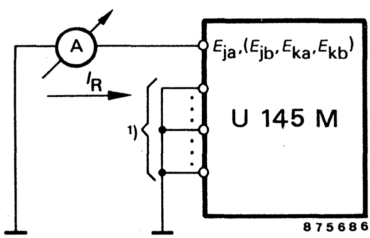
Fig. 11 Circuit 9

$a_{üv,1} = P_S - P_E$ (dB)

For designation without parenthesis and i ≠ j, m, n; j ≠ m, n; m ≠ n.
Only cross points $E_i - A_1$, $E_j - A_1$, $E_m - A_2$ and En - $A2$ are conducting.

$a_{üv,2} = P_S - P_E$ (dB)

For designation with parenthesis and i ≠ m
Only cross points E_i-A_1 and E_m-A_2 are conducting

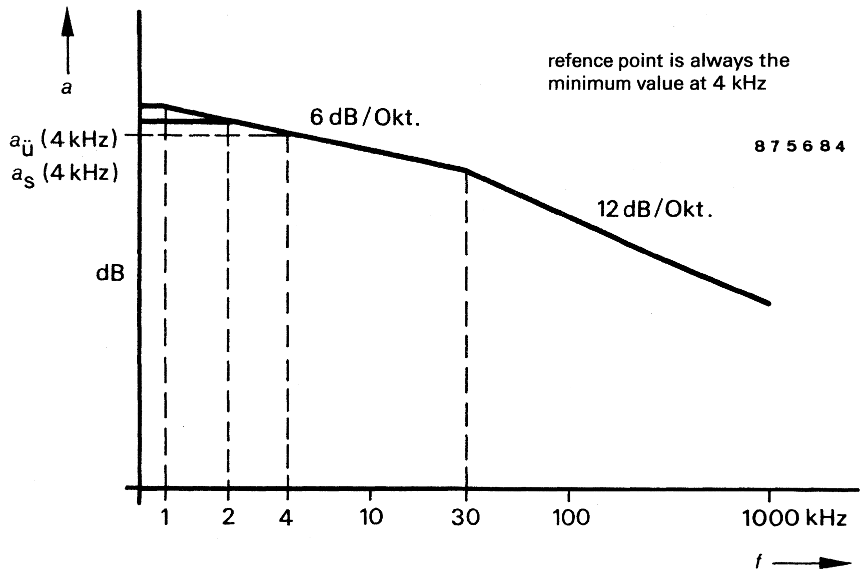


*) All the other speech paths are inputs and outputs

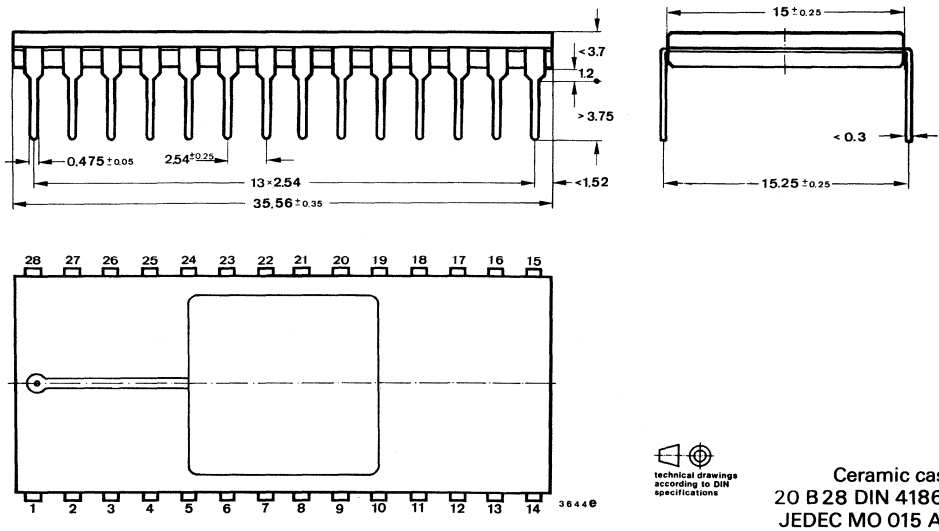
All cross points are switched off
j = 1...5, k = 1, 2

Fig. 12 Circuit 10

Diagram 1 Tolerance limit of the frequency response of a_s and $a_ü$



Dimensions in mm



technical drawings according to DIN specifications

Ceramic case
20 B 28 DIN 41866
JEDEC MO 015 AH
DIP 28
Weight max. 1.8 g

Monolithic Integrated Circuit

Application: Limiter to limit the voltage on symmetrical two wire speech branches in PABX, especially in connection with cross point array U 145 M

Features:

- Symmetrical limitation of noise voltage up to ± 3.2 V
- Simultaneously effective for a- and b-branch
- Low ohmic due to active circuit
- High input current 1.2 A
- Short rise time 10 V/µs

Preliminary specifications

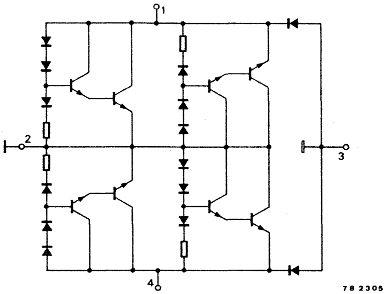


Fig. 1 Circuit diagram

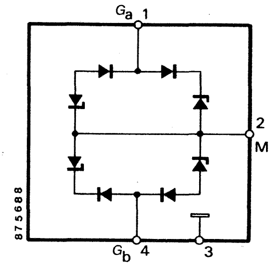


Fig. 2 Equivalent circuit diagram

Absolute maximum ratings

Supply voltage range	$-V_S$	3.5...20	V
Power dissipation $T_{amb} = 70$ °C	P_{tot}	180	mW
Peak power dissipation $T_{amb} = 70$ °C, $t_p = 100$ ms, 2 p.c. duty cycle	P_M	5	W
Input voltage $T_{amb} = 70$ °C, $t_p = 100$ ms	V_G	3.45	V
Input current $t_p = 100$ ms, 2 p.c. duty cycle	I_G	1.7	A
Junction temperature	T_j	+125	°C
Ambient temperature range	T_{amb}	0...+ 70	°C
Storage temperature range	T_{stg}	−55...+150	°C