

HARRIS



HFA-0003 HFA-0003L

PRELIMINARY

August 1991

Ultra-High Speed Comparator

Features

- Low Propagation Delay (0003/0003L) 2.0/2.1ns
- Low Latch Set-up Time 0.8ns
- Low Offset Voltage, Drift Coefficient 1.0mV, 4 μ V/ $^{\circ}$ C
- Wide Common Mode Range +5.2/-2.8V
- Low Power Dissipation 200mW
- Large Differential Input Resistance 1M Ω
- Complementary ECL Outputs; 50 Ω Driving Capability
- Resistor Programmable Hysteresis with '0003L
- Pin Compatible with MAX9690/9685 & AD96685
- Available in SOIC

Applications

- Window Detector
- High Speed Peak Detector
- High Speed Threshold Detector
- High Speed Data Acquisition Systems
- Fiber Optic Decision Circuits
- High Speed Phase Detector
- Frequency Counter

Description

The HFA-0003/0003L are monolithic, ultra high speed, voltage comparators. These comparators combine a low input offset voltage (1.0mV) with a low propagation delay (2.0ns) to achieve a large dynamic input range. The low offset voltage also makes these comparators ideally suited for high speed, precision analog-to-digital processing applications. The circuits have differential analog inputs, and provide complementary, ECL compatible (10K and 100K) logic outputs. The outputs are capable of supplying the current required by terminated 50 Ω transmission lines. Both outputs are open emitter structures, requiring external pull-down resistors. The recommended circuit is 50 Ω connected to -2.0V, but any equivalent ECL termination circuit may be used.

The HFA-0003L is a latched version of the HFA-0003. The latch function allows the HFA-0003L to operate in sample-hold or track-hold modes, when synchronous detection is required. The Latch Enable (LE) input can be driven by a standard ECL gate. See the Applications section on page 4 for more information on this feature.

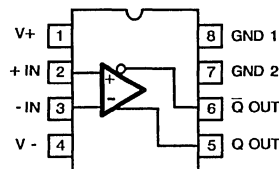
The HFA-0003L also has an additional feature, user programmable hysteresis. By connecting a resistor from the HYS pin to GND the user can select up to 20mV of input hysteresis. See the Applications section on page 4 for more information on this feature.

The HFA-0003 is pin compatible with the MAX9690, and SP9680 while providing improved performance. The HFA-0003L is pin compatible with the MAX9685, AD96685, SP9685, HCMP96850, and the VC7695 while providing improved performance.

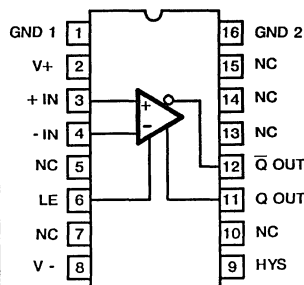
The performance of the HFA-0003/0003L-9 is guaranteed from -40 $^{\circ}$ C to +85 $^{\circ}$ C, while the HFA-0003/0003L-5 is guaranteed from 0 $^{\circ}$ C to +75 $^{\circ}$ C. The HFA-0003 is available in 8 pin Plastic DIP, Ceramic Sidebraze DIP, and SOIC. The HFA-0003L is available in 16 pin Plastic DIP, Ceramic Sidebraze DIP, SOIC, and a TO-100 Metal Can package. Refer to the /883 datasheets for military compliant product.

Pinouts

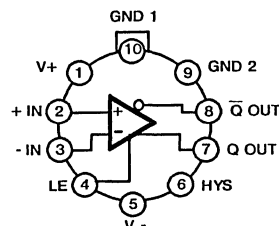
HFA7-0003-5/-9
(CERAMIC SIDEBRAZE DIP)
HFA3-0003-5/-9 (PLASTIC MINI-DIP)
HFA9P0003-5/-9 (SOIC)
TOP VIEW



HFA1-0003L-5/-9
(CERAMIC SIDEBRAZE DIP)
HFA3-0003L-5/-9 (PLASTIC DIP)
HFA9P0003L-5/-9 (SOIC)
TOP VIEW

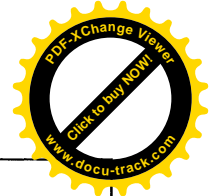
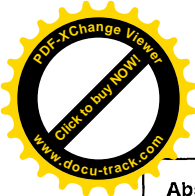


HFA2-0003L-5/-9
(TO-100 METAL CAN)
TOP VIEW



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COMPARATORS



Specifications HFA-0003/HFA-0003L

Absolute Maximum Ratings (Note 1)

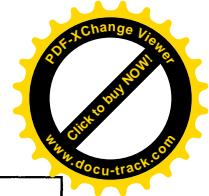
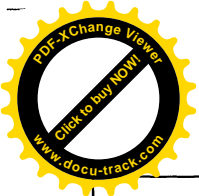
Voltage Between V+ and V- Terminals	20V
Supply Voltage (GND to V+)	8V
Supply Voltage (GND to V-)	18V
Differential Input Voltage	5.5V
Common Mode Voltage	±5V
Differential Ground Voltage (GND1 to GND2)	±1V
Peak (Short Duration) Output Current (Note 2)	-35mA
Maximum Junction Temperature	+175°C
Maximum Junction Temperature (Plastic Packages)	+150°C

Operating Temperature Range

HFA-0003/HFA-0003L-9	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
HFA-0003/HFA-0003L-5	$0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$
Storage Temperature Range	$-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$
Thermal Package Characteristics	θ_{jc} θ_{ja}
8 Pin Ceramic Sidebrazed DIP	39 95
8 Pin Plastic DIP	34 96
8 Pin SOIC	42 161
16 Pin Ceramic Sidebrazed DIP	34 79
16 Pin Plastic DIP	32 92
16 Pin SOIC	35 114
TO-100 Metal Can	32 108

Electrical Specifications V+ = 5V, V- = -5.2V, R_L = 50Ω to -2V, Unless Otherwise Specified

PARAMETER	TEMP	HFA-0003-5/-9			HFA-0003L-5/-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Offset Voltage (V _{OS})	+25°C	-	1	3	-	1	3	mV
	Full	-	-	4	-	-	4	mV
Average Offset Voltage Drift (Note 8)	Full	-	-	4	-	-	4	μV/°C
Input Bias Current	+25°C	-	5	8	-	5	8	μA
	Full	-	8	13	-	8	13	μA
Input Offset Current	+25°C	-	0.15	0.2	-	0.15	0.2	μA
	Full	-	-	0.3	-	-	0.3	μA
Common Mode Range	Full	-2.8	-	+5.2	-2.8	-	+5.2	V
Differential Input Resistance	+25°C	-	1	-	-	1	-	MΩ
Common Mode Input Resistance	+25°C	-	9.5	-	-	9.5	-	MΩ
Input Capacitance	+25°C	-	1	-	-	1	-	pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	+25°C	-	3100	-	-	3100	-	V/V
	Full	-	1200	-	-	1200	-	V/V
Common Mode Rejection Ratio (Note 3)	+25°C	70	75	-	70	75	-	dB
	Full	70	-	-	70	-	-	dB
Tracking Bandwidth (Note 4)	+25°C	-	270	-	-	270	-	MHz
SWITCHING CHARACTERISTICS								
Propagation Delay Input to Output (t _{pd}) (Notes 5, 8, 9)	+25°C	-	2.0	2.4	-	2.1	2.6	ns
	Full	-	-	2.8	-	-	3.0	ns
Maximum Dispersion (Notes 6, 8)	Full	-	-	200	-	-	200	ps
OUTPUT CHARACTERISTICS								
Output Voltage Level Logic Low (V _{OL})	+25°C	-	-1.83	-1.65	-	-1.83	-1.65	V
	Full	-	-1.83	-1.57	-	-1.83	-1.57	V
Logic High (V _{OH})	+25°C	-0.938	-0.85	-	-0.938	-0.85	-	V
	Full	-1.05	-0.96	-	-1.05	-0.96	-	V
Continuous Output Current (Note 2)	Full	-30	-	-	-30	-	-	mA



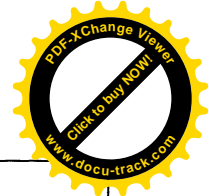
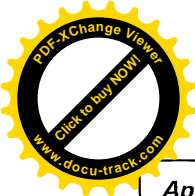
Specifications HFA-0003/HFA-0003L

Electrical Specifications (Continued) $V_+ = 5V$, $V_- = -5.2V$, $R_L = 50\Omega$ to $-2V$, Unless Otherwise Specified

PARAMETER	TEMP	HFA-0003-5/-9			HFA-0003L-5/-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
LATCH CHARACTERISTICS (HFA-0003L ONLY)								
LE Input Voltage Level								
Logic Low (V _{IL})	Full	-	-	-	-	-	-1.475	V
Logic High (V _{IH})	Full	-	-	-	-1.105	-	-	V
LE Input Current Level								
Logic Low (V _{IL} = -1.85V)	Full	-	-	-	-	0.06	0.5	μA
Logic High (V _{IH} = -0.81V)	Full	-	-	-	-	11	20	μA
Propagation Delay from LE to Output (t _{pDL})	+25°C	-	-	-	-	2.2	2.7	ns
(Notes 5, 8, 9)	Full	-	-	-	-	2.6	3.1	ns
Minimum Set-Up Time (t _s)	+25°C	-	-	-	-	0.8	1.2	ns
(Notes 8, 9)	Full	-	-	-	-	-	1.5	ns
Minimum Hold Time (t _h)	Full	-	-	-	-	0.5	1.0	ns
Minimum LE Pulse Width (t _{pW})	+25°C	-	-	-	-	0.9	0.95	ns
(Notes 8, 9)	Full	-	-	-	-	-	1.1	ns
POWER SUPPLY								
PSRR (Note 7)	+25°C	70	80	-	70	80	-	dB
	Full	65	-	-	65	-	-	dB
I _{CC}	Full	-	11	13	-	11	13	mA
I _{EE}	Full	-	19	22	-	19	22	mA
Power Dissipation	Full	-	-	200	-	-	200	mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the servability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. Outputs have no sink current (+I) capability, since they are open emitter NPN transistors.
3. $-2.0V \leq V_{CM} \leq +4.0V$.
4. Tracking Bandwidth (TBW) is defined as the maximum input frequency at which the outputs still switch between V_{OL} and V_{OH} . $V_{IN} = 15mV_{p-p}$ sinewave centered on OV.
5. $V_{IN} = 100mV$. V_{OD} is the amount of input overdrive.
6. Dispersion is defined as the change in propagation delay for input overdrives between 0.1V and 1.0V.
7. $+4.0V \leq V_+ \leq +5.5V$ or $-6.2V \leq V_- \leq -4.7V$.
8. This parameter is not tested. It is guaranteed by design, and by device characterization.
9. $V_{OD} = 10mV$.



Applications Information

HFA-0003L Latch Functionality

The Latch Enable (LE) pin of the '0003L controls the function of the on chip latch. When the LE input is at an ECL Logic 1, the latch is open (transparent) and the comparator functions normally. When the LE input switches to a Logic 0, the outputs are latched in unambiguous states dependant on the current input state, providing the set-up and hold times are met. If the latch function is not utilized, the LE input must be connected to an ECL Logic 1 (e.g. GND).

HFA-0003L Hysteresis Functionality

To improve performance in systems with slow transition times, and/or high noise levels, the HFA-0003L allows the user to easily set the amount of input hysteresis. The hysteresis level is set by the current flowing into the HYS input; the larger the current the larger the level of hysteresis. This current is provided by connecting a resistor (R_H) between the HYS pin and GND, and it is recommended that the input

current not exceed 1mA. The input current can be approximated from the following formula:

$$I_H = \frac{GND - (V_-) - 0.7V}{R_H}$$

The table below gives approximate levels of hysteresis for some values of I_H , at $T_A = +25^\circ\text{C}$.

I_H (mA)	0.2	0.4	0.6	0.8	1.0
HYS (mV)	1	4	8	13	22

If the hysteresis function isn't used, the HYS input may be left floating, or may be connected to V_- . The HYS input **MUST NEVER BE CONNECTED** directly to GND or V_+ , as device damage will occur. **Before inserting an HFA-0003L into a competitor socket**, the user must ensure that the corresponding socket pin is a true no-connect (i.e. is floating).

Timing Diagram

