12.05.09

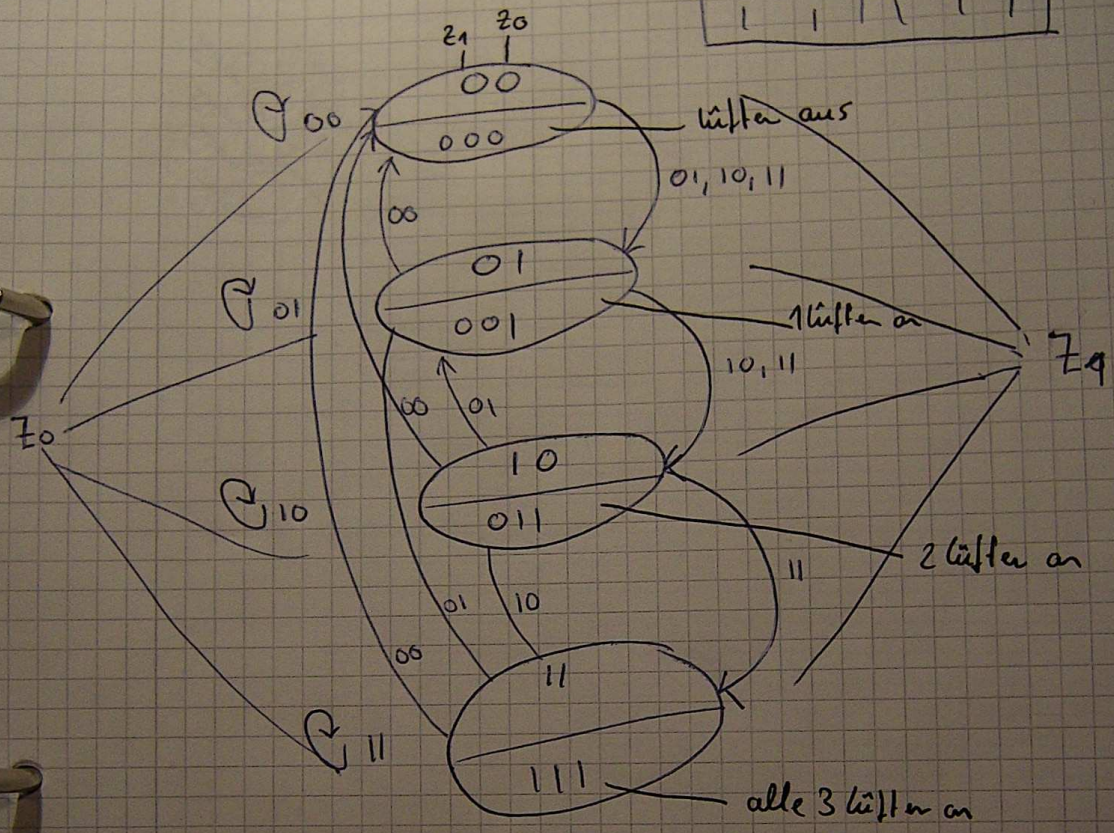
Übung Mikroprozessoren

(17)

Legende

Zustände Z_1, Z_0 / V_1, V_2, V_3 — $\overline{T}_1, \overline{T}_0$

$\overline{T}_1$	$\overline{T}_0$	V_3	V_2	V_1
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1



$\overline{T}_1$	$\overline{T}_0$	Z_1	Z_0	Z_1^+	Z_0^+	V_1	V_2	V_3
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	0	1	1	0	0	1	1	1
0	1	0	0	0	1	0	0	0
0	1	0	1	0	1	0	0	1
0	1	1	0	0	1	0	1	1
0	1	1	1	0	1	1	1	1
1	0	0	0	1	0	0	0	0
1	0	0	1	1	0	0	0	1
1	0	1	0	1	0	0	1	1
1	0	1	1	1	0	1	1	1
1	1	0	0	1	1	0	0	0
1	1	0	1	1	1	0	0	1
1	1	1	0	1	1	0	1	1
1	1	1	1	1	1	1	1	1

Übergangstabelle