TI Designs

Power Supply with Programmable Output Voltage and Protection for Position Encoder Interfaces

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TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00180	Design Folder
TPS54040A	Product Folder
TPS24750	Product Folder
TPL0401A-10	Product Folder
SN74CB3Q3125	Product Folder
TIDA-00172	Referenced Design Folder
TIDA-00175	Referenced Design Folder

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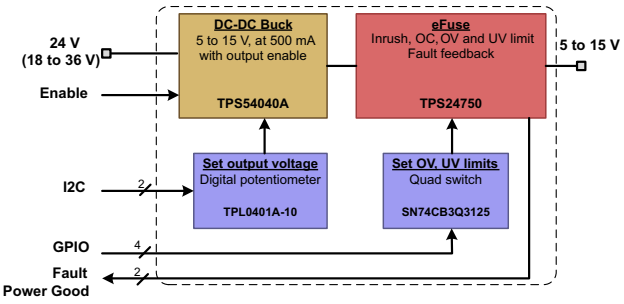
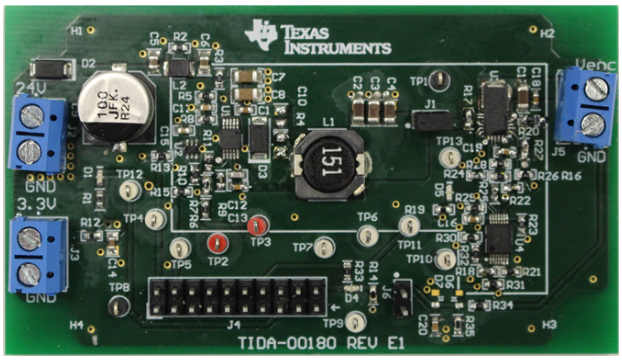
Design Features

- Power Supply Design Supports Different Supply Voltage Requirements for a Wide Range of Position Encoders with Digital or Analog Interface
- Wide Input Voltage Range, 18 to 36 V (24-V Nominal) and High Efficiency (>80%)
- Output Voltage Programmable from 5 to 15 V with <15-mVpp Ripple at 300-mA Load Current
- Output Protection with Innovative eFuse Technology with Inrush-Current Limitation and Fast Protection against Overcurrent and Over- and Undervoltage with Limits Constant across the Industrial Temperature Range
- Fault Handling: Disconnect in Case of Fault, Enable Pin for Power Supply; Fault and Power Good Indicator Flags for Diagnostics
- Designed to Meet EMC Requirements for ESD, EFT, Surge according to IEC61800-3

Featured Applications

- Industrial Drives
- Position Encoder Interface Modules





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1 System Description

1.1 TI Design Overview

This TI design implements a power supply with programmable output voltage, configurable inrush- and overcurrent (OC), over- (OV) and undervoltage (UV) protection, targeting for use in a position encoder interface module on a frequency inverter or servo drive, as shown in Figure 1.

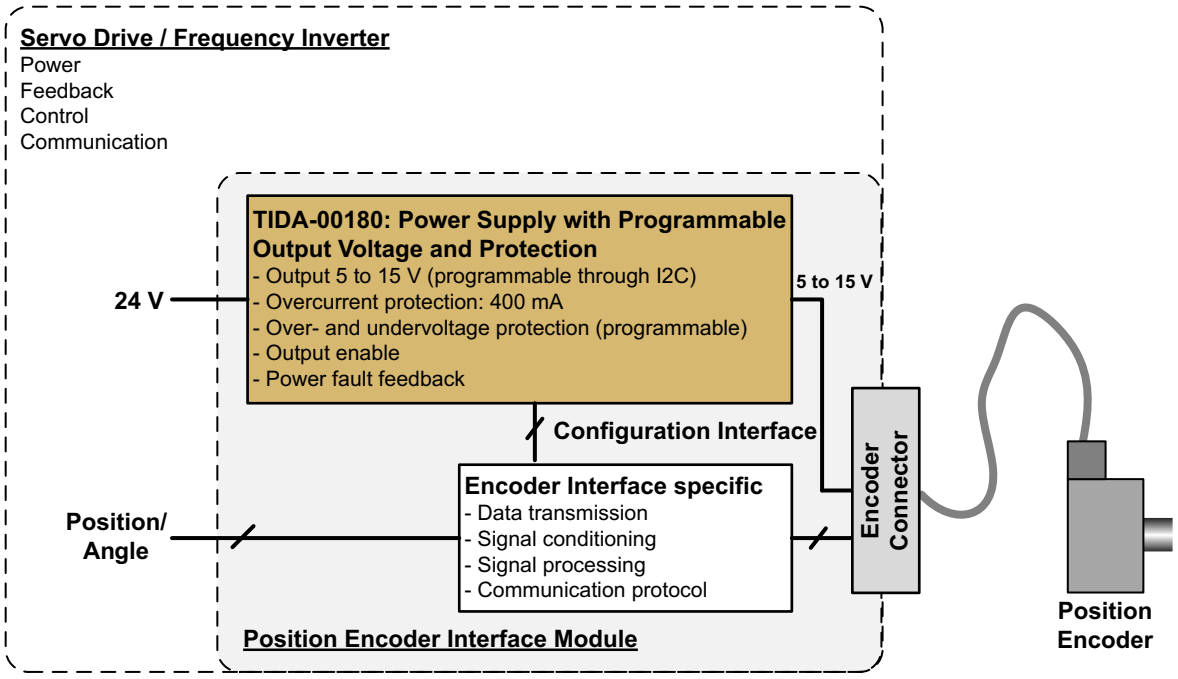

Figure 1. Block Diagram of an Encoder Interface Module with a Servo Drive Featuring TIDA-00180 Power Supply Design

This TI design consists of two major functional blocks: a DC-DC buck converter with programmable output voltage and output protection, as shown in Figure 2.

The DC-to-DC converter accepts a wide input voltage range from 18 to 36 V (24-V nominal) and features a user programmable output voltage configurable between 5 and 15 V, with a 300-mA nominal current.

The output protection is implemented with innovative electronic fuse (eFuse) technology. The eFuse provides an inrush-current limitation and fast OC protection as well as OV and UV protection. Current and voltage limits of the eFuse are accurate across the industrial temperature range. A brief overview on the eFuse technology versus polymeric positive temperature coefficient (PTC) fuses is shown in Section 2.2.1.

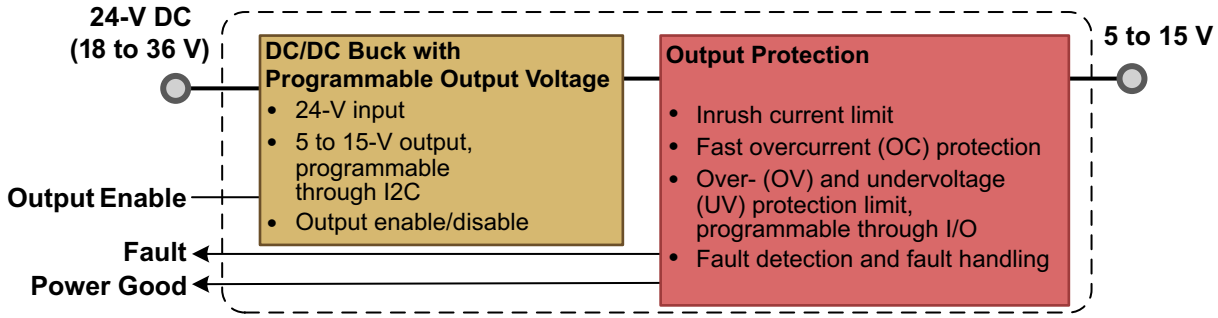

Figure 2. Block Diagram of the Power Supply with Programmable Output Voltage and Protection

This design is intended to supply position encoders with different input voltage requirements, as outlined in Table 1. Thanks to the programmable output voltage from 5 to 15 V, the design does not need to provide multiple power supplies and load switches. This design offers additional safety features like a short-circuit protection with accurate and temperature independent current limit as well as OV and UV protection. A host processor, which already implements the communication interface like an EnDat 2.2 Master, or the signal processing for an analog SinCos Encoder can be leveraged to also control this power supply. Therefore, no additional host MCU is required. The host processor can control the output voltage and OV and UV limits depending on the selected position encoder interface. The processor can further monitor the eFuse's fault and power good (PG) indicator signals for fault analysis and use the DC-DC buck's enable signal to reset the eFuse in case of a temporary fault or to turn off the DC-DC buck to save power if no encoder is connected. For more details on a specific encoder interface solution including communication and power, see the TI designs TIDA-00172 and TIDA-00175.

1.2 Supply Voltage Ranges of Position Encoders

Various position encoders are available for industrial applications from different vendors with vendor specific or open-source interface standard. The supply voltage range is encoder specific and typically depends on the analog and digital interface standard it supports. Encoders with TTL or analog SinCos interface are typically offered with a 5-V input. Encoders with mixed analog and digital communication interface or pure digital communication interface typically require a vendor specific supply voltage range. Table 1 provides an overview on widely used encoders with respect to the corresponding interface standard.

Table 1. Typical Position Encoders Interface Standards and Supply Voltage Ranges

ENCODER INTERFACE STANDARD	PROTOCOL OWNER	INTERFACE (PHY)	SUPPLY VOLTAGE
EnDat 2.2	Heidenhain	RS-485	3.6 to 14 V
BiSS	iC-Haus GmbH(1)	RS-422	5 V, 10 to 30 V(2)
Hiperface DSL	Sick	RS-485	7 to 12 V
SSI	Open(3)	RS-422	5 V, 10 to 30 V(2)
EnDat 2.1	Heidenhain	RS-485 and Sine/Cosine (analog, 1 Vpp)	3.6 to 5.25 V
Hiperface	Sick	RS-485 and Sine/Cosine (analog, 1 Vpp)	7 to 12 V
SinCos	N/A	Sine/Cosine (analog, 1 Vpp)	5 V(2)
Incremental	N/A	TTL or HTL	5 V (TTL), 10 to 30 V (HTL)

(1) Open source protocol, multiple encoder vendors
(2) Typical, some vendors offer 5- to 30-V range
(3) Max Stegmann GmbH (Sick)

2 Design Features

As outlined in Section 1, the major building blocks are the DC-DC converter with an I2C-programmable output voltage and the eFuse to realize the inrush- and OC limit as well as OV and UV protection and fault indicator.

Feature overview:

- Wide input voltage range: 18 to 36 V (24-V nominal) with reverse polarity protection
- Output voltage programmable from 5 to 15 V with a <15-mVpp ripple from a 0 to 300-mA load current
- Protection: Configurable inrush- and OC protection. Programmable OV and UV protection limits. Protection limits OC, UV, and OV are constant across the industrial temperature range
- Diagnostics and fault handling: Enable signal for output voltage, fault and PG indicator flags to host controller for diagnostics and further fault handling
- Designed to meet IEC 61800-3 EMC requirements and specific test methods applicable in adjustable speed electrical power drive systems

2.1 Output Voltage Specification

The DC-DC power supply specification is outlined in Table 2. The 24-V input voltage is assumed to be derived from a standard, isolated power supply rail with a 24-V output already available on the drive's frequency inverter.

Table 2. Part I: Output Voltage Specification

ENCODER POWER SUPPLY PARAMETERS	TIDA-00180
Input voltage(1)	24-V DC (18 to 36 V)
Output voltage range	5 to 15 V
Output voltage accuracy(2)	<±4%
Output voltage, low frequency ripple	<30 mVpp
Output current (nominal)	300 mA
Efficiency at 5 V/200 mA, 8 V/125 mA, 10 V/100 mA, and 15 V/66 mA	>80% (including eFuse)
Output enable/disable	Yes

(1) Assuming an isolated 24-V DC voltage (SELV)
(2) With software calibration

The output enable/disable pin of the power supply can be used to save power when no encoder is connected or to permanently switch off the power supply (for example in case of an external short circuit).

2.2 Output Protection Specification

Innovative eFuse technology realizes the protection limits as specified in Table 3.

Table 3. Part II: Power Supply Output Protection Specification

PROTECTION FEATURES: ENCODER POWER SUPPLY	TIDA-00180
Output voltage enable/disable pin	Yes
eFuse: Inrush current limit	400 mA (0°C to 85°C; configurable)
eFuse: OC trip limit	400 mA for more than 10 ms (configurable, see turn-off time below)
eFuse: OV trip limit	6 V, 12 V, 14 V, and 16 V (programmable)
eFuse: UV trip limit	4 V and 7 V (programmable)
eFuse: Fault timer	10 ms (configurable)
eFuse: Maximum capacitive load(1)	CMAX = 400 mA × 10 ms / 15 V = 266 µF
eFuse: Fault and power good indication	Yes

(1) The maximum capacitive load is a function of the eFuse's inrush current limit and the eFuse turn-off time and calculates according to $C_{MAX} = I_{LIM} \times t_{FAULT\_TIMER} / V_{OUT}$.

2.2.1 eFuse versus Polymeric PTC Fuse

An eFuse offers several advantages over a PTC fuse, which help to increase the system reliability as well as maintenance and diagnostics in case of temporary or permanent power faults.

A PTC fuse, also known as resettable fuse or Polyfuse, is placed in series to the load for OC protection. During an OC event, the PTC fuse changes from a low-resistance to a high resistance. Therefore, the PTC fuse protects the load (or the power supply) from OC. However, the PTC fuse's OC limit depends on the temperature. Also, the PTC fuse response time to switch to high impedance (off-state) is typically in the range of a few milliseconds. In an off-state, a small leakage current still remains.

An eFuse provides highly integrated load protection. The inrush current is limited to a user configurable limit. In case of an OC event, the user-configured OC limit will be allowed to flow until a programmed time-out, except in extreme overload events when load is immediately (a few microsecond) disconnected from source. The eFuse offers additional load protection due to configurable OV and UV limits. In case of a fault, an eFuse with auto-retry feature automatically initiates a restart after a fault has caused it to turn off the internal FET. For an eFuse without auto-retry, the FET remains turned off. The FET can be re-enabled by asserting the enable pin or by power cycling. PG, fault, and current monitor outputs are provided for system status monitoring and downstream load control.

2.2.1.1 OC Protection with eFuse

Innovative eFuse technology can electronically limit the inrush current during power-up or hot plugin of the encoder in case of large bulk capacity as well as disconnect the power supply from encoder in case of an OC condition like a short in the encoder cable, as shown in Figure 3.

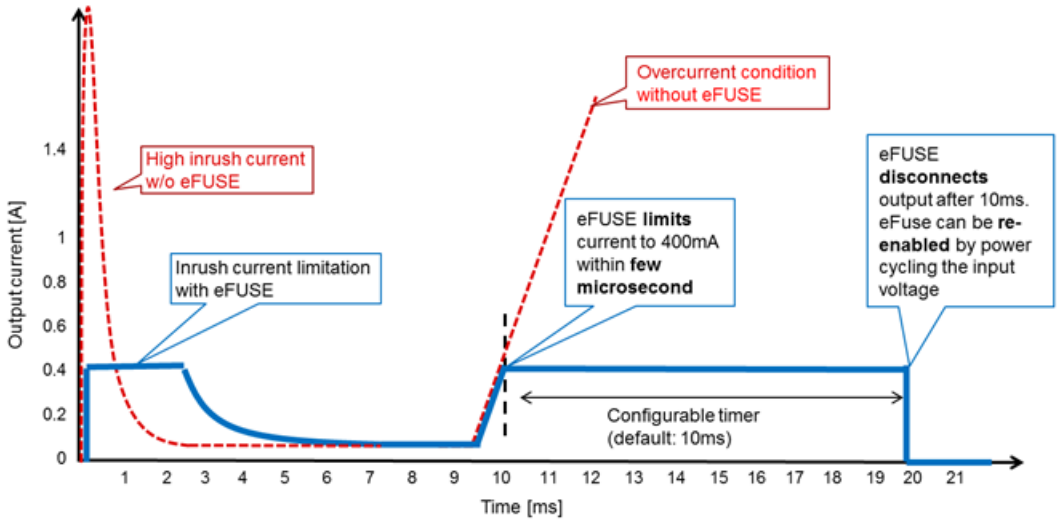

Figure 3. Inrush Current Limitation and OC Protection through eFuse

2.2.1.2 OV and UV Protection

The selected eFuse TPS24750 provides the advantage of configurable limits for OV as well as UV. These limits are constant over the temperature range too. In case of an OV or UV event, the eFuse disconnects the load, which protects the load form damage.

2.2.1.3 Fault Monitoring

The selected eFuse TPS24750 provides fault and PG indicators. The fault signal (FLT) indicates that the overload current fault timer has turned-off the internal FET to disconnect the output from the load. The PG signal indicates the output voltage is within the selected OV and UV limits.

An additional feature that is not implemented in this design allows for current monitoring. The voltage present at the TPS24750 IMON pin is proportional to the current flowing through the sense resistor R_{SENSE}. This voltage can be used as a means of monitoring current flow through the system.

2.3 EMC Immunity Requirements According to IEC61800-3

IEC618000-3 specifies the EMC requirements for adjustable speed electrical power drive systems. The intention of this TI design has been to for use in such drives. IEC618000-3 per Table 4 specifies the minimum requirements for EMC, applicable for a case or cabinet and connectors, for example.

Assuming this power supply design is part of encoder interface module on an electrical power drive, only the connector to the position encoder can be accessed, and shielded cables are used connect an encoder. According to IEC61800-3, the connector would then fall under “Ports for process measurement and control lines, DC auxiliary supplies lower than 60V”. Since the encoder cable can exceed 30 m, ESD, EFT, Surge, and conducted RF common mode applies per Table 4 for use in Environment 2.

Table 4. Extract of IEC61800-3 EMC Requirements for Second Environment

PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION
Enclosure ports	ESD	IEC61000-4-2	±4-kV CD or 8-kV AD, if CD not possible	B
	Radiated RF	IEC61000-4-3	80 to 1000 Mhz, 10 V/m, 80% AM (1 kHz) 1.4 to 2 GHz, 3 V/m, 80% AM (1 kHz) 2 to 2.7 GHz, 3 V/m, 80% AM (1 kHz)	A
Ports for control lines and DC auxiliary supplies <60 V	Fast transient burst (EFT)	IEC61000-4-4	±2 kV/5 kHz, capacitive clamp	B
	Surge 1.2/50 us, 8/20 us	IEC61000-4-5	±1 kV. Since shielded cable >20 m, direct coupling to shield (2 Ω/500 A)	B
	Conducted RF	IEC61000-4-6	0.15 to 80 Mhz, 10 V/m, 80% AM (1 kHz)	A

The performance (acceptance) criterion is defined, as follows:

Table 5. Performance Criteria

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module must continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, the module must continue to operate as intended without manual intervention.
C	During the test, loss of functions is accepted, but not the destruction of hardware or software. After the test, the module must continue to operate as intended automatically, after a manual restart, power off, or power on.

3 Block Diagram

Figure 4 shows the system block diagram. The major building blocks are the DC-DC buck converter with I2C-programmable output voltage and the eFuse with quad-FET switches to implement inrush and OC limit as well as programmable OV and UV protection and fault indicator. The output voltage of the DC-DC buck is configured with a digital potentiometer through I2C to support voltages from 5 to 15 V. The OV and UV protection limits of the eFuse can set with quad FETs configured through GPIO pins to adjust limits according to the load's specified supply voltage range.

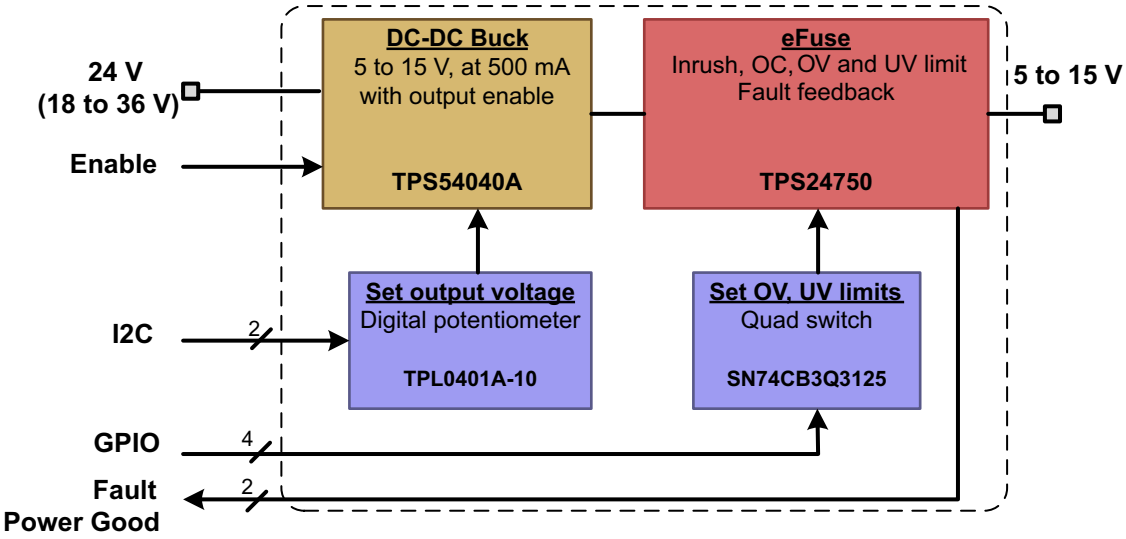

Figure 4. System Block Diagram of TIDA-00180

4 Circuit Design and Component Selection

The power supply with programmable output voltage and protection can be split into three blocks: the input filter, the DC-DC buck with adjustable output voltage, and the output protection with OC, OV, and UV protection limits.

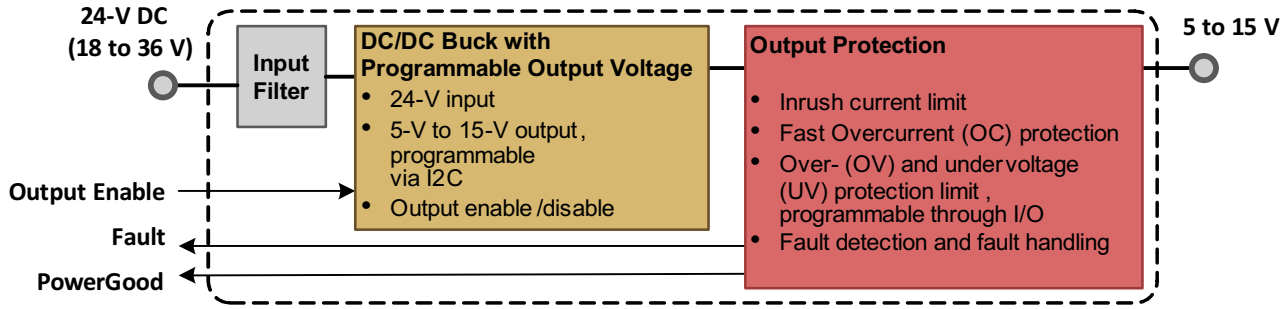

Figure 5. Block Diagram of Power Supply with Programmable Output Voltage and Protection

4.1 Input Filter

Conducted EMI are generated by the normal operation of switching circuits. Large discontinuous currents are generated by the power switches turn on and off. In a buck topology, large discontinuous currents are present at the input. The voltage ripple, created by those discontinuous currents, can couple into the rest of the system and cause EMI issues. To prevent this, an input filter reduces the input voltage ripple accordingly. In our case, this input filter consist of a PI-filter with the cutoff frequency around 1/10 of the switching frequency of the converters in order to have 40 dB of attenuation at the switching frequency. The converter implemented has a switching frequency of approximately 700 kHz, so the input filter has:

$$f_c = \frac{1}{2 \times \pi \times \sqrt{L_2 \times C_6}} \quad (1)$$

L2 is usually in the range of 1 to 10 µH. Set L2 to 4.7 µH and fc at 70 kHz. These settings yield a capacitor value of 1 µF for C6.

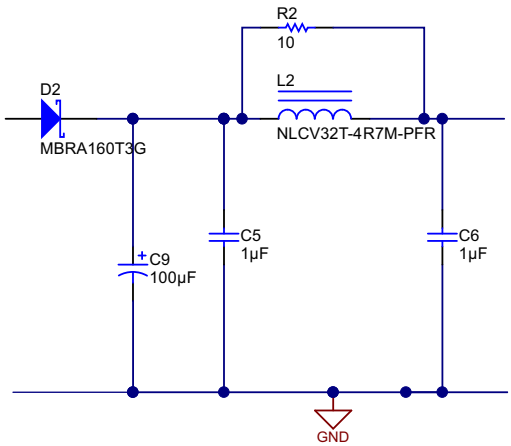

Figure 6. Schematic of Input Filter Including Reverse Polarity Protection

4.2 DC-DC Buck with Programmable Output Voltage

This block consists of a DC-DC buck converter with programmable resistive feedback for variable output voltage. The programmable feedback resistor is realized with a digital potentiometer.

4.2.1 DC-DC Buck with TPS54040A

The specifications are:

- Input voltage: Vin = 18 to 36 V, 24-V nominal, reverse polarity protection
- Output voltage: Configurable from 5 to 15V at 300 mA
- Switching frequency = 700 kHz, hardware adjustable
- Output voltage ripple max: 30 mA
- Output voltage can be switched on and off (enable signal)
- Efficiency: >80% at 1-W output power, 5 V/200 mA, 8 V/125 mA, 10 V/100 mA and 15 V/66 mA
- Non-isolated

This design uses the TPS54040A buck converter with integrated FET, 3.5- to 42-V input voltage and 0.8- to 39-V output voltage at a 500-mA output current. Its frequency can be adjusted from 100 kHz to 2.5 MHz or can be synchronized with an external clock. The device can also be enabled or disabled. All those features make the TPS54040A a good fit to the design requirements. Note that the TPS54040A is pin-to-pin compatible with the TPS5401, which is a lower cost version of the TPS54040A with similar performance but less accurate output voltage and enable threshold. Also, the TPS54040A is pin-to-pin compatible with the TPS54140A, TPS54240, TPS54340, and TPS54540, which all have the same specifications of the TPS54040A with respectively 1.5 A, 2.5 A, 3.5 A, and 5 A capability. The schematic of the DC-DC buck converter is shown in Figure 7.

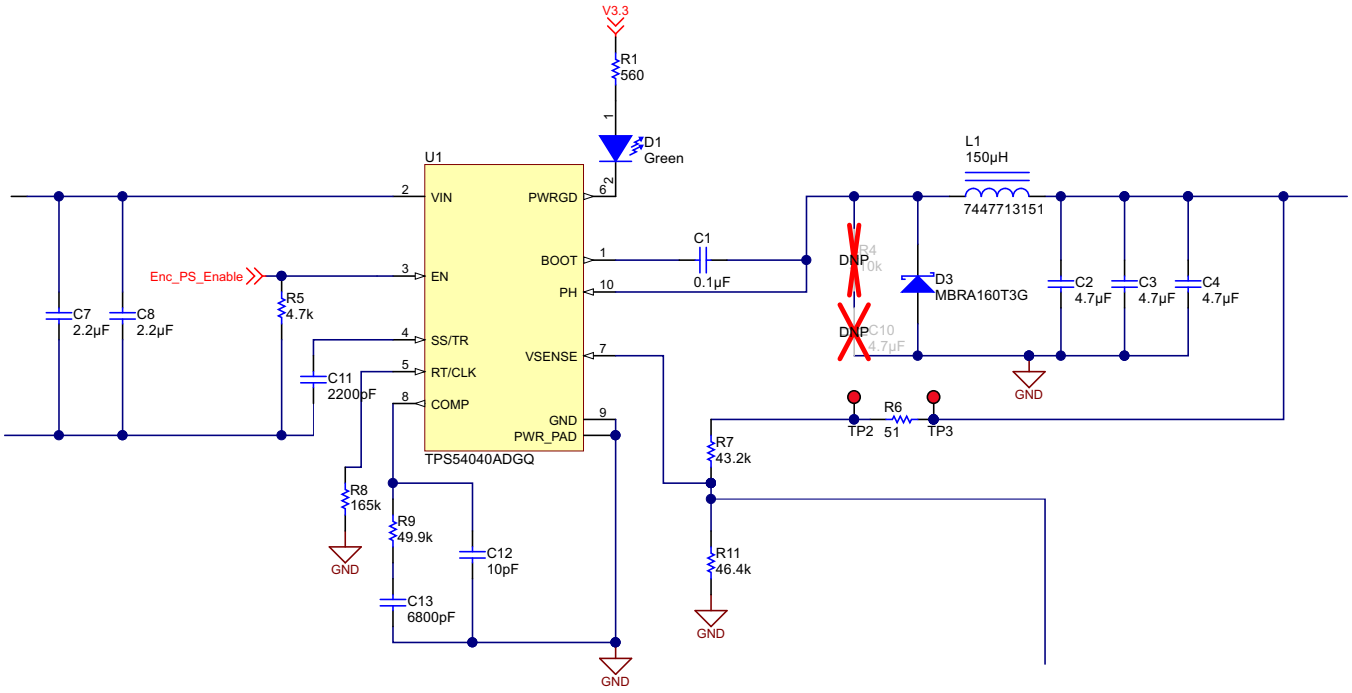

Figure 7. Schematic of DC-DC Buck Converter with TPS54040A

4.2.1.1 Passive Components Calculations

The first step is to decide and set the switching frequency of the regulator. In the TIDA-00180, the switching frequency (Fsw) is set to 700 kHz by R8. Equation 2 indicates that R8 should be 164.51 kΩ. 165 kΩ is then used as value for R8. The TPS54040A can also be synchronized with an external clock. For more details, see page 21 to 23 of the TPS54040A datasheet.

$$R_8 = \frac{206033}{F_{SW}^{1.0888}} \tag{2}$$

with Fsw in kHz and R8 in kΩ.

Once the switching frequency is set, the minimum inductor value of the output inductor (L1) is calculated with Equation 3. To calculate the minimum inductor value, we use the maximum input voltage (36 V), the maximum output voltage (15 V), the maximum output current (300 mA), the switching frequency set in the previous step (700 kHz) and Kind, which is the coefficient that represent the amount of inductor ripple relative to the maximum output current. For low ESR output capacitors, Kind should be 0.3 (0.2 for higher ESR output capacitors). Equation 3 indicates that L1 should be higher than 139 µH. 150 µH is then used as value for L1.

$$L_{min} = \frac{V_{inmax} - V_{outmax}}{I_{out} \times K_{ind}} \times \frac{V_{outmax}}{V_{inmax} \times F_{sw}} \tag{3}$$

By knowing the output inductor value, the ripple current, RMS current and peak current can be calculated with Equation 4, Equation 5, and Equation 6, which gives 0.08 A, 0.3 A, and 0.34 A, respectively.

$$I_{ripple} = \frac{V_{outmax} \times (V_{inmax} - V_{outmax})}{V_{inmax} \times L \times F_{sw}} \tag{4}$$

$$I_{Lrms} = \sqrt{(I_{out})^2 + \frac{1}{12} \times \left(\frac{V_{outmax} \times (V_{inmax} - V_{outmax})}{V_{inmax} \times L \times F_{sw}} \right)^2} \tag{5}$$

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2} \tag{6}$$

The maximum desired output voltage ripple and the transient response to load changes are the parameters to take into account for selecting the value of the output capacitors. Cout should be selected based on the most stringent of the following equations.

$$C_{out} > \frac{2 \times (I_{OH} - I_{OL})}{F_{sw} \times \Delta V_{out}} \tag{7}$$

With IOH, the output current under heavy load (0.3 A), IOL the output current under light load (0 A) and ΔVout the allowable change of output voltage during the load step.

$$C_{out} > L \times \frac{\left(I_{OH}^2 - I_{OL}^2 \right)}{\left[(V_{out} + \Delta V_{out})^2 - V_{out}^2 \right]} \tag{8}$$

$$C_{out} > \frac{1}{8 \times F_{sw}} \times \frac{1}{\left(\frac{V_{outripple}}{I_{ripple}} \right)} \tag{9}$$

with Voutripple the maximum output ripple required.

Equation 7, Equation 8, and Equation 9, when used for both maximum and minimum output voltage, indicate that Cout should be higher than 8.9 µF. Three 4.7 µF in parallel where chosen to fit the Cout requirements. Equation 10 calculates the maximum ESR of the output capacitor to meet the maximum output ripple required. The equivalent ESR of the output capacitors C2, C3, and C4 should be lower than 1.219 Ω.

$$R_{ESR} < \frac{V_{outripple}}{I_{ripple}} \tag{10}$$

Capacitors usually have a maximum current ripple that they can handle without failing or producing excess heat. The RMS value of the maximum ripple current that the output capacitors should handle is calculated in Equation 11, which gives 12 mA. This current will be shared across all the output capacitors.

$$I_{Coutrms} = \frac{V_{out} \times (V_{inmax} - V_{out})}{\sqrt{12} \times V_{inmax} \times L \times F_{sw}} \quad (11)$$

The TPS54040A requires high quality ceramic (X5R or X7R) input decoupling capacitor of at least 3 µF. The Input voltage ripple (1% of Vinmax) is dependent on the input capacitor and can be calculated with Equation 12, which gives 0.3 µF. Two 2.2 µF in parallel where chosen to fit the Cin requirements.

$$C_{in} = \frac{I_{out} \times 0.25}{\Delta V_{in} \times F_{sw}} \quad (12)$$

The RMS value of the maximum ripple current that the output capacitors should handle is calculated in Equation 13, which gives 137 mA. This current will be shared across all the input capacitors (C7 and C8).

$$I_{Cinrms} = I_{out} \times \sqrt{\frac{V_{out} \times (V_{inmin} - V_{out})}{V_{inmin}^2}} \quad (13)$$

The slow start capacitor (C11) determines the minimum amount of time it will take the output voltage to reach its programmed value during start up. This capacitor also limits the inrush current in the TPS54040A (current require to charge the output capacitors to the programmed value).

$$C_{11} = \frac{T_{ss} \times I_{ss}}{V_{ref} \times 0.8} \quad (14)$$

Once the power stage is set, the next step is to calculate the compensation circuit. There are several methods used to compensate DC-DC regulators, the following method is the one described in the datasheet of the TPS54040A. As the output voltage is programmable from 5 to 15 V in the TIDA-00180, the mean value (Vout = 10 V) is used for the following equations.

The first step is to calculate the target crossover frequency (fco). For this, the modulator pole (Equation 15) and the ESR zero (Equation 16) are used. The targeted crossover frequency is then the lower value of Equation 17 and Equation 18. The crossover frequency used here is 13 kHz

$$f_{pmod} = \frac{I_{outmax}}{2 \times \pi \times V_{out} \times C_{out}} \quad (15)$$

$$f_{zmod} = \frac{1}{2 \times \pi \times R_{esr} \times C_{out}} \quad (16)$$

$$f_{co} = \sqrt{f_{pmod} \times f_{zmod}} \quad (17)$$

$$f_{co} = \sqrt{f_{pmod} \times \frac{F_{sw}}{2}} \quad (18)$$

Once the crossover frequency is set, the compensation resistor (R9) can be calculated in Equation 19, which gives R9 = 50.77 kΩ, 49.9 kΩ is then used.

$$R_9 = \left(\frac{2 \times \pi \times f_{co} \times C_{out}}{g_{MPS}} \right) \times \left(\frac{V_{out}}{V_{ref} \times g_{MEA}} \right) \quad (19)$$

with

- g_{MPS} (power stage transconductance) = 1.9 A/V
- g_{MEA} (amplifier transconductance) = 92 µA/V
- Vref = 0.8

Equation 20 set the compensation zero to the modulator pole frequency, and Equation 21 yields 6.1 nF, 6.8 nF is then used.

$$C_{13} = \frac{1}{2 \times \pi \times R_{esr} \times C_{out}} \quad (20)$$

C12 set the compensation pole and should be set to the larger value of Equation 21 and Equation 22. Equation 22 gives 9.1 pF. 10 pF is then used as a value for C12.

$$C_{12} = \frac{C_{out} \times R_{esr}}{R_4} \quad (21)$$

$$C_{12} = \frac{1}{\pi \times R_4 \times F_{sw}} \quad (22)$$

On the TPS54040A schematics, some components are marked as do not populate (DNP), which is the case of the snubber network formed by R4 and C10. A snubber network is a solution to reduce the ringing on the switch node and overshoot of the MOSFET if needed. For more details of other options, please see the application note *Ringing Reduction Techniques for NexFETTM High Performance MOSFETs* on how to use and calculate your snubber network.

4.2.2 Output Voltage Configuration with TPL401A-10

On a typical DC-DC buck converter application the output voltage is set due to a simple resistor divider network. Equation 23 gives the value of the upper resistor according to the output voltage, the reference voltage (0.8 V for the TPS54040A) and the lower resistor (usually fixed to 10 kΩ).

$$R_{up} = R_{low} \times \frac{V_{out} - V_{ref}}{V_{ref}} \quad (23)$$

In the TIDA-00180, the output voltage can be selected by the user between 5 and 15 V. To be able to change the output voltage, several methods were evaluated: Switching resistors thanks to FETs, using a DAC (LM10011) with current output, and using a digital potentiometer (TPL0401A-10).

The TPL0401A-10 was chosen due to its linear taper resistor range (0 to 10 kΩ), with 128 wiper positions and the position of the wiper can be controlled through I2C. This yields a high step resolution especially at a 5-V output voltage with minimum control signal required to set the output voltage. Figure 8 outlines the digital potentiometer (TPL0401A-10) used as an adjustable feedback resistor.

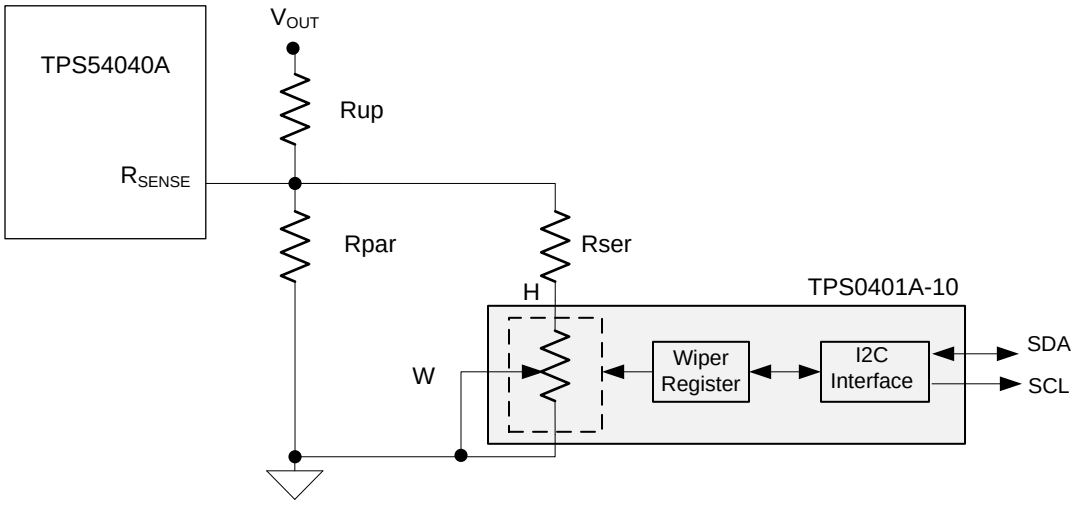

Figure 8. Configurable Output Voltage Using a Digital Potentiometer

The schematic is shown in Figure 9. One parallel resistor (Rpar = R11) and one series resistor (Rser = R10) are added to improve system reliability and safety. Those resistors help defining the output voltage range, and ensure that the output voltage will stay in a define state below 15 V, independent of the resister divider value of the digital potentiometer TPL0401A-10 for example during power up.

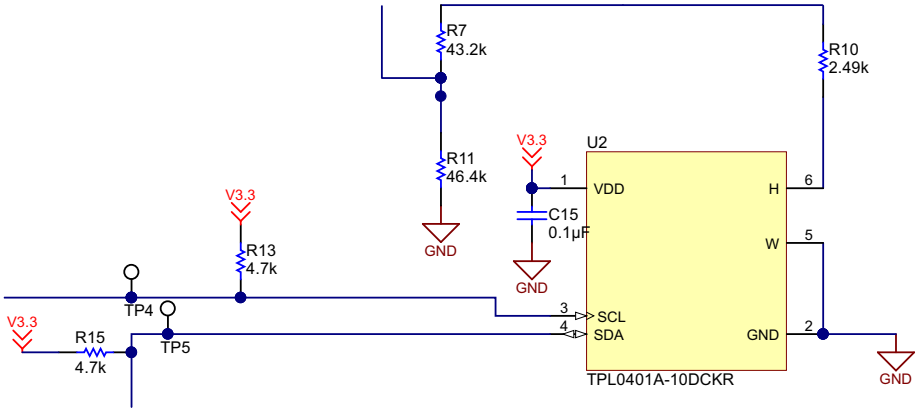

Figure 9. Schematic of Output Voltage Configuration Circuit with Digital Potentiometer TPL0401A-10

The maximum resistance of the TPL0401A-10 is 10 kΩ typical with a tolerance of ±20%, which is from 8 to 12 kΩ according to the datasheet. To handle this tolerance the range used in this design is from 0 Ω (Rpotmin) to 7.5 kΩ (Rpotmax). With these resistor values Vmax is 15 V (Rpotmin) and Vmin is 5 V (Rpotmax). The values of the three resistors that help setting the output voltage with the TPL0401A-10 can be adjusted during the test phase. R10 was set to 2.49 kΩ.

Then R11 and R7 can be calculated as follows:

$$R_{11} = \frac{(V_{max} - V_{min}) \times (R_{10} + R_{potmin}) \times (R_{10} + R_{potmax})}{V_{min} \times (R_{10} + R_{potmax}) - V_{max} \times (R_{10} + R_{potmin}) \times (R_{potmax} - R_{potmin})} \quad (24)$$

$$R_7 = \frac{\frac{V_{max}}{V_{ref}} - 1}{\frac{1}{R_{11}} + \frac{1}{R_{10} + R_{potmin}}} \quad (25)$$

4.2.3 Other Methods to Configure the Output Voltage

Other methods may be used to control the output voltage of the TPS54040A.

The first method would be to use switches to add resistors in parallel in a resistor divider setting to change dynamically the divider ratio. In case a few steps are required, a default resistor divider is calculated to fit the higher or lower divider ratio. Then, resistors are added in parallel to change the ratio (added on parallel to the upper resistor to increase the ratio, added to the lower resistor to decrease the ratio), as shown on Figure 10. Changing the ratio is the method used to set the OV and UV threshold of the e-Fuse of TIDA-00180 (see Section 4.3.3).

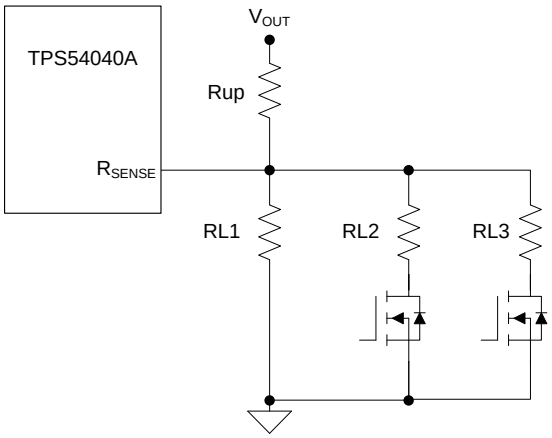

Figure 10. Adjustable Voltage Using Parallel Resistors with FET Switches

In case more steps are required, more resistors (and switches) can be added. A technic could be to double the value of each additional resistor to achieve a “binary” resistors scale, as shown on Figure 11.

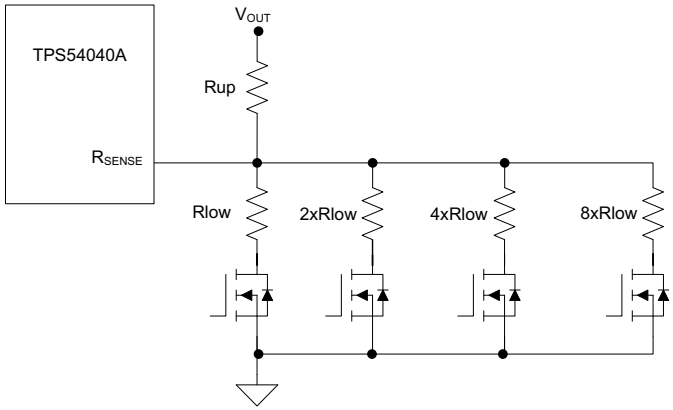

Figure 11. Adjustable Voltage Due to Switching Resistors with "Binary" Scale

NOTE: The switch function could be, for example, implemented with the SN74CB3Q3125 (Quadruple FET Bus Switch) as done for the eFuse section of the TIDA-00180 (see Section 4.3.3).

A second method is to use a current output DAC as shown on Figure 12. The LM10011, for example, is a 6/4-Bit VID Programmable Current DAC for Point of Load Regulators with Adjustable Start- Up Current. The DAC converts here the digital value wished for the output voltage into a current. This current is then injected into the resistor divider, biasing this one and changing the voltage applied to the VSENSE pin of the TPS54040A.

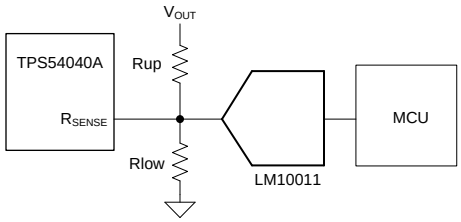

Figure 12. Adjustable Voltage using Current Output DAC LM10011

4.2.4 Layout Guidelines

Please refer to page 38 of the TPS54040A datasheet and Figure 105.

4.3 Output Protection

The specifications are:

- Maximum voltage drop at 400 mA: <50 mV
- Current limit: 400 mA
- Inrush current limit: 400 mA
- OC reaction time: <100 µs
- OC fault disconnect time: 10 ms, adjustable
- OV limit (OVP): 6 V, 12 V, 14 V, and 16 V, programmable
- UV lockout (UVLO): 4 V and 7 V, programmable
- Latch/disconnect when fault is detected
- Fault feedback
- Resetable

4.3.1 Component Selection

This block consist of an eFuse to realize the OC, OV and UV protection as well as a quad FET bus switch, allowing the configuration of the OV and UV protection limits.

4.3.1.1 TPS24750 eFuse

The TPS24750 is a 12-A e-Fuse, 2.5- to 18-V bus operation with integrated MOSFET with a 3-mΩ RDSON, and has an OV protection, an UV lockout, and a programmable current and power limit with programmable fault timer. This part fits the requirements, and it has a very low series resistance to minimize voltage drop as well as an external sense resistor for precise current limit detection. The schematic of the eFuse is shown in Figure 13. The passive components calculation is shown in Section 4.3.2 and Section 4.3.3.

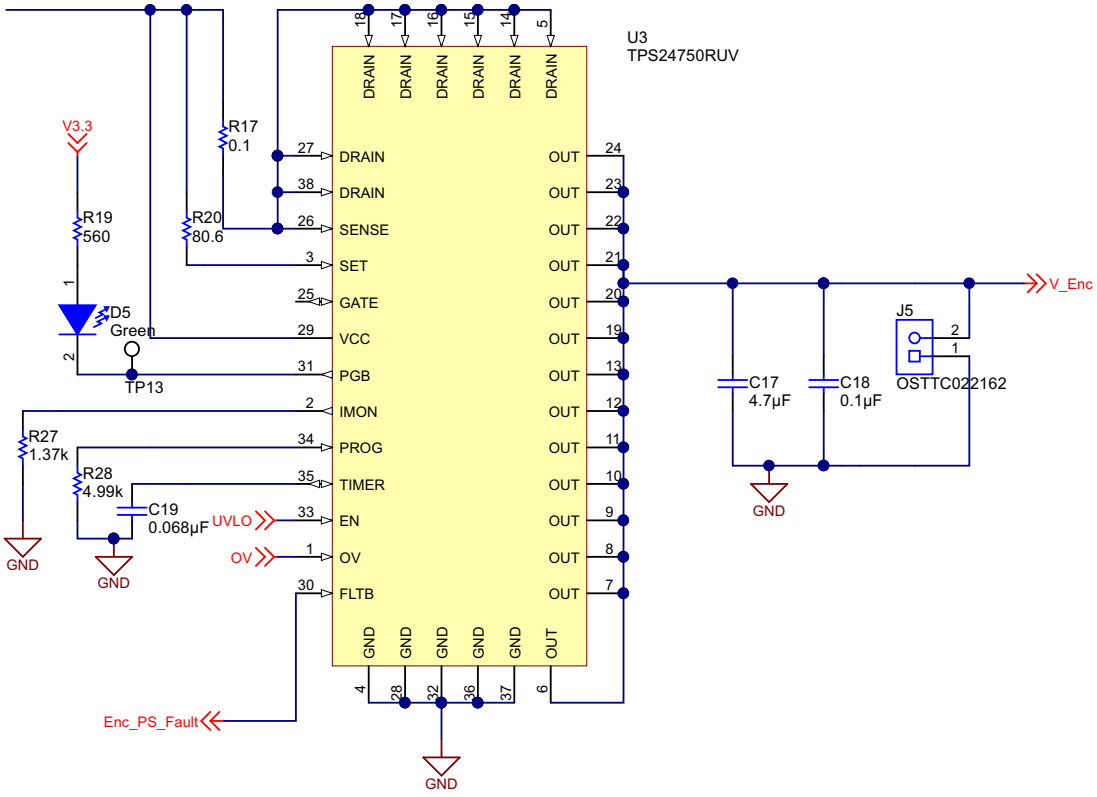

Figure 13. TPS24750 eFuse Schematic

4.3.1.2 Quad-FET Bus Switch: SN74CB3Q3125

The SN74CB3Q3125 is a Quadruple FET Bus Switch with a flat ON-state resistance (Ron = 3 Ω typical) characteristics over operating range. This part was chosen as four switches were required to configure the OV and UV limits. The schematic is shown in Figure 14. The calculation of the passive components is explained in Section 4.3.3.

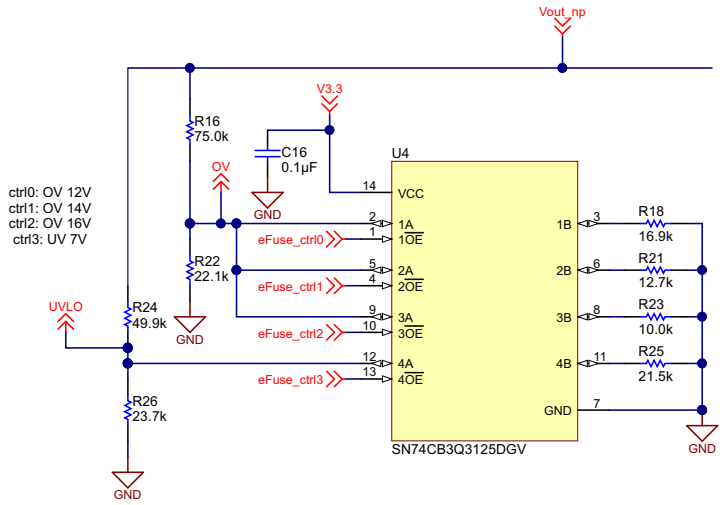

Figure 14. Schematic of Quad-FET SN74CB3Q3125 to Set OV and UV Limits

4.3.2 Setting Current Limits

The first step while designing with the TPS24750 is to select the sense resistor (R17). The TPS24750 has two current limit thresholds.

The first one is the current limit (Ilim, 400 mA) set by Equation 26. Once the current reaches Ilim, the fault timer, set by Equation 30, starts and the current is limited to Ilim. If the current is still limited to Ilim when the fault timer expires, the internal FET is open and the fault pin is asserted. As the latch version of the TPS24750 is used in the TIDA-00180, a power cycle of the TPS54040A is required to clear a fault.

The second current limit is the fast trip limit (Ifast_trip, 600 mA). If the fast trip current limit is reached (severe overload or dead short circuit), the gate of the internal FET is immediately pulled to ground. The fast trip circuit holds the internal FET open for a few micro seconds. Then the TPS24750 turns back on allowing the current limit feedback loop to take over the gate control and start the fault timer. If the current is still limited to Ilim when the fault timer expires, the internal FET is open and the Fault pin is asserted.

Equation 26 is used to determinate the sense resistor (R17) corresponding to the fast trip current threshold desired. The recommended range of the current limit threshold voltage extends from 10 to 42 mV. That means that Equation 27 needs to be verified when selecting the sense resistor.

$$R_{17} = \frac{60\,mV}{I_{fast\_trip}} \tag{26}$$

$$10\,mV \le R_{17} \times I_{lim} \le 42\,mV \tag{27}$$

For best performance, a current of approximately 0.5 mA should flow into the SET pin when the TPS24750 is in current limit. The voltage across the SET resistor (R20) nominally equals the voltage across the sense resistor. Equation 28 calculates the SET resistor accordingly.

$$R_{20} = \frac{R_{17} \times I_{lim}}{0.5\,mA} \tag{28}$$

Using Equation 29, the IMON resistor (R27) can be calculated to fix the current limit to the desired threshold.

$$R_{27} = \frac{0.675\,V \times R_{20}}{I_{lim} \times R_{17}} \tag{29}$$

C19 set the fault timer period.

$$C_{19} = \frac{10\,\mu A \times t_{flt}}{1.35} \tag{30}$$

4.3.3 Setting Voltage Limits

On a typical application the OV and the UV are set by a three-resistor divider network as shown on Figure 15 and calculated using Equation 31 and Equation 32.

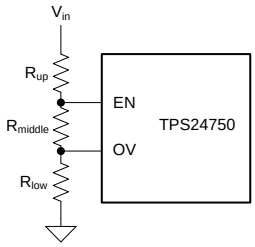

Figure 15. Typical Resistor Divider for OV and UV

$$R_{middle} = \frac{R_{low} \times (OV + UV_{ref} - OV_{ref} - UV)}{OV_{ref} + UV - UV_{ref}} \quad (31)$$

$$R_{up} = (R_{middle} + R_{low}) \times \frac{UV - UV_{ref}}{UV_{ref}} \quad (32)$$

with

- UVref = 1.3 V
- OVref = 1.35 V
- Rlow fixed at 15 kΩ

In TIDA-00180 the OV and UV can be configured to meet the different standards voltage range as shown on Table 1. The OV and UV can be configured as described in Table 6 and Table 7.

Table 6. OV Limit Setting

eFuse_ctrl0	eFuse_ctrl1	eFuse_ctrl2	OV
1	1	1	5 V
0	1	1	12 V
1	0	1	14 V
1	1	0	16 V

Table 7. UV Limit Setting

eFuse_ctrl3	UV
1	4 V
0	7 V

Similar to the method described in the Section 4.2.3, the different OV and UV settings are set by adding resistors in parallel to a resistor divider.

The SN74CB3Q3125 is used to replace the four MOSFETs that would be usually needed. R16 and R24 are set to 75 kΩ and 49.9 kΩ, respectively.

The default OV setting (OV = 6 V) is set using the resistor divider described in Equation 33, which gives R22 = 21.8 kΩ, 22.1 kΩ was chosen.

$$R_{22} = \frac{R_{16} \times OV_{ref}}{OV_1 - OV_{ref}} \tag{33}$$

The next OV setting (OV = 12 V) is set by adding R18 in parallel to R22. Equation 34 gives R18 = 16.9 kΩ.

$$R_{18} = \frac{R_{16} \times OV_{ref} \times R_{22}}{R_{22\times}\left(OV_2 - OV_{ref}\right) - R_{16} \times OV_{ref}} \tag{34}$$

The next OV setting (OV = 14 V) is set by adding R21 in parallel to R22. Equation 35 gives R21 = 12.7 kΩ.

$$R_{21} = \frac{R_{16} \times OV_{ref} \times R_{22}}{R_{22\times}\left(OV_3 - OV_{ref}\right) - R_{16} \times OV_{ref}} \tag{35}$$

The last OV setting (OV = 16 V) is set by adding R23 in parallel to R22. Equation 36 gives R23 = 10.1 kΩ, 10 kΩ was chosen.

$$R_{23} = \frac{R_{16} \times OV_{ref} \times R_{22}}{R_{22\times}\left(OV_4 - OV_{ref}\right) - R_{16} \times OV_{ref}} \tag{36}$$

The default UV setting (UV = 4 V) is set using the resistor divider described in Equation 37, which gives R26 = 24 kΩ, 23.7 kΩ was chosen.

$$R_{26} = \frac{R_{24} \times UV_{ref}}{UV_1 - UV_{ref}} \tag{37}$$

The last UV setting (UV = 7 V) is set by adding R25 in parallel to R26. Equation 38 gives R25 = 21.6 kΩ, 21.5 kΩ was chosen.

$$R_{25} = \frac{R_{24} \times UV_{ref} \times R_{26}}{R_{26\times}\left(UV_2 - UV_{ref}\right) - R_{24} \times UV_{ref}} \tag{38}$$

4.3.4 Layout Guidelines

Please refer to page 31 of the TPS24750 datasheet and Figure 106. Pay special attention to the layout for the sense resistor R_{SENSE}.

4.4 Power Supply Configuration Interface

The TIDA-00180 power supply offers configurable output voltage through I2C, configurable OV and UV limits as well as the fault and PG indicators through a 3.3-V TTL compatible GPIO. A host processor, which already implements the communication interface to the encoder (for example EnDat 2.2 Master) can be leveraged to also control this power supply.

4.4.1 Output Voltage Configuration through I2C

The digital potentiometer used is the TPL0401A-10. This device can be configured through standard I2C interface. The bidirectional I2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy. I2C communication with this device is initiated by the master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 16). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

The 7-bit slave address of the TPL0401A-10 is 0x2E. The data byte defines the resistance of the potentiometer. The I2C write and read can be seen in Figure 16.

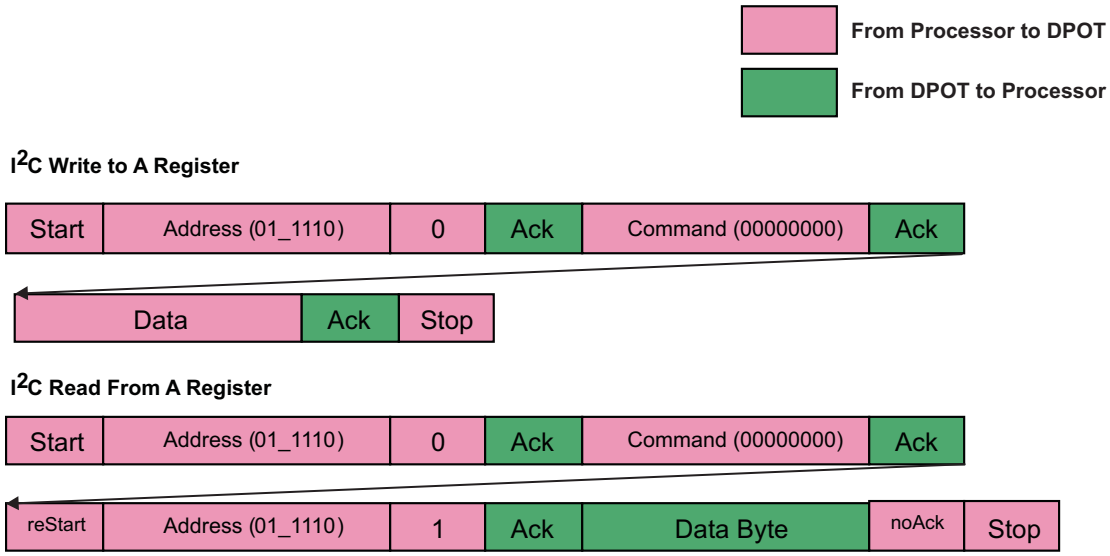

Figure 16. TPL0401A-10 I2C Write and Read Protocol

For more details refer to the TPL0401A-10 data sheet.

Table 8 shows the hex code with the corresponding resistor setting.

NOTE: The absolute resistor values have a tolerance and a software calibration will be needed initially to adjust accordingly. These settings are with respect to an ideal 10-kΩ resistance.

Table 8. Wiper Settings for Minimum and Maximum Voltage

HEX CODE	Rwh [kΩ]	Vout [V]
0x20	7.5	5
0x7F	0.08	15

4.4.2 OV and UV Protection Limits Configuration through GPIO

The resistor settings for the TPS24750 eFuse OV and UV settings are controlled with FET bus switches using the SN74CB3Q3125 device. Each individual switch is enabled with a low-level and disabled with a high level.

Refer to Table 6 and Table 7 in Section 4.3.3 for OV and UV settings.

4.4.3 Flowchart for Voltage and Protection Limits Configuration

Figure 17 shows the recommend software structure for the host microcontroller to initialize the communication to the power supply after power up, set or change the desired output voltage as well as OV, UV protection limits and fault handling.

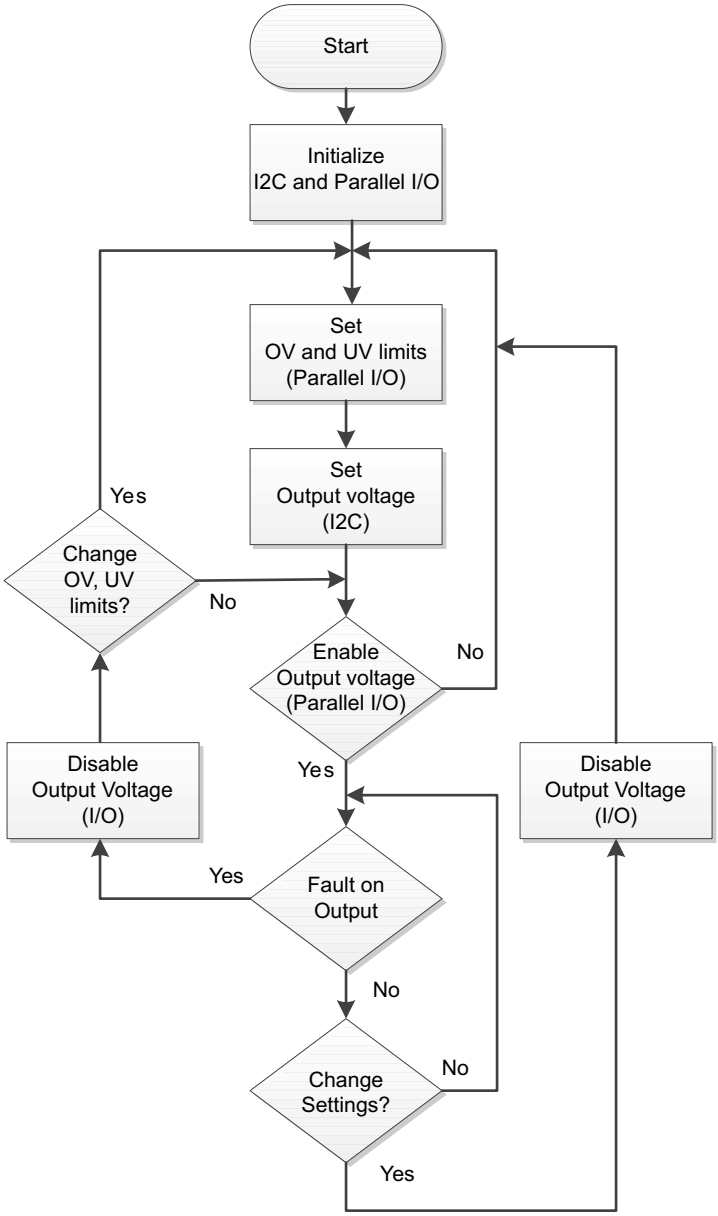

Figure 17. Flowchart for Voltage and Protection Limits Configuration

During the test of the TIDA00180 power supply design a C2000 LaunchPad was used to configure the output voltage, OV and UV protection limits as well as control the power supply enable signal and monitor the fault signal.

5 Getting Started

5.1 PCB Overview

A picture of the PCB with the function blocks is shown in Figure 18.

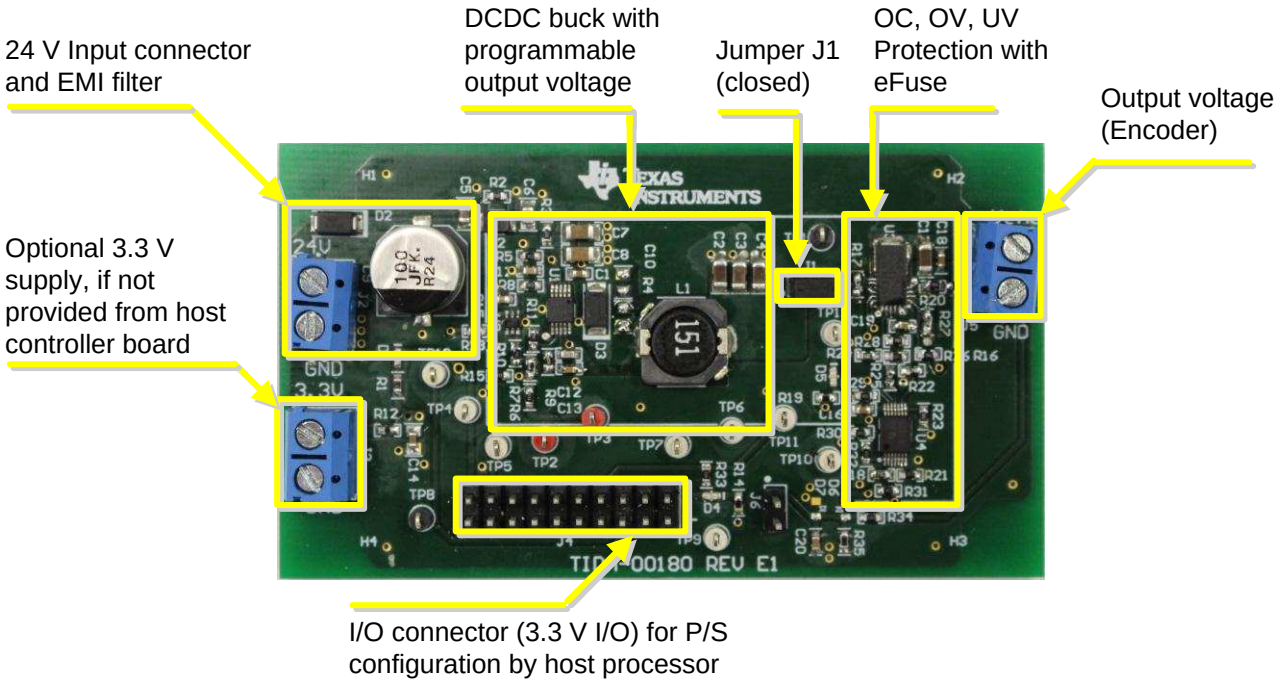

Figure 18. TIDA-00180 PCB with Functional Blocks

5.2 Connectors and Jumper Settings

The connector assignment and jumper settings are outlined here.

Add a jumper at J1 to connect the output of the DC-DC buck to the input of the eFuse. This jumper has been added for test and measurement purpose only.

Table 9. J2: Input Voltage Connector

PIN	DESCRIPTION
1	Input voltage (18 to 36 V)
2	GND

Table 10. J3: 3.3-V Connector

PIN	DESCRIPTION
1	3.3 V
2	GND

Table 11. J4: Configuration Interface (3.3-V I/O)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	GND	11	SCL (TPL0401A-10) (I)
2	GND	12	SDA (TPL0401A-10) (I/O)
3	GND	13	eFuse_ctrl0 (TPS24750) (I)
4	GND	14	eFuse_ctrl1 (TPS24750) (I)
5	GND	15	eFuse_ctrl2 (TPS24750) (I)
6	GND	16	eFuse_ctrl3 (TPS24750) (I)
7	GND	17	Fault (TPS24750) (O)
8	GND	18	Enable (TPS54040A) (I)
9	GND	19	3.3 V
10	GND	20	3.3 V

Table 12. J5: Output Voltage

PIN	DESCRIPTION
1	Output voltage
2	GND

6 Test Results

6.1 Setup

Figure 19 shows the setup and the test equipment used.

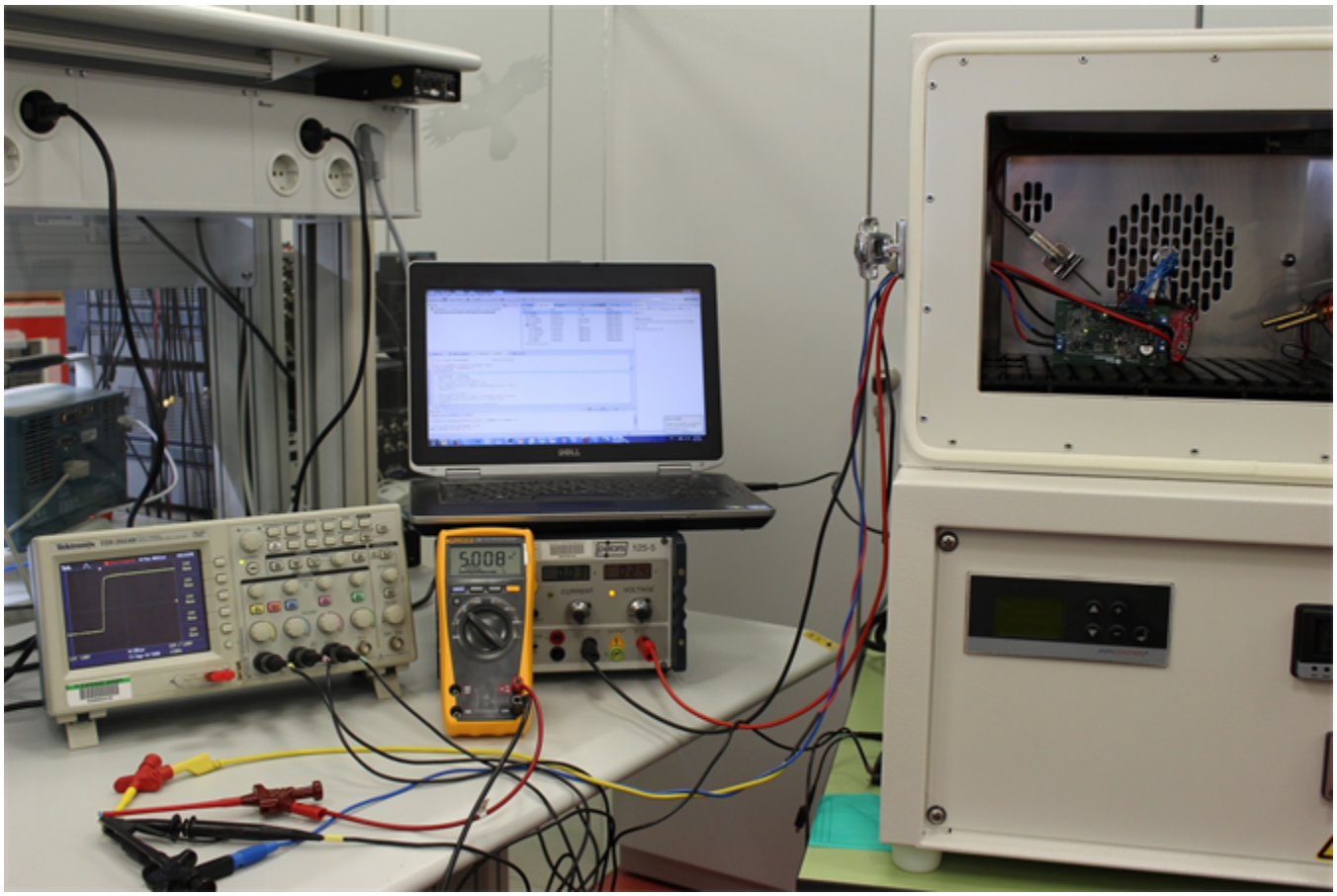

Figure 19. Picture of Test Setup for TIDA-00180 Temperature Performance tests

Table 13. Test Equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscopes	Tektronix TDS2024B, TDS794D, P6330/P6339A diff/passive probes
Current probe	LEM HEME PR30
Temperature test chamber	Voetsch vt4002
Microcontroller	C2000 Piccolo LaunchPad, http://www.ti.com/tool/launchxl-f28027

6.2 Output Voltage Performance

6.2.1 Output Voltage Setting

Table 14 shows the output voltage obtained at the connector J5 depending on which step was sent to the digital potentiometer. The values in Table 14 where measured with a 24-V input voltage and 100-mA load current.

Table 14. Output Voltage Setting

POTENTIOMETER STEP (HEX)	Vout at 25°C	Vout at 85°C
0x23	5.02 V	5.03 V
0x3E	5.99 V	6.01 V
0x50	7.00 V	7.02 V
0x5C	7.97 V	7.98 V
0x65	8.97 V	8.99 V
0x6C	9.98 V	10.00 V
0x72	11.10 V	11.12 V
0x76	12.03 V	12.04 V
0x7A	13.16 V	13.18 V
0x7D	14.18 V	14.19 V
0x7F	14.97 V	14.98 V

Figure 20 shows the output voltage step size versus the output voltage. The resolution at a lower voltage is higher, or in other words the voltage steps size is smaller. At 5 V, the step size is as small as 30 mV, which allows accurate setting of 5 V or a slightly higher 5.25 V to compensate for cable losses.

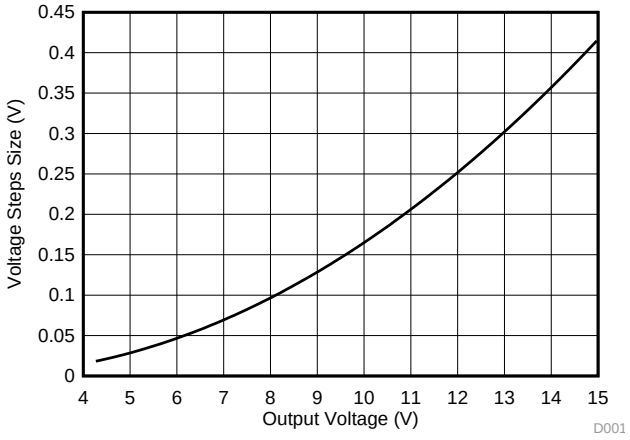

Figure 20. Voltage Steps Size versus Output Voltage

6.2.2 Output Voltage Characteristics

Figure 21 through Figure 28 show the output voltage variation, depending load current, and input voltage. There is almost negligible impact on the output voltage at a 1% maximum.

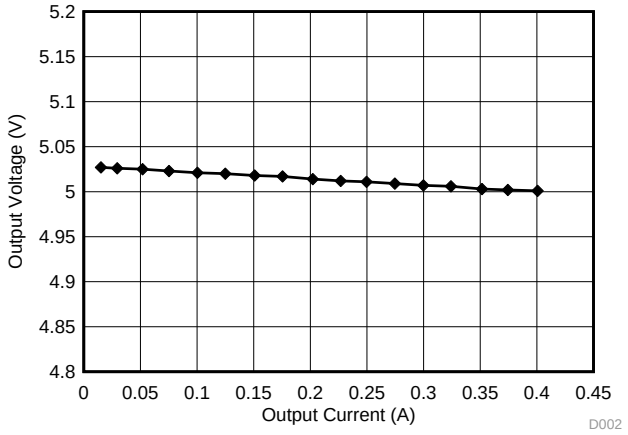

Figure 21. Output Voltage versus Output Current at 24 Vin and 5 Vout

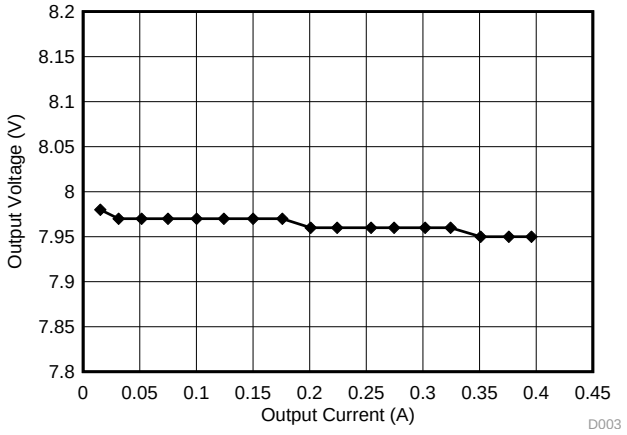

Figure 22. Output Voltage versus Output Current at 24 Vin and 8 Vout

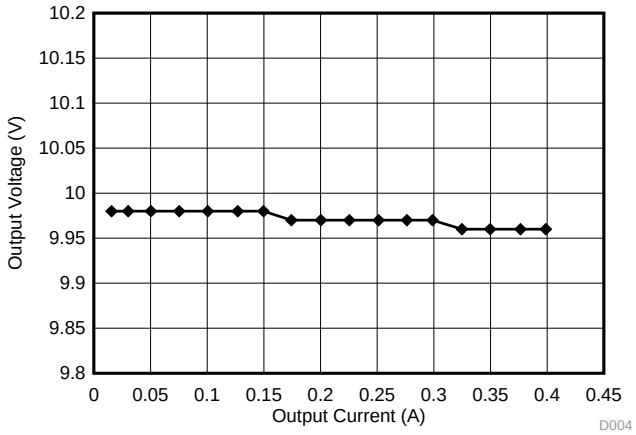

Figure 23. Output Voltage versus Output Current at 24 Vin and 10 Vout

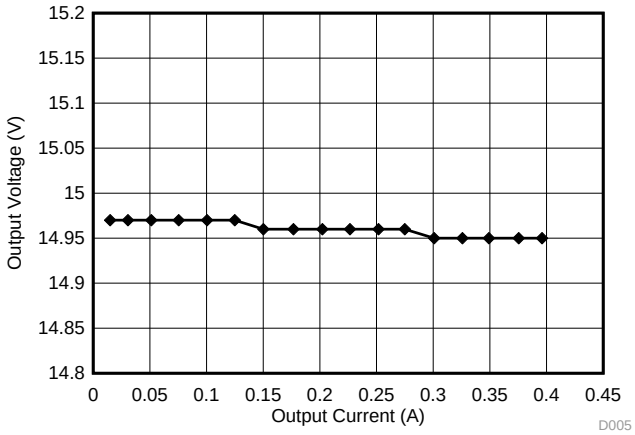

Figure 24. Output Voltage versus Output Current at 24 Vin and 15 Vout

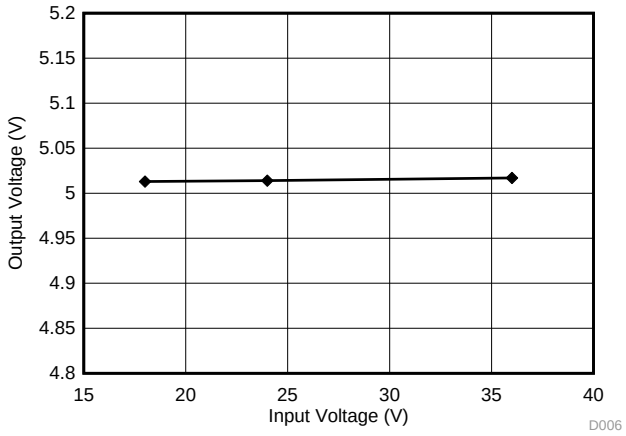

Figure 25. Output Voltage versus Input Voltage at 5 Vout and 200-mA load

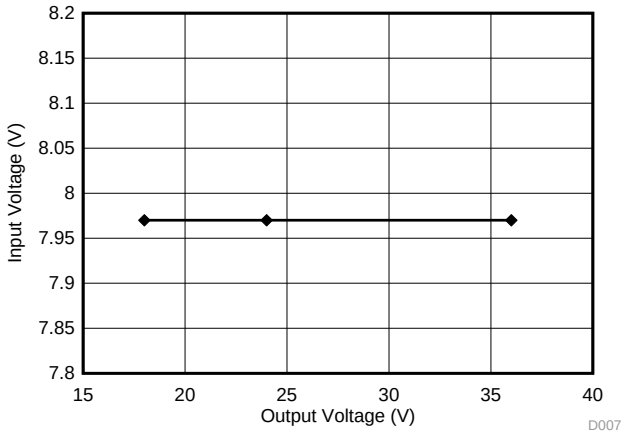

Figure 26. Output Voltage versus Input Voltage at 8 Vout and 125-mA load

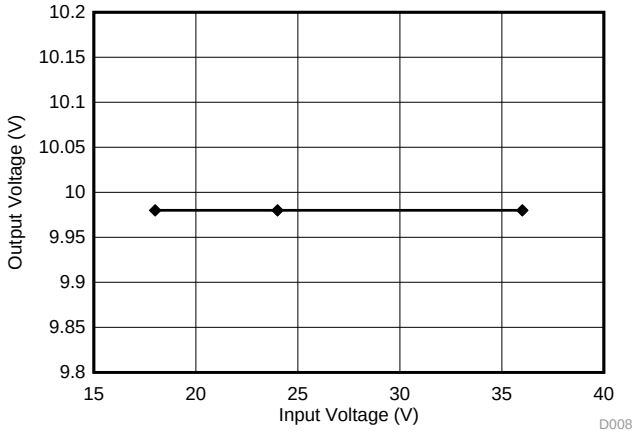

Figure 27. Output Voltage versus Input Voltage at 10 Vout and 100-mA load

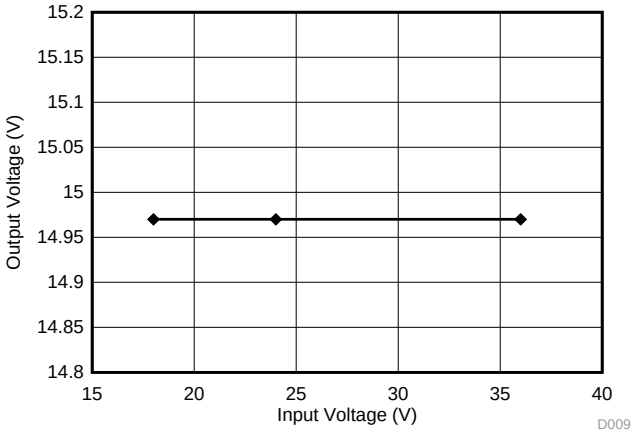

Figure 28. Output Voltage versus Input Voltage at 15 Vout and 66-mA load

6.2.3 Output-Voltage Ripple

The output-voltage ripple of the encoder supply remains below 15 mVpp over the entire output current range. Figure 29 through Figure 32 show the output voltage ripple at a 1-W load, with the oscilloscope in AC-coupling mode.

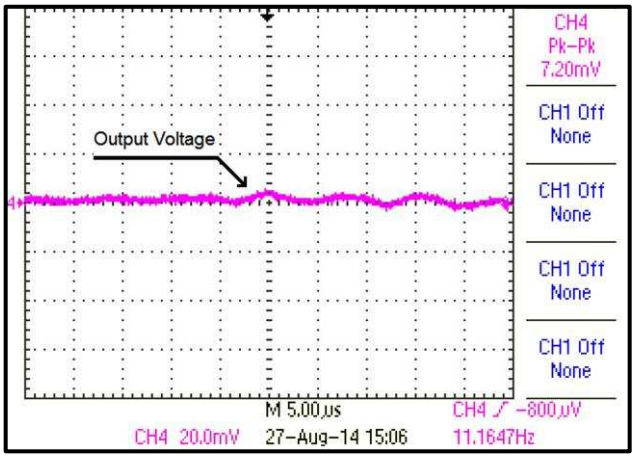

Figure 29. Output Voltage Ripple with 24 Vin, 5 Vout at 200-mA Load

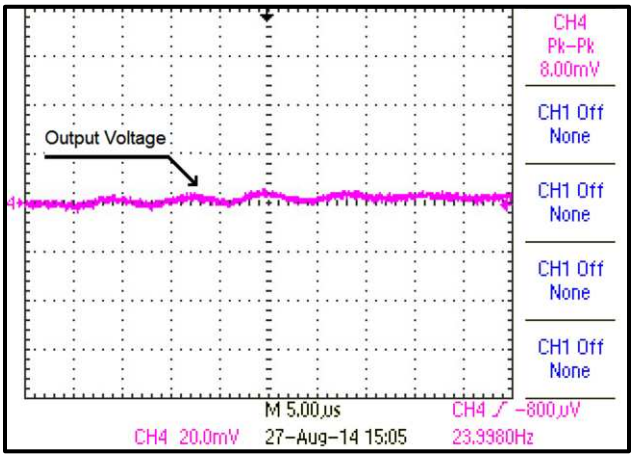

Figure 30. Output Voltage Ripple with 24 Vin, 8 Vout at 125-mA Load

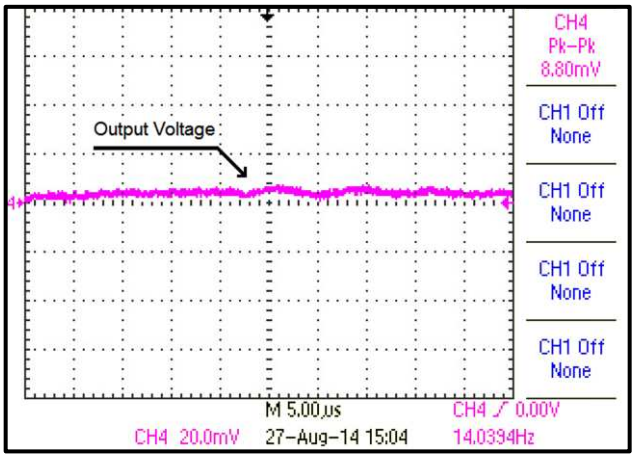

Figure 31. Output Voltage Ripple with 24 Vin, 10 Vout at 100-mA Load

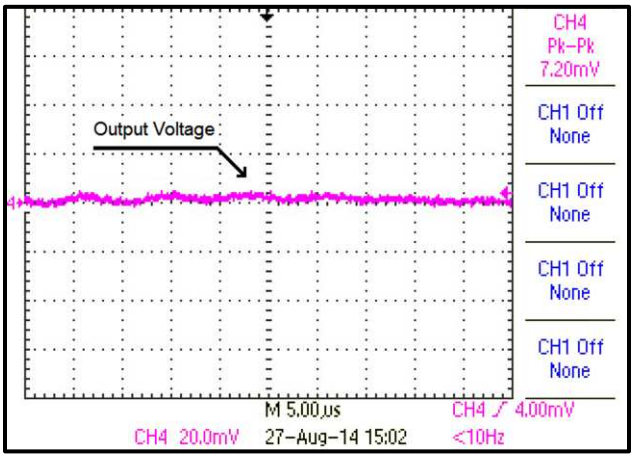

Figure 32. Output Voltage Ripple with 24 Vin, 15 Vout at 66-mA Load

6.2.4 Efficiency

The efficiency was calculated by measuring the voltage and current through the 24-V input connector (J2) and the voltage and current through the output connector (J5). Measuring through J2 and J5 means that this efficiency curve includes the input filter, the DC-DC converter (TPS54040A), and the eFuse (TPS24750). This design achieves above 80% efficiency overall at 5 V/200 mA, 8 V/125 mA, 10 V/100 mA, and 15 V/66 mA.

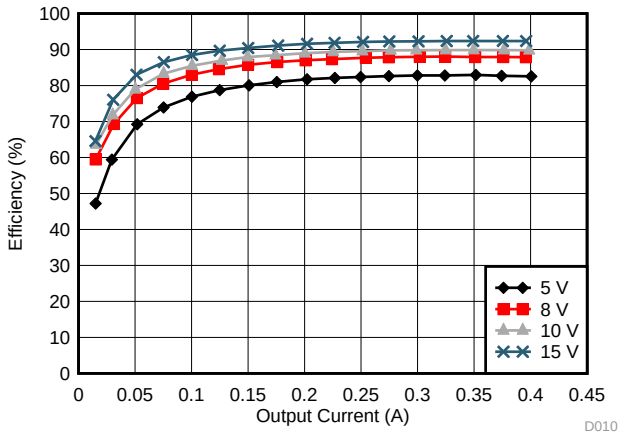

Figure 33. Efficiency as Function of Output Current and Output Voltage

6.2.5 Switch Node Waveforms

Figure 34 through Figure 49 show the switch node waveforms at nominal load and light load as shown. These curves were measured across the diode D3.

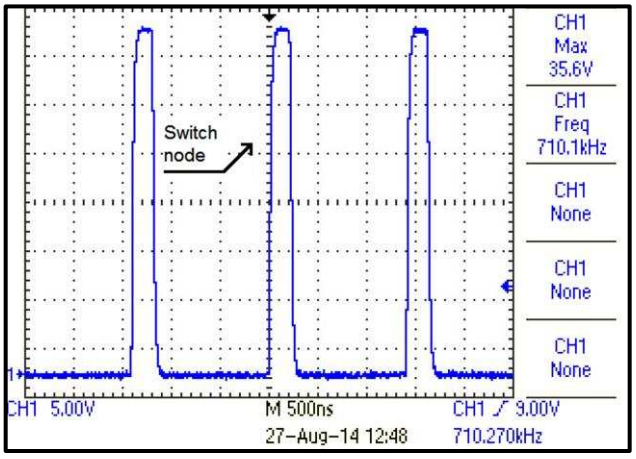

Figure 34. Switch Node Voltage with 36 Vin, 5 Vout at 300-mA Load

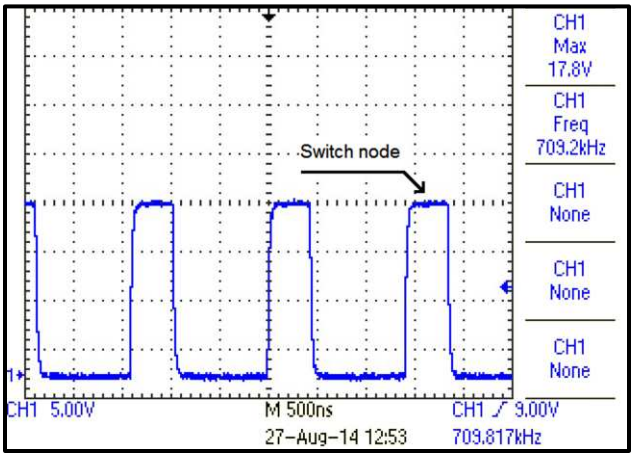

Figure 35. Switch Node Voltage with 18 Vin, 5 Vout at 300-mA Load

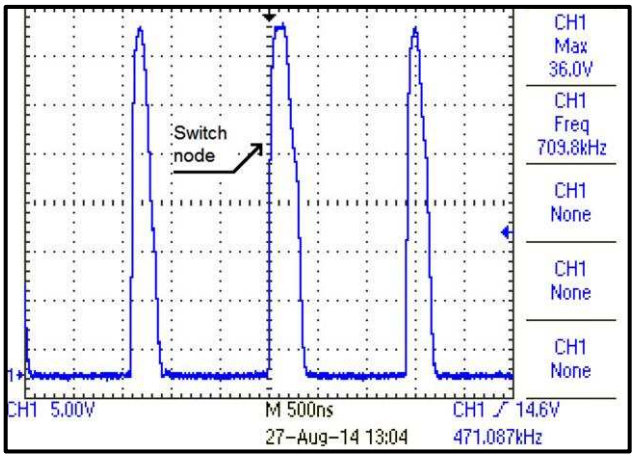

Figure 36. Switch Node Voltage with 36 Vin, 5 Vout at 30-mA Load

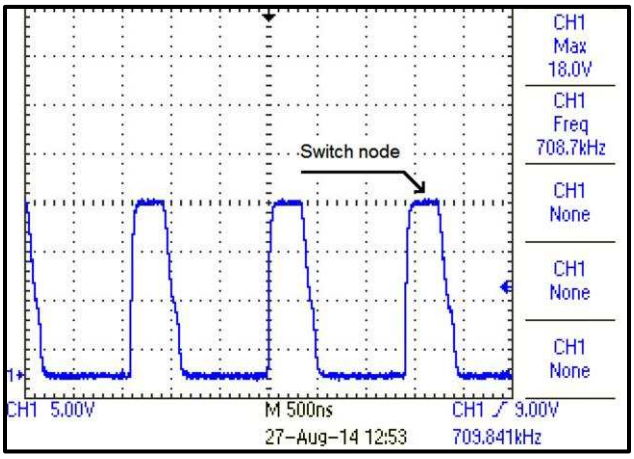

Figure 37. Switch Node Voltage with 18 Vin, 5 Vout at 30-mA Load

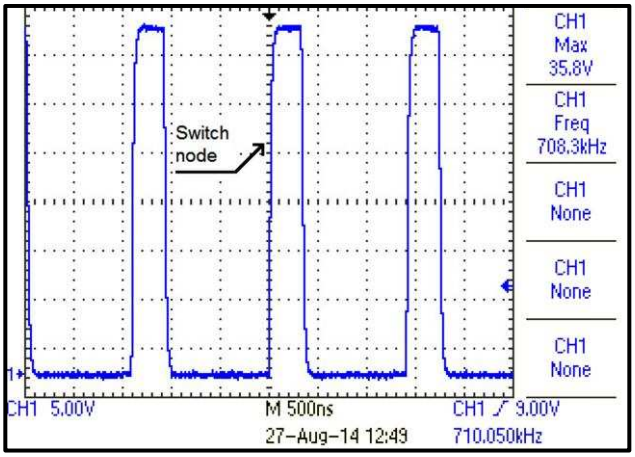

Figure 38. Switch Node Voltage with 36 Vin, 8 Vout at 300-mA Load

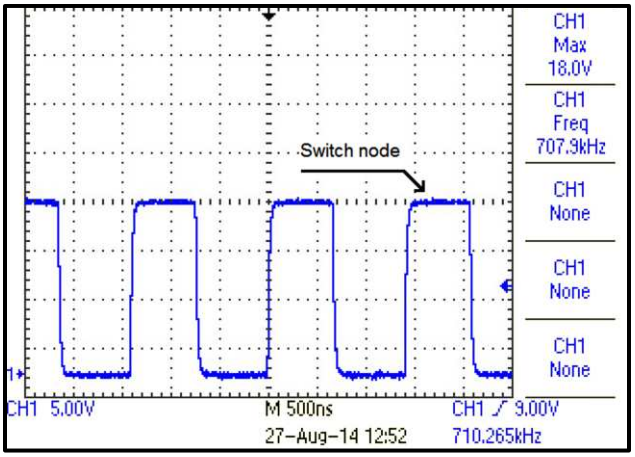

Figure 39. Switch Node Voltage with 18 Vin, 8 Vout at 300-mA Load

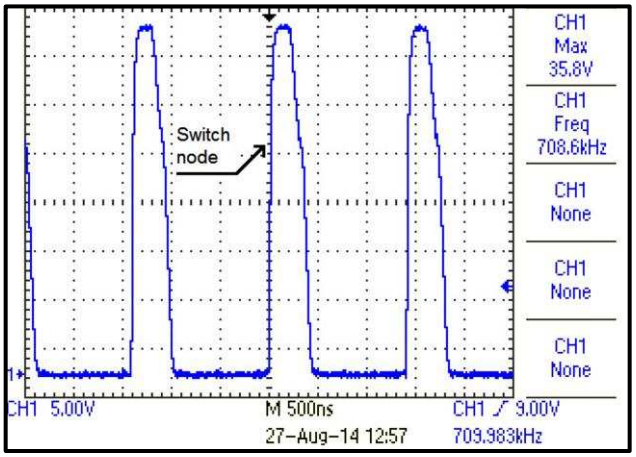

Figure 40. Switch Node Voltage with 36 Vin, 8 Vout at 30-mA Load

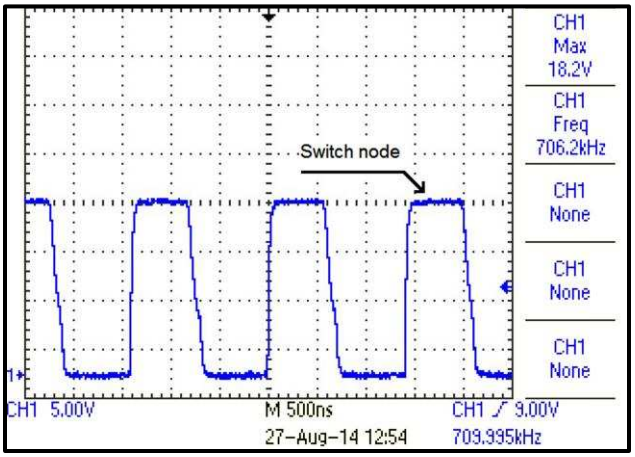

Figure 41. Switch Node Voltage with 18 Vin, 8 Vout at 30-mA Load

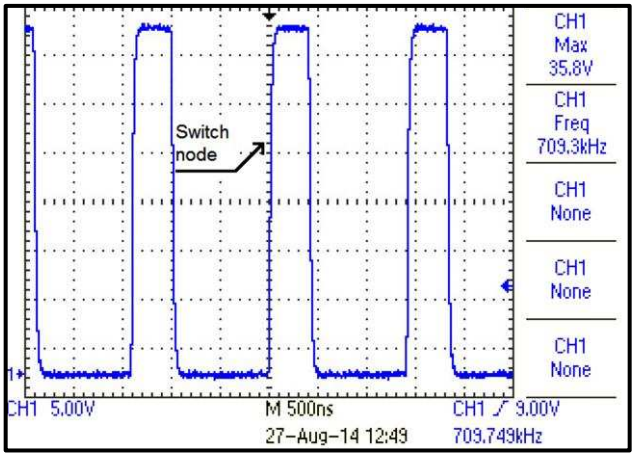

Figure 42. Switch Node Voltage with 36 Vin, 10 Vout at 300-mA Load

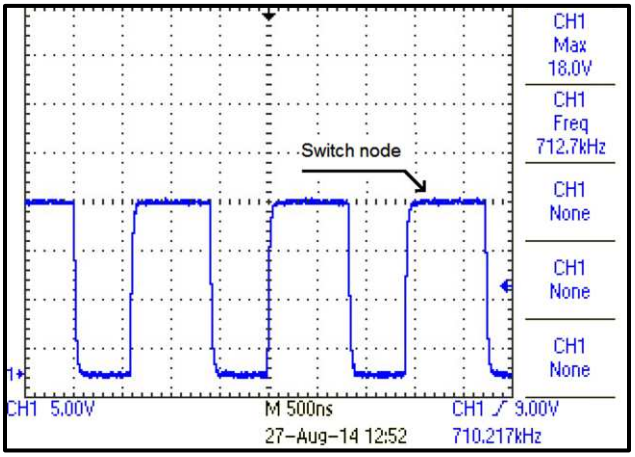

Figure 43. Switch Node Voltage with 18 Vin, 10 Vout at 300-mA Load

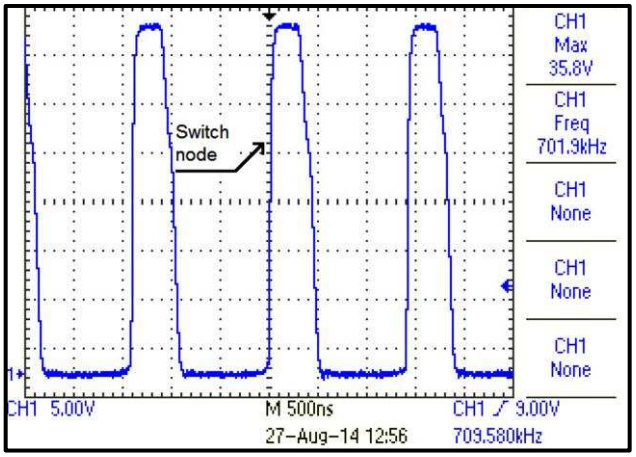

Figure 44. Switch Node Voltage with 36 Vin, 10 Vout at 30-mA Load

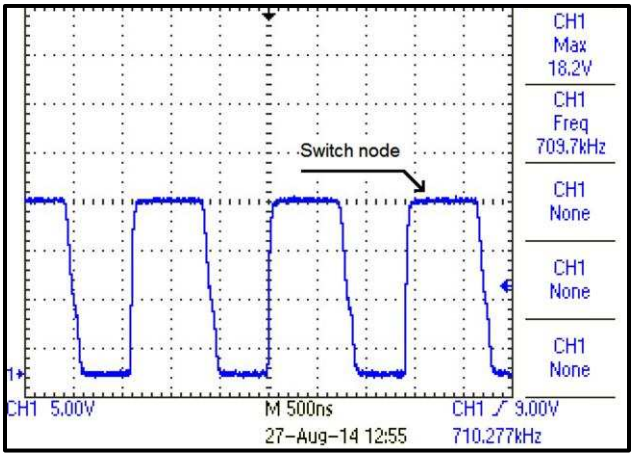

Figure 45. Switch Node Voltage with 18 Vin, 10 Vout at 30-mA Load

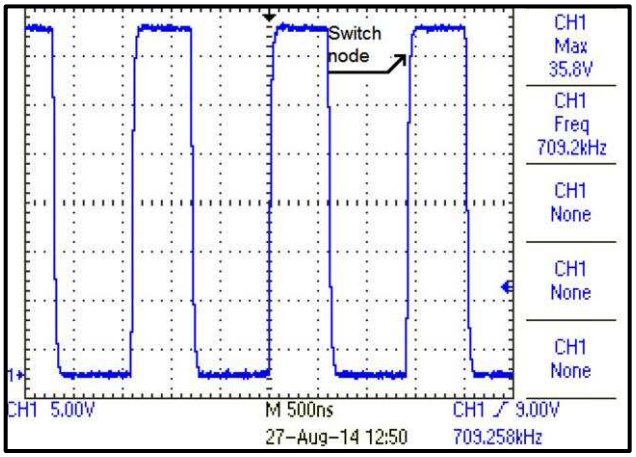

Figure 46. Switch Node Voltage with 36 Vin, 15 Vout at 300-mA Load

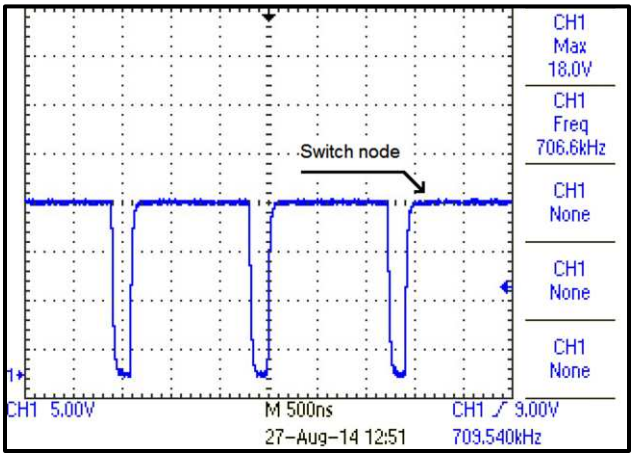

Figure 47. Switch Node Voltage with 18 Vin, 15 Vout at 300-mA Load

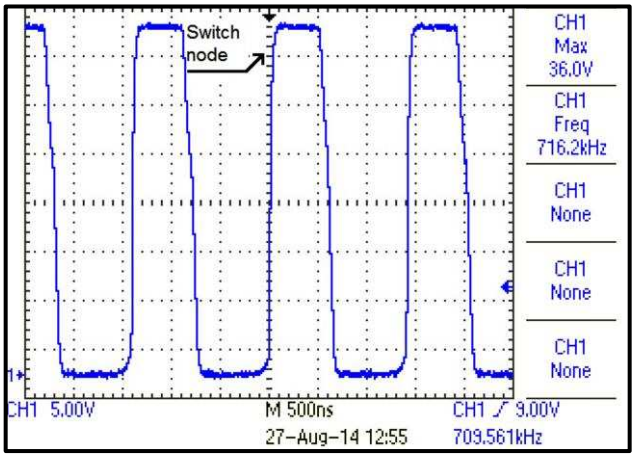

Figure 48. Switch Node Voltage with 36 Vin, 15 Vout at 30-mA Load

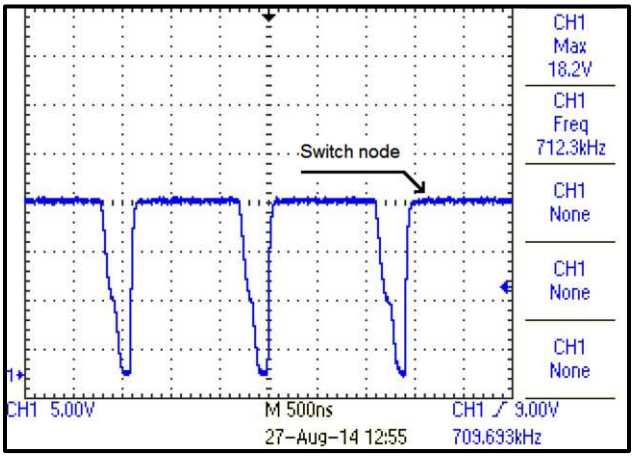

Figure 49. Switch Node Voltage with 18 Vin, 15 Vout at 30-mA Load

6.2.6 Bode Plots

The bode plot allows verifying that the loop is stable. A second order compensation has been implemented through R9, C12, and C13. The Bode plots have been measured for the lower input voltage limit of 18 V and upper limit of 36 V. The output voltage was set to 5 V/200 mA and 15 V/66 mA.

As shown in Table 15 and Figure 50, there is enough phase and gain margin for the entire input voltage range.

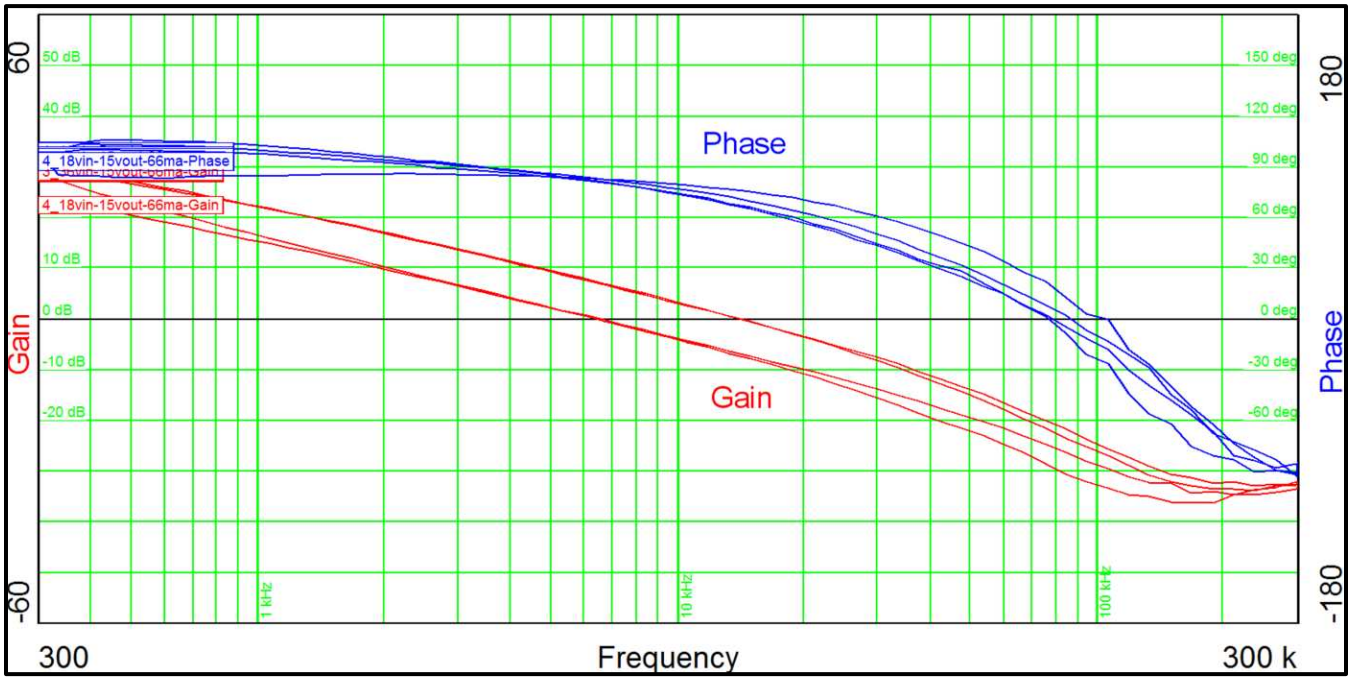

Figure 50. Bode Plot

Table 15. Phase and Gain Margin

	PHASE MARGIN	GAIN MARGIN
Input: 36 V, Output: 5 V at 200 mA	70.91 degree	–22.2 dB
Input: 18 V, Output: 5 V at 200 mA	66.34 degree	–22.19 dB
Input: 36 V, Output: 15 V at 66 mA	83.37 degree	–29.4 dB
Input: 18 V, Output: 15 V at 66 mA	81.15 degree	–28.89 dB

6.3 OC, OV and UV Protection Performance at 25°C and 85°C

6.3.1 Short Circuit Protection at 25°C and 85°C

The function of the OC fault timer was tested during start-up by connecting a resistive load of 1 Ω at the connector J5, the 1-Ω resistor draws more than the maximum current specified, allowing to trigger the fault once the timer expires.

Figure 51 through Figure 54 show that the current is limited to around 390 mA in both cases until the fault timer expires and the eFuse disconnects to prevent damage from the power supply.

As seen on Figure 51 and Figure 52, the fault timer at 25°C is 10 ms. At 85°C the fault timer is 8 ms, as seen Figure 53 and Figure 54 due to the variation of the timing capacitor C19 over temperature.

In Figure 51 through Figure 54, the black curve is the enable signal, the green curve is the output voltage at J5 connector, and the red curve is the output current through J5.

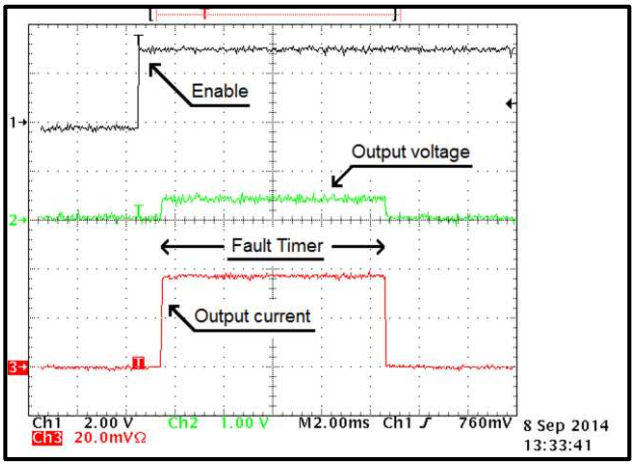

Figure 51. eFuse OC Protection with Disconnect after 10 ms with 24 Vin, 5 Vout and 1-Ω load at 25°C

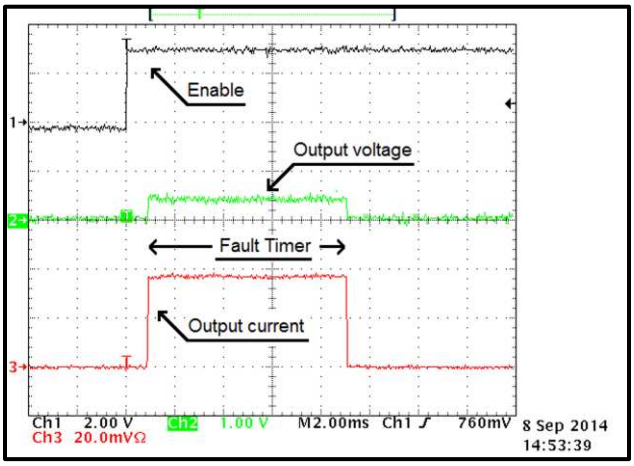

Figure 52. eFuse OC Protection with Disconnect after 8 ms with 24 Vin, 5 Vout and 1-Ω load at 85°C

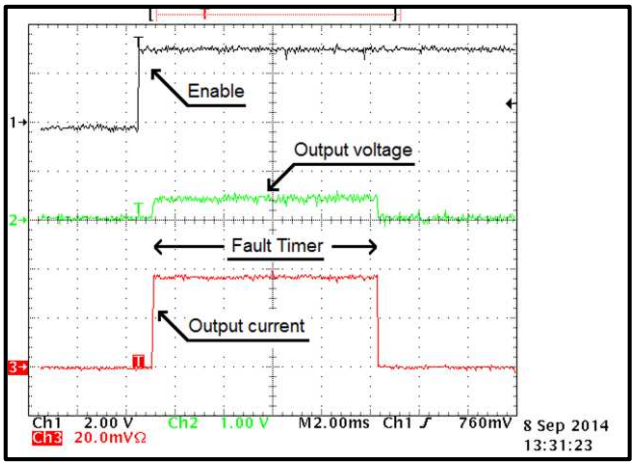

Figure 53. eFuse OC Protection with Disconnect after 10 ms with 24 Vin, 15 Vout and 1-Ω load at 25°C

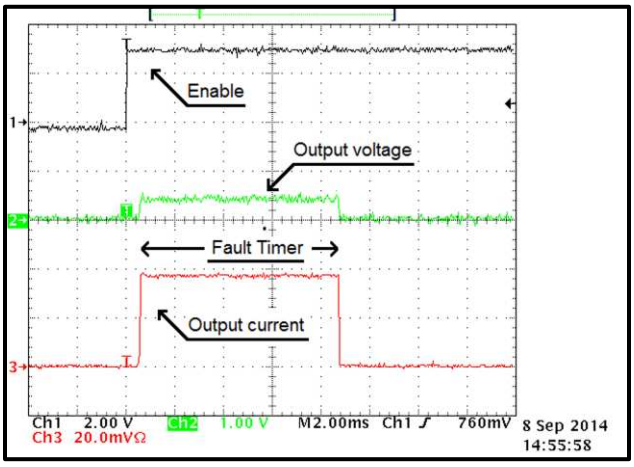

Figure 54. eFuse OC Protection with Disconnect after 8 ms with 24 Vin, 15 Vout and 1-Ω load at 85°C

6.3.2 Inrush Current Limitation at 25°C and 85°C

A 100-uF load capacitor was used to test the inrush-current and OC limitation feature of the eFuse. As shown in Figure 55 through Figure 62, the eFuse limits the inrush current until the capacitor is charged. The output voltage ramps up to its nominal value. Therefore, it is possible even with encoders that have a large bulk capacity. However, it will be required to adjust the fault timer accordingly to the maximum bulk-capacitive load to prevent unwanted fault trigger and disconnect during power-up.

Please note that the measured inrush current is around 370 mA and hence around 20 mA lower than with a resistive load. The reason for this is that during startup the 4.7-µF capacitor at the eFuse output is charged in parallel to the 100-µF load capacitor, which yields a capacitive current divider. Due to that around 5% of the around 390-mA inrush current = 20 mA charges the 4.7-µF load cap, while the remaining 370 mA charge the load capacitor, where the load current was measured.

In Figure 55 through Figure 62, the black curve is the enable signal, the green curve is the output voltage at J5 connector, and the red curve is the output current through J5.

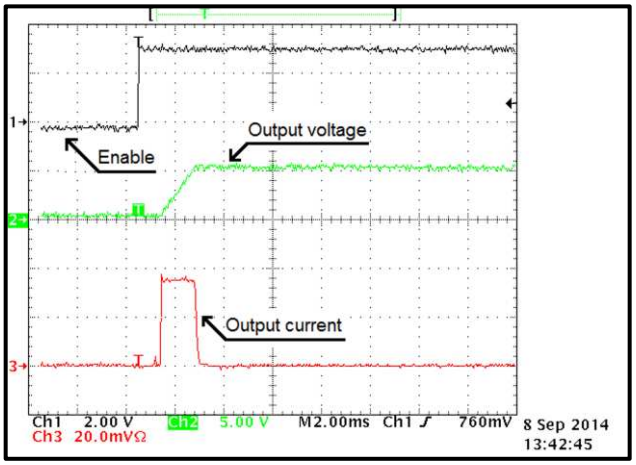

Figure 55. Inrush-Current Limitation with 24 Vin, 5 Vout, and 100-µF Capacitive Load at 25°C

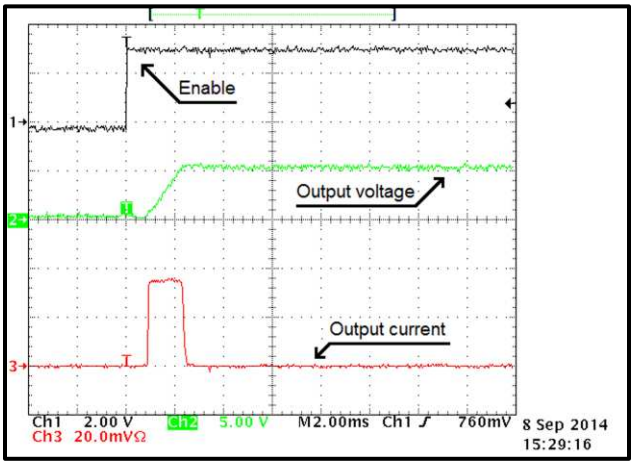

Figure 56. Inrush-Current Limitation with 24 Vin, 5 Vout, and 100-µF Capacitive Load at 85°C

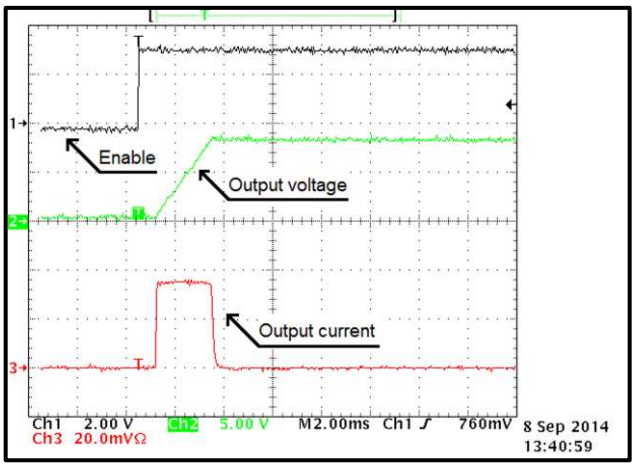

Figure 57. Inrush-Current Limitation with 24 Vin, 8 Vout, and 100-µF Capacitive Load at 25°C

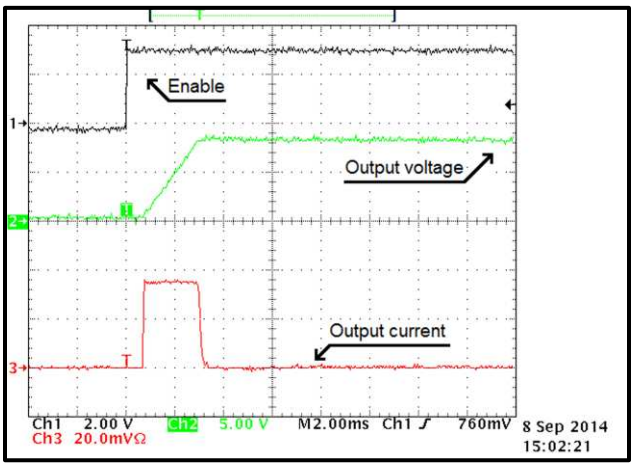

Figure 58. Inrush-Current Limitation with 24 Vin, 8 Vout, and 100-µF Capacitive Load at 85°C

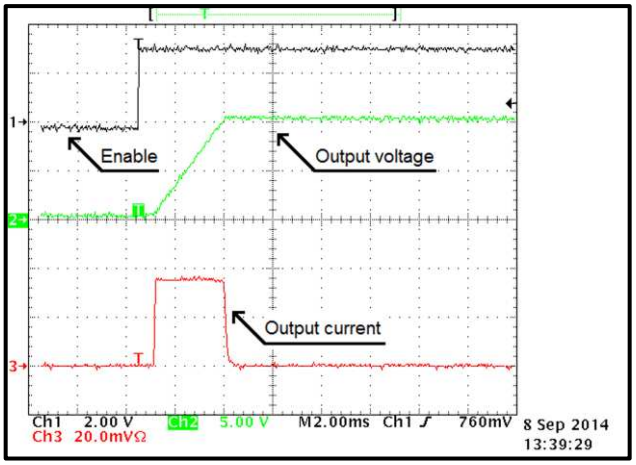

Figure 59. Inrush-Current Limitation with 24 Vin, 10 Vout, and 100-µF Capacitive Load at 25°C

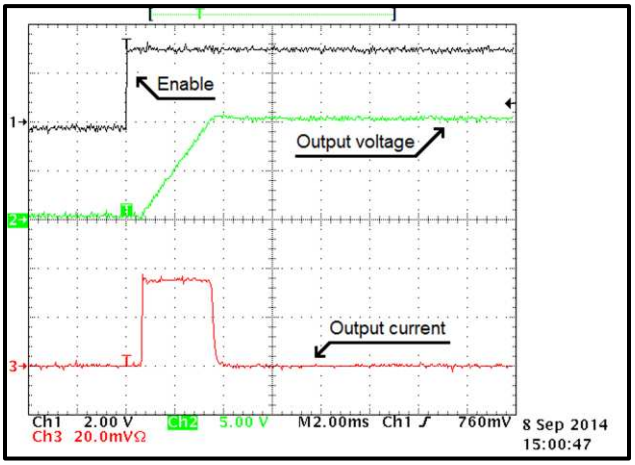

Figure 60. Inrush-Current Limitation with 24 Vin, 10 Vout, and 100-µF Capacitive Load at 85°C

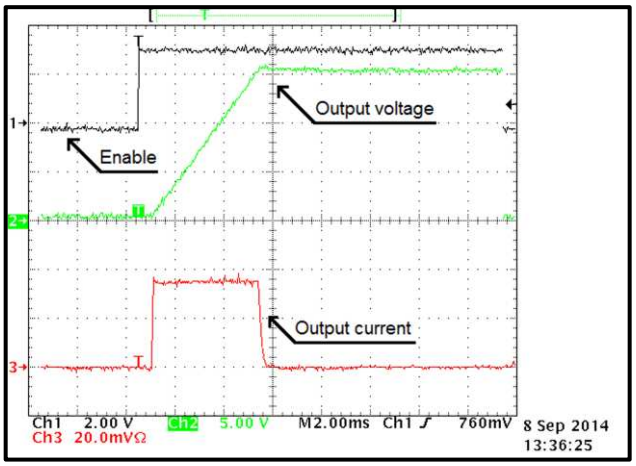

Figure 61. Inrush-Current Limitation with 24 Vin, 15 Vout, and 100-µF Capacitive Load at 25°C

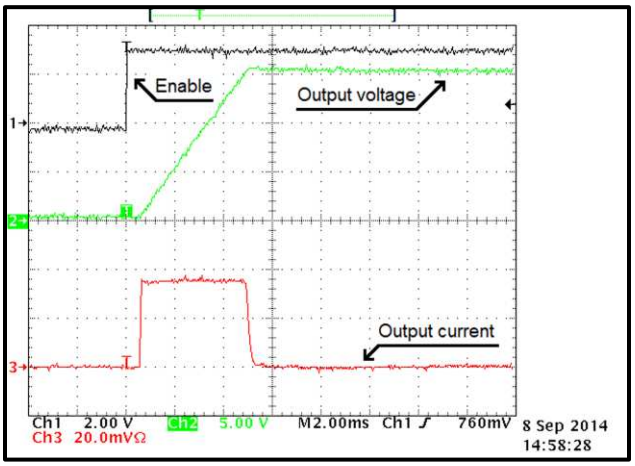

Figure 62. Inrush-Current Limitation with 24 Vin, 15 Vout, and 100-µF Capacitive Load at 85°C

6.3.3 OV and UV Limits

The OV and UV limits were tested by starting the design with an output voltage within the OV and UV boundaries. Then a different voltage was set thanks to the TPL0401A-10. The input voltage is 24 V and the output load is 100 mA. The input voltage of the eFuse was measured on the jumper J1, the output voltage was measured at J5.

As shown in Figure 63 through Figure 72, the OV and UV limits are accurate over the temperature range.

Please note that the TIDA-00180 cannot supply a voltage lower than 4 V or higher than 15 V (due to design specifications). Therefore, to test the 4-V UV, the TPS54040A was first set to 5 V then disabled. The voltage then drops due to the 100-mA load. Once the 4-V UV limit is reached, the eFuse disconnects the output. The output voltage continue to drop due to the 100-mA load while the eFuse input voltage stays at 4 V due to the output capacitors of the TPS54040A (C2, C3 and C4). To test the 16-V OV, an external power supply was used to power the eFuse through the jumper J1. The 16-V OV limit was measured at 16.1 V at both 25°C and 85°C.

Figure 63 to Figure 68 show successful trigger of the OV protection at 25°C and 85°C at the selected limits. The output voltage drops after the trip event. Due to 4.7 µF at output and 100-mA load current the voltage decrease accordingly by around 2 V/100 us.

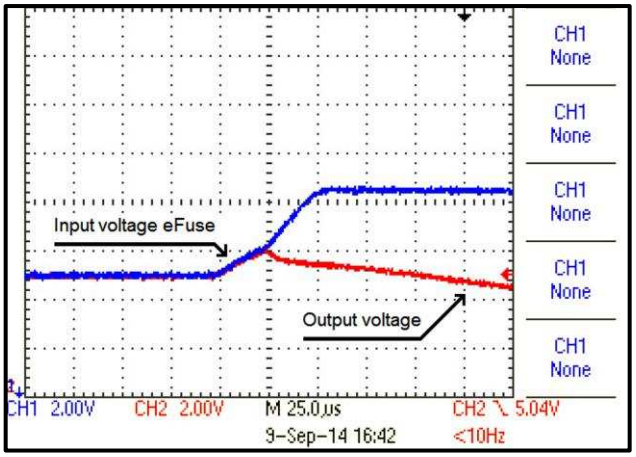

Figure 63. 6-V OV Event at 25°C, Voltage Step from 5 to 8 V at 100 mA

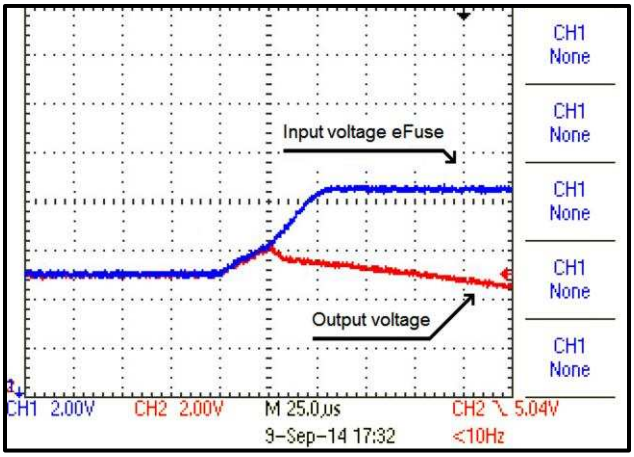

Figure 64. 6-V OV Event at 85°C, Voltage Step from 5 to 8 V at 100-mA Load

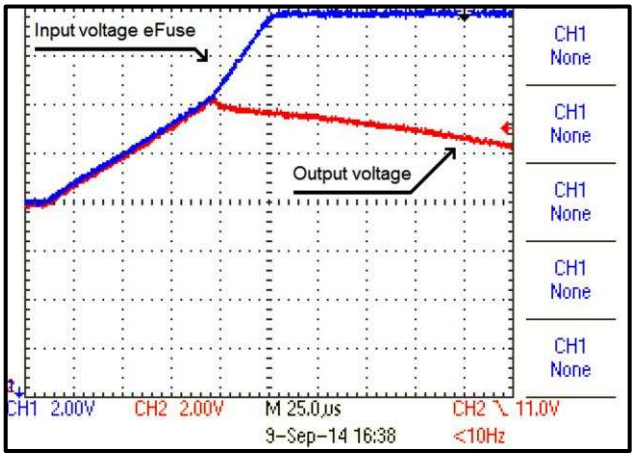

Figure 65. 12-V OV Event at 25°C, Voltage Step from 8 to 15 V at 100-mA Load

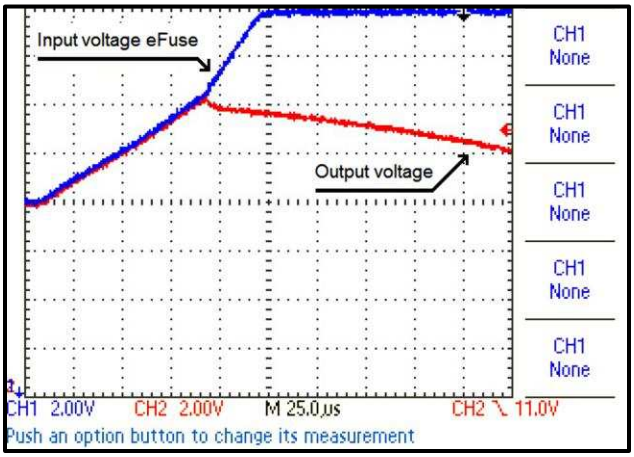

Figure 66. 12-V OV Event at 85°C, Voltage Step from 8 to 15 V at 100 mA Load

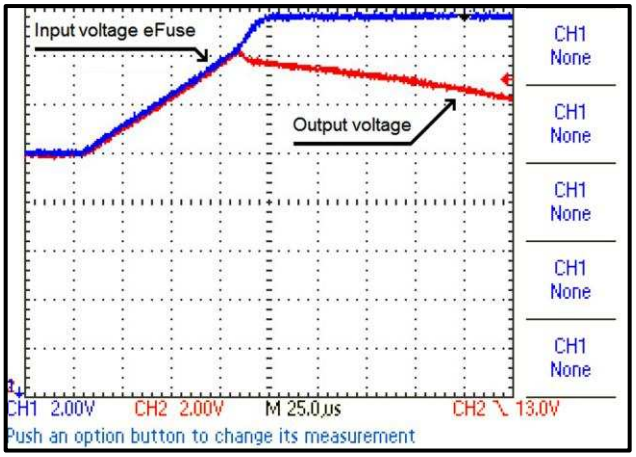

Figure 67. 14-V OV Event at 25°C, Voltage Step from 10 to 15 V at 100-mA Load

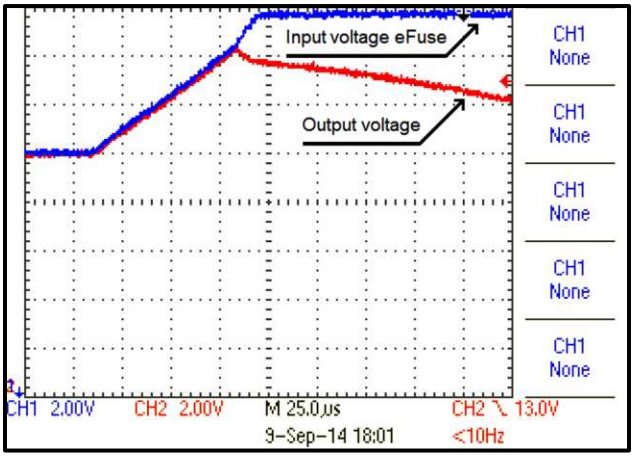

Figure 68. 14-V OV Event at 85°C, Voltage Step from 10 to 15 V at 100-mA Load

Figure 69 to Figure 72 show successful trigger of the UV protection at 25°C and 85°C at the selected limits. The output voltage drops after the trip event. Due to 4.7-µF at output and 100-mA load current, the voltage decrease accordingly by around 2 V/100 us.

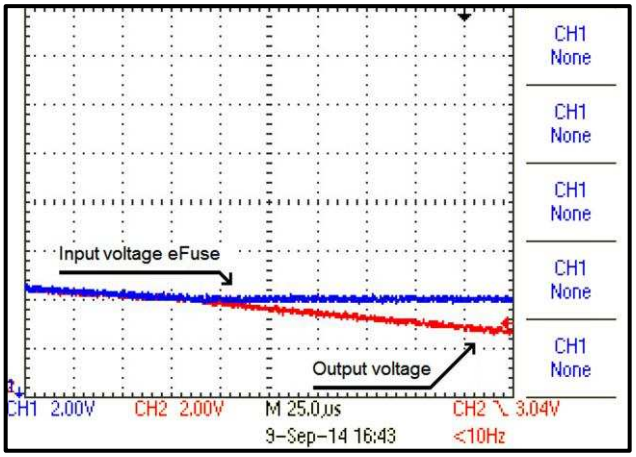

Figure 69. 4-V UV Event at 25°C

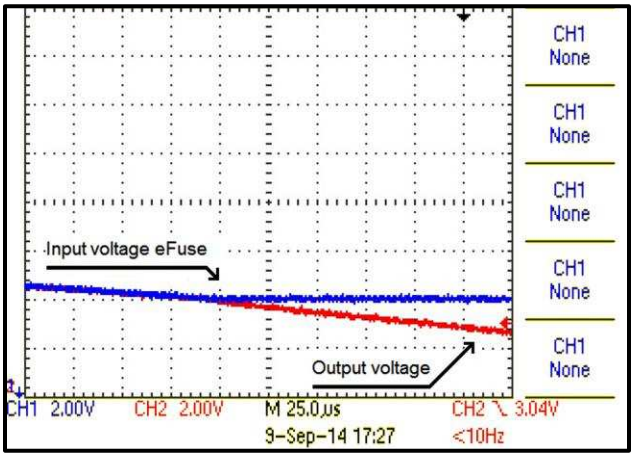

Figure 70. 4-V UV Event at 85°C

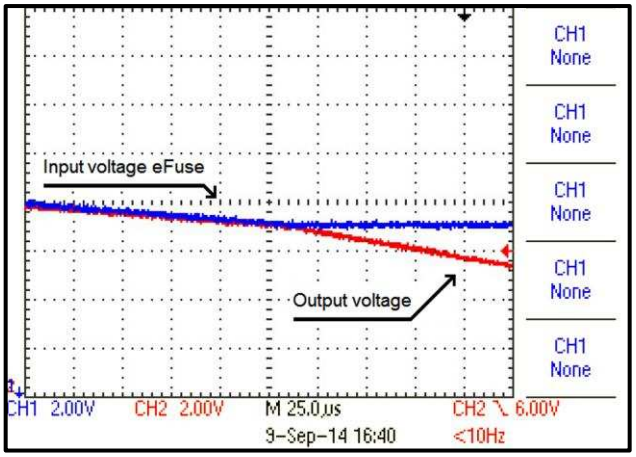

Figure 71. 7-V UV Event at 25°C, Voltage Step from 10 to 5 V at 100-mA Load

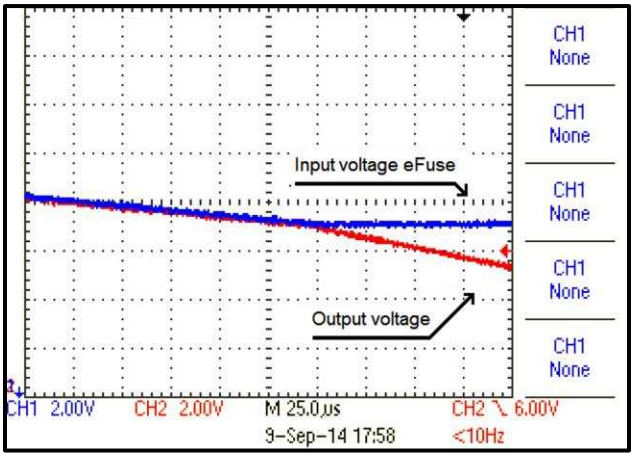

Figure 72. 7-V UV Event at 85°C, Voltage Step from 10 to 5 V at 100-mA Load

6.3.4 Fault and PG Signals during OV and OC Condition

As shown in Figure 73, when the voltage is out of specification (like an OV or UV) the PG pin is pulled high after the 3.4-ms deglitch time. The fault pin is not impacted as it is not dependent of the output voltage.

When an OC condition occurs, the output current is immediately limited and the fault timer starts. If the fault timer expires, the eFuse internal FET switch opens and the fault pin is asserted. Figure 74 shows a short circuit occurring while the system is on. As the voltage drops, the PG pin is then pulled high. Note that the short current spike is due to the discharging of the 4.7-µF (C17 and C18) at the output of the eFuse.

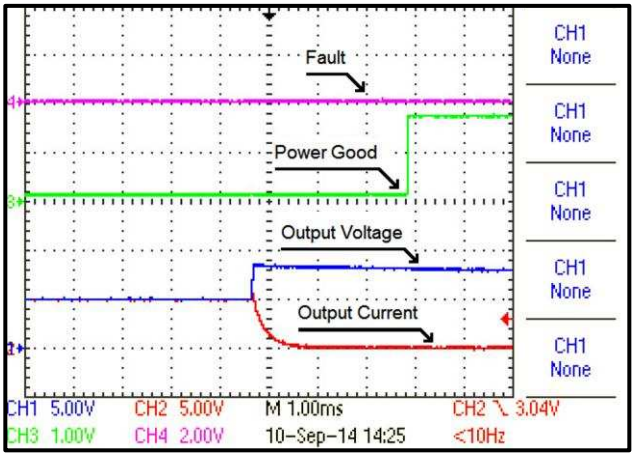

Figure 73. Fault and PG Signals during an OV Condition: 5 to 8 Vout at 100-mA Load

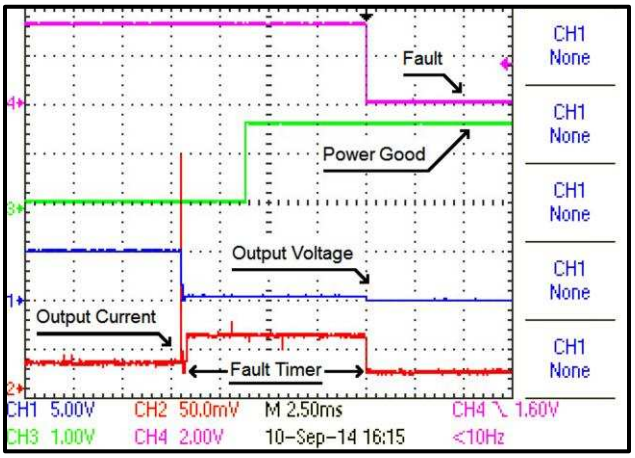

Figure 74. Fault and PG Signals during a Short Circuit Condition

6.4 System Tests

6.4.1 Start-Up

The start-up behavior was tested with a 47-µF capacitor in parallel to a resistor calculated to draw 100 mA. This capacitor and resistor are used to emulate the behavior of an encoder being supplied by the TIDA-00180.

In Figure 75 through Figure 82, the black curve is the enable signal, the green curve is the output voltage at J5 connector, and the red curve is the output current through J5.

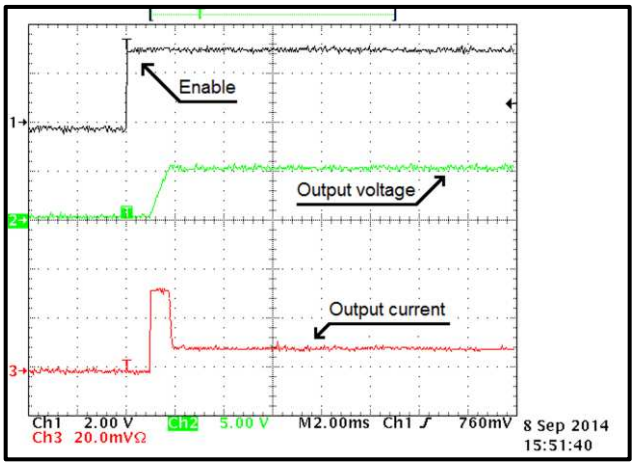

Figure 75. Start-Up at 24 Vin, 5 Vout with 51 Ω and 47-µF Load at 25°C

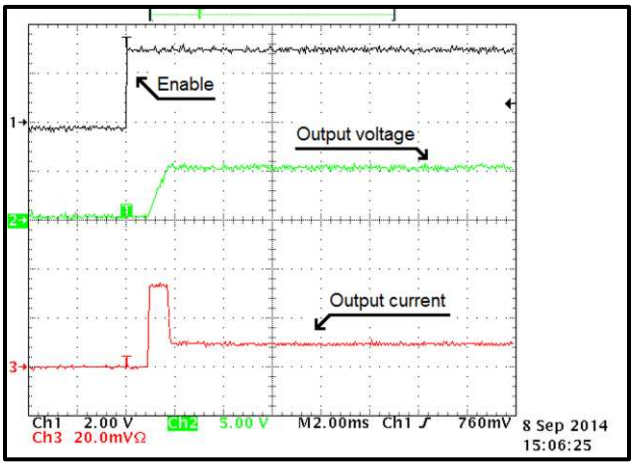

Figure 76. Start-Up at 24 Vin, 5 Vout with 51 Ω and 47-µF Load at 85°C

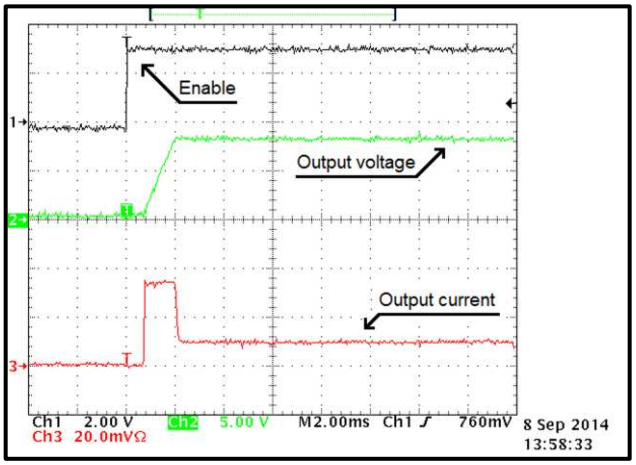

Figure 77. Start-Up at 24 Vin, 8 Vout with 82 Ω and 47-µF Load at 25°C

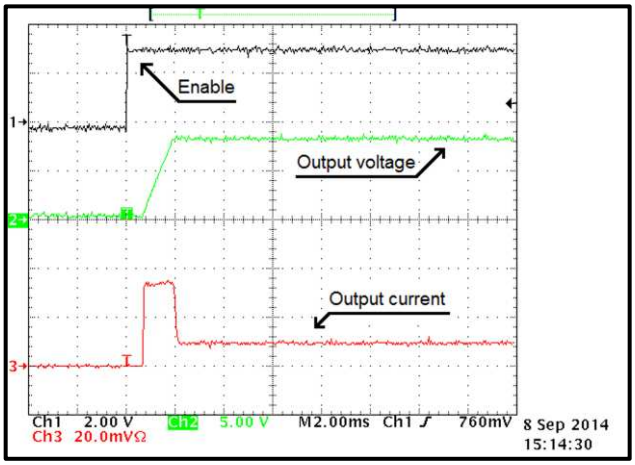

Figure 78. Start-Up at 24 Vin, 8 Vout with 82 Ω and 47-µF Load at 85°C

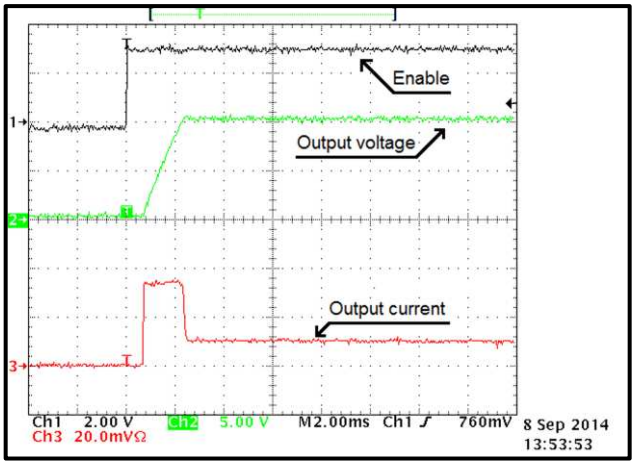

Figure 79. Start-Up at 24 Vin, 10 Vout with 100 Ω and 47-µF Load at 25°C

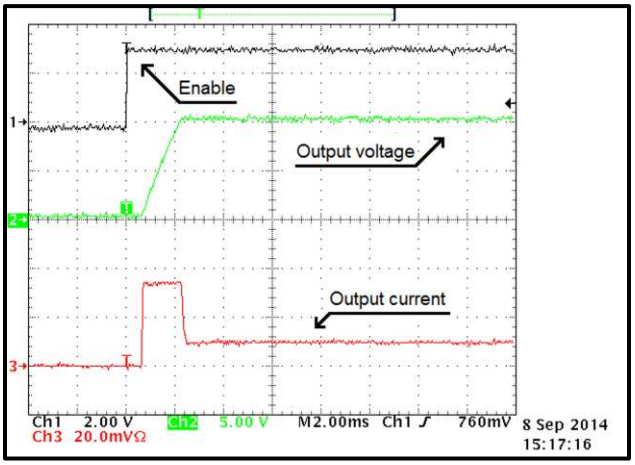

Figure 80. Start-Up at 24 Vin, 10 Vout with 100 Ω and 47-µF Load at 85°C

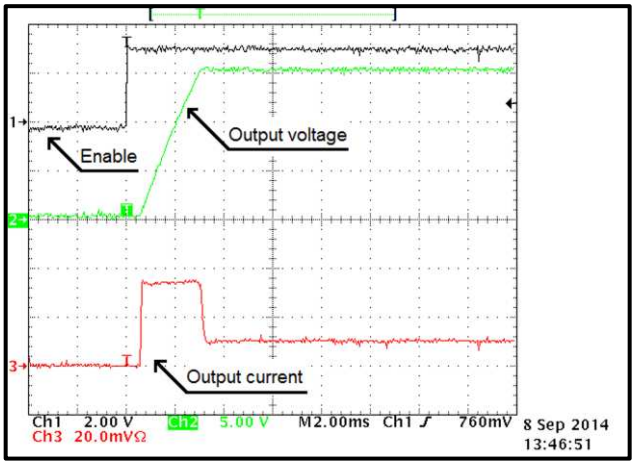

Figure 81. Start-Up at 24 Vin, 15 Vout with 150 Ω and 47-µF Load at 25°C

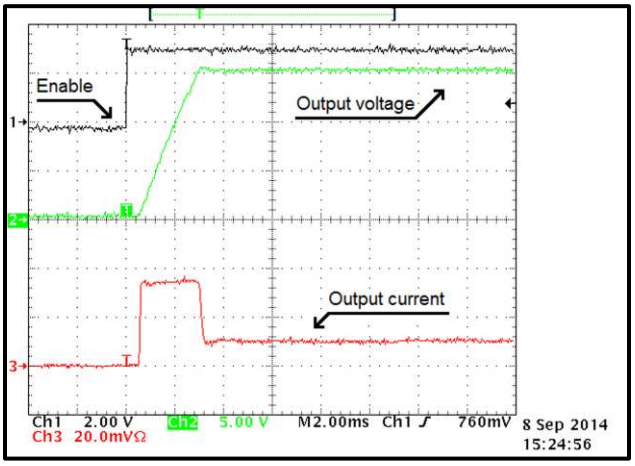

Figure 82. Start-Up at 24 Vin, 15 Vout with 150 Ω and 47-µF Load at 85°C

6.4.2 Shutdown

The shutdown behavior was tested with a 47-µF capacitor in parallel to a resistor calculated to draw 100 mA. This capacitor and resistor are used to emulate the behavior of an encoder being supplied by the TIDA-00180.

In Figure 83 through Figure 90, the black curve is the enable signal, the green curve is the output voltage at J5 connector, and the red curve is the output current through J5.

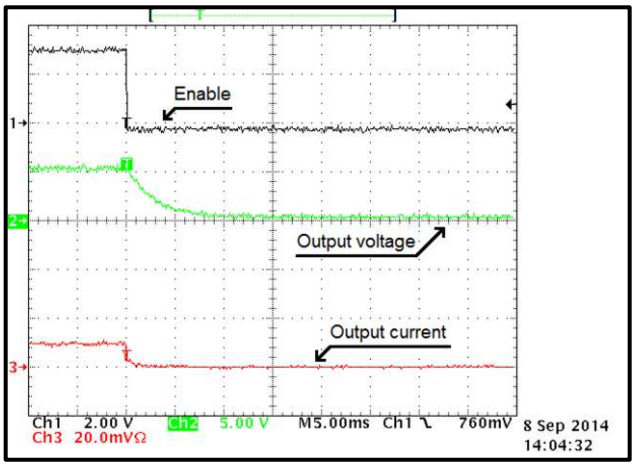

Figure 83. Shutdown at 24 Vin, 5 Vout with 51 Ω and 47-µF Load at 25°C

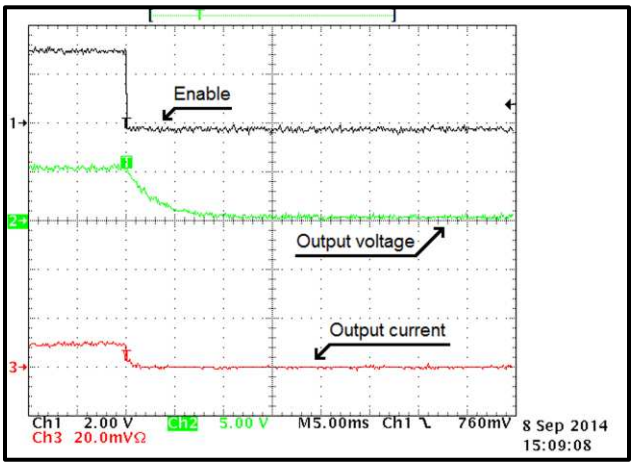

Figure 84. Shutdown at 24 Vin, 5 Vout with 51 Ω and 47-µF Load at 85°C

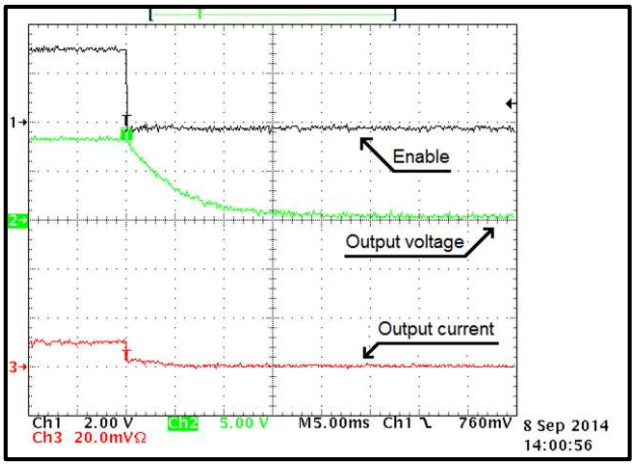

Figure 85. Shutdown at 24 Vin, 8 Vout with 82 Ω and 47-µF Load at 25°C

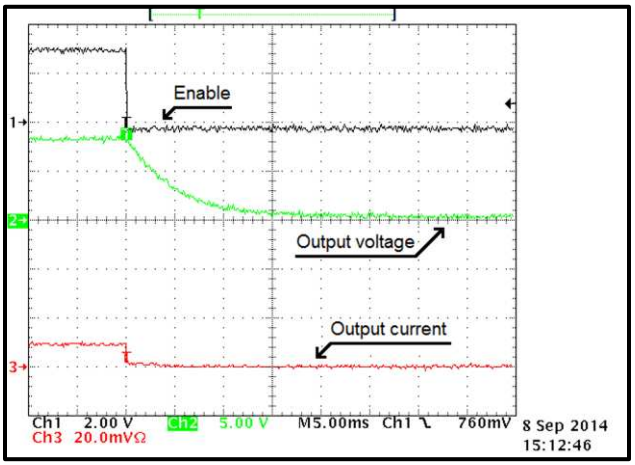

Figure 86. Shutdown at 24 Vin, 8 Vout with 82 Ω and 47-µF Load at 85°C

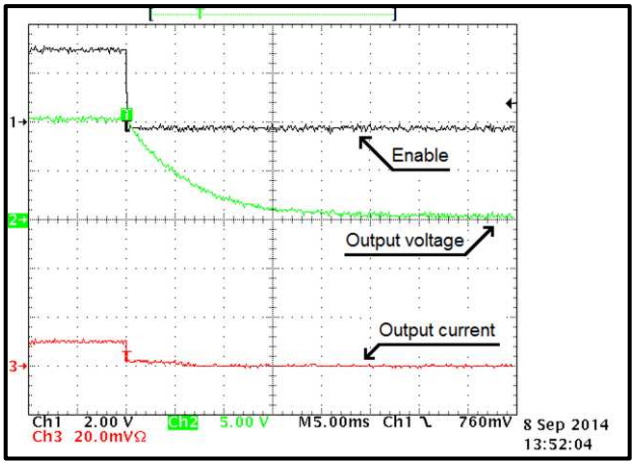

Figure 87. Shutdown at 24 Vin, 10 Vout with 100 Ω and 47-µF Load at 25°C

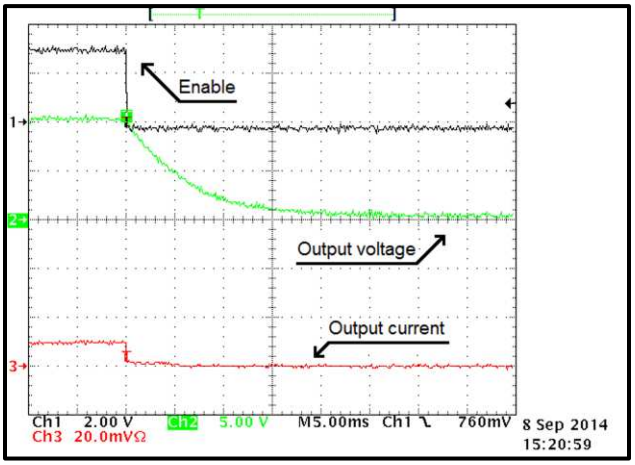

Figure 88. Shutdown at 24 Vin, 10 Vout with 100 Ω and 47-µF Load at 85°C

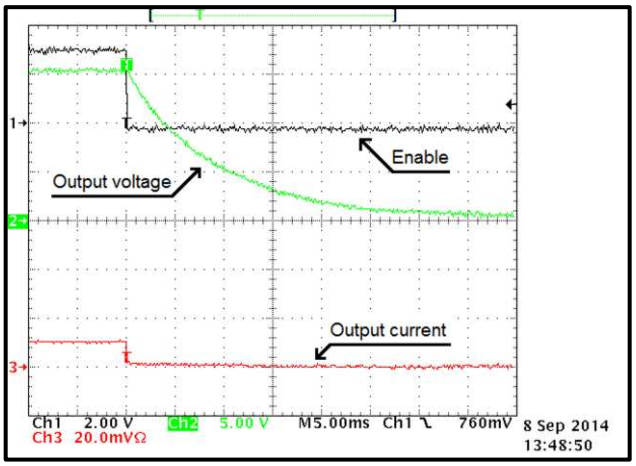

Figure 89. Shutdown at 24 Vin, 15 Vout with 150 Ω and 47-µF Load at 25°C

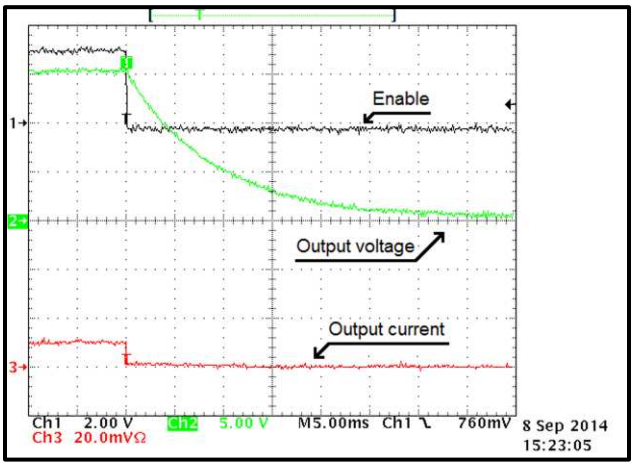

Figure 90. Shutdown at 24 Vin, 15 Vout with 150 Ω and 47-µF Load at 85°C

6.4.3 System Tests with Encoders

Figure 91 through Figure 93 show the startup of the power supply with an encoder connected. The black curve is the enable signal, the green curve is the output voltage at J5 connector, and the red curve is the output current through J5.

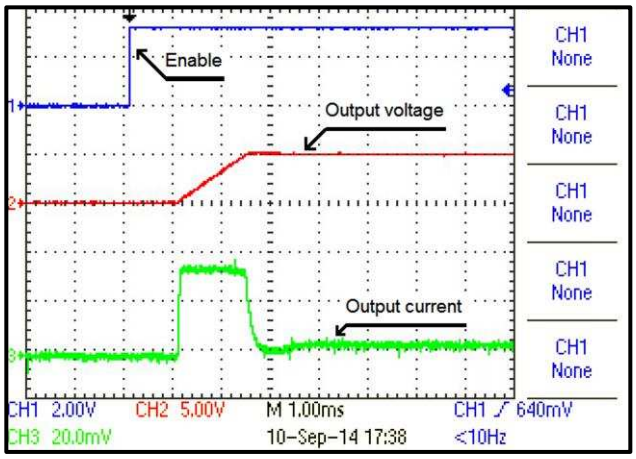

Figure 91. Output Voltage and Current Ramp-Up of TIDA-00180 Power Supply Configured to 5 V with GBPAS BiSS-C Encoder (Baumer)

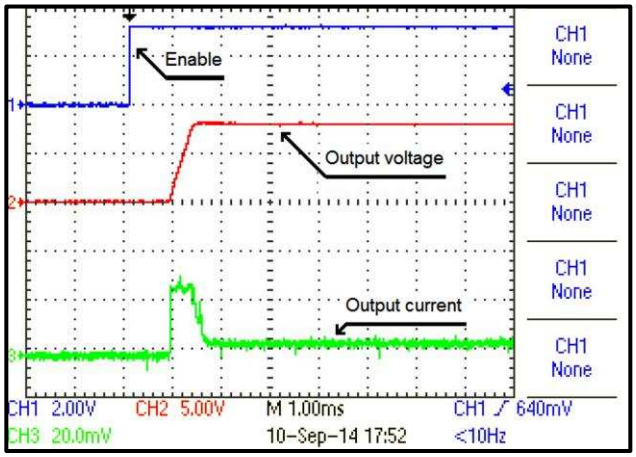

Figure 92. Output Voltage and Current Ramp-Up of TIDA-00180 Power Supply Configured to 8 V with ROQ1035 EnDat 2.2 Position Encoder (Heidenhain)

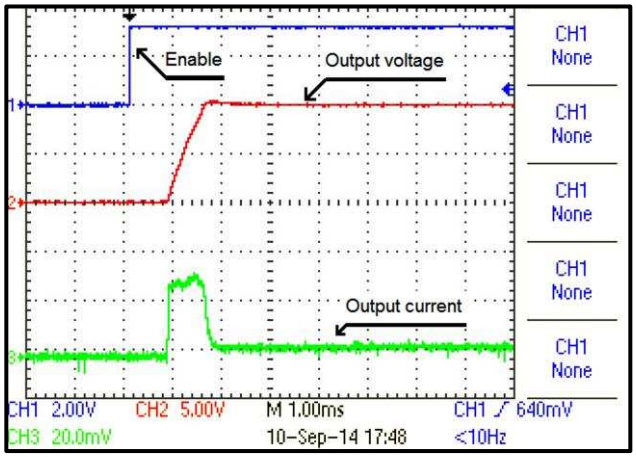

Figure 93. Output Voltage and Current Ramp-Up of TIDA-00180 Power Supply Configured to 10 V with ROC425 EnDat 2.2 Position Encoder (Heidenhain)

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00180.

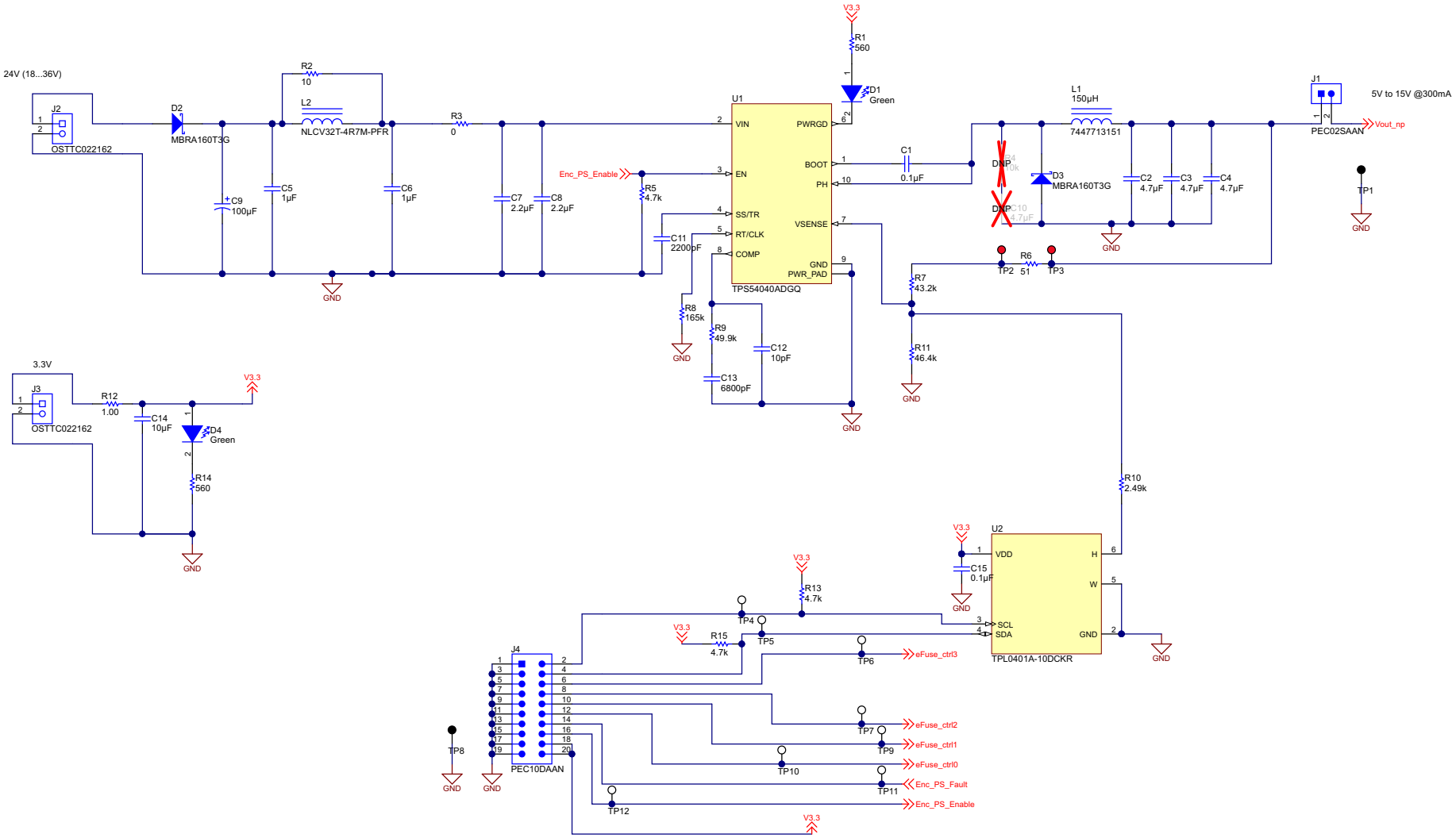

Figure 94. DC-DC Buck Converter with Programmable Output Voltage

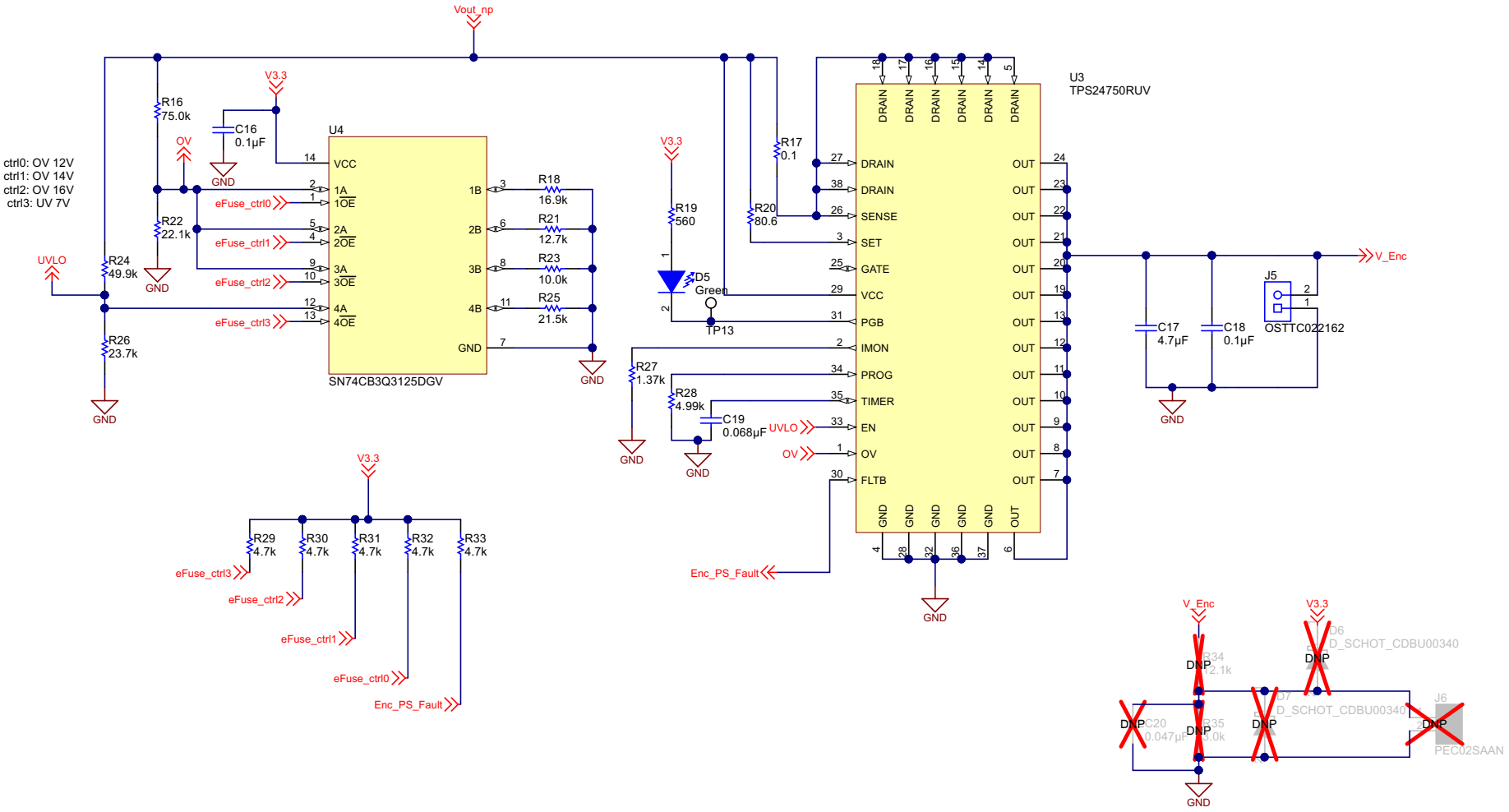

Figure 95. Output Protection with eFuse

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00180.

Table 16. BOM

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
2	C1, C18	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603	MuRata	GRM188R71H104KA93D	0603
4	C2, C3, C4, C17	CAP, CERM, 4.7 µF, 50 V, ±10%, X5R, 0805	TDK	C2012X5R1H475K125AB	0805
2	C5, C6	CAP, CERM, 1 µF, 50 V, ±10%, X7R, 0805	MuRata	GRM21BR71H105KA12L	0805
2	C7, C8	CAP, CERM, 2.2 µF, 50 V, ±10%, X5R, 1206	MuRata	GRM31CR61H225KA88L	1206
1	C9	CAP, AL, 100 µF, 63 V, ±20%, 0.35 Ω, SMD	Panasonic	EEE-FK1J101P	SMT Radial G
1	C11	CAP, CERM, 2200 pF, 16 V, ±10%, X7R, 0603	MuRata	GRM188R71C222KA01D	0603
1	C12	CAP, CERM, 10 pF, 50 V, ±5%, C0G/NP0, 0603	MuRata	GRM1885C1H100JA01D	0603
1	C13	CAP, CERM, 6800 pF, 25 V, ±10%, X7R, 0603	MuRata	GRM188R71E682KA01D	0603
1	C14	CAP, CERM, 10 µF, 25 V, ±10%, X5R, 0805	TDK	C2012X5R1E106K125AB	0805
2	C15, C16	CAP, CERM, 0.1 µF, 25 V, ±10%, X5R, 0603	AVX	06033D104KAT2A	0603
1	C19	CAP, CERM, 0.068 µF, 16 V, ±10%, X7R, 0603	MuRata	GRM188R71C683KA01D	0603
3	D1, D4, D5	LED, Green, SMD	OSRAM	LG L29K-G2J1-24-Z	1.7 × 0.65 × 0.8 mm
2	D2, D3	Diode, Schottky, 60 V, 1 A, SMA	ON Semiconductor	MBRA160T3G	SMA
4	H1, H2, H3, H4	Machine Screw Pan Phillips M3 5 mm	B&F Fastener Supply	MPMS 003 0005 PH	Screw M3 Phillips head
1	J1	Header, 100-mil, 2×1, Tin plated, TH	Sullins Connector Solutions	PEC02SAAN	Header, 2 Pin, 100-mil, Tin
3	J2, J3, J5	Terminal Block, 2-pole, 200-mil, TH	On-Shore Technology	OSTTC022162	THD, 2-Leads, Body 10.16×7.6 mm, Pitch 5.08 mm
1	J4	Header, 10×2, 2.54-mm, TH	Sullins Connector Solutions	PEC10DAAN	Header, 10×2, 2.54-mm, TH
1	L1	Inductor, Shielded Drum Core, Ferrite, 150uH, 0.7A, 0.57 ohm, SMD	Wurth Elektronik eiSos	7447713151	10 × 3× 10 mm
1	L2	Inductor, Wirewound, Ferrite, 4.7 µH, 0.9 A, 0.2 Ω, SMD	TDK	NLCV32T-4R7M-PFR	3.2 × 2.2 × 2.5 mm
3	R1, R14, R19	RES, 560 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603560RJNEA	0603
1	R2	RES, 10 Ω, 5%, 0.25 W, 0603	Vishay-Dale	CRCW060310R0JNEAHP	0603
1	R3	RES, 0 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603
8	R5, R13, R15, R29, R30, R31, R32, R33	RES, 4.7 kΩ, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06034K70JNEA	0603
1	R6	RES, 51 Ω, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060351R0JNEA	0603
1	R7	RES, 43.2 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060343K2FKEA	0603
1	R8	RES, 165 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603165KFKEA	0603
2	R9, R24	RES, 49.9 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060349K9FKEA	0603
1	R10	RES, 2.49 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06032K49FKEA	0603

Table 16. BOM (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT
1	R11	RES, 46.4 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060346K4FKEA	0603
1	R12	RES, 1.00, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031R00FKEA	0603
1	R16	RES, 75.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060375K0FKEA	0603
1	R17	RES, 0.1, 1%, 0.1 W, 0603	Panasonic	ERJ-3RSFR10V	0603
1	R18	RES, 16.9 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060316K9FKEA	0603
1	R20	RES, 80.6, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060380R6FKEA	0603
1	R21	RES, 12.7 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060312K7FKEA	0603
1	R22	RES, 22.1 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060322K1FKEA	0603
1	R23	RES, 10.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0FKEA	0603
1	R25	RES, 21.5 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060321K5FKEA	0603
1	R26	RES, 23.7 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060323K7FKEA	0603
1	R27	RES, 1.37 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K37FKEA	0603
1	R28	RES, 4.99 kΩ, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06034K99FKEA	0603
2	TP1, TP8	Test Point, Miniature, Black, TH	Keystone	5001	Black Miniature Testpoint
2	TP2, TP3	Test Point, Miniature, Red, TH	Keystone	5000	Red Miniature Testpoint
9	TP4, TP5, TP6, TP7, TP9, TP10, TP11, TP12, TP13	Test Point, Miniature, White, TH	Keystone	5002	White Miniature Testpoint
1	U1	0.5-A, 42-V Step Down DC/DC Converter with Eco-mode, DGQ0010D	Texas Instruments	TPS54040ADGQ	DGQ0010D
1	U2	128 TAPS Single Channel Digital Potentiometer with I2C Interface, DCK0006A	Texas Instruments	TPL0401A-10DCKR	DCK0006A
1	U3	2.5- to 18-V Positive Voltage 10-A Integrated Hot-Swap Controller, RUV0036A	Texas Instruments	TPS24750RUV	RUV0036A
1	U4	Quadruple FET Bus Switch, 2.5-V/3.3-V Low-Voltage High-Bandwidth Bus Switch, DGV0014A	Texas Instruments	SN74CB3Q3125DGV	DGV0014A
0	C10	CAP, CERM, 4.7 µF, 50 V, ±10%, X5R, 0805	TDK	C2012X5R1H475K125AB	0805
0	C20	CAP, CERM, 0.047 µF, 6.3 V, ±10%, X7R, 0603	MuRata	GRM188R70J473KA01D	0603
0	D6, D7	Diode, Schottky, 30 mA, 40 V	Comchip	CDBU00340	0603
0	J6	Header, 100-mil, 2×1, Tin plated, TH	Sullins Connector Solutions	PEC02SAAN	Header, 2 Pin, 100-mil, Tin
0	R4	RES, 10 kΩ, 5%, 0.125 W, 0805	Vishay-Dale	CRCW080510K0JNEA	0805
0	R34	RES, 12.1 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060312K1FKEA	0603
0	R35	RES, 3.0 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06033K00JNEA	0603

7.3 Layer Plots

To download the layer plots, see the design files at TIDA-00180.

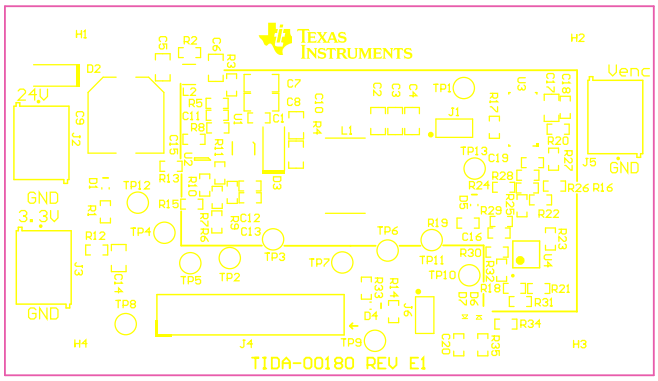

Figure 96. Top Overlay

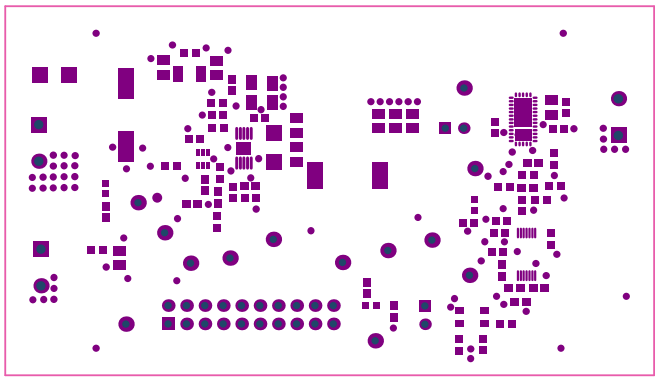

Figure 97. Top Solder Mask

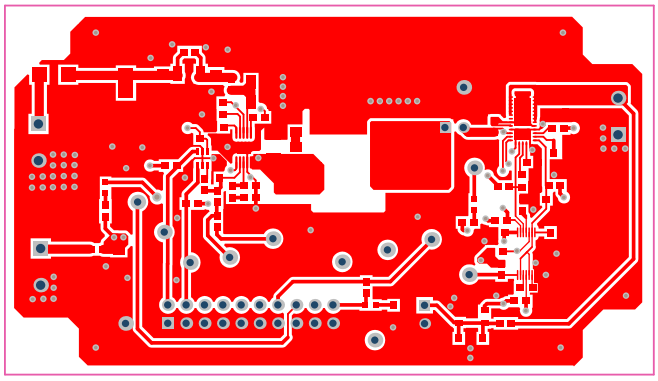

Figure 98. Top Layer

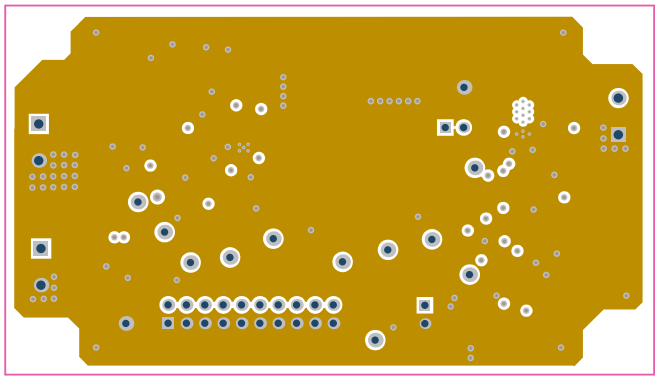

Figure 99. Mid Layer 1: GND

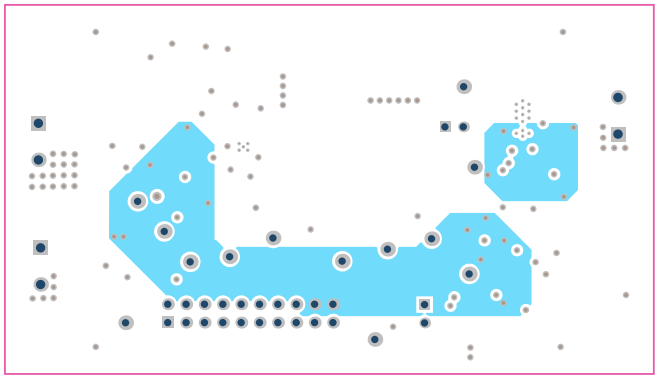

Figure 100. Mid Layer 2: Supply Plane

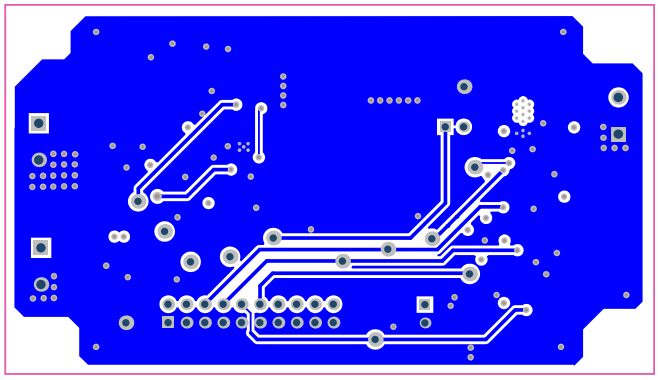

Figure 101. Bottom Layer

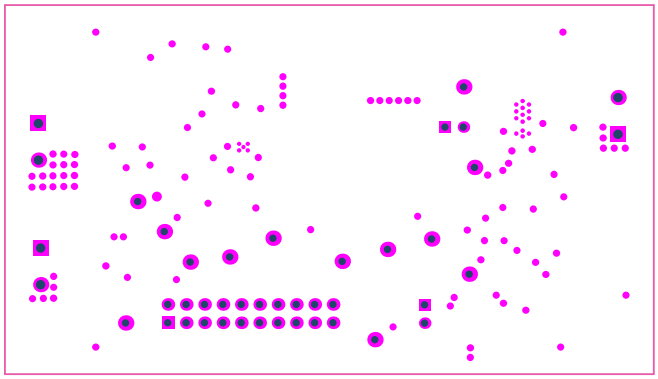

Figure 102. Bottom Solder Mask

Figure 103. Bottom Overlay

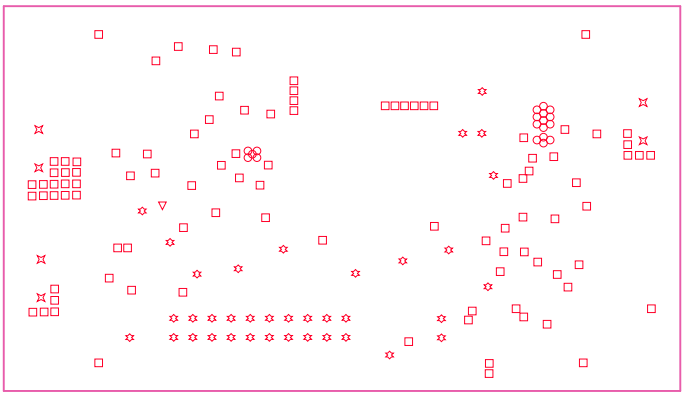

Figure 104. Drill Drawing

7.4 Layout Guidelines

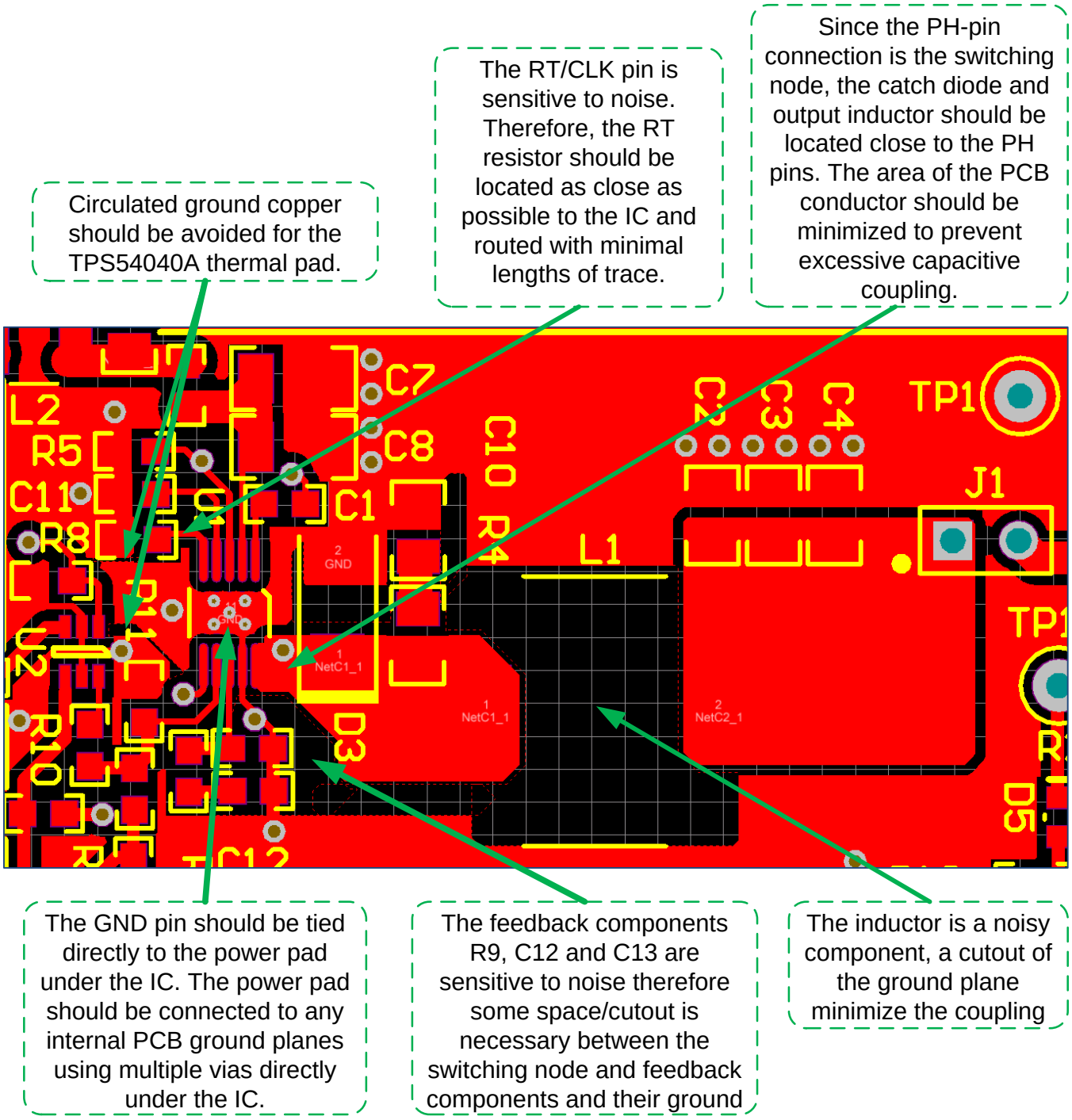

Figure 105. Layout Guidelines for TPS54040A

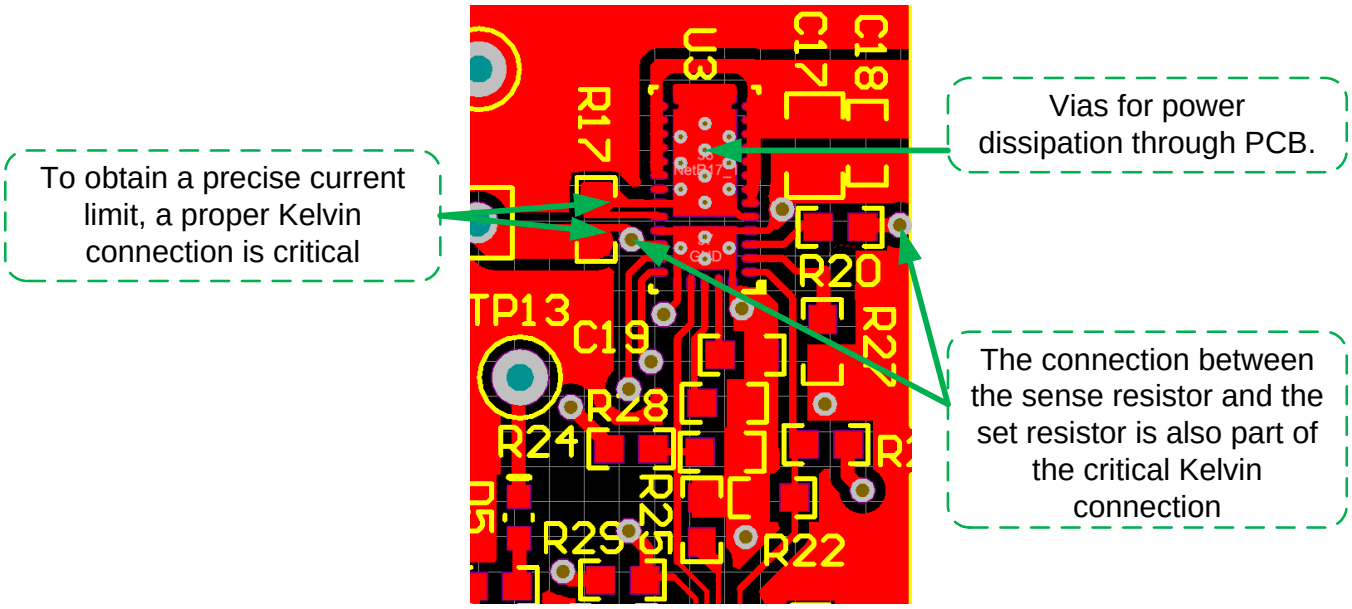

Figure 106. Layout Guideline for TPS24750 eFuse

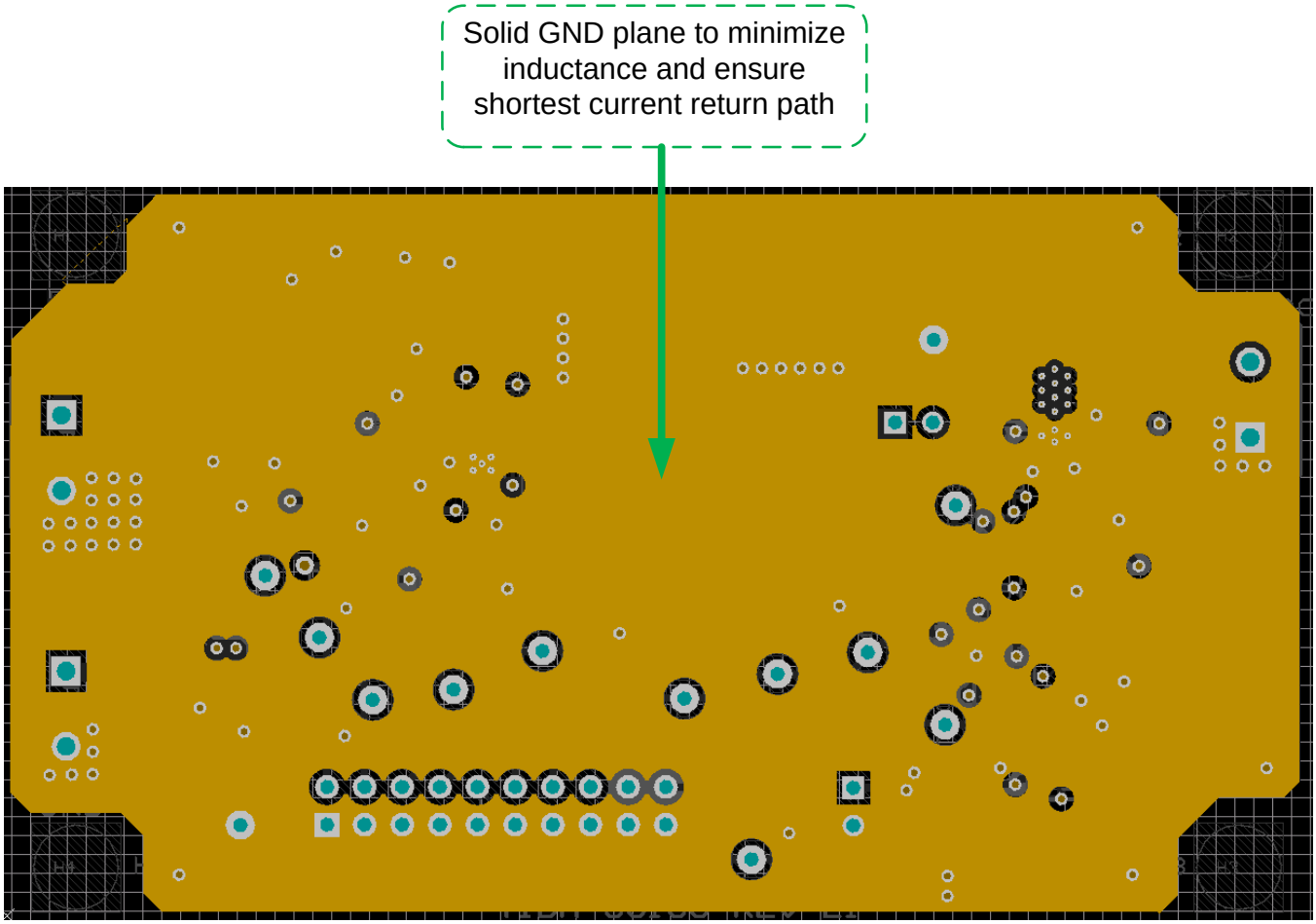

Figure 107. GND Layer

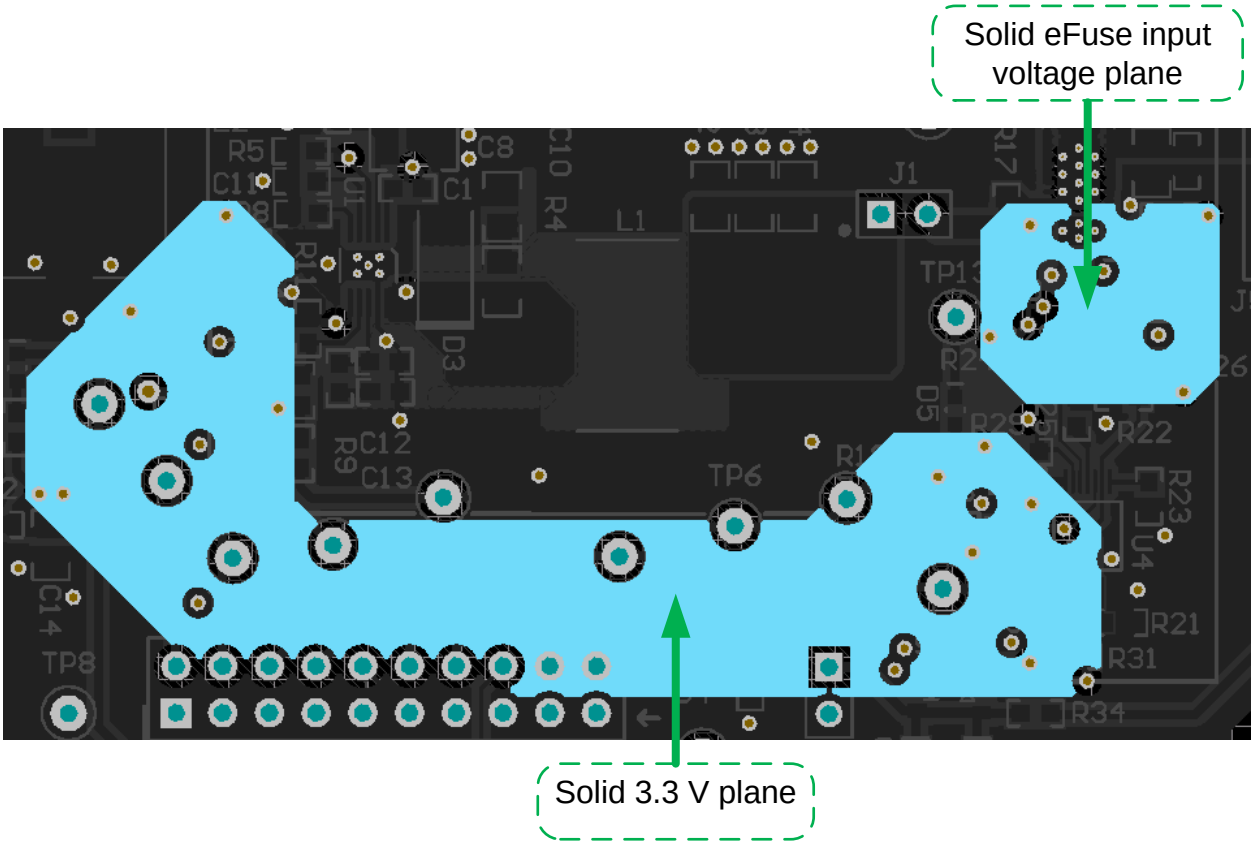

Figure 108. Supply Voltage Layer

7.5 Altium Project

To download the Altium project files, see the design files at TIDA-00180.

7.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00180.

7.7 Assembly Drawings

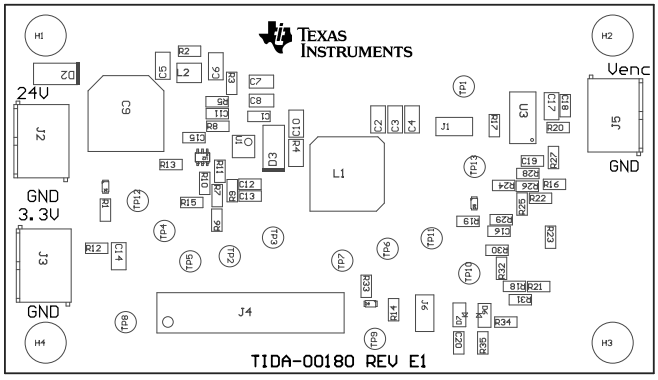

Figure 109. Top Assembly Drawing

Figure 110. Bottom Assembly Drawing

8 References

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2. Texas Instruments, C2000 Piccolo LaunchPad (Product Page)
3. IEC 61800-3 ed2.0 (2004–08), Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods
4. IEC 61800-3-am1 ed2.0 (2011–11), Amendment 1 - Adjustable speed electrical power drive systems - Part 3: EMC requirements and specific test methods
5. Reference Design for an Interface to a Position Encoder with EnDat 2.2 (TIDA-00172 Design Folder)
6. Interface to a 5V BiSS Position Encoder Reference Design (TIDA-00175 Design Folder)

9 About the Author

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