CA3193, CA3193A

1.2MHz, BiCMOS Precision Operational Amplifiers

January 1998

Features

- Low V_{IO}
  - CA3193A . . . . . 200μV (Max)
  - CA3193 . . . . . 500μV (Max)
- Low $\Delta V_{IO}/\Delta T$
  - CA3193A . . . . . 3μV/°C (Max)
  - CA3193 . . . . . 5μV/°C (Max)
- Low I_{IO} and I_I
- Low $\Delta I_{IO}/\Delta T$: CA3193 . . . . . 150pA/°C (Max)
- Low $\Delta I_I/\Delta T$: CA3193 . . . . . 3.7nA/°C (Max)

Applications

- Thermocouple Preamplifiers
- Strain Gauge Bridge Amplifiers
- Summing Amplifiers
- Differential Amplifiers
- Bilateral Current Sources
- Log Amplifiers
- Differential Voltmeters
- Precision Voltage References
- Active Filters
- Buffers
- Integrators
- Sample-and-Hold Circuits
- Low Frequency Filters

Description

The CA3193A and CA3193 are ultra-stable, precision instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3193A and CA3193 amplifiers are internally phase compensated and provide a gain bandwidth product of 1.2MHz. They are pin compatible with the industry 741 series and many other IC op amps, and may be used as replacements for 741 series types in most applications.

The CA3193A and CA3193 can also be used as functional replacements for op amp types 725, 108A, OP-5, OP-7, LM11 and LM714 in many applications where nulling is not employed. Because of their low offset voltage and low offset voltage vs temperature coefficient the CA3193A and CA3193 amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high gain filters, buffer, strain gauge bridge amplifiers and precision voltage references.

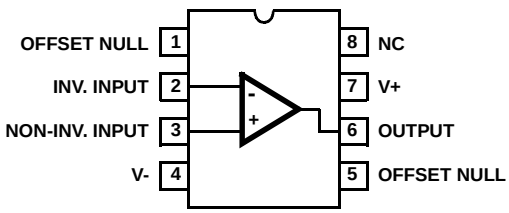
The two types in the CA3193 series are functionally identical. The CA3193A and CA3193 operate from supply voltages of ±3.5V to ±18V.

Part Number Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3193AE	-25 to 85	8 Ld PDIP	E8.3
CA3193E	0 to 70	8 Ld PDIP	E8.3

Pinout

CA3193
(PDIP)
TOP VIEW



Absolute Maximum Ratings

DC Supply Voltage . . . . . ±18V
Differential Input Voltage 5V
DC Input Voltage . . . . . (V+ -4), V-
Input Current. 1mA
Output Short Circuit Duration (Note 2) . . . . . Indefinite

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	100	N/A

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions

Temperature Range
CA3193A. . . . . -25^oC to 85^oC
CA3193. . . . . 0^oC to 70^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Short circuit may be applied to ground or to either supply.

Electrical Specifications

$T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	SYMBOL	CA3193			CA3193A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage $\lvert V_{IO} \rvert$	25^oC	V_{IO}	-	300	500	-	140	200	µV
	T_{MAX}		-	-	725	-	-	380	µV
Input Offset Voltage Temperature Coefficient (Over Specified Temperature Range for Each Device)		$\Delta V_{IO}/\Delta T$	-	1	5	-	1	3	$\mu V/^oC$
Input Offset Current	25^oC	I_{IO}	-	5	10	-	3	5	nA
	T_{MAX}		-	-	17	-	-	11	nA
Input Offset Current Temperature Coefficient (Over Specified Temperature Range for Each Device)		$\Delta I_{IO}/\Delta T$	-	0.04	0.15	-	0.03	0.10	$nA/^oC$
Input Bias Current	25^oC	I_I	-	20	40	-	10	20	nA
	T_{MAX}		-	-	207	-	-	83	nA
Input Bias Current Temperature Coefficient		$\Delta I_I/\Delta T$	-	0.15	3.70	-	0.10	1.18	$nA/^oC$
Input Noise Voltage	0.1 to 10Hz	$e_{N\ P-P}$	-	0.36	-	-	0.36	-	μV_{P-P}
Input Noise Voltage Density	f = 10Hz	e_N	-	25	-	-	25	-	$nV/\sqrt{Hz}$
	f = 100Hz		-	25	-	-	25	-	$nV/\sqrt{Hz}$
	f = 1000Hz		-	24	-	-	24	-	$nV/\sqrt{Hz}$
	f = 10kHz		-	24	-	-	24	-	$nV/\sqrt{Hz}$
	f = 100kHz		-	22	-	-	22	-	$nV/\sqrt{Hz}$
Input Noise Current	0.1 to 10 Hz	$I_{N\ P-P}$	-	12	20	-	12	20	pA_{P-P}
Input Noise Current Density	f = 10Hz	I_N	-	0.83	-	-	0.83	-	$pA/\sqrt{Hz}$
	f = 100Hz		-	0.80	-	-	0.80	-	$pA/\sqrt{Hz}$
	f = 1000Hz		-	0.75	-	-	0.75	-	$pA/\sqrt{Hz}$
	f = 10kHz		-	0.72	-	-	0.72	-	$pA/\sqrt{Hz}$
	f = 100kHz		-	0.60	-	-	0.60	-	$pA/\sqrt{Hz}$
Common-Mode Input Voltage Range		V_{ICR}	-12	-13.5 to 11.5	10	-12	-13.5 to 11.5	10	V
Common-Mode Rejection Ratio	$V_{CM} = V_{ICR}$	CMRR	100	110	-	110	115	-	dB
			-	3.16	10	-	1.78	3.16	µV/V
Power Supply Rejection Ratio $\Delta V_{IO}/\Delta V\pm$		PSRR	100	130	-	100	130	-	dB
			-	0.316	10	-	0.316	10	µV/V
Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	V_{OM}	±13.0	±13.5	-	±13.0	±13.5	-	V
Large-Signal Voltage Gain ($V_O = \pm10$)	$R_L \geq 2k\Omega$	A_{OL}	100	110	-	110	115	-	dB
	$R_L \geq 10k\Omega$		-	115	-	-	125	-	dB

Electrical Specifications $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	SYMBOL	CA3193			CA3193A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Short-Circuit Output Current to the Opposite Rail		$I_{OM}+$, $I_{OM}-$	-25	±7	25	-25	±7	25	mA
Slew Rate	$R_L \geq 2k\Omega$, $A_V = +1$	SR	-	0.25	-	-	0.25	-	V/µs
Gain-Bandwidth Product	$A_{OL} = 0dB$, $R_L = 2k\Omega$, $C_L = 100pF$, $V_{IN} = 20mV_{P-P}$, f = 1kHz	f_T	-	1.20	-	-	1.20	-	MHz
Rise and Fall Time	$V_{IN} = 20mV_{P-P}$, f = 1kHz	t_R	-	0.29	-	-	0.29	-	µs
Supply Current	$R_L = \infty$, $V_S = \pm15V$	I+	-	2.3	3.5	-	2.3	3.5	mA

Test Circuits and Waveforms

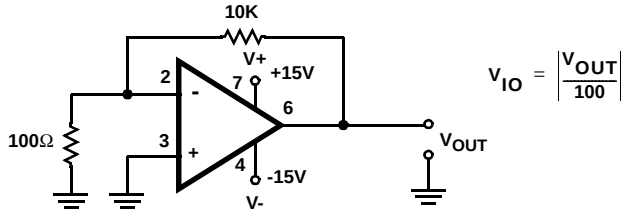


FIGURE 1. INPUT OFFSET VOLTAGE TEST CIRCUIT

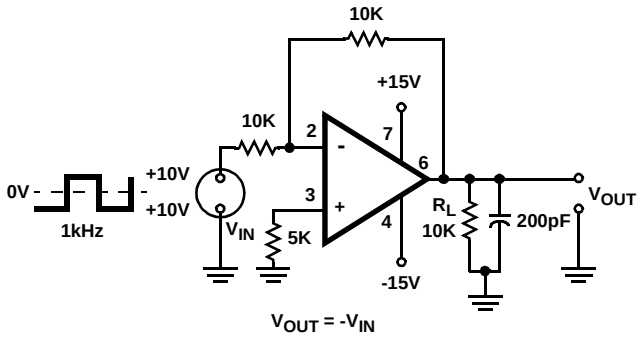
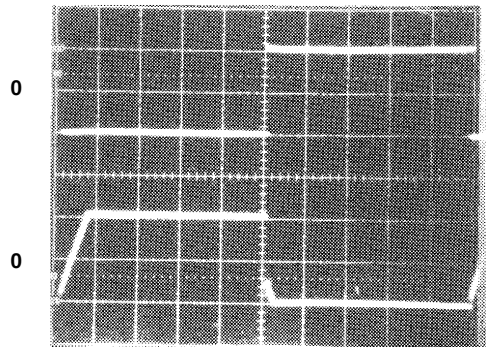


FIGURE 2A. TEST CIRCUIT



Top Trace: Input Voltage, Bottom Trace: Output Voltage
Vertical Scale: 10V/Div., Horizontal Scale: 0.1ms/Div.

FIGURE 2B. RESPONSE TO 1kHz, $20V_{P-P}$ SQUARE WAVE

FIGURE 2. INVERTING AMPLIFIER

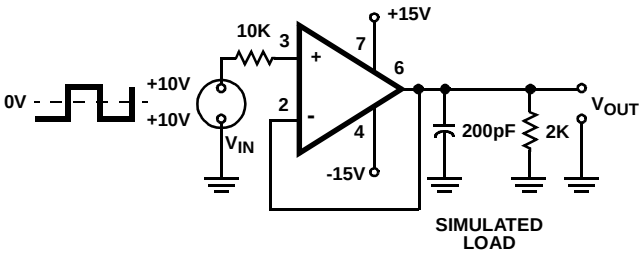
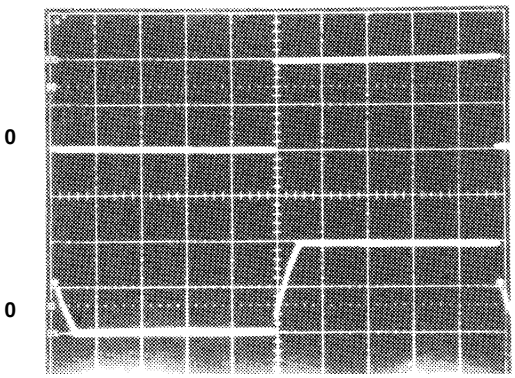


FIGURE 3A. TEST CIRCUIT



Top Trace: Input Voltage; Bottom Trace: Output Voltage
Vertical Scale: 10V/Div.; Horizontal Scale: 0.1ms/Div.

FIGURE 3B. RESPONSE TO $20V_{P-P}$, 1kHz SQUARE WAVE INPUT

Test Circuits and Waveforms (Continued)

FIGURE 3. VOLTAGE FOLLOWER

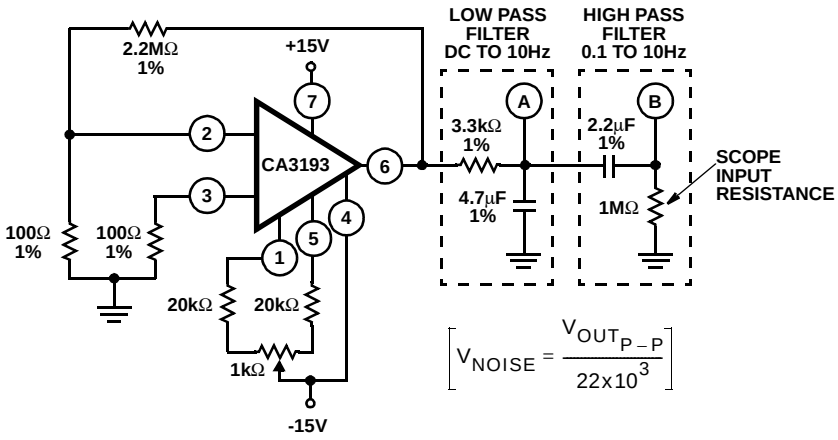


FIGURE 4A. TEST CIRCUIT - 0.1Hz TO 10Hz

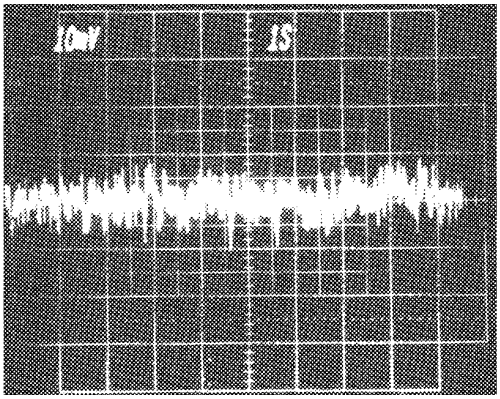


FIGURE 4B. OUTPUT (A) WAVEFORM - 0Hz TO 10Hz NOISE

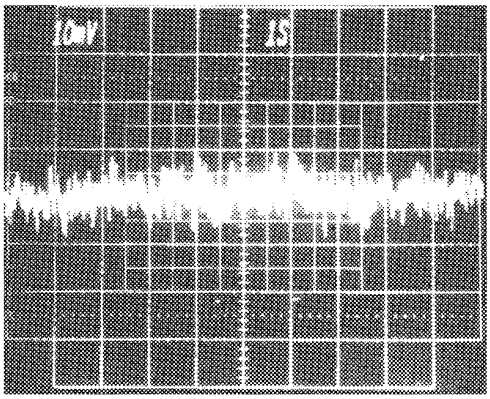
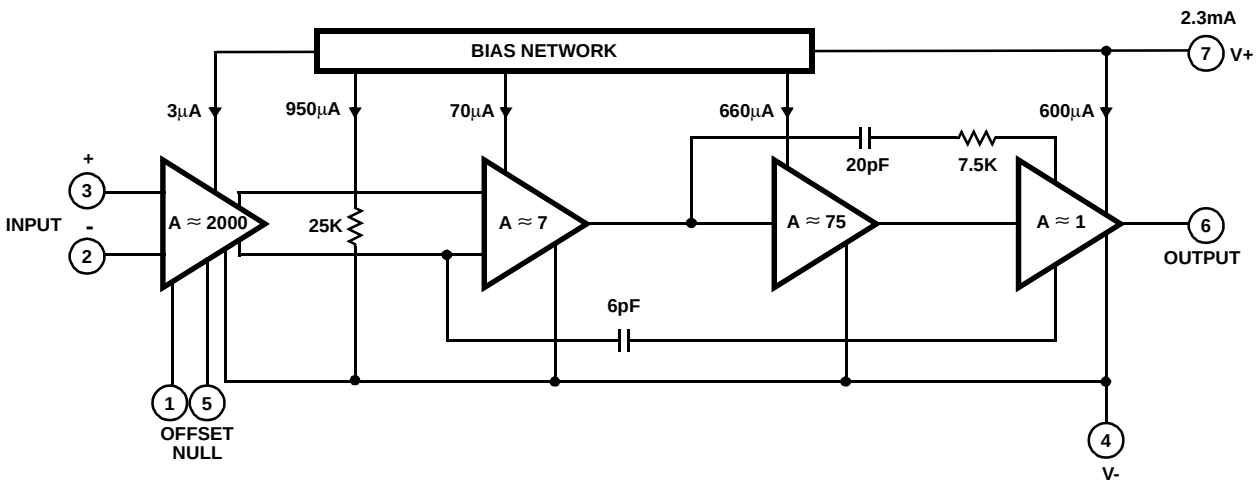


FIGURE 4C. OUTPUT (B) WAVEFORM - 0.1Hz TO 10Hz NOISE

FIGURE 4. LOW FREQUENCY NOISE

Functional Block Diagram



Schematic Diagrams

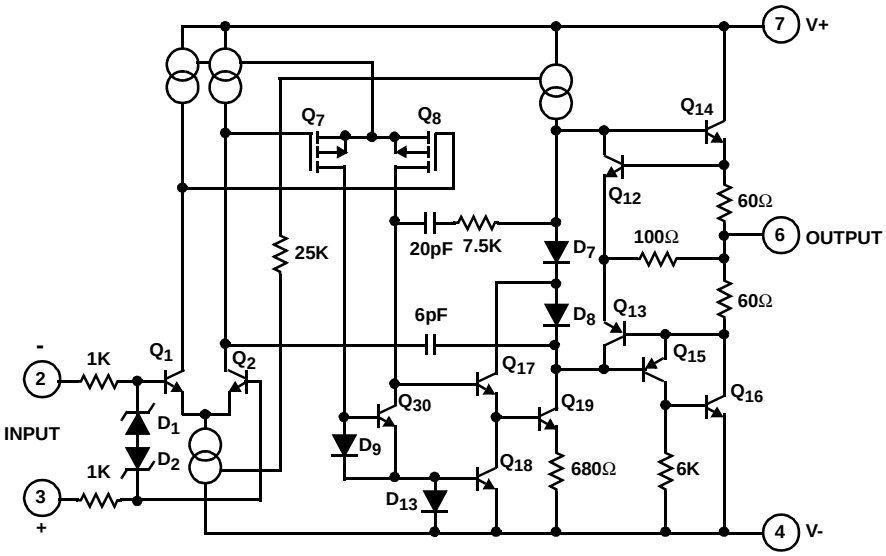


FIGURE 5. CA3193 SIMPLIFIED SCHEMATIC DIAGRAM

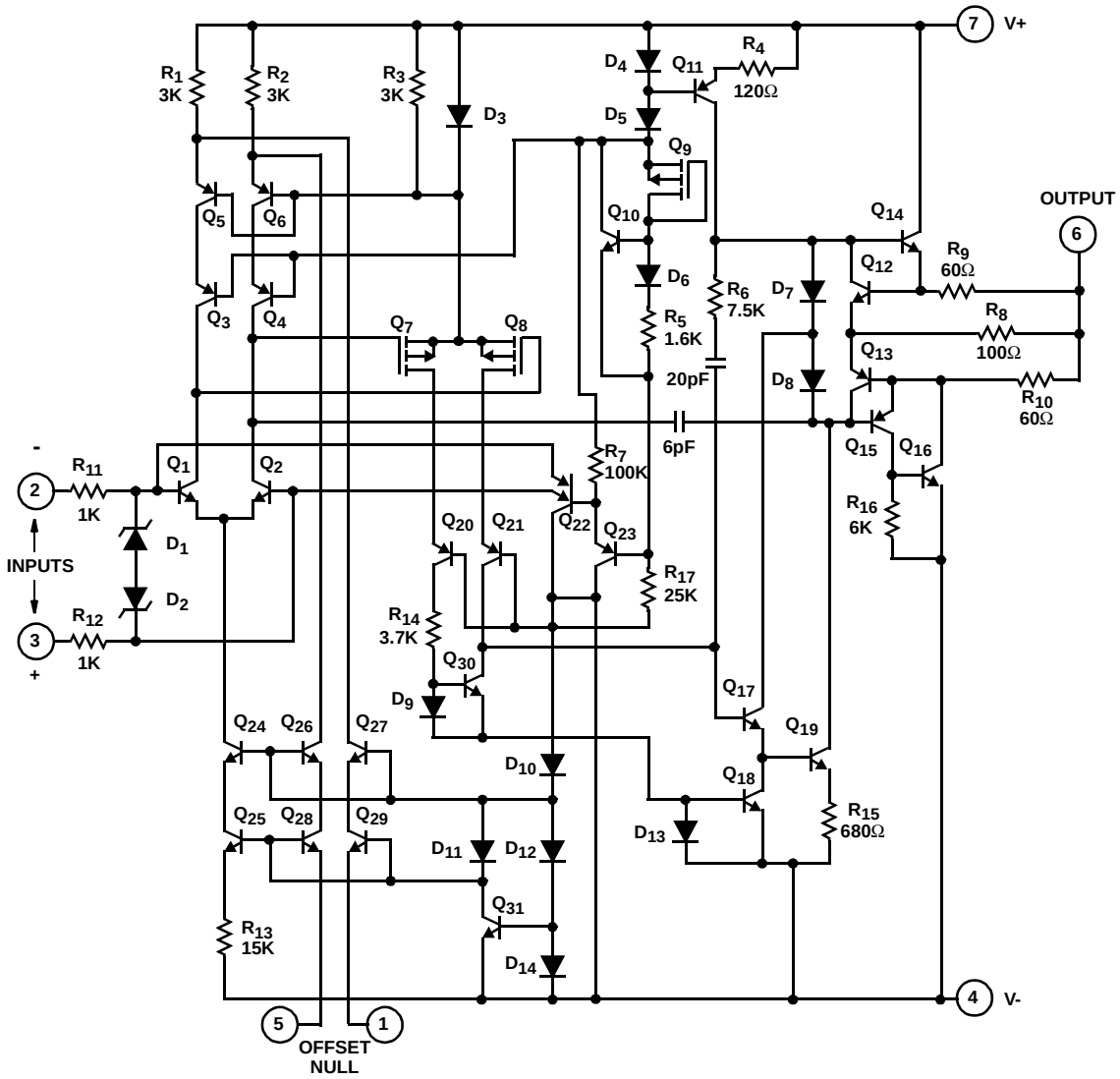


FIGURE 6. SCHEMATIC DIAGRAM OF CA3193A AND CA3193

Application Information

Circuit Description

The block diagram of the CA3193 amplifier shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3193 amplifier are shown in Figures 5 and 6, respectively.

A quad of physically cross-connected NPN transistors comprise the input-stage differential pair (Q_1, Q_2 in Figures 5 and 6); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q_1, Q_2) are provided by the cascode-connected PNP transistors Q_3, Q_5 and Q_4, Q_6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q_7, Q_8 in Figures 5 and 6) with appropriate drain loading. Since Q_7 and Q_8 are M0S/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D_9, Q_{30} (Figures 5 and 6) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected NPN transistors (Q_{17}, Q_{19} in Figures 5 and 6), driving the quasi-complementary Class AB output stage (Q_{14} and Q_{15}, Q_{16} in Figures 5 and 6). Output-stage short-circuit protection is activated by voltage drops developed across the 60Ω resistors adjacent to the output terminal (R_9 and R_{10}, Figure 6). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{BE}, the respective protective transistor (Q_{12} or Q_{13}) is activated and shunts the base drive from the bases of the output stage transistors (Q_{14} and Q_{15}, Q_{16}).

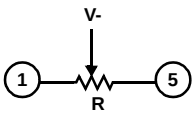
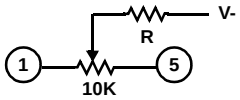
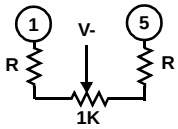
Internal frequency compensation for the CA3193 amplifier is provided by two internal networks, a 6pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20pF capacitor in series with a 7.5kΩ resistor connected between the input and output nodes of the third stage.

Offset Voltage Nulling

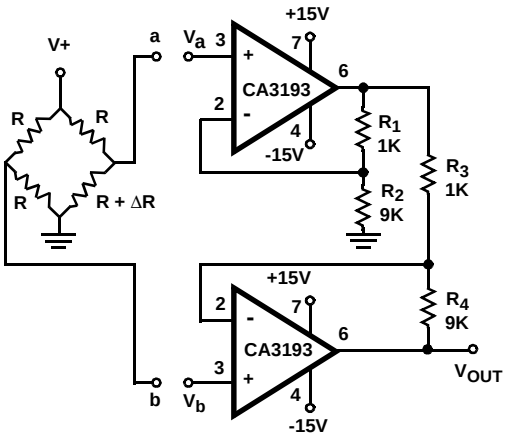
The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 5, with its wiper returned to V-, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3193 amplifiers will be damaged if they are plugged into op amp circuits employing nulling with respect to the V+ supply bus.

Offset Voltage Nulling

OFFSET NULLING CIRCUITS			
TYPE	**RESISTOR R VALUE**	**RESISTOR R VALUE**	**RESISTOR R VALUE**
CA3193A	10K	50K	10K
CA3193	10K	20K	5K
	Gross Offset Adjustment	Finer Offset Adjustments	

Typical Applications



$$V_{OUT} = -V_a\left(\frac{R_2}{R_1}+1\right)\frac{R_4}{R_3} + V_b\left(\frac{R_4}{R_3}+1\right)$$

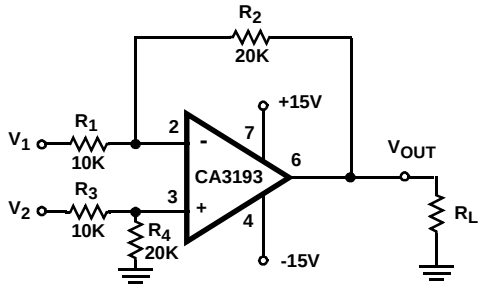
For Ideal Resistors with $\frac{R_1}{R_2} = \frac{R_3}{R_4}$

$$V_{OUT} = V_b - V_a\left(\frac{R_4}{R_3}+1\right)$$

$$A = \frac{V_{OUT}}{V_b - V_a} = \left(\frac{R_4}{R_3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (V_b - V_a)(I_O)$

FIGURE 7. TYPICAL TWO OP AMP BRIDGE-TYPE DIFFERENTIAL AMPLIFIER



ALL RESISTANCE VALUES ARE IN OHMS.

$$V_{OUT} = V_2\left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_1}\right) - V_1\left(\frac{R_2}{R_1}\right)$$

If $R_4 = R_2$, $R_3 = R_1$ and $\frac{R_2}{R_1} = \frac{R_4}{R_3}$

THEN $V_{OUT} = (V_2 - V_1)\left(\frac{R_2}{R_1}\right)$

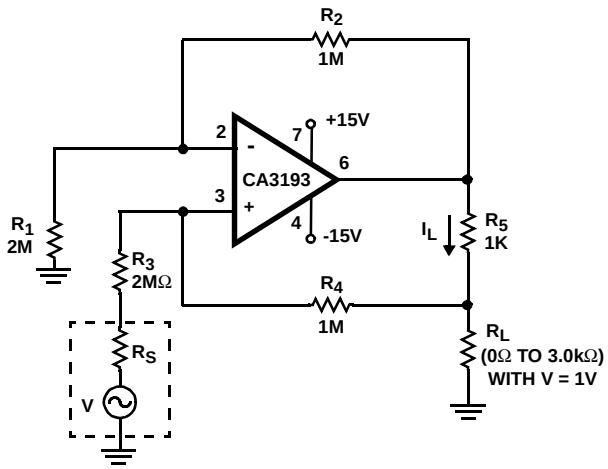
For values above $V_{OUT} = 2(V_2 - V_1)$:

If A_V is To be made 1 and if $R_1 = R_3 = R_4 = R$ with $R_2 = 0.999R$ (0.1% mismatch in R_2)

Then $V_{OCM} = 0.0005\ V_{IN}$ or CMRR = 66dB

Thus, the CMRR of this circuit is limited by the matching or mismatching of this network rather than the amplifier.

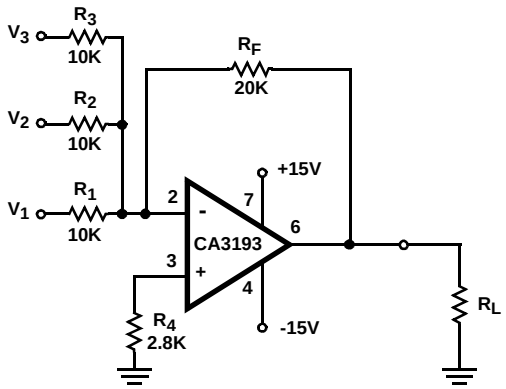
FIGURE 8. DIFFERENTIAL AMPLIFIER (SIMPLE SUBTRACTER) USING CA3193



ALL RESISTORS ARE 1%
IF $R_1 = R_3$ AND $R_2 \approx R_4 + R_5$, THEN
I_L IS INDEPENDENT OF VARIATIONS IN R_L
FOR R_L VALUES OF 0Ω TO 3kΩ WITH V = 1V

$$I_L = \frac{VR_4}{R_3R_5} = \frac{V(1M)}{(2M)(1K)} = \frac{V}{2K} = 500\mu A$$

FIGURE 9. USING CA3193 AS A BILATERAL CURRENT SOURCE



$$V_{OUT} = -\left(\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2 + \frac{R_F}{R_3}V_3\right)$$

$V_{OUT} = -(2V_1 + 2V_2 + 2V_3)$

ALL RESISTANCE VALUES ARE IN OHMS.

FIGURE 10. TYPICAL SUMMING AMPLIFIER APPLICATION

Typical Applications (Continued)

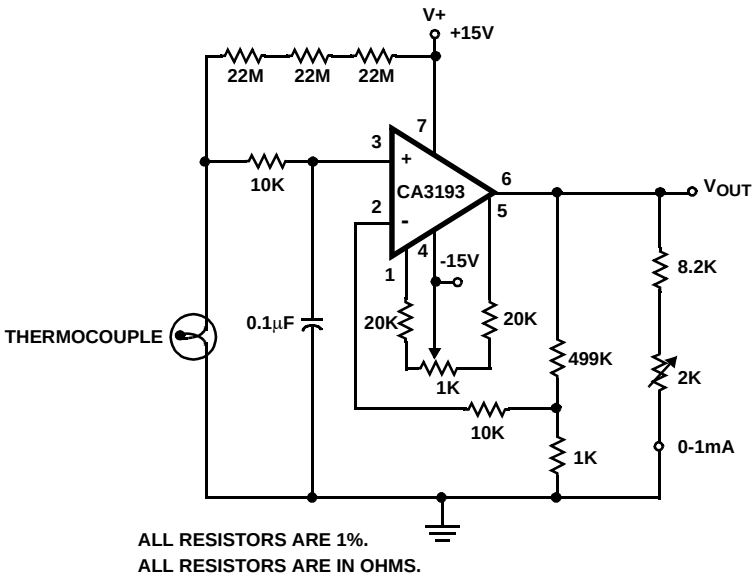


FIGURE 11. THE CA3193 USED IN A THERMOCOUPLE CIRCUIT

The CA3193 is an excellent choice for use with thermocouples. In Figure 11, the CA3193 amplifies the generated signal 500 times. The three 22MΩ resistors will provide full-scale output if the thermocouple opens.

Typical Performance Curves

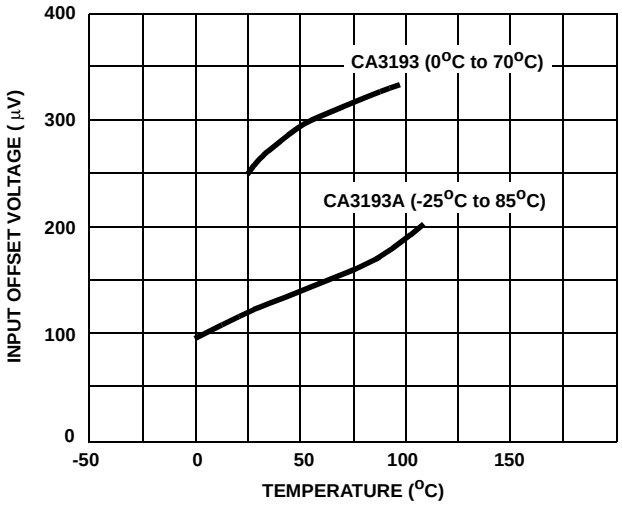


FIGURE 12. TYPICAL INPUT OFFSET VOLTAGE TEMPERATURE CHARACTERISTIC

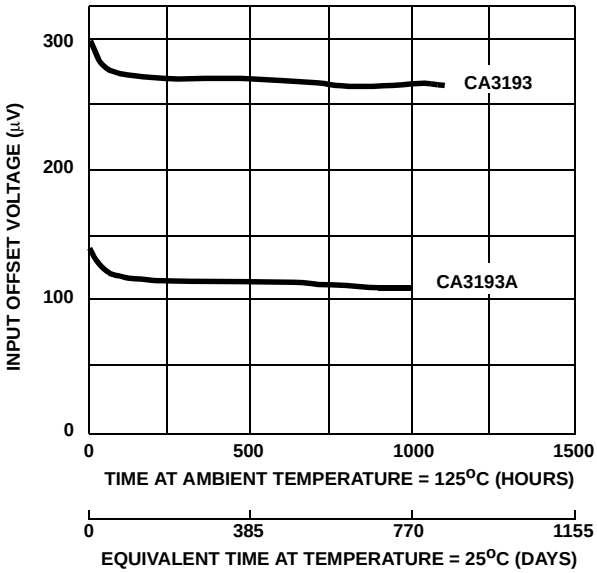


FIGURE 13. INPUT OFFSET VOLTAGE vs TIME

Typical Performance Curves (Continued)

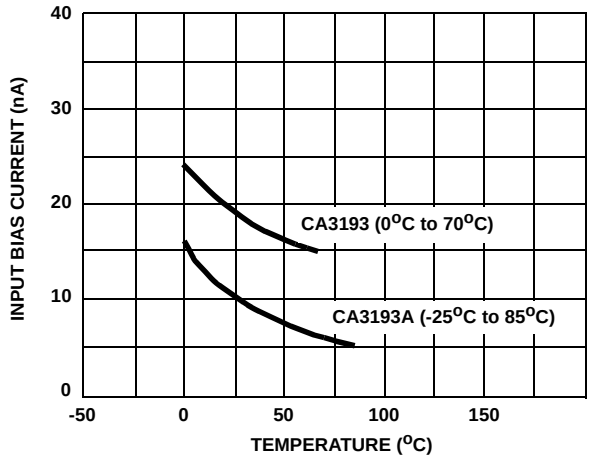


FIGURE 14. TYPICAL INPUT BIAS CURRENT vs TEMPERATURE

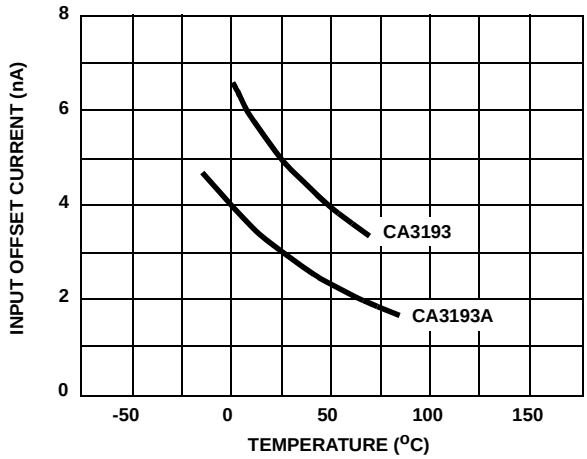


FIGURE 15. TYPICAL INPUT OFFSET CURRENT vs TEMPERATURE

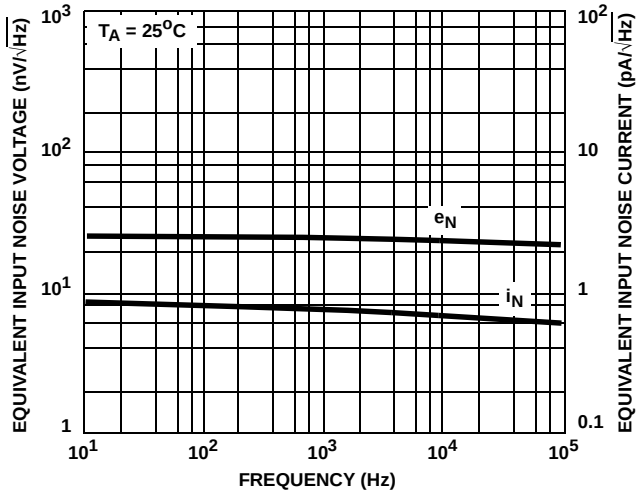


FIGURE 16. INPUT NOISE VOLTAGE AND CURRENT DENSITY vs FREQUENCY

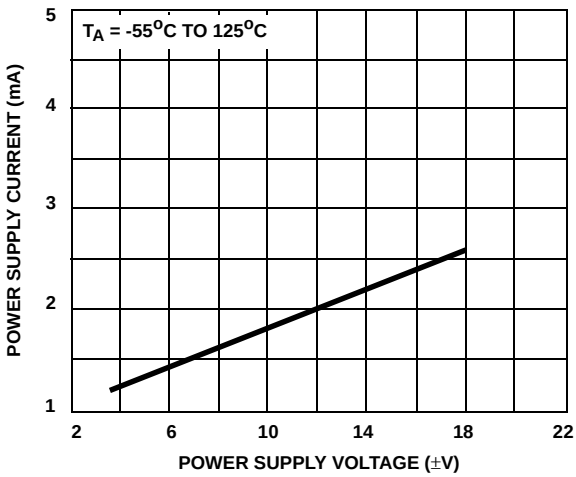


FIGURE 17. POWER SUPPLY CURRENT vs SUPPLY VOLTAGE

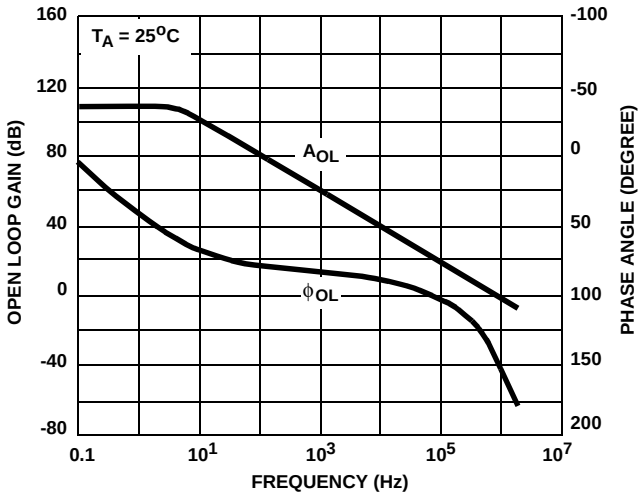


FIGURE 18. OPEN LOOP GAIN AND PHASE SHIFT RESPONSE

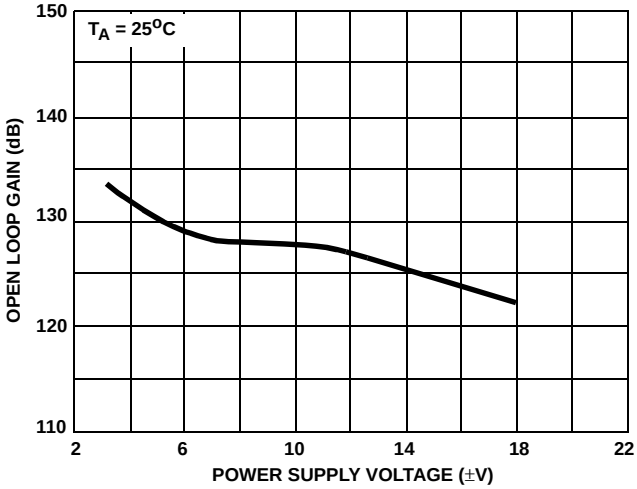


FIGURE 19. OPEN LOOP GAIN vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

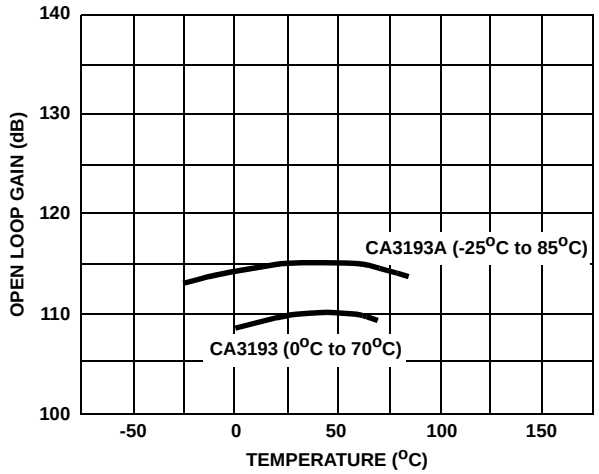


FIGURE 20. OPEN LOOP GAIN vs TEMPERATURE

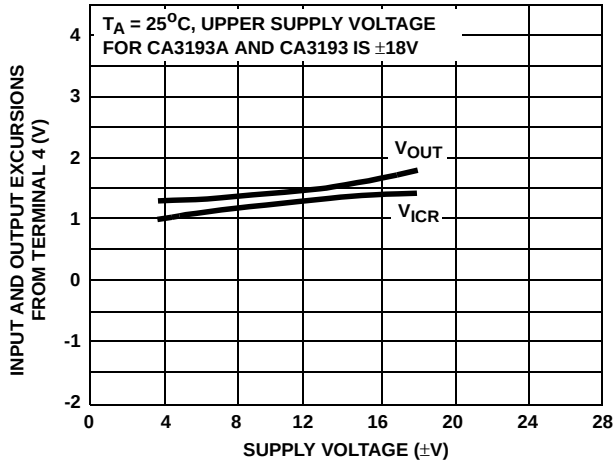


FIGURE 21.

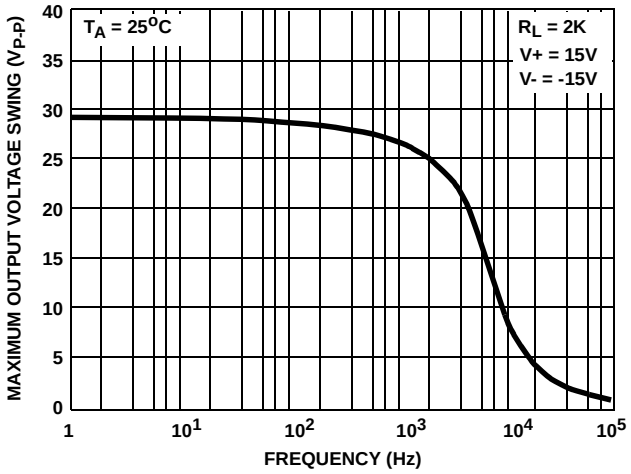


FIGURE 22. MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY

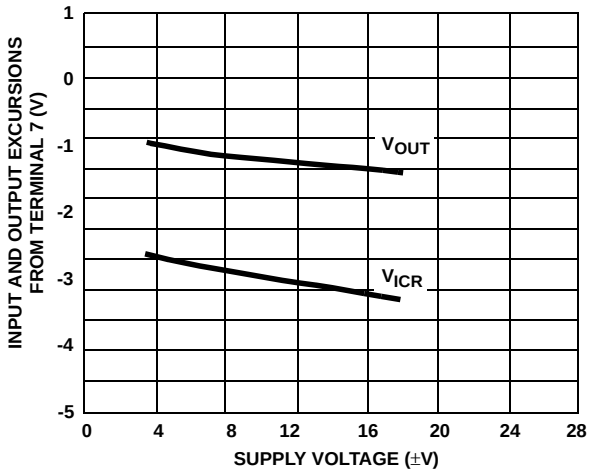
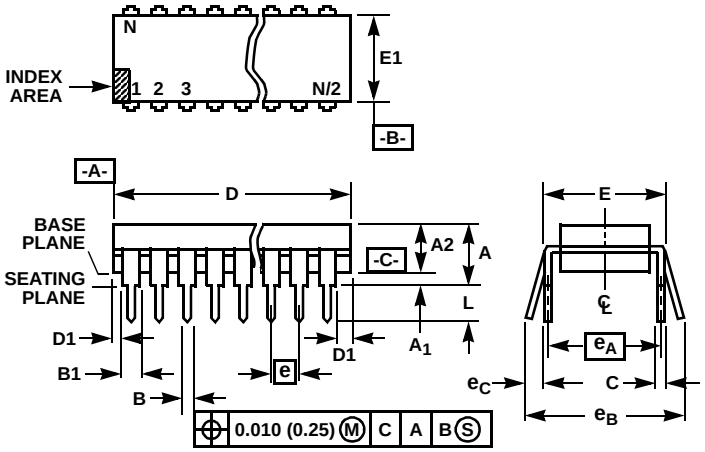


FIGURE 23. OUTPUT VOLTAGE SWING CAPABILITY AND COMMON MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93