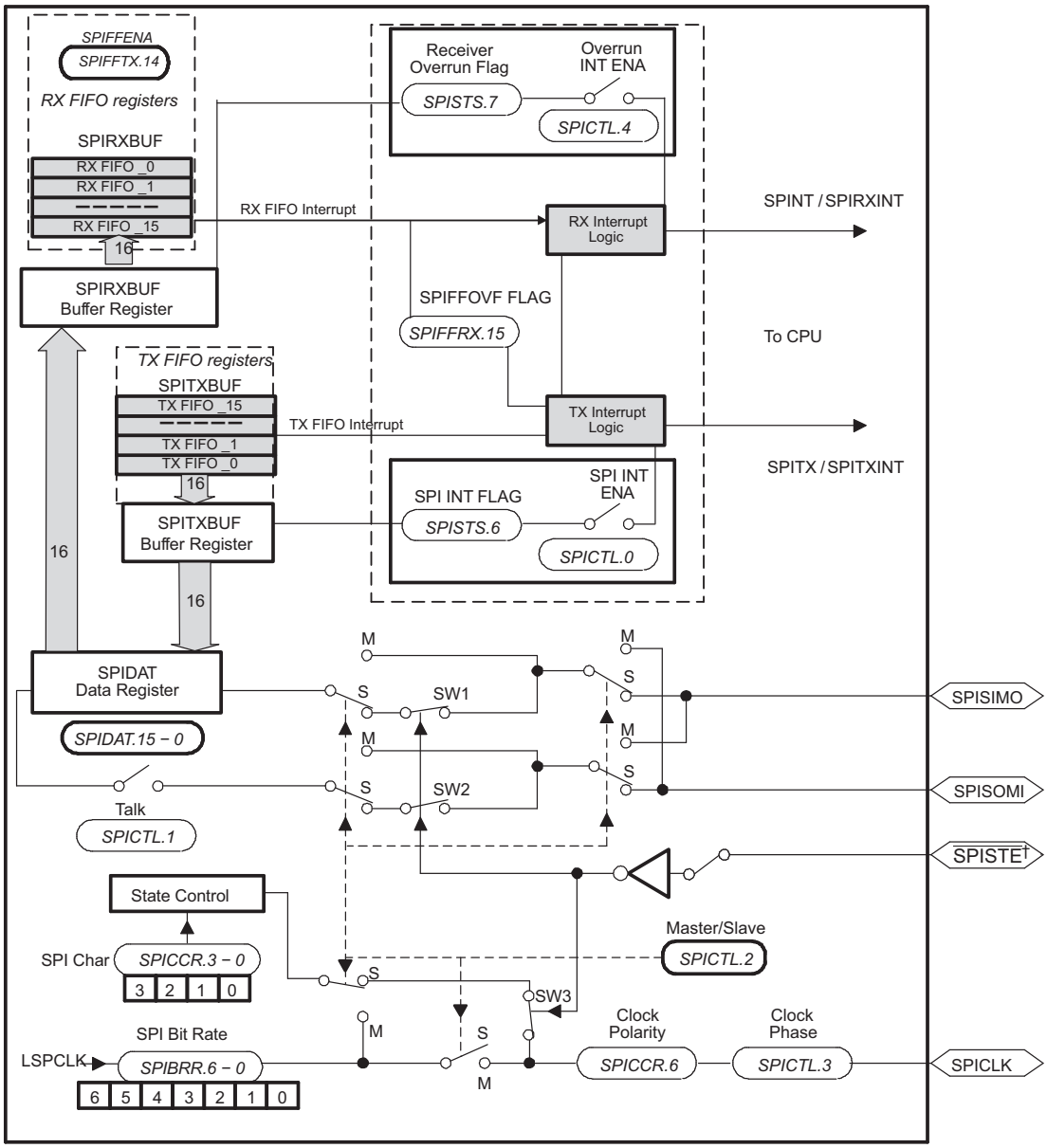
1.1.1 SPI Block Diagram

Figure 1-2 is a block diagram of the SPI in slave mode, showing the basic control blocks available on the 28x SPI module.

Figure 1-2. Serial Peripheral Interface Module Block Diagram



A SPISTE of a slave device is driven low by the master.

1.1.2 SPI Module Signal Summary

Table 1-1. SPI Module Signal Summary

Signal Name	Description
External Signals	
SPICLK	SPI clock
SPISIMO	SPI slave in, master out
SPISOMI	SPI slave out, master in
$\overline{\text{SPISTE}}$	SPI slave transmit enable
Control	
SPI Clock Rate	LSPCLK
Interrupt signals	
SPIRXINT	Transmit interrupt/ Receive Interrupt in non FIFO mode (referred to as SPI INT)
	Receive in interrupt in FIFO mode
SPITXINT	Transmit interrupt – FIFO

1.2 Overview of SPI Module Registers

The SPI port operation is configured and controlled by the registers listed in Table 1-2.

Table 1-2. SPI Registers

Name	Address Range	Size (x16)	Description
SPICCR	0x0000-7040	1	SPI Configuration Control Register
SPICTL	0x0000-7041	1	SPI Operation Control Register
SPIST	0x0000-7042	1	SPI Status Register
SPIBRR	0x0000-7044	1	SPI Baud Rate Register
SPIEMU	0x0000-7046	1	SPI Emulation Buffer Register
SPIRXBUF	0x0000-7047	1	SPI Serial Input Buffer Register
SPITXBUF	0x0000-7048	1	SPI Serial Output Buffer Register
SPIDAT	0x0000-7049	1	SPI Serial Data Register
SPIFFTX	0x0000-704A	1	SPI FIFO Transmit Register
SPIFFRX	0x0000-704B	1	SPI FIFO Receive Register
SPIFFCT	0x0000-704C	1	SPI FIFO Control Register
SPIPRI	0x0000-704F	1	SPI Priority Control Register

This SPI has 16-bit transmit and receive capability, with double-buffered transmit and double-buffered receive. All data registers are 16-bits wide.

The SPI is no longer limited to a maximum transmission rate of LSPCLK/8 in slave mode. The maximum transmission rate in both slave mode and master mode is now LSPCLK/4.

Writes of transmit data to the serial data register, SPIDAT (and the new transmit buffer, SPITXBUF), must be left-justified within a 16-bit register.

The control and data bits for general-purpose bit I/O multiplexing have been removed from this peripheral, along with the associated registers, SPIPC1 (704Dh) and SPIPC2 (704Eh). These bits are now in the General-Purpose I/O registers.

Twelve registers inside the SPI module control the SPI operations:

- SPICCR (SPI configuration control register). Contains control bits used for SPI configuration
  - SPI module software reset
  - SPICLK polarity selection
  - Four SPI character-length control bits