## A2.2 Circuit Details

The schematic diagrams in figures A2.8–A2.17 show the design of a complete MAYBE computer, which may be constructed from readily available parts. These diagrams focus on details useful in the construction of a MAYBE (for example, integrated-circuit packages and pin numbers) rather than the architectural structure of the machine; for insight into the latter, the reader will fare much better using the diagrams in chapter 11.
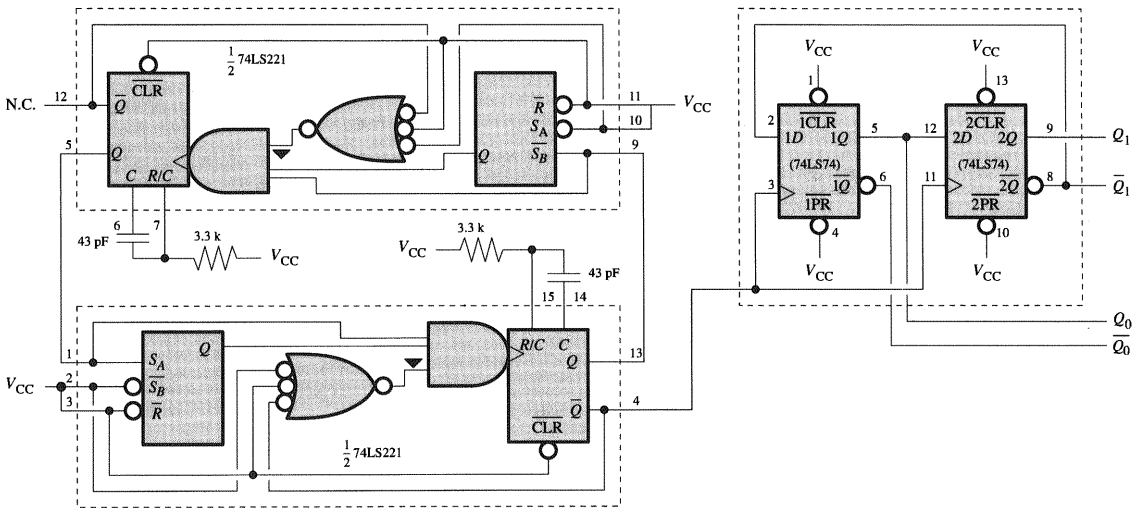
Figure A2.8 Left: System clock (nominal frequency is 3.7 MHz). Right: Gray-code counter.
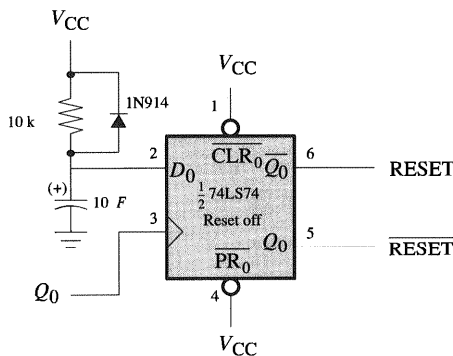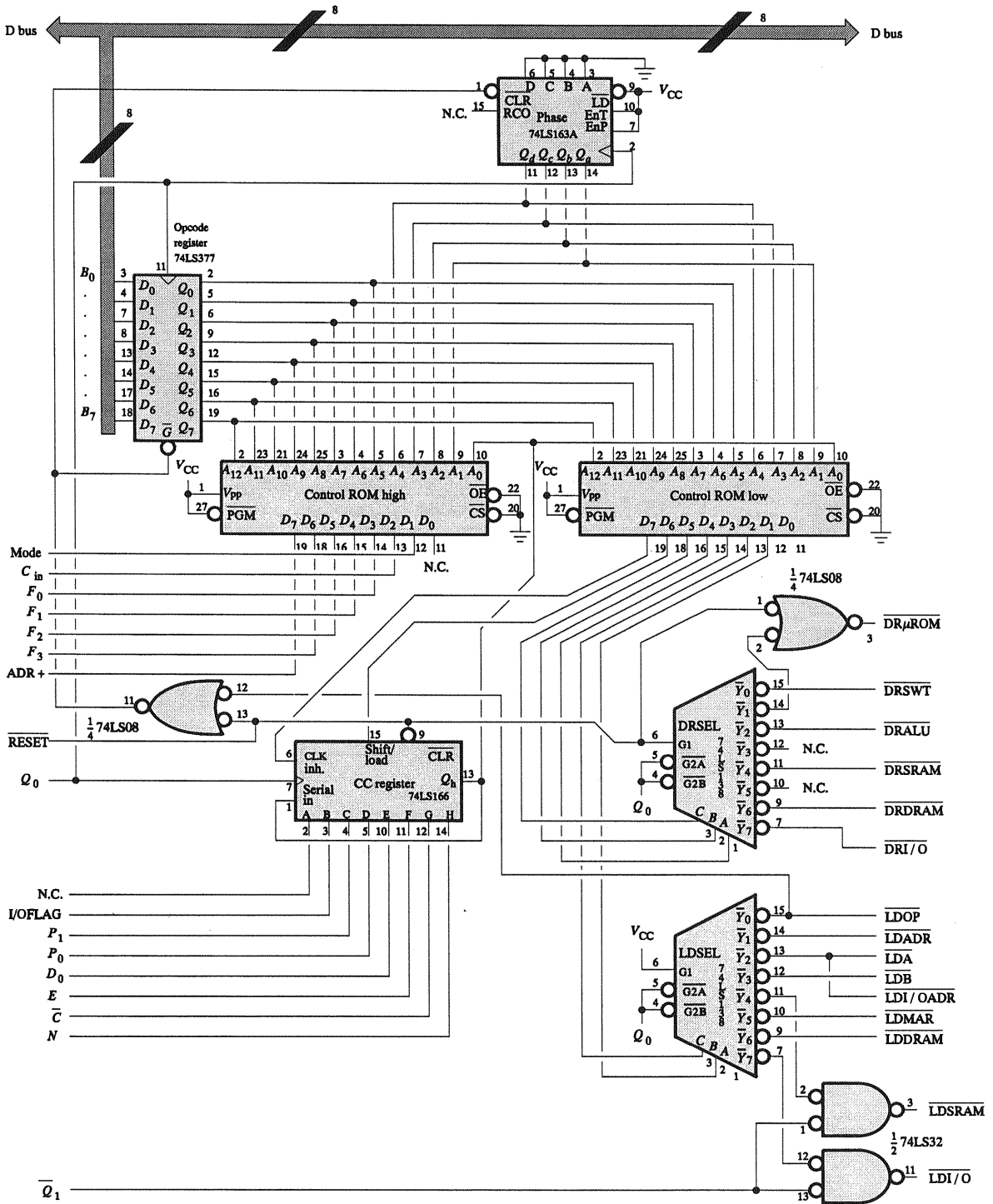

Figure A2.9 Reset circuitry.
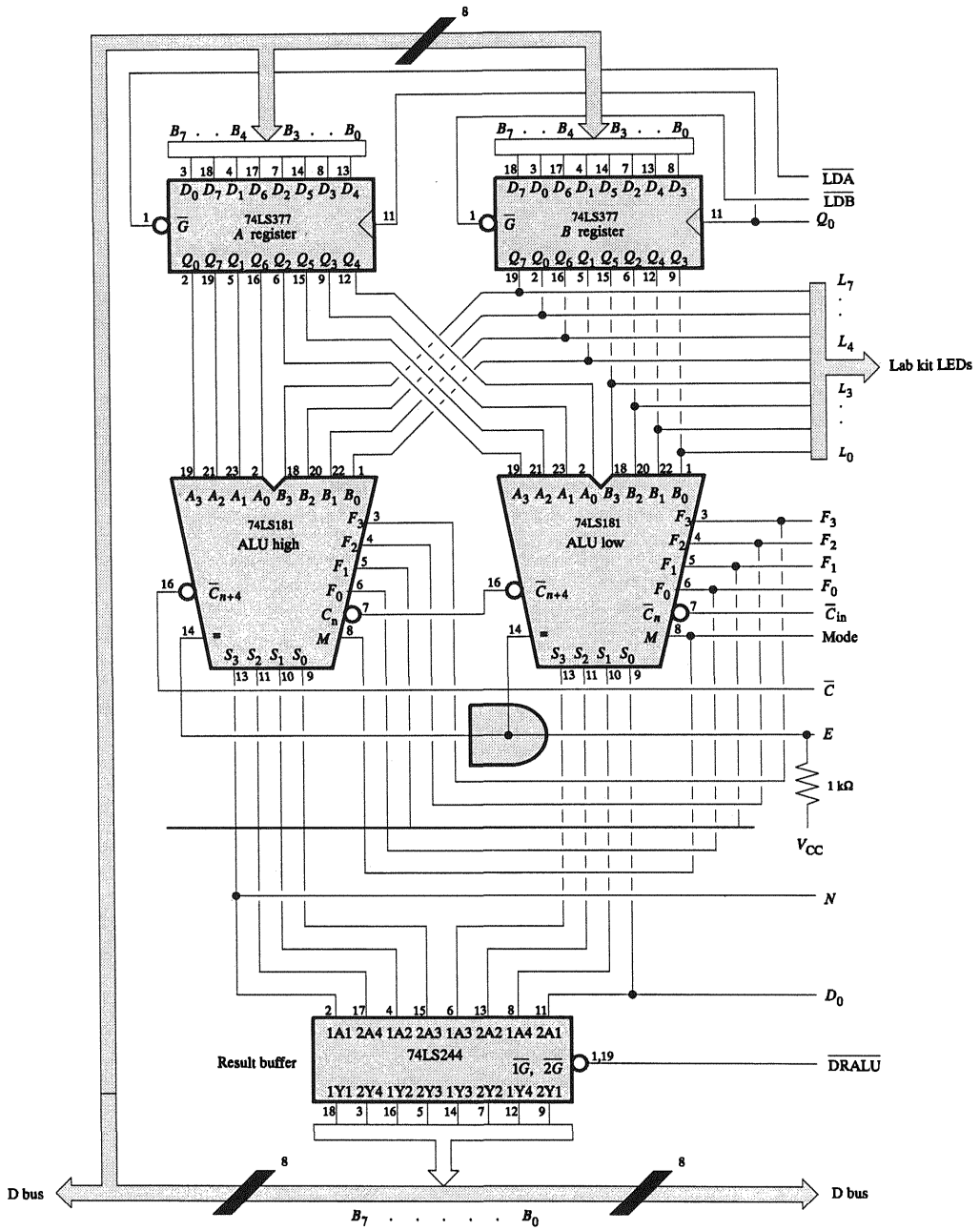
Figure A2.10 Control ROM.
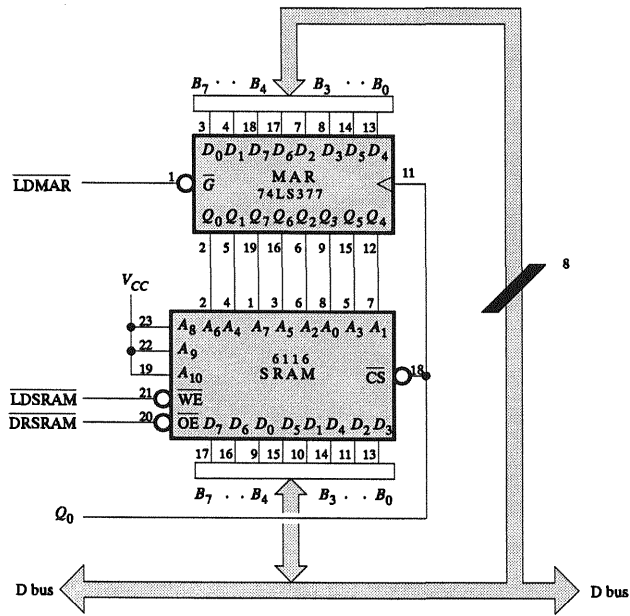
Figure A2.11 Arithmetic logic unit (PC card).
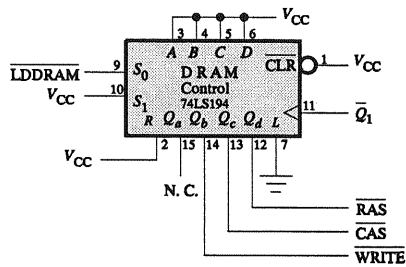
Figure A2.12 Static RAM (PC card).

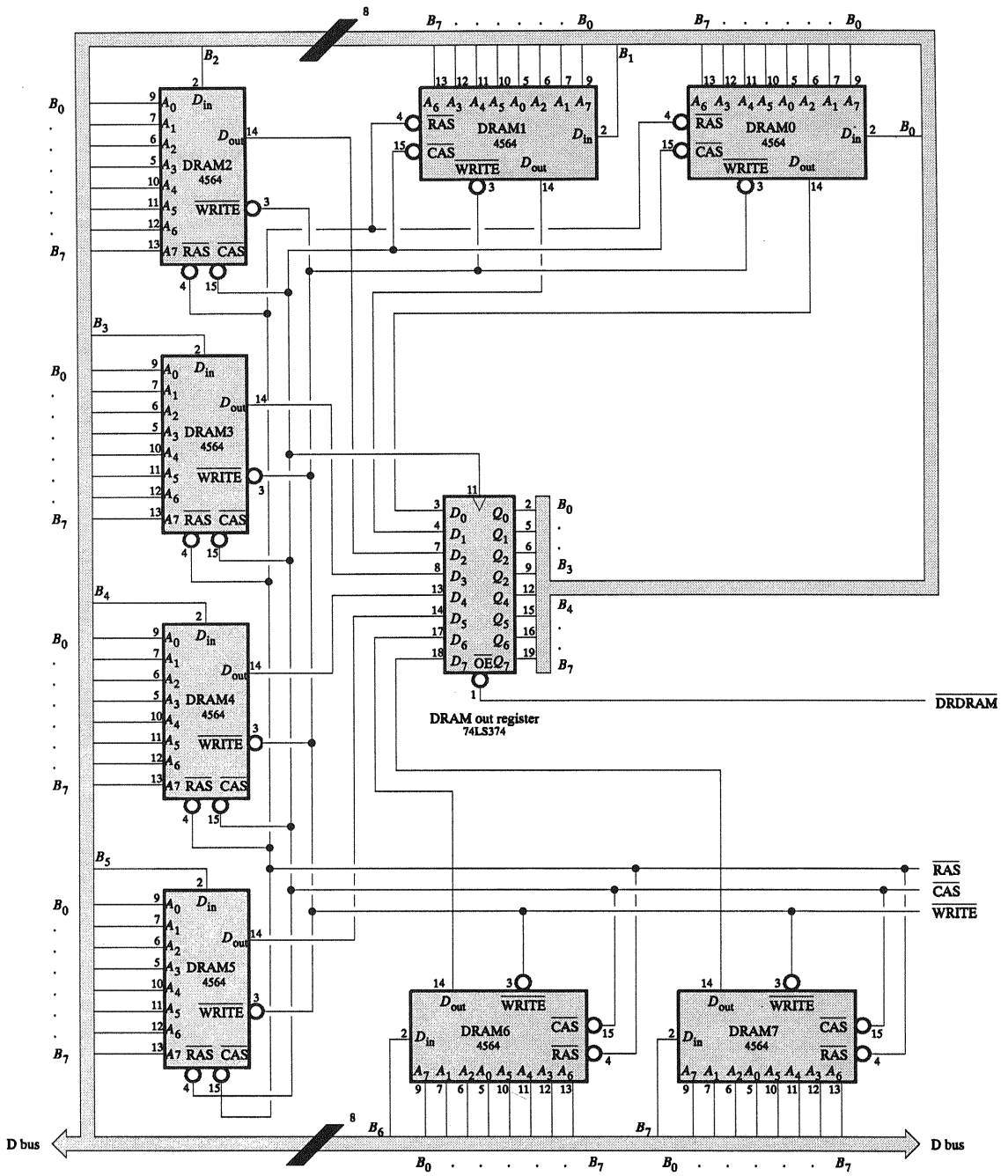**Figure A2.13** Dynamic RAM controller.
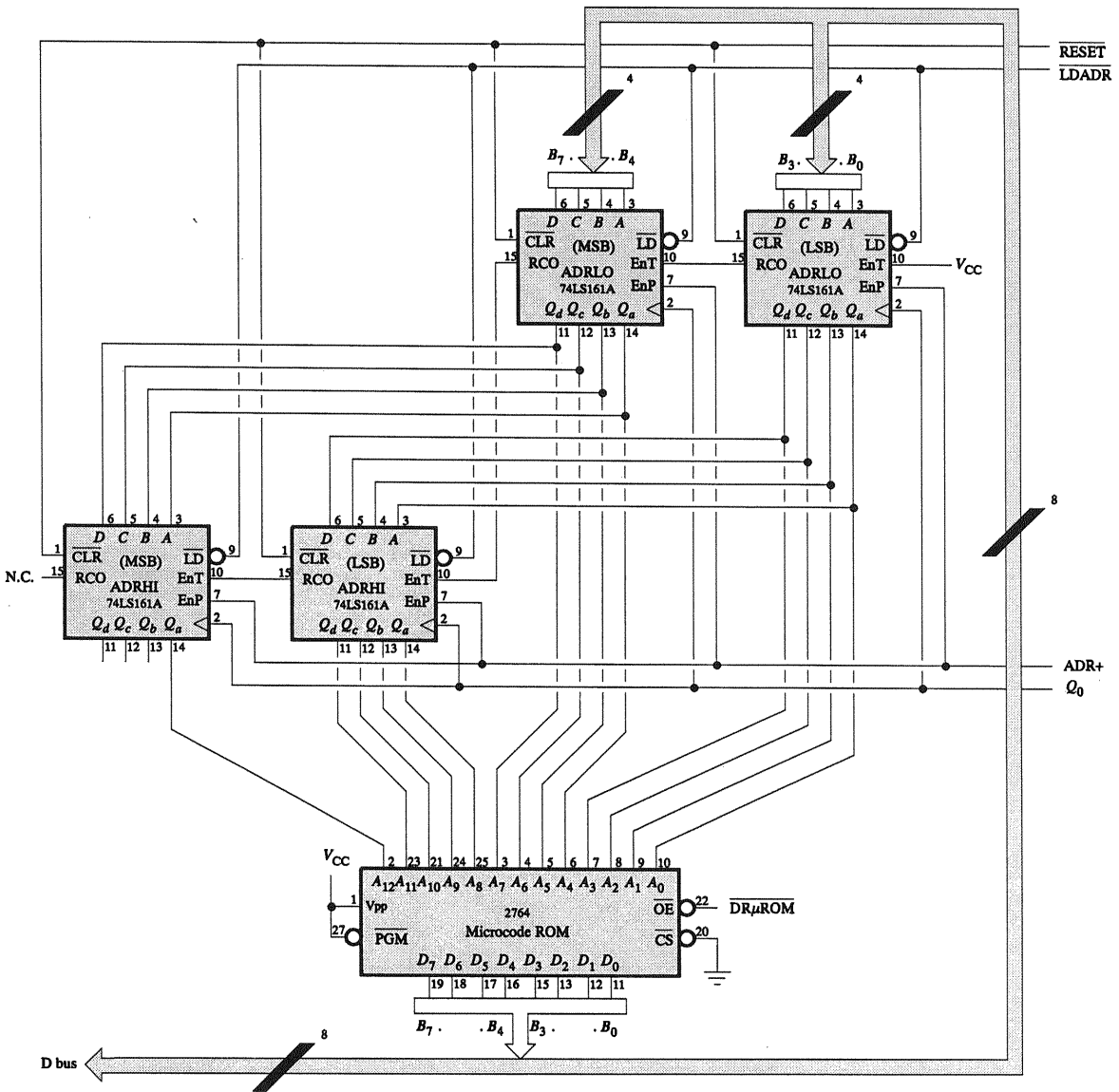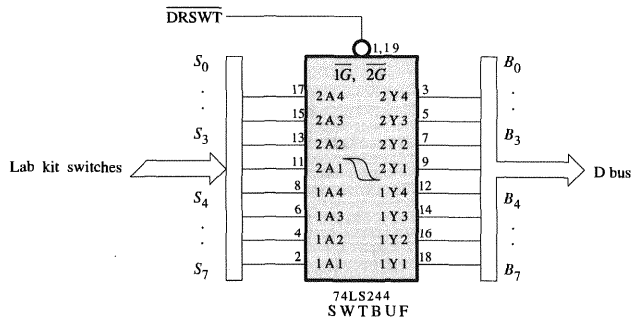
Figure A2.14 Dynamic RAM (PC card).

Figure A2.15   Microcode ROM (PC card).

Figure A2.16 Switch buffer.