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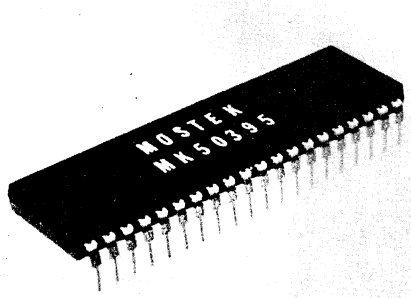
MOSTEK®

SIX DECADE COUNTER / DISPLAY DECODER

MK50395/6/7

FEATURES

- ☐ Single power supply
- ☐ Schmitt Trigger on the count input
- ☐ Six decades of synchronous up/down counting
- ☐ Look-ahead carry or borrow
- ☐ Loadable counter
- ☐ Loadable compare register with comparator output
- ☐ Multiplexed BCD and seven-segment outputs
- ☐ Internal scan oscillator
- ☐ Direct LED segment drive
- ☐ Interfaces directly with CMOS logic
- ☐ Leading zero blanking
- ☐ MK 50396 programmed to count time: 99 hrs. 59 min. 59 sec.
- ☐ MK 50397 programmed to count time: 59 min. 59 sec. 99/100 sec.



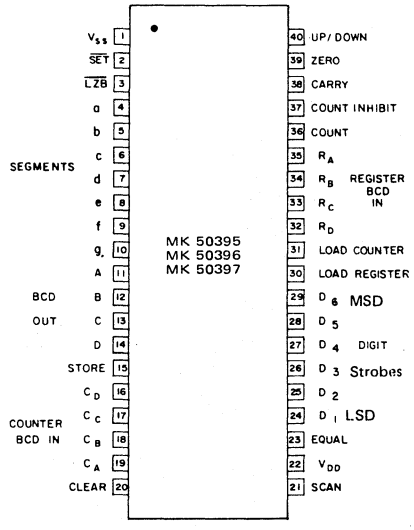
DESCRIPTION

The MK 50395 is an ion-implanted, P-channel MOS six-decade synchronous up/down counter/display driver with compare register and storage latches. The counter as well as the register can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The six-decade register is constantly compared to the state of the six-decade counter and when both the register and the counter have the same content, an EQUAL signal is generated. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7-segment format to the output. The seven-segment decoder incorporates a leading-zero blanking circuit which can be disabled by an external signal. This device is intended to interface directly with the standard CMOS logic families.

The MK 50396 and MK 50397 operate identically to the MK 50395 except that two digits in each were reprogrammed to provide divide by six circuitry instead of divide by ten. The MK 50396 is well suited for industrial timer applications while the MK 50397 is best suited for stop watch or real-time computer clock applications.

PIN CONNECTIONS
FIGURE 1



V COUNTER DISPLAY DECODERS

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OPERATIONS:

SIX-DECADE COUNTER, LATCH

The six-decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input; the count input is inhibited when the count inhibit is high.

The counter will increment when the up/down input is high (V_{SS}) and will decrement when the up/down input is low. The up/down input can be changed 0.75 μs prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six-digit latch or the scan counter.

As long as the store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when the store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded digit-by-digit corresponding to the digit strobe outputs. BCD thumb wheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The load counter pulse must be at V_{SS} 2 microseconds prior to the positive transition of the digit strobe of the digit to be loaded. The load counter pulse may be removed after the positive transition of the digit strobe since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the digit strobe.

INPUTS, OUTPUTS

The seven segment outputs are open drain and capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at V_{SS}. The Carry, Equal, Zero, BCD and digit strobe outputs are push-pull and are on when at V_{SS}. All inputs except Counter BCD, Register BCD, and SCAN inputs are high-impedance CMOS compatible.

Three basic outputs originate from the counter: Zero output, Equal output, and Carry output. Each output goes high on the positive- (V_{SS}) going edge of the count input under the following conditions:

The Zero output goes high for one count period when all decades contain zero. During a load counter operation the zero output is inhibited.

The Equal output goes high for one count period when the contents of the counter and compare register are equal. The equal output is inhibited by a load counter or load register operation, which lasts until the next interdigit blanking period following a negative transition of Load Counter or Load Register.

The Carry output goes high with the leading edge of the count input at the count of 000000 when counting up or at 999999* when counting down and goes low with the negative going edge of the same count input.

A count frequency of 1 MHz can be achieved if the Equal output, Zero output and Carry output are not used. These outputs do not respond at this frequency due to their output delay, as illustrated on the timing diagram, Figure 3.

SIX-DECADE COMPARE REGISTER

The register is loaded identically as described in the load counter paragraph. The register may be loaded independently of the counter. However, the Clear input will not remove the register contents. Contents of the register are not displayed by the BCD or seven-segment outputs.

BCD & SEVEN-SEGMENT OUTPUTS

BCD or seven-segment outputs are available. Digit strobes are decoded internally by a divide-by-six Johnson counter. This counter scans from MSD to LSD. By bringing the SET input low, this counter will be forced to the MSD decade count. During this time, the segment outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when SET is low. Applying V_{SS} to SET allows normal scan to resume. Digit 6 output is active (V_{SS}) until the next scan clock pulse brings up the digit 5 output.

The segment outputs and digit strobes are blanked during the interdigit blanking time. Leading zero blanking affects only the segment outputs. This option is disabled by bringing the LZB input high. Typically, the interdigit blanking time is 5 to 25 microseconds when using the internal scan oscillator.

BCD output data changes at the beginning of the interdigit blanking time. Therefore, the BCD output data is valid when the positive transition of a digit output occurs.

SCAN OSCILLATOR

The MK 50395 has an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and the scan input. The wave form present on the scan oscillator input is triangular in the self-oscillate mode.

An external oscillator may also be used to drive the scan input.

In the internal drive mode, the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self-oscillate blanking time (5 → 25 μsec). Display brightness can be controlled by the duty cycle of the external scan oscillator.

*Carry occurs at 99 59 59 for the MK 50396 and 59 59 99 for the MK 50397

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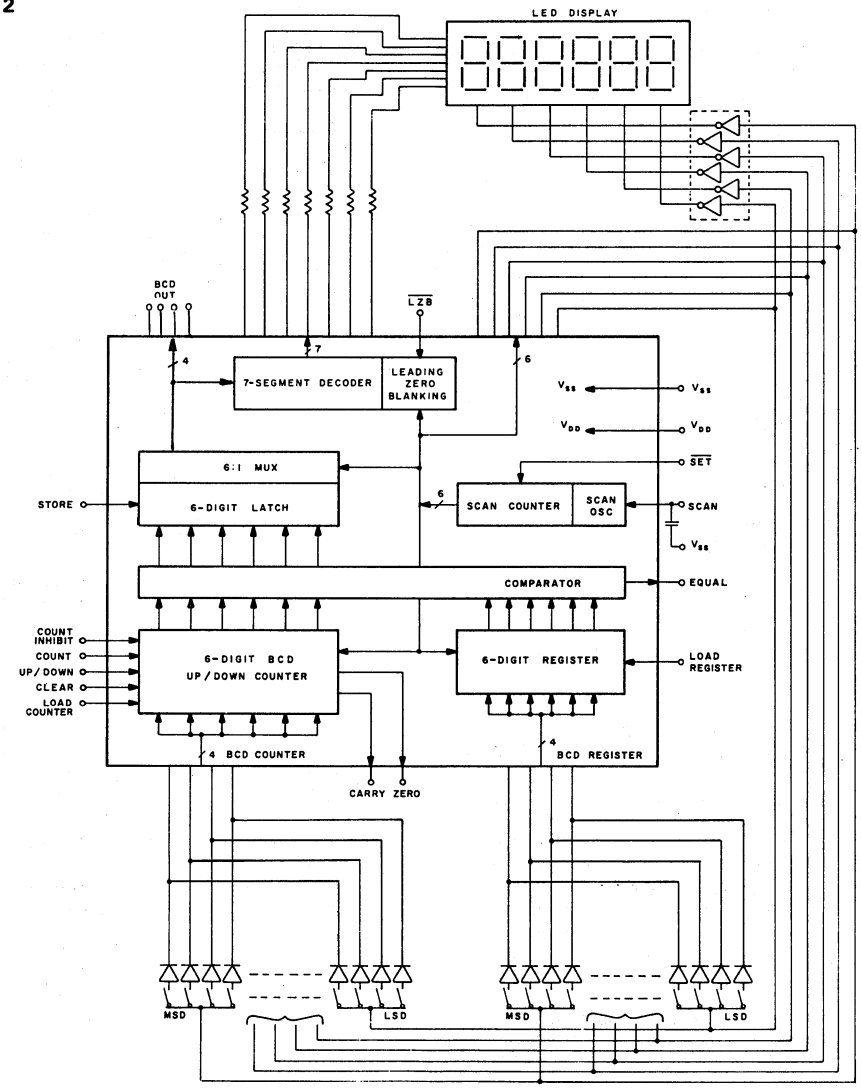
ypically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor values from Vss to the Scan input:

	Min	Max	
	820pF	1.4kHz	4.8kHz
	470pF	2.0kHz	6.8kHz
	120pF	7.0kHz	20kHz

FUNCTIONAL DIAGRAM
FIGURE 2



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ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . . +0.3V to −20V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range (Ambient) . . . . . -40°C to +100°C

MAXIMUM OPERATING CONDITIONS

	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Operating Temperature	0	70	°C	
V_{SS}	Supply Voltage (V_{DD} = 0V)	10	15	V	
I_{SS}	Supply Current		30	mA	1
B_V	Break-Down Voltage (Segment only @ 10 μA)		V_{SS} − 26	V	
P_D	Power Dissipation		670	mW	2

ELECTRICAL CHARACTERISTICS

(V_{DD} = 0V, V_{SS} = + 10.0V to + 15.0V, 0°C ≤ T_A ≤ 70°C)

Static Operating Conditions

	PARAMETER	MIN	MAX	UNITS	NOTES
V_{IL}	Input Low Voltage, "0"	V_{DD}	20% of V_{SS}	V	
V_{IH}	Input High Voltage, "1"	V_{SS}−1	V_{SS}	V	3
V_{OL}	Output Voltage "0" @ 30 μA		20% of V_{SS}	V	4
V_{OH}	Output Voltage "1" @ 1.5 mA	80% of V_{SS}		V	4
I_{OH}	Output Current "1"				
	digit strobes	3.0		mA	5
	segment outputs	10.0		mA	6
I_{SCAN}	Scan Input Pullup Current @ 0V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15V	2	40	μA	
$I_{\overline{SET}}$	$\overline{SET}$ Input Pullup Current @ 0V	5	60	μA	

NOTES:
1. I_{SS} with inputs and outputs open at 0°C 28mA at 25°C and 25mA at 70°C. This does not include segment current. Total power per segment must be limited so as not to exceed power dissipation of package. (Θ_{JA} = 100°C/Watt)
2. All outputs loaded.
3. MIN V_{IH} from R_A R_B R_C R_D C_A C_B C_C C_D inputs is V_{SS} −2.5V. Those inputs have internal pulldown resistors to V_{DD}.
4. This applies to the push-pull CMOS compatible outputs. Does not include digit strobes or segment outputs.
5. For V_{OUT} = V_{SS} −2.0 volts. Average value over one digit cycle.
6. For V_{OUT} = V_{SS} −3.0 volts. Average value over one digit cycle.

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Dynamic Operating Conditions

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
f_{CI}	Count Input Frequency	0	1.00	MHz	7, 8
f_{SI}	Scan Input Frequency	0	20	kHz	
t_{CPW}	Count Pulse Width	400		ns	9
t_{SPW}	Store Pulse Width	2.0		μs	
t_{SS}	Store Setup Time	0		μs	10
t_{CIS}	Count Inhibit Setup Time	0		μs	10
t_{UDS}	Up/Down Setup Time	- 0.75		μs	10
t_{CPW}	Clear Pulse Width	2.0		μs	10
t_{CS}	Clear Setup Time	- 0.5		μs	10
t_{OA}	Zero Access Time		3.0	μs	10
t_{OH}	Zero Hold Time		1.5	μs	10
t_{CA}	Carry Access Time		1.5	μs	10
t_{CH}	Carry Hold Time		0.9	μs	11
t_{EA}	Equal Access Time		2.0	μs	10
t_{EH}	Equal Hold Time		1.5	μs	10
t_L	Load Time	$1/6\ f_{SI}$			

NOTES:
7. Measured at 50% duty cycle.
8. If Carry, Equal, or Zero outputs are used, the count frequency will be limited by their respective output times.
9. The count pulse width must be greater than the carry access time when using the carry output.
10. The positive edge of the count input is the t - 0 reference.
11. Measured from negative edge of count input.

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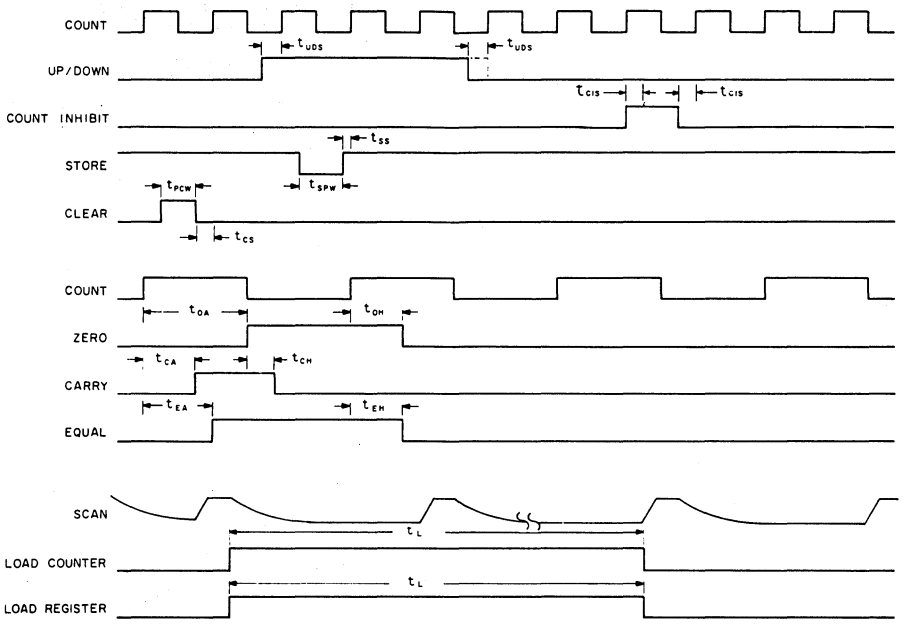
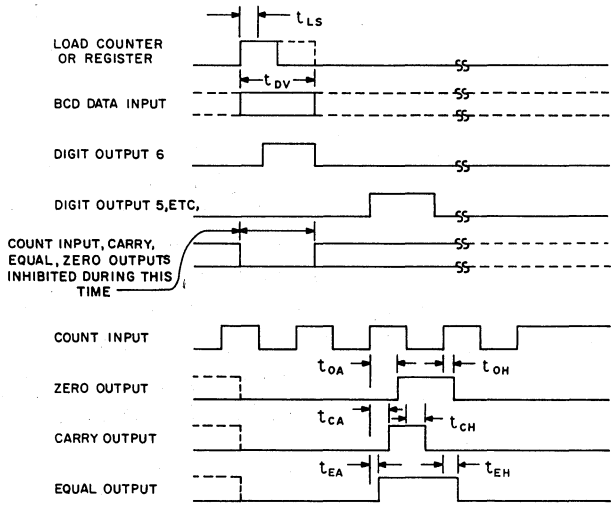
IGURE 3



LOADING COUNTER, REGISTER (1 DIGIT)
FIGURE 4



t_{LS} 2.0 μsec min NOTE: REF TO POSITIVE TRANSITION OF DIGIT OUTPUT

t_{DV} 2.0 μsec min NOTE: REF TO NEGATIVE EDGE OF DIGIT OUTPUT

NOTE:

The inhibit function of the Zero or Equal outputs does not end when the Load Counter input goes to a "0" unless that transition occurs during interdigit blanking period at least 2.0 μsec prior to a positive transition of a digit output. This same timing restriction hold for Equal and Load Register.