(2) External clock

When an external clock is selected by setting SIO1CR<SCK> to "111B", the clock via the $\overline{SCK1}$ pin from an external source is used as the serial clock.

To ensure shift operation, the serial clock pulse width must be 4/fc or more for both "H" and "L" levels.

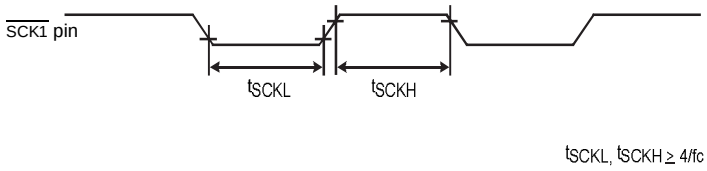


Figure 14-3 External Clock

14.3.1.2 Shift edge

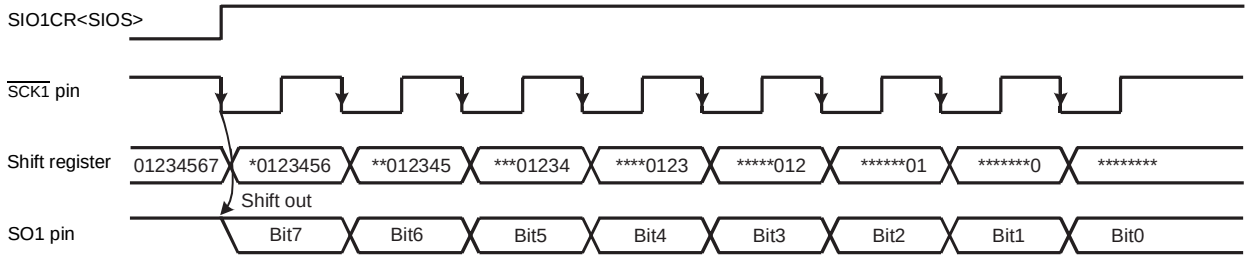
The leading edge is used to transmit data, and the trailing edge is used to receive data.

(1) Leading edge shift

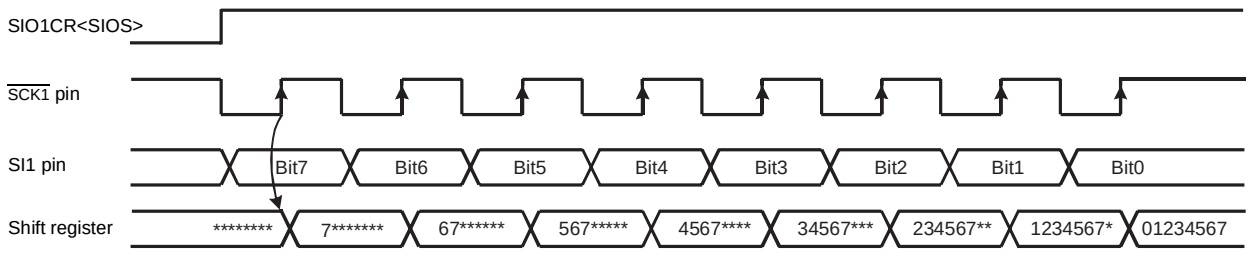
Data is shifted on the leading edge of the serial clock (falling edge of the $\overline{SCK1}$ pin input/output).

(2) Trailing edge shift

Data is shifted on the trailing edge of the serial clock (rising edge of the $\overline{SCK1}$ pin input/output).



(a) Leading edge shift (Example of MSB transfer)



(b) Trailing edge shift (Example of MSB transfer)

Figure 14-4 Shift Edge