Designing A SEPIC Converter

National Semiconductor
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Introduction

In a SEPIC (Single Ended Primary Inductance Converter) design, the output voltage can be higher or lower than the input voltage. The SEPIC converter shown in Figure 1 uses two inductors, L1 and L2. The two inductors can be wound on the same core since the same voltages are applied to them throughout the switching cycle. Using a coupled inductor takes up less space on the PCB and tends to be lower cost than two separate inductors. The capacitor Cs isolates the input from the output and provides protection against a shorted load. Figures 2 and 3 show the SEPIC converter current flow and switching waveforms.

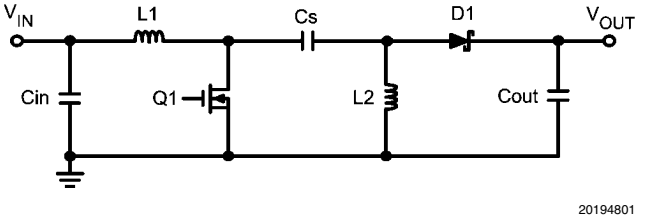

FIGURE 1. SEPIC Topology

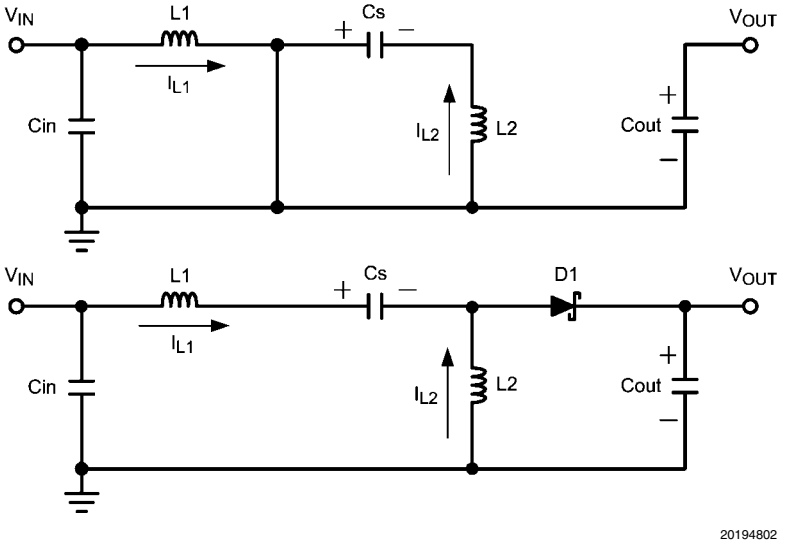

FIGURE 2. SEPIC Converter Current Flow
Top: During Q1 On-Time,
Bottom: During Q1 Off-Time

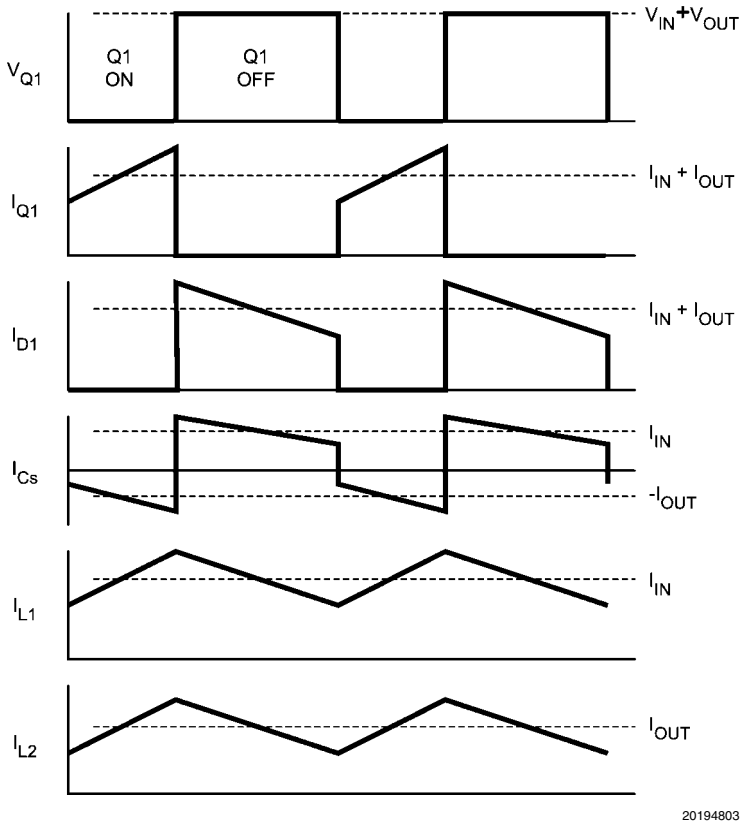

FIGURE 3. SEPIC Converter Switching Waveforms (V_{Q1}: Q1 Drain to Source Voltage)

Duty Cycle Consideration

For a SEPIC converter operating in a continuous conduction mode (CCM), the duty cycle is given by:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_{OUT} + V_D}$$

V_D is the forward voltage drop of the diode D1. The maximum duty cycle is:

$$D_{max} = \frac{V_{OUT} + V_D}{V_{IN\,(min)} + V_{OUT} + V_D}$$

Inductor Selection

A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage. The ripple current flowing in equal value inductors L1 and L2 is given by:

$$\Delta I_L = I_{IN} \times 40\% = I_{OUT} \times \frac{V_{OUT}}{V_{IN\,(min)}} \times 40\%$$

The inductor value is calculated by:

$$L1 = L2 = L = \frac{V_{IN\,(min)}}{\Delta I_L \times f_{sw}} \times D_{max}$$

f_{sw} is the switching frequency and D_{max} is the duty cycle at the minimum V_{in}. The peak current in the inductor, to ensure the inductor does not saturate, is given by:

$$I_{L1\,(peak)} = I_{OUT} \times \frac{V_{OUT} + V_D}{V_{IN\,(min)}} \times \left(1 + \frac{40\%}{2}\right)$$

$$I_{L2\,(peak)} = I_{OUT} \times \left(1 + \frac{40\%}{2}\right)$$

If L1 and L2 are wound on the same core, the value of inductance in the equation above is replaced by 2L due to mutual inductance. The inductor value is calculated by:

$$L1' = L2' = \frac{L}{2} = \frac{V_{IN\,(min)}}{2 \times \Delta I_L \times f_{sw}} \times D_{max}$$

Power MOSFET Selection

The parameters governing the selection of the MOSFET are the minimum threshold voltage $V_{th(min)}$, the on-resistance $R_{DS(ON)}$, gate-drain charge Q_{GD}, and the maximum drain to source voltage, $V_{DS(max)}$. Logic level or sublogic-level threshold MOSFETs should be used based on the gate drive voltage.

The peak switch voltage is equal to Vin + Vout. The peak switch current is given by:

$$I_{Q1\ (peak)} = I_{L1\ (peak)} + I_{L2\ (peak)}$$

The RMS current through the switch is given by:

$$I_{Q1\ (rms)} = I_{OUT} \sqrt{\frac{(V_{OUT} + V_{IN\ (min)} + V_D) \times (V_{OUT} + V_D)}{V_{IN\ (min)}^2}}$$

The MOSFET power dissipation PQ1 is approximately:

$$P_{Q1} = I_{Q1\ (rms)}^2 \times R_{DS\ (ON)} \times D_{max} + (V_{IN\ (min)} + V_{OUT}) \times I_{Q1\ (peak)} \times \frac{Q_{GD} \times f_{sw}}{I_G}$$

P_{Q1}, the total power dissipation for MOSFETs includes conduction loss (as shown in the first term of the above equation) and switching loss as shown in the second term. I_G is the gate drive current. The $R_{DS(ON)}$ value should be selected at maximum operating junction temperature and is typically given in the MOSFET datasheet. Ensure that the conduction losses plus the switching losses do not exceed the package ratings or exceed the overall thermal budget.

Output Diode Selection

The output diode must be selected to handle the peak current and the reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current $I_{Q1(peak)}$. The minimum peak reverse voltage the diode must withstand is:

$$V_{RD1} = V_{IN\ (max)} + V_{OUT\ (max)}$$

Similar to the boost converter, the average diode current is equal to the output current. The power dissipation of the diode is equal to the output current multiplied by the forward voltage drop of the diode. Schottky diodes are recommended in order to minimize the efficiency loss.

SEPIC Coupling Capacitor Selection

The selection of SEPIC capacitor, Cs, depends on the RMS current, which is given by:

$$I_{Cs\ (rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT} + V_D}{V_{IN\ (min)}}}$$

The SEPIC capacitor must be rated for a large RMS current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum and ceramic capacitors are the best choice for SMT, having high RMS current ratings relative to size. Electrolytic capacitors work well for through-hole applications where the size is not limited and they can accommodate the required RMS current rating.

The peak-to-peak ripple voltage on Cs (assuming no ESR):

$$\Delta V_{Cs} = \frac{I_{OUT} \times D_{max}}{Cs \times f_{sw}} \quad (1)$$

A capacitor that meets the RMS current requirement would mostly produce small ripple voltage on Cs. Hence, the peak voltage is typically close to the input voltage.

Output Capacitor Selection

In a SEPIC converter, when the power switch Q1 is turned on, the inductor is charging and the output current is supplied by the output capacitor. As a result, the output capacitor sees large ripple currents. Thus the selected output capacitor must be capable of handling the maximum RMS current. The RMS current in the output capacitor is:

$$I_{Cout\ (rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT} + V_D}{V_{IN\ (min)}}} \quad (2)$$

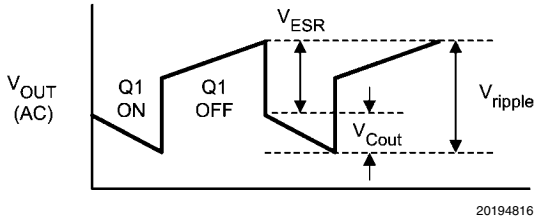

FIGURE 4. Output Ripple Voltage

The ESR, ESL, and the bulk capacitance of the output capacitor directly control the output ripple. As shown in Figure 4, we assume half of the ripple is caused by the ESR and the other half is caused by the amount of capacitance. Hence,

$$ESR \leq \frac{V_{ripple} \times 0.5}{I_{L1\ (peak)} + I_{L2\ (peak)}} \quad (3)$$

$$Cout \geq \frac{I_{OUT} \times D}{V_{ripple} \times 0.5 \times f_{sw}} \quad (4)$$

The output cap must meet the RMS current, ESR and capacitance requirements. In surface mount applications, tantalum, polymer electrolytic, and polymer tantalum, or multi-layer ceramic capacitors are recommended at the output.

Input Capacitor Selection

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. The RMS current in the input capacitor is given by:

$$I_{Cin\ (rms)} = \frac{\Delta I_L}{\sqrt{12}} \quad (5)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not so critical in a SEPIC application, a 10 µF or higher value, good quality ca-

pacitor would prevent impedance interactions with the input supply.

SEPIC Converter Design Example

Input voltage (V_{IN}): 3.0V-5.7V LM3478 controller is used in this example. Schematic is shown in Figure 5.

Output voltage (V_{OUT}): 3.3V

Output current (I_{OUT}): 2.5A

Switching frequency f_{sw}: 330kHz

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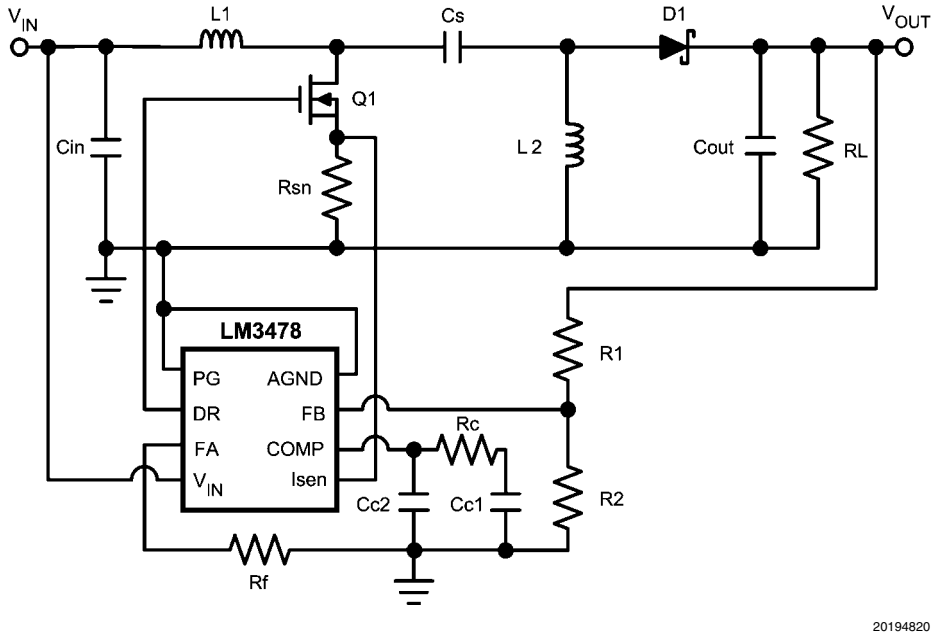

FIGURE 5. Schematic

Step 1: Duty cycle calculation

We assume that the V_D is 0.5V,

$$D_{max} = \frac{V_{OUT} + V_D}{V_{IN\,(min)} + V_{OUT} + V_D} = \frac{3.3 + 0.5}{3.0 + 3.3 + 0.5} = 0.56 \quad (6)$$

$$D_{min} = \frac{V_{OUT} + V_D}{V_{IN\,(max)} + V_{OUT} + V_D} = \frac{3.3 + 0.5}{5.7 + 3.3 + 0.5} = 0.40 \quad (7)$$

Step 2: Inductor selection

The input inductor L1 ripple current is:

$$\Delta I_L = I_{OUT} \times \frac{V_{OUT}}{V_{IN\,(min)}} \times 40\% = 2.5 \times \frac{3.3}{3.0} \times 0.4 = 1.1A \quad (8)$$

and the inductance for L1 and L2 is:

$$L1 = L2 = L = \frac{V_{IN\,(min)}}{\Delta I_L \times f_{sw}} \times D_{max} = \frac{3.0}{1.1 \times 330k} \times 0.56 = 4.6\ \mu H \quad (9)$$

The closest standard value of an off-the-shelf inductor is 4.7 µH. The peak input inductor current is:

$$I_{L1\,(peak)} = I_{OUT} \times \frac{V_{OUT} + V_D}{V_{IN\,(min)}} \times \left(1 + \frac{40\%}{2}\right) = 2.5 \times \frac{3.3 + 0.5}{3.0} \times 1.2 = 3.8A \quad (10)$$

The peak current for L2 is:

$$I_{L2\,(peak)} = I_{OUT} \times \left(1 + \frac{40\%}{2}\right) = 2.5 \times 1.2 = 3A \quad (11)$$

Step 3: Power MOSFET selection

The MOSFET peak current is:

$$I_{Q1\,(peak)} = I_{L1\,(peak)} + I_{L2\,(peak)} = 3.8 + 3 = 6.8A \quad (12)$$

and the RMS current is:

$$I_{Q1(rms)} = I_{OUT} \sqrt{\frac{(V_{OUT} + V_{IN(min)} + V_D) \times (V_{OUT} + V_D)}{V_{IN(min)}^2}} = 2.5 \times \sqrt{\frac{(3.3 + 3.0 + 0.5) \times (3.3 + 0.5)}{3.0^2}} = 4.2A \quad (13)$$

The rated drain voltage for the MOSFET must be higher than $V_{IN}+V_{OUT}$. Si4442DY ($R_{DS(ON)}$ = 8mΩ and Q_{GD} = 10nC) is selected in this design. The gate drive current I_G of the LM3478 is 0.3A. The estimated power loss is:

$$P_{Q1} = I^2_{Q1\,(rms)} \times R_{DS\,(ON)} \times D_{max} + (V_{IN\,(min)} + V_{OUT}) \times I_{Q1\,(peak)} \times \frac{Q_{GD} \times f_{sw}}{I_G}$$
$$= 4.2^2 \times 8m \times 0.56 + (3 + 3.3) \times 6.8 \times \frac{10n \times 330k}{0.3} = 0.55W \quad (14)$$

Step 4: Output diode selection

The rated reverse voltage of the diode must be higher than $V_{IN}+V_{OUT}$ and the average diode current is equal to the output current at full load.

Step 5: SEPIC coupling capacitor selection

The RMS current of the Cs is:

$$I_{cs\,(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT} + V_D}{V_{IN\,(min)}}}$$
$$= 2.5 \times \sqrt{\frac{3.3 + 0.5}{3.0}} = 2.8A$$

and the ripple voltage is

$$\Delta V_{Cs} = \frac{I_{OUT} \times D_{max}}{Cs \times f_{sw}} = \frac{2.5 \times 0.56}{10\mu \times 330k} = 0.42V$$

A 10 µF ceramic cap is selected.

Step 6: Output capacitor selection

The RMS current of the output capacitor is:

$$I_{Cout(rms)} = I_{Cs(rms)} = 2.8A$$

Assuming the peak-to-peak ripple is 2% of the 3.3V output voltage, the ESR of the output capacitor is:

$$ESR \leq \frac{V_{ripple} \times 0.5}{I_{L1(peak)} + I_{L2(peak)}} = \frac{0.02 \times 3.3 \times 0.5}{3.8 + 3}$$
$$= 4.8\ m\Omega$$

and the capacitance is:

$$Cout \geq \frac{I_{OUT} \times D_{max}}{V_{ripple} \times 0.5 \times f_{sw}} = \frac{2.5 \times 0.56}{0.02 \times 3.3 \times 0.5 \times 300k}$$
$$= 141\ \mu F$$

Two pieces of 100 µF (6mΩ ESR) ceramic caps are used. For cost-sensitive applications, an electrolytic capacitor and a ceramic capacitor can be used together. Noise sensitive applications can include a second stage filter.

Step 7: Input capacitor selection

The RMS current of the input capacitor is:

$$I_{Cin(rms)} = \frac{\Delta I_L}{\sqrt{12}} = \frac{1.1}{\sqrt{12}} = 0.32A$$

Step 8: Feedback resistors, current sensing resistor calculation and frequency set resistor

R1 is the top resistor and R2 is the bottom resistor of the voltage divider. The feedback reference voltage is 1.26V.

If R1 = 20 kΩ, then:

$$R2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1 = \frac{1.26}{3.3 - 1.26} \times 20k$$
$$= 12.4\ k\Omega$$

For the LM3478, the threshold voltage to trigger the current protection varies with duty cycle. The threshold is a ramp which is defined by Vsense at 0% duty cycle and Vsense – Vsl at 100% duty cycle. The values for Vsense and Vsl can be taken from the electrical characteristics section of the LM3478 datasheet. There is also a plot in the datasheet showing the typical current sense voltage vs duty cycle. In our example the duty cycle was calculated to be about 50% and so we use the current limit threshold of 130mV for the following calculation to keep things simple. Thus the sensing resistor value is:

$$Rsn = \frac{130\ mV}{I_{Q1(peak)}} = \frac{130m}{6.8} = 19\ m\Omega$$

Rf is approximately 50 kΩ for 330 kHz operation.

Step 9: Compensation Design

In the control to output transfer function of a peak current mode controlled SEPIC converter, the load pole can be estimated as 1/(2πRL*Cout); The ESR zero of the output capacitor is 1/(2πESR*Cout), where RL is the load resistant, Cout is the output capacitor and ESR is the Equivalent Series Resistance of the output capacitor. There is also a right-half-plane zero (f_{RHPZ}), given by:

$$f_{RHPZ} = \frac{(1 - D_{max})^2 \times V_{OUT}}{2\pi \times D_{max} \times L2 \times 0.5 \times I_{OUT}}$$
$$= \frac{(1 - 0.56)^2 \times 3.3}{2\pi \times 0.56 \times 4.7\mu \times 0.5 \times 2.5} = 31\ kHz$$

We can also see a “glitch” in the magnitude plot at the resonant frequency of the network formed by the SEPIC capacitor Cs and the inductor L2:

$$f_R = \frac{1}{2\pi \times \sqrt{L2 \times Cs}} = \frac{1}{2\pi \times \sqrt{4.7\mu H \times 10\mu F}}$$
$$= 23\ kHz$$

The crossover frequency is set at one sixth of the f_{RHPZ} or f_R, whichever is lower:

$$f_c = \frac{f_R}{6} = \frac{23k}{6} = 3.8\ kHz$$

Parts Cc1, Cc2 and Rc form a compensation network, which has one zero at 1/(2πRc*Cc1), one pole at the origin, and another pole at 1/(2πRc*Cc2).

Where, V_{REF} is the reference voltage of 1.26V, V_{OUT} is the output voltage, G_{cs} is the current sense gain (roughly 1/Rsn) 100A/V, and G_{ma} is the error amplifier transconductance (800 µmho).

Rc is chosen to set the desired crossover frequency.

$$Rc = \frac{2\pi \times f_c \times C_{OUT} \times V_{OUT}^2 \times (1 + D_{max})}{G_{cs} \times G_{ma} \times V_{REF} \times V_{IN\,(min)} \times D_{max}}$$

$$= \frac{2\pi \times 3.8k \times 200\mu \times 3.3^2 \times (1 + 0.56)}{91 \times 800\mu \times 1.26 \times 3.0 \times 0.56}$$

$$= 523\Omega$$

Cc1 is chosen to set the compensator zero to ¼ of the crossover frequency

$$Cc1 = \frac{4}{2\pi \times f_c \times Rc} = \frac{4}{2\pi \times 3.8k \times 523} = 330\ nF$$

The pole at 1/(2πRc*Cc2) is to cancel the ESR zero 1/(2πESR*Cout),

$$Cc2 = \frac{C_{OUT} \times ESR}{Rc} = \frac{200\mu \times 3m}{523} = 1.2\ nF$$

Notes

Notes

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